LMK61PD0A2 超低抖动引脚可选振荡器

1 特性

- 超低噪声、高性能
  - 抖动：f_{OUT} > 100MHz 时的典型值为 90fs (RMS)
  - 高电源抑制比 (PSRR)：-70dBc，出色的电源抗扰度
- 灵活的输出频率和格式；用户可选择
  - 频率：62.5MHz、100MHz、106.25MHz、125MHz、156.25MHz、212.5MHz、312.5MHz
  - 格式：低电压正射极耦合逻辑 (LVPECL)、低压差分信令 (LVDS) 或高速收发器逻辑 (HSTL)
- 总频率容差：±50ppm
- 内部存储器存储了多个启动配置，可通过引脚控制进行选择
- 3.3V 工作电压
- 工业温度范围（-40ºC 至 +85ºC）
- 7mm x 5mm 8 引脚封装

2 应用

- 晶体振荡器、表面声波 (SAW) 振荡器或芯片振荡器的高性能替换产品
- 开关、路由器、网卡、基带装置 (BBU)、服务器、存储/SAN
- 测试和测量
- 医疗成像
- 现场可编程门阵列 (FPGA)，处理器连接

3 说明

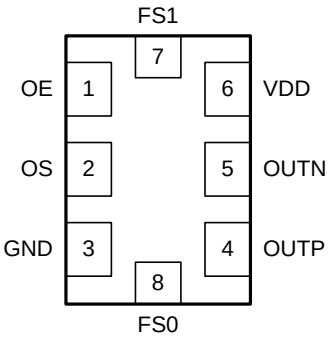
LMK61PD0A2 是一款超低抖动的 PLLatinum™ 引脚可选振荡器。该振荡器可生成通用基准时钟。 该器件在出厂前进行了预编程，可支持七种不同基准时钟频率。相应频率可通过将每个 FS[1:0] 配置为 VDD、GND 或 NC（无连接）进行选择。 输出格式可通过将操作系统 (OS) 的引脚配置为 VDD、GND 或 NC 进行选择，三种配置方式分别对应格式 LVPECL、LVDS 以及 HCSL。 内部电源调节功能提供出色的电源纹波抑制 (PSRR)，降低了供电网络的成本和复杂性。 该器件由单个 3.3V ± 5% 电源供电。

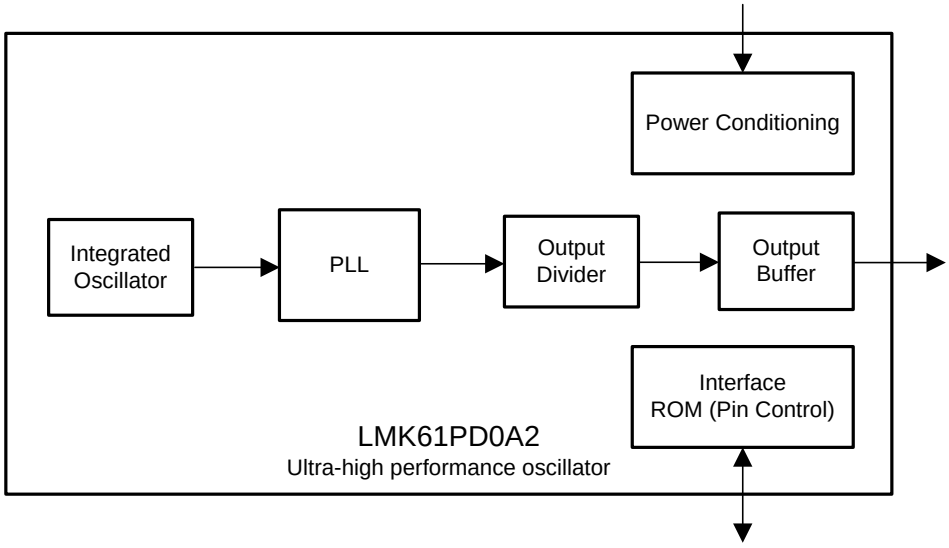
器件信息(1)

部件号	封装	封装尺寸（标称值）
LMK61PD0A2	8 引脚 QFM (SIA)	7.0mm x 5.0mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

引脚分布和简化框图





目录

4 修订历史记录

Changes from Original (October 2015) to Revision A **Page**

- “产品预览”至“量产数据” ... 1

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5 Device Control

Table 1. Output Frequency Mapping for FS[1:0] Selection

FS1	FS0	OUT FREQUENCY (MHz)	RELEVANT STANDARDS
0	0	100	PCI Express
0	NC	312.5	10 Gbps Ethernet
0	1	125	1 Gbps Ethernet
NC	0	106.25	Fiber Channel
NC	NC	156.25	10 Gbps Ethernet
NC	1	212.5	Fiber Channel
1	0	62.5	1 Gbps Ethernet
1	NC	Reserved	n/a
1	1	Reserved	n/a

Table 2. Output Type Mapping for OS, OE Selection

OS	OE	OUTPUT TYPE
X	0	Disabled (PLL functional)
0	1	LVPECL
NC	1	LVDS
1	1	HCSL

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6 Pin Configuration and Functions

SIA Package
8 pin QFM

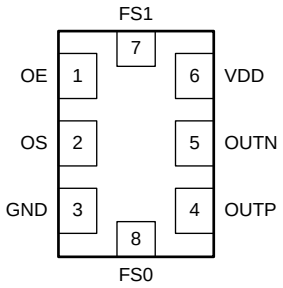

Table 3. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device Ground.
VDD	6	Analog	3.3 V Power Supply.
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential Output Pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
FS[1:0]	7, 8	LVCMOS	Output Frequency Select. Refer toTable 1.
OE	1	LVCMOS	Output Enable (internal pullup). Refer toTable 2.
OS	3	LVCMOS	Output Type Select. Refer toTable 2.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device Supply Voltage	-0.3	3.6	V
V_{IN}	Output Voltage Range for Logic Inputs	-0.3	VDD + 0.3	V
V_{OUT}	Output Voltage Range for Clock Outputs	-0.3	VDD + 0.3	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	-40	25	85	°C
T_J	Junction Temperature			125	°C
t_{RAMP}	VDD Power-Up Ramp Time	0.1		100	ms

7.4 Thermal Information

THERMAL METRIC(1)		LMK61PD0A2 (2) (3) (4) QFM (SIA) 8 PINS			UNIT
		Airflow (LFM) 0	Airflow (LFM) 200	Airflow (LFM) 400	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54	44	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34	n/a	n/a	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.7	n/a	n/a	
ψ_{JT}	Junction-to-top characterization parameter	11.2	16.9	21.9	
ψ_{JB}	Junction-to-board characterization parameter	36.7	37.8	38.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal resistance is calculated on a 4 layer JEDEC board.
(3) Connected to GND with 3 thermal vias (0.3-mm diameter).
(4) ψJB (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

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7.5 Electrical Characteristics - Power Supply(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device Current Consumption	LVPECL(2)		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device Current Consumption when output is disabled	OE = GND		136		

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 ohm termination resistors, from total power dissipation.

7.6 LVPECL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output Frequency(2)		62.5		312.5	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})(2)		700	800	1200	mV
$V_{OUT, DIFF, PP}$	Differential Output Peak-to-Peak Swing			2 x $\|V_{OD}\|$		V
V_{OS}	Output Common Mode Voltage			VDD – 1.55		V
t_R / t_F	Output Rise/Fall Time (20% to 80%)(3)			120	200	ps
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	156.25 MHz		-165		dBc/Hz
ODC	Output Duty Cycle(3)		45%		55%	

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

7.7 LVDS Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output Frequency(1)		62.5		312.5	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential Output Peak-to-Peak Swing			2 x $\|V_{OD}\|$		V
V_{OS}	Output Common Mode Voltage			1.2		V
t_R / t_F	Output Rise/Fall Time (20% to 80%)(2)			150	250	ps
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	156.25 MHz		-162		dBc/Hz
ODC	Output Duty Cycle(2)		45%		55%	
R_{OUT}	Differential Output Impedance			125		Ohm

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

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7.8 HCSL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output Frequency		62.5		312.5	MHz
V_{OH}	Output High Voltage		600		850	mV
V_{OL}	Output Low Voltage		-100		100	mV
V_{CROSS}	Absolute Crossing Voltage(2)(3)		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS}(2)(3)		0		140	mV
dV/dt	Slew Rate(4)		0.8		2	V/ns
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	100 MHz		-164		dBc/Hz
ODC	Output Duty Cycle(4)		45%		55%	

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

7.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.6	V
I_{IH}	Input High Current	V_{IH} = VDD	-40		40	uA
I_{IL}	Input Low Current	V_{IL} = GND	-40		40	uA
C_{IN}	Input Capacitance			2		pF

7.10 OS, FS[1:0] Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.4	V
I_{IH}	Input High Current	V_{IH} = VDD	-40		40	uA
I_{IL}	Input Low Current	V_{IL} = GND	-40		40	uA
C_{IN}	Input Capacitance			2		pF

7.11 Frequency Tolerance Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total Frequency Tolerance	All output formats, frequency bands and device junction temperature up to 125°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (10 years)	-50		50	ppm

(1) Ensured by characterization.

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7.12 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold Voltage(1)		2.72		2.95	V
V_{DROOP}	Allowable Voltage Droop(2)				0.1	V
$t_{STARTUP}$	Startup Time (1)	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time(2)	Time elapsed from OE at V_{IH} to output enabled			50	us
t_{OE-DIS}	Output disable time(2)	Time elapsed from OE at V_{IL} to output disabled			50	us

(1) Ensured by characterization.
(2) Ensured by design.

7.13 PSRR Characteristics(1)

VDD = 3.3 V, T_A = 25°C, FS[1:0] = NC, NC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs Induced by 50 mV Power Supply Ripple(2)(3) at 156.25 MHz output, all output types	Sine wave at 50 kHz		-70		dBc
		Sine wave at 100 kHz		-70		
		Sine wave at 500 kHz		-70		
		Sine wave at 1 MHz		-70		

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2*10(SPUR/20) / (π*f_{OUT})]*1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

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7.14 PLL Clock Output Jitter Characteristics[1][2]

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS Phase Jitter[3] (12 kHz – 20 MHz) (1 kHz – 5 MHz)	f_{OUT} ≥ 100 MHz, All output frequencies and output types		100	200	fs RMS
RJ	RMS Phase Jitter[3] (12 kHz – 20 MHz) (1 kHz – 5 MHz)	f_{OUT} = 62.5 MHz, All output frequencies and output types		200	400	fs RMS

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).
(3) Ensured by characterization.

7.15 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

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7.16 Typical Performance Characteristics

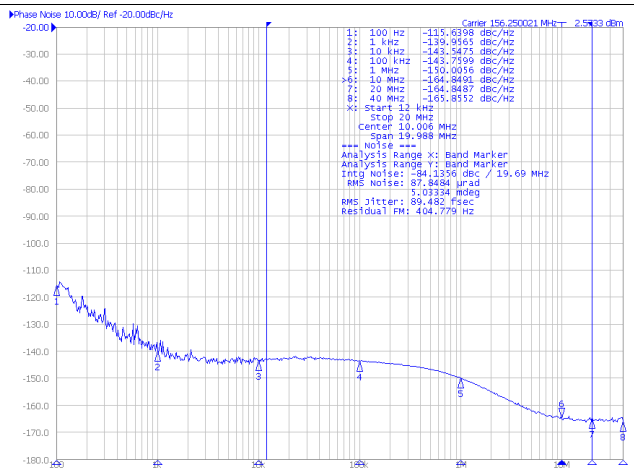

Figure 1. Phase Noise of LVPECL Differential Output at 156.25 MHz with FS[1:0] = NC, NC, OS = GND

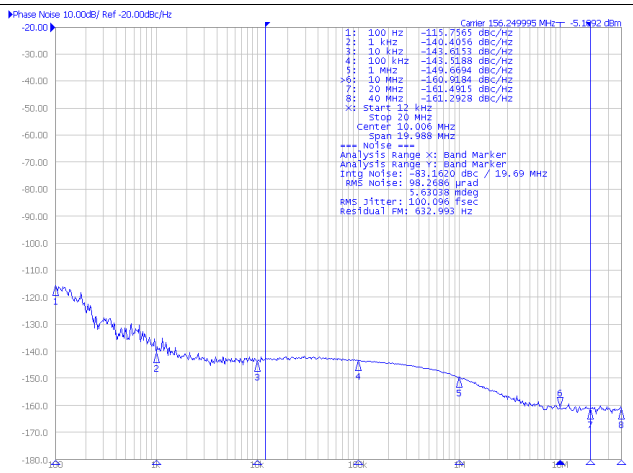

Figure 2. Phase Noise of LVDS Differential Output at 156.25 MHz with FS[1:0] = NC, NC, OS = NC

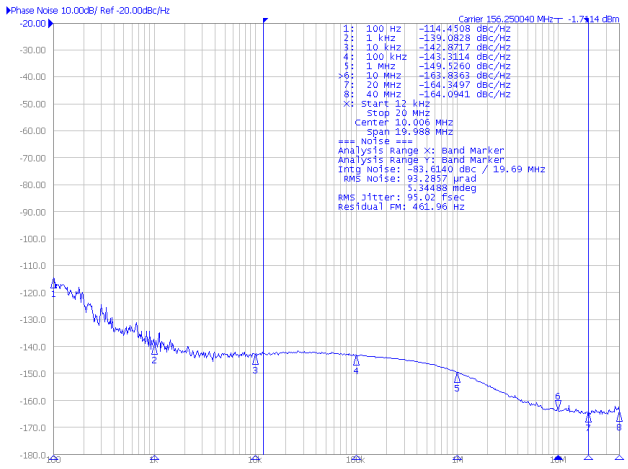

Figure 3. Phase Noise of HCSL Differential Output at 156.25 MHz with FS[1:0] = NC, NC, OS = VDD

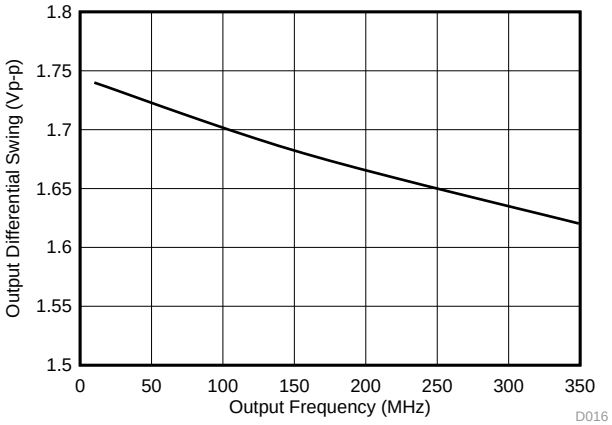

Figure 4. LVPECL Differential Output Swing vs Frequency

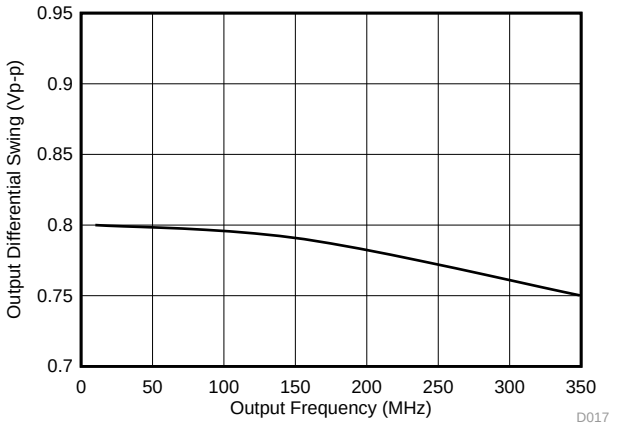

Figure 5. LVDS Differential Output Swing vs Frequency

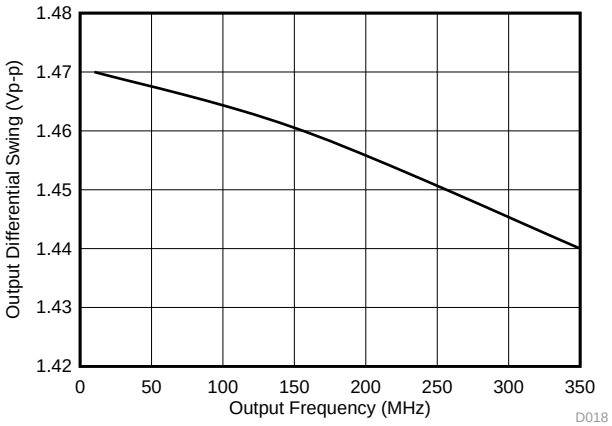

Figure 6. HCSL Differential Output Swing vs Frequency

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8 Parameter Measurement Information

8.1 Device Output Configurations

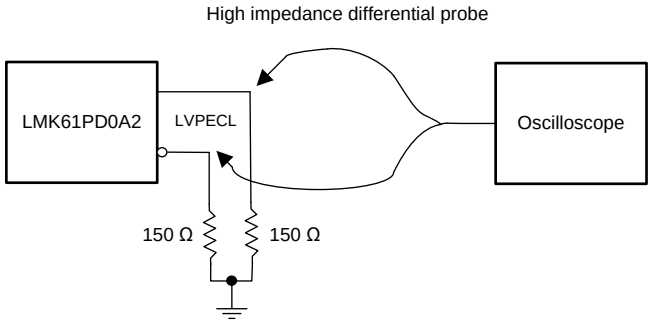

Figure 7. LVPECL Output DC Configuration during Device Test

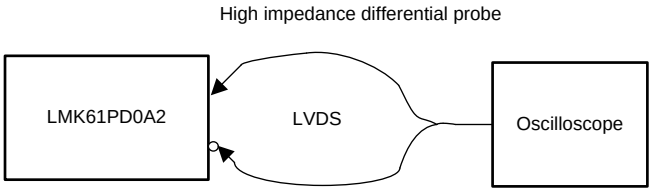

Figure 8. LVDS Output DC Configuration during Device Test

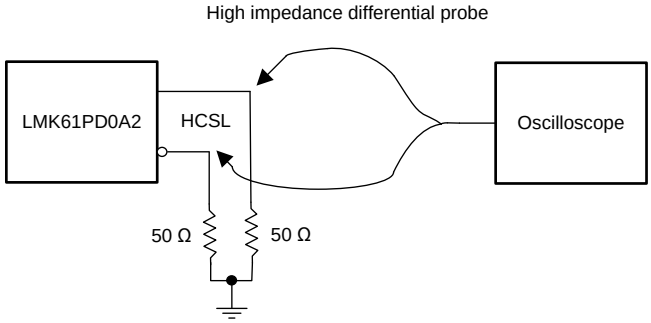

Figure 9. HCSL Output DC Configuration during Device Test

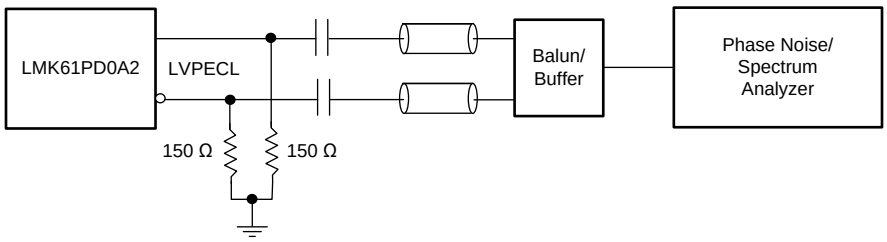

Figure 10. LVPECL Output AC Configuration during Device Test

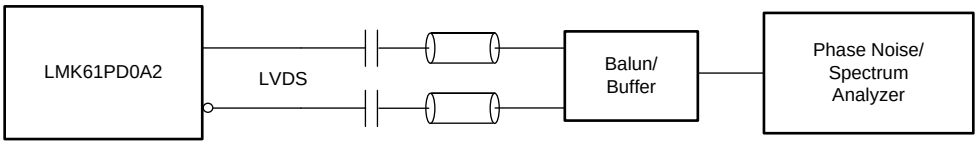

Figure 11. LVDS Output AC Configuration during Device Test

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Device Output Configurations (continued)

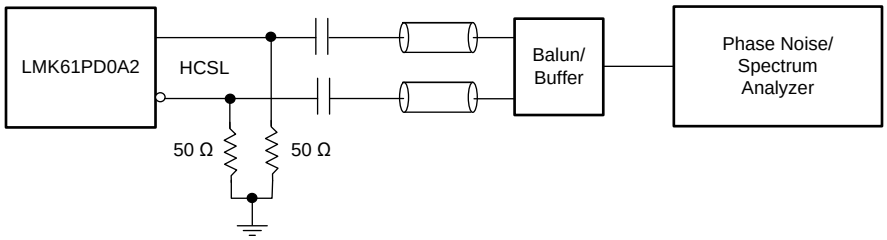

Figure 12. HCSL Output AC Configuration during Device Test

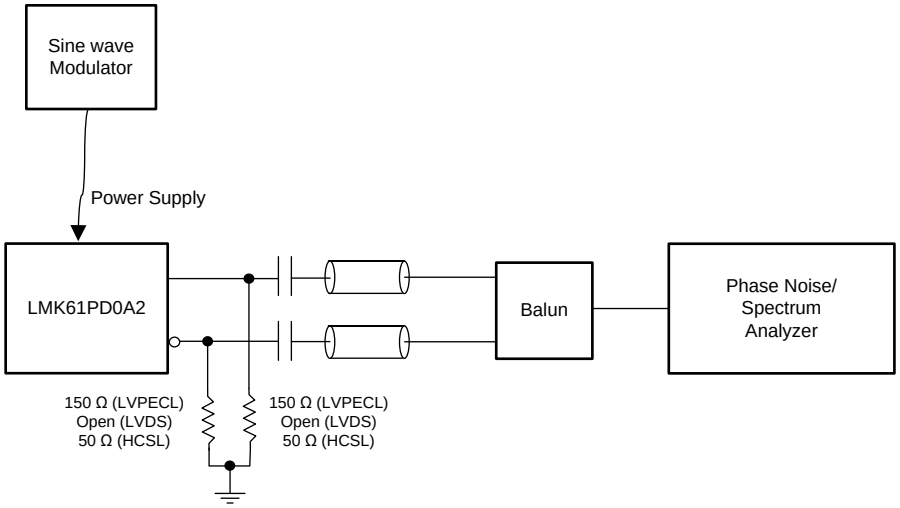

Figure 13. PSRR Test Setup

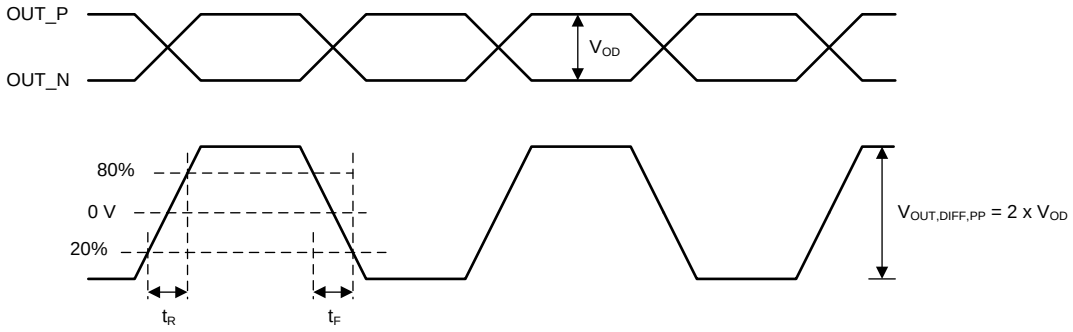

Figure 14. Differential Output Voltage and Rise/Fall Time

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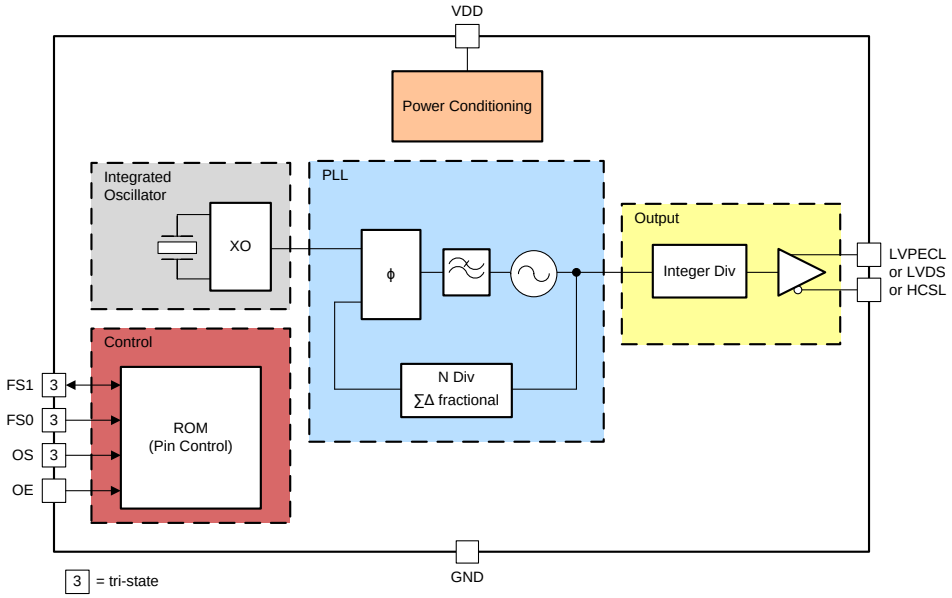
9 Detailed Description

9.1 Overview

The LMK61PD0A2 is a pin selectable oscillator that generates commonly used reference clocks, greater than 100 MHz, with less than 200 fs, rms max random jitter.

9.2 Functional Block Diagram



NOTE

Control blocks are compatible with 1.8/2.5/3.3 V I/O voltage levels.

9.3 Feature Description

9.3.1 Device Block-Level Description

The LMK61PD0A2 comprises of an integrated oscillator that includes a 50 MHz crystal, a fractional PLL with integrated VCO. Completing the device is the combination of an integer output divider and a universal differential output buffer. The on-chip ROM contains seven pre-programmed output frequency plans that selects the appropriate settings for the integrated oscillator, PLL blocks and output divider. Table 1 lists the supported output frequency plans that can be selected by pin-strapping FS[1:0] as required. Table 2 lists the supported output types that can be selected by pin-strapping OS and OE as required. The device is powered by on-chip low dropout (LDO) linear voltage regulators and the regulated supply network is partitioned such that the sensitive analog supplies are running from separate LDOs than the digital supplies which use their own LDO. The LDOs provide isolation from any noise in the external power supply rail with a PSRR of better than -70 dBc at 50 kHz to 1 MHz ripple frequencies at 3.3 V device supply.

9.3.2 Device Configuration Control

The LMK61PD0A2 selects an output frequency plan and output type using control pins FS[1:0].

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LMK61PD0A2 is an ultra-low jitter pin selectable oscillator that can be used to provide reference clocks for high-speed serial links resulting in improved system performance.

10.2 Typical Application

10.2.1 Jitter Considerations in Serdes Systems

Jitter-sensitive applications such as 10 Gbps or 100 Gbps Ethernet, deploy a serial link utilizing a Serializer in the transmit section (TX) and a De-serializer in the receive section (RX). These SERDES blocks are typically embedded in an ASIC or FPGA. Estimating the clock jitter impact on the link budget requires understanding of the TX PLL bandwidth and the RX CDR bandwidth.

As can be seen in Figure 15, the pass band region between the TX low pass cutoff and RX high pass cutoff frequencies is the range over which the reference clock jitter adds without any attenuation to the jitter budget of the link. Outside of these frequencies, the SERDES link will attenuate the reference clock jitter with a 20 dB/dec or even steeper roll-off. Modern ASIC or FPGA designs have some flexibility on deciding the optimal RX CDR bandwidth and TX PLL bandwidth. These bandwidths are typically set based on what is achievable in the ASIC or FPGA process node, without increasing design complexity, and on any jitter tolerance or wander specification that needs to be met, as related to the RX CDR bandwidth.

The overall allowable jitter in a serial link is dictated by IEEE or other relevant standards. For example, IEEE802.3ba states that the maximum transmit jitter (peak-peak) for 10 Gbps Ethernet should be no more than 0.28 * UI and this equates to a 27.1516 ps, p-p for the overall allowable transmit jitter.

The jitter contributing elements are made up of the reference clock, generated potentially from a device like LMK61PD0A2, the transmit medium, transmit driver etc. Only a portion of the overall allowable transmit jitter is allocated to the reference clock, typically 20% or lower. Therefore, the allowable reference clock jitter, for a 20% clock jitter budget, is 5.43 ps, p-p.

Jitter in a reference clock is made up of deterministic jitter (arising from spurious signals due to supply noise or mixing from other outputs or from the reference input) and random jitter (usually due to thermal noise and other uncorrelated noise sources). A typical clock tree in a serial link system consists of clock generators and fanout buffers. The allowable reference clock jitter of 5.43 ps, p-p is needed at the output of the fanout buffer. Modern fanout buffers have low additive random jitter (less than 100 fs, rms) with no substantial contribution to the deterministic jitter. Therefore, the clock generator and fanout buffer contribute to the random jitter while the primary contributor to the deterministic jitter is the clock generator. Rule of thumb, for modern clock generators, is to allocate 25% of allowable reference clock jitter to the deterministic jitter and 75% to the random jitter. This amounts to an allowable deterministic jitter of 1.36 ps, p-p and an allowable random jitter of 4.07 ps, p-p. For serial link systems that need to meet a bit error rate (BER) of 10^{-12}, the allowable random jitter in root-mean-square is 0.29 ps, rms. This is calculated by dividing the p-p jitter by 14 for a BER of 10^{-12}. Accounting for random jitter from the fanout buffer, the random jitter needed from the clock generator is 0.27 ps, rms. This is calculated by the root-mean-square subtraction from the desired jitter at the fanout buffer's output assuming 100 fs, rms of additive jitter from the fanout buffer.

With careful frequency planning techniques, like spur optimization (covered in the Spur Mitigation Techniques section) and on-chip LDOs to suppress supply noise, the LMK61PD0A2 is able to generate clock outputs with deterministic jitter that is below 1 ps, p-p and random jitter that is below 0.2 ps, rms. This gives the serial link system with additional margin on the allowable transmit jitter resulting in a BER better than 10^{-12}.

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Typical Application (continued)

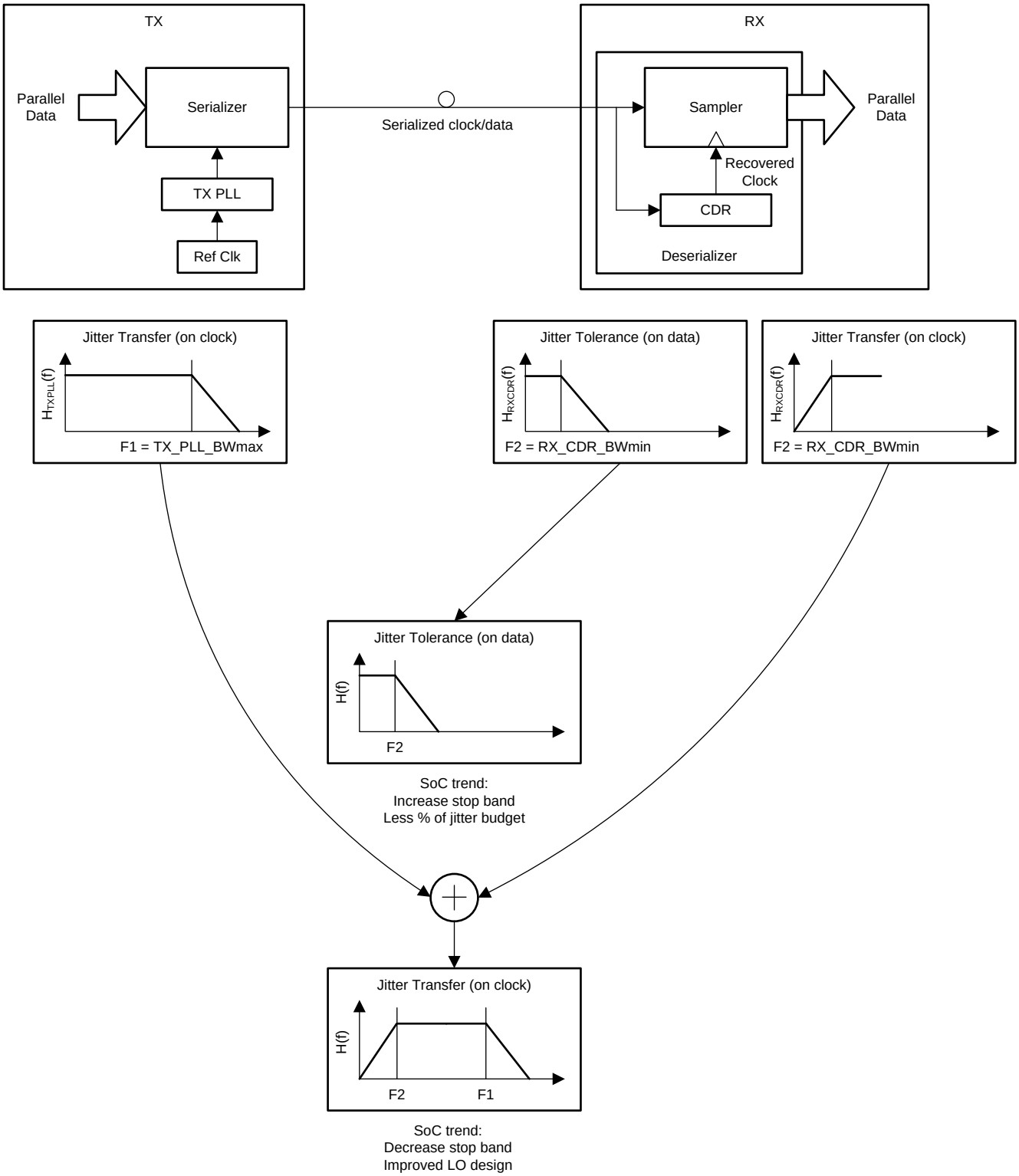

Figure 15. Dependence of Clock Jitter in Serial Links

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11 Power Supply Recommendations

For best electrical performance of LMK61PD0A2, it is preferred to utilize a combination of 10 uF, 1 uF and 0.1 uF on its power supply bypass network. It is also recommended to utilize component side mounting of the power supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 16 shows the layout recommendation for power supply decoupling of LMK61PD0A2.

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12 Layout

12.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK61PD0A2 to ensure good thermal / electrical performance and overall signal integrity of entire system.

12.1.1 Ensuring Thermal Reliability

The LMK61PD0A2 is a high performance device. Therefore careful attention must be paid to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in Figure 16, to maximize thermal dissipation out of the package.

Equation 1 describes the relationship between the PCB temperature around the LMK61PD0A2 and its junction temperature.

$$T_B = T_J – \Psi_{JB} * P \quad (1)$$

where

- T_B: PCB temperature around the LMK61PD0A2
- T_J: Junction temperature of LMK61PD0A2
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK61PD0A2 (36.7°C/W without airflow)
- P: On-chip power dissipation of LMK61PD0A2

In order to ensure that the maximum junction temperature of LMK61PD0A2 is below 125°C, it can be calculated that the maximum PCB temperature without airflow should be at 100°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68 W.

12.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK61PD0A2, it is recommended to route vias into decoupling capacitors and then into the LMK61PD0A2. It is also recommended to increase the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. Figure 16 shows the layout recommendation for LMK61PD0A2.

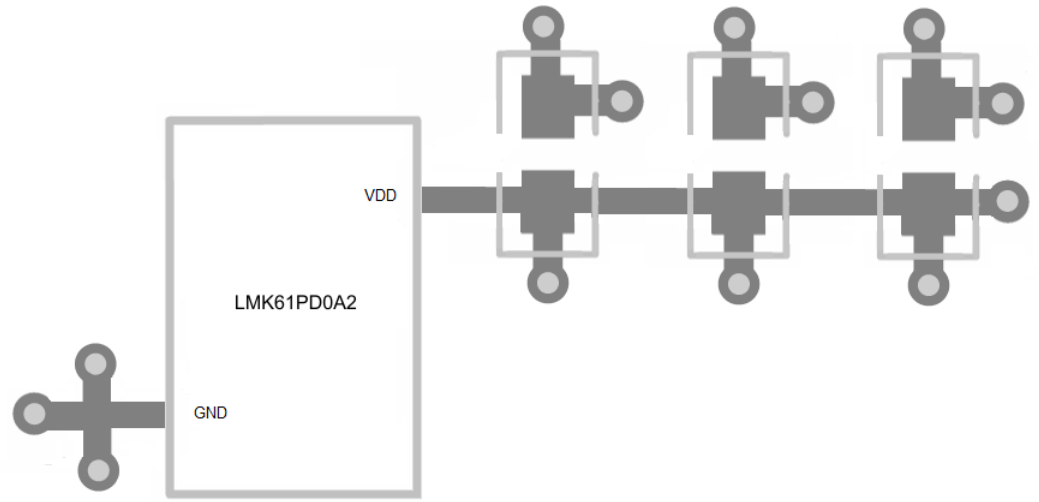

Figure 16. LMK61PD0A2 Layout Recommendation for Power Supply and Ground

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Layout Guidelines (接下页)

12.1.3 Recommended Solder Reflow Profile

It is recommended to follow the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferrable for the LMK61PD0A2 to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

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13 器件和文档支持

13.1 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 商标

E2E is a trademark of Texas Instruments.

13.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK61PD0A2-SIAR	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61 PD0A2
LMK61PD0A2-SIAR.A	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61 PD0A2
LMK61PD0A2-SIAR.B	Active	Production	QFM (SIA) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK61PD0A2-SIAT	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61 PD0A2
LMK61PD0A2-SIAT.A	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61 PD0A2
LMK61PD0A2-SIAT.B	Active	Production	QFM (SIA) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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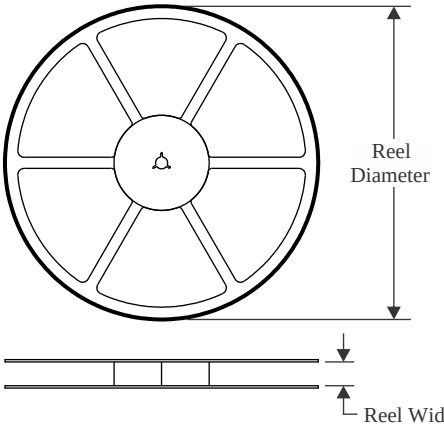
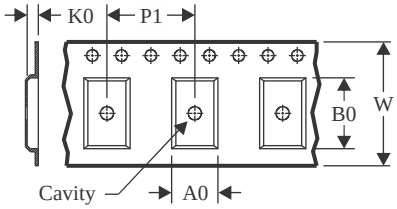
TAPE AND REEL INFORMATION

REEL DIMENSIONS

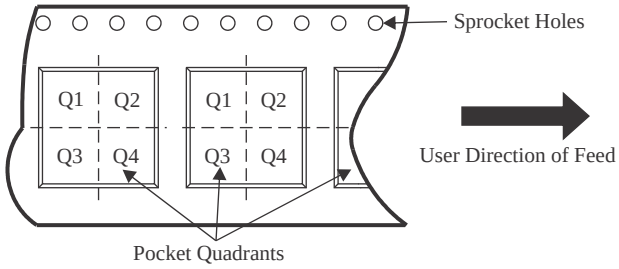


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

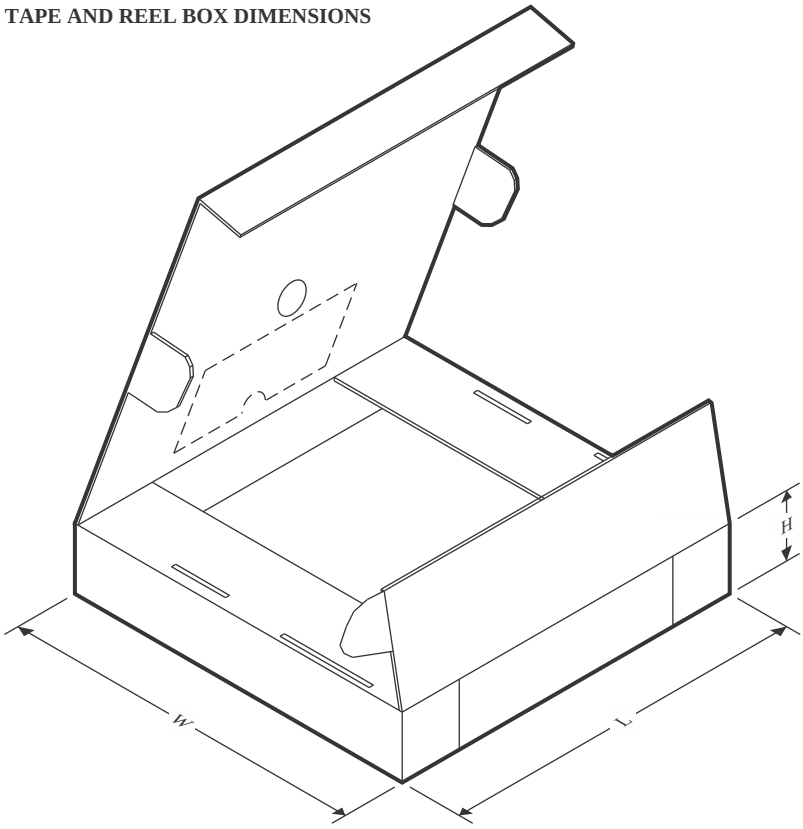
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK61PD0A2-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61PD0A2-SIAT	QFM	SIA	8	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

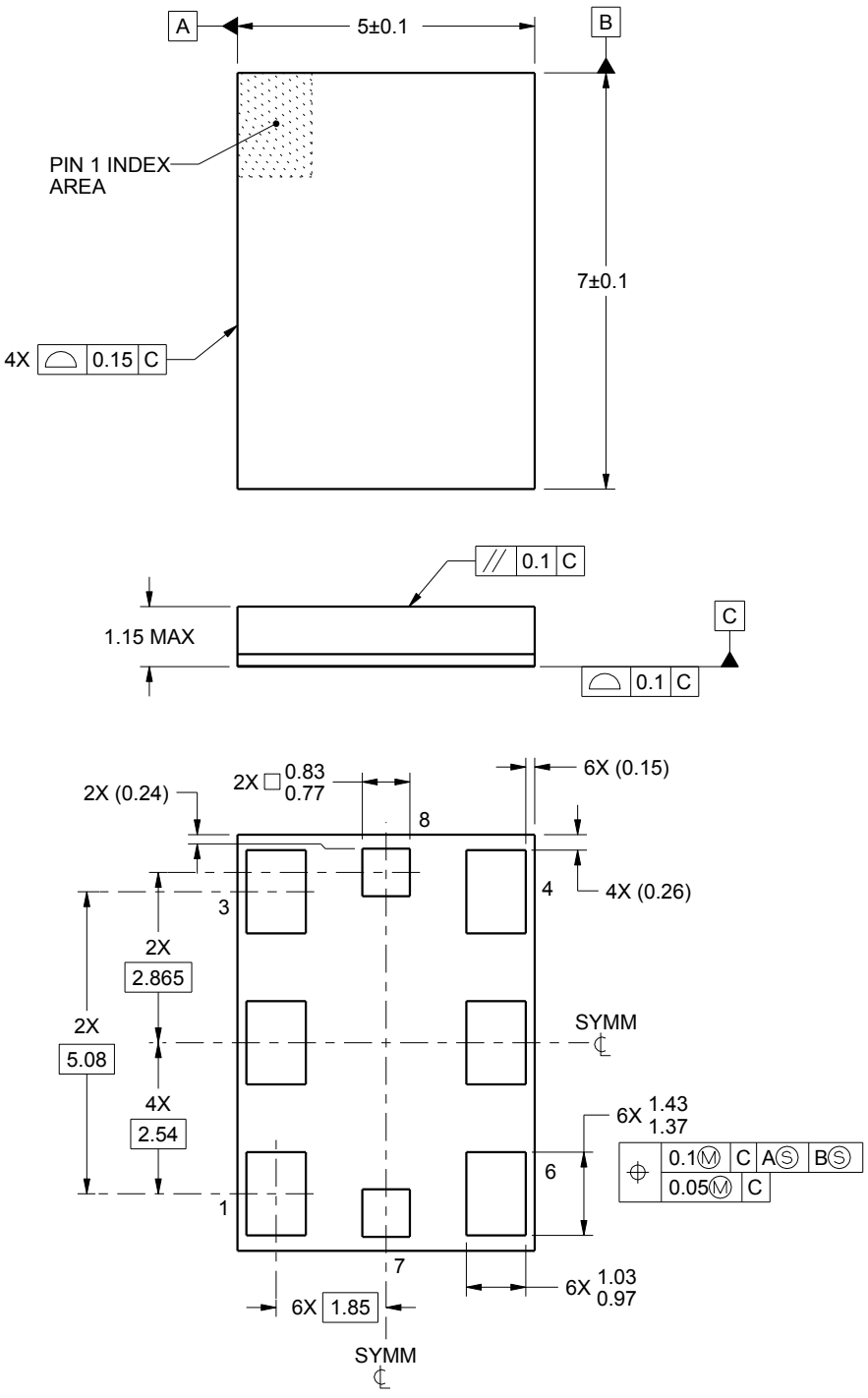
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK61PD0A2-SIAR	QFM	SIA	8	2500	356.0	356.0	36.0
LMK61PD0A2-SIAT	QFM	SIA	8	250	208.0	191.0	35.0

PACKAGE OUTLINE

SIA0008B

QFM - 1.15 mm max height

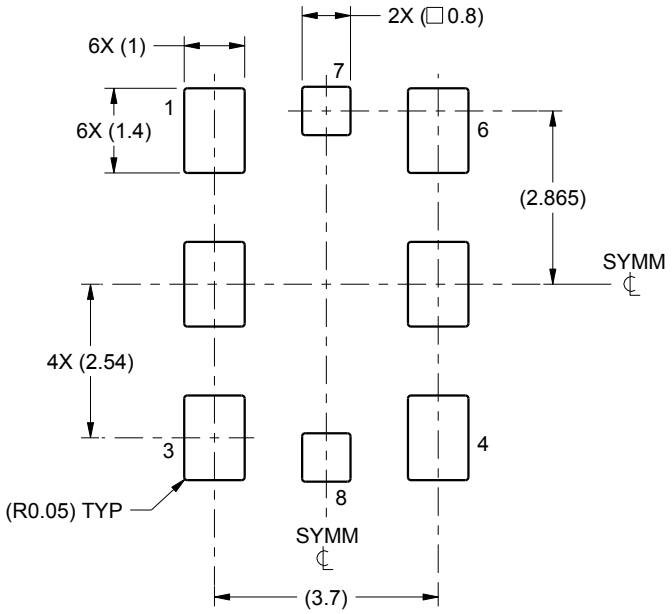
QUAD FLAT MODULE



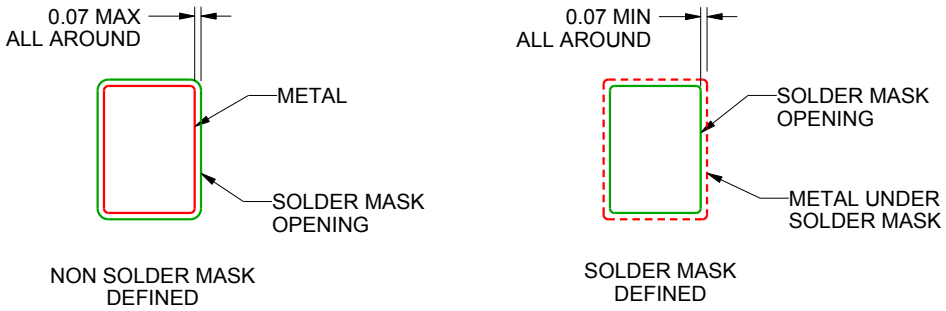
4221443/B 09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

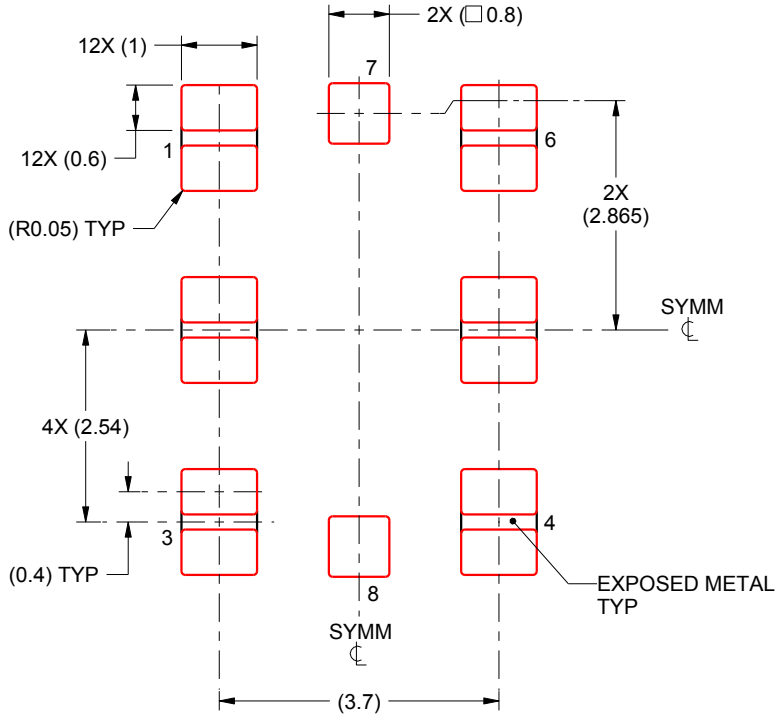
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0008B

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 1-3 & 4-6: 86%
SCALE:10X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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