具有可编程增益和偏移的单电源、自动置零传感器放大器

查询样品: PGA308-Q1

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 器件温度 **1** 级： **-40**℃ 至 **+125**℃ 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C3B**
- 针对桥式传感器的数字校准
- 偏移选择：粗略选择和精准选择
- 增益选择：粗略选择和精准选择
- 桥式故障监控器
- 用于引线交换的输入复用器
- 过程量/欠程量限制
- D_{OUT}/ V_{OUT} 钳位功能
- 七插槽一次性可编程 **(OTP)** 内存
- 一线制数字通用异步收发器 **(UART)** 接口
- 运行电压：**+2.7 V** 至 **+5.5 V**
- **MSOP-10** 和 **3mm x 4mm DFN-10** 封装

应用范围

- 桥式传感器
- 远程 **4-20 mA** 发射器
- 应变、负载、衡器
- 车载传感器

评估工具

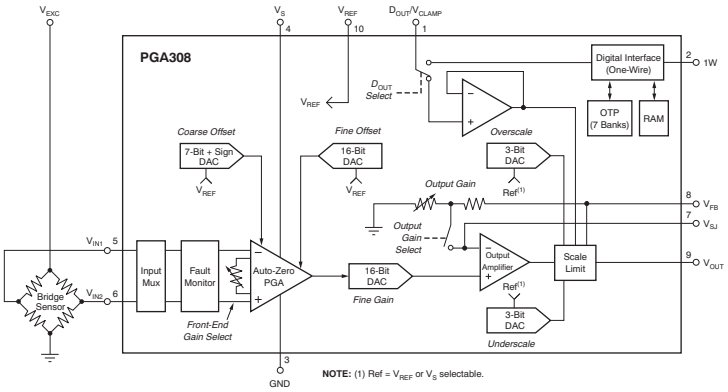
- **PGA308EVM** （硬件和软件）
  - 校准和配置
  - 传感器仿真

说明

PGA308-Q1 是一款可编程模拟传感器信号调节器。此模拟信号路径放大传感器信号并且为偏移和增益提供数字校准。 校准通过 1W 引脚、一个数字单线制 UART 兼容接口来完成。 对于三端传感器模块，1W 可连接至 V_{OUT} 并且此组件可通过 V_{OUT} 引脚进行编程。 增益和偏移校准参数被存储在板载一次性可编程 (OTP) 内存的七个内存库中。 加电复位 (POR) OTP 内存库总共可编程四次。

全模拟信号路径包含有一个 2 x 2 输入复用器 (mux) 以实现电子传感器引线交换、一个粗略偏移调整、一个自动置零可编程增益测量仪器放大器 (PGA)、一个精准增益调整、一个精准偏移调整、和一个可编程增益输出放大器。 故障监控电路检测并发出传感器烧断、过载、和系统故障状态信号。 过程量/欠程量限制为系统电平诊断提供额外了方法。 此两用 D_{OUT}/V_{CLAMP} 引脚可被用作一个可编程数字输出或者一个 V_{OUT} 过压钳位。

要获得详细的应用信息，请从网站 PGA308 用户指南 (SBOU069) 可供下载 www.ti.com。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
PGA308AQDGSRQ1	MSOP-10	DGS	JAAQ

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		PGA308-Q1	UNIT
Supply Voltage, V_S		+5.5	V
D_{OUT}/V_{CLAMP} Output Current Limit		±10	mA
Pin Protection	Input Current	–10 to +10	mA
	V_{IN1}, V_{IN2}, V_{REF}, 1W, D_{OUT}/V_{CLAMP}, V_{SJ} (2)	GND – 0.3 to V_S + 0.3	V
	V_{FB} Terminal Voltage	–30 to 30	V
	V_{FB} Terminal Current	–10 to 10	mA
	V_{OUT}	–160 to 160	mA
Operating Temperature Range		–40 to +150	°C
Storage Temperature Range		–55 to +150	°C
Junction Temperature		+165	°C
ESD Rating	Human Body Model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C3B	750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Terminals are diode-clamped to the power-supply rails, V_S and GND. Limit current to 10mA or less.

THERMAL INFORMATION

THERMAL METRIC(1)		PGA308-Q1 DGS 10 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	154.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	48.3	
θ_{JB}	Junction-to-board thermal resistance(4)	75.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	3.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	73.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +5V, GND = 0V, D_{OUT}/V_{CLAMP} = +5V, and V_{REF} = +5V, unless otherwise noted.

PARAMETER		CONDITIONS	PGA308-Q1[1] MIN	TYP	MAX	UNIT
V_{OUT}/V_{IN} Differential Signal Gains [2] (Front-End PGA + Output Amplifier)		Front-End PGA gains (G_F): 4, 6, 8, 12, 16, 32, 64, 100, 200, 400, 480, 600, 800, 960, 1200, 1600 Output Amplifier gains: 2, 2.4, 3, 3.6, 4, 4.5, 6 Fine Gain Adjust = 0.33 to 1	2.67		9600	V/V
V_{OUT}/V_{IN} Slew Rate (Front-End PGA + Output Amplifier)		CMP_SEL [CFG1 register] = 0		0.6		V/µs
		CMP_SEL [CFG1 register] = 1		0.3		V/µs
V_{OUT}/V_{IN} Settling Time (0.01%FSR) (Front-End PGA + Output Amplifier)		V_{OUT}/V_{IN} differential gain = 8, V_{OUT} = +0.5V to +4.5V step, comp off, no capacitive load		13		µs
		V_{OUT}/V_{IN} differential gain = 200, V_{OUT} = +0.5V to +4.5V step, comp off, no capacitive load		15		µs
FRONT-END PGA						
Auto-Zero Internal Frequency				40		kHz
Offset Voltage (RTI)[3]		Coarse Offset Adjust disabled		±5	±40	µV
vs Temperature		**Coarse Offset Adjust disabled**		**±0.2**		**µV/°C**
vs Supply Voltage, V_S		Coarse Offset Adjust disabled		2 + 150/G_F	10 + 1000/G_F	µV/V
vs Common-Mode Voltage		G_F = Front-End PGA gain, Coarse Offset Adjust disabled		1 + 250/G_F	10 + 2000/G_F	µV/V
Offset Voltage Programming Range (RTI)[3]		Coarse Offset Adjust enabled, Coarse Offset Adjust controls offset	–100		100	mV
vs Temperature		**Coarse Offset Adjust enabled**		**±0.2**		**µV/°C**
vs Supply Voltage, V_S		Coarse Offset Adjust enabled		2 + 150/G_F		µV/V
vs Common-Mode Voltage		G_F = Front-End PGA gain, Coarse Offset Adjust enabled		1 + 250/G_F		µV/V
Linear Input Voltage Range[4]			0.2		V_S – 1.4	V
Input Bias Current				±0.3	±1.5	nA
vs Temperature				**10**		**pA/°C**
Input Offset Current				±0.1	±1.5	nA
vs Temperature				**10**		**pA/°C**
Input Impedance: Differential				30 ‖ 6		GΩ ‖ pF
Input Impedance: Common-Mode				50 ‖ 20		GΩ ‖ pF
Input Voltage Noise		RTI, dc to 10Hz, G_F = 100, R_S = 0Ω		1.2		μV_{PP}
Input Voltage Noise Density		RTI, voltage noise density, f = 1kHz, Coarse Offset Adjust = 0V		50		nV/√Hz
		RTI, voltage noise density, f = 1kHz, Coarse Offset Adjust = 100mV		80		nV/√Hz
Input EMI Filter Frequency	f_{3dB}	Input EMI filter to GND, V_{IN1} and V_{IN2}		40		MHz
PGA Gain[5]						
Gain Range Steps		4, 6, 8, 12, 16, 32, 64, 100, 200, 400, 480, 600, 800, 960, 1200, 1600	4		1600	V/V
Initial Gain Error		$G_F \le 16$		±0.03	±0.25	%
		$32 \le G_F \le 480$		±0.1	±0.4	%
		$600 \le G_F \le 1600$		±0.3	±1	%
vs Temperature				**6**		**ppm/°C**
Output Voltage Range			0.05		V_S – 0.05	V
Bandwidth		G_F = 4		400		kHz
		G_F = 1600		10		kHz

(1) External Sensor Output Sensitivity with condition $V_S = V_{REF} = V_{CLAMP}$ = +5V has a range of 0.08mV/V to 296mV/V. This is based on a bridge sensor excitation voltage of +5V and PGA308-Q1 output voltage span of 4V. Individual applications must consider noise, small-signal bandwidth, and required system error to assess if the PGA308-Q1 will work for a given sensor sensitivity.
(2) PGA308-Q1 total differential gain from input ($V_{IN1} – V_{IN2}$) to output (V_{OUT}): $V_{OUT} / (V_{IN1} – V_{IN2})$ = (PGA gain) × (output amplifier gain) × (fine gain adjust) with output amplifier internal gains used.
(3) RTI = Referred-to-input.
(4) Linear input range is the allowed min/max voltage on the V_{IN1} and V_{IN2} pins for the front-end PGA to continue to operate in a linear region. The allowed common-mode and differential voltage depends on gain and offset settings. Refer to the PGA308 User's Guide (SBOU069), for more information.
(5) I_{REF} current load is typically 100µA while in Shutdown mode. Although the output amplifier is disabled in Shutdown mode, RFO and RGO (180kΩ typical total) remain connected in series between V_{FB} and GND while in Shutdown mode. See Figure 37, *Detailed Block Diagram*, for more information.

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +5V, GND = 0V, D_{OUT}/V_{CLAMP} = +5V, and V_{REF} = +5V, unless otherwise noted.

PARAMETER		CONDITIONS	PGA308-Q1[1] MIN	TYP	MAX	UNIT
Coarse Offset Adjust (RTI of Front-End PGA)[6]						
Range		V_{REF} = +5V	–100		+100	mV
Resolution		7 bit + sign, V_{REF} = +5V		1		mV
PSRR				2		µV/V
CMRR				1		µV/V
Drift		**Coarse Offset Adjust = 100mV**		**1.2**		**µV/°C**
Fine Offset Adjust (Zero DAC)						
Programming Range		RTO of Front-End PGA	$–0.5V_{REF}$		$+0.5V_{REF}$	V
Output Voltage Range			0.1		V_S – 0.1	V
Resolution		65,536 steps, 16-bit DAC, V_{REF} = +5V		76		µV
Integral Nonlinearity				±6		LSB
Differential Nonlinearity				±0.5		LSB
Gain Error				±0.5		%
Gain Error Drift				**±4**		**ppm/°C**
Offset				±4		mV
Offset Drift				**±10**		**µV/°C**
PSRR				±200		µV/V
Output Amplifier						
Output Fine Gain Adjust (Gain DAC)						
Range			0.33		1	V/V
Resolution		65,536 steps, 16-bit DAC		10		µV/V
Integral Nonlinearity				±6		LSB
Differential Nonlinearity				±0.5		LSB
Gain Error					±0.2	%
Gain Drift				**3**		**ppm/°C**
Output Amplifier						
Offset Voltage (RTI of Output Amplifier)[6]				±3		mV
vs Temperature				**±5**		**µV/°C**
vs Supply Voltage, V_S				±100		µV/V
Common-Mode Input Range			0		V_S – 1.5	V
Input Bias Current				±100		pA
Amplifier Internal Gain						
Gain Range Steps		2, 2.4, 3, 3.6, 4, 4.5, 6	2		6	V/V
Initial Gain Error				±0.05	±0.25	%
vs Temperature				**±1**		**ppm/°C**
Output Voltage Range		I_{OUT} = 0.5mA[7]	0.03		V_S – 0.06	V
		I_{OUT} = 4mA[7]	0.1		V_S – 0.1	V
Output Short-Circuit Current	I_{SC}	Sourcing/sinking	10			mA
Open-Loop Gain at 0.1Hz				106		dB
Gain-Bandwidth Product				2		MHz
Phase Margin		Gain = 2, C_L = 200pF		45		deg
Output Resistance	R_O	AC small-signal, open-loop, f = 1MHz, I_{OUT} = 0, see Figure 28		500		Ω

(6) RTI = Referred-to-input.
(7) Unless limited by the over/under-scale setting, or V_{CLAMP} pin.

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +5V, GND = 0V, D_{OUT}/V_{CLAMP} = +5V, and V_{REF} = +5V, unless otherwise noted.

PARAMETER		CONDITIONS	PGA308-Q1[1] MIN	TYP	MAX	UNIT
Over- and Under-Scale Limits						
Over-Scale Thresholds		V_{LIM} = 4V, register-selectable ratio of V_{LIM}				
	OS0	HL[2:0] (CFG1 register D[5:3]) = 000	0.97	0.9805	0.99	V/V
	OS1	HL[2:0] (CFG1 register D[5:3]) = 001	0.9588	0.9688	0.9788	V/V
	OS2	HL[2:0] (CFG1 register D[5:3]) = 010	0.9509	0.9609	0.9709	V/V
	OS3	HL[2:0] (CFG1 register D[5:3]) = 011	0.9392	0.9492	0.9492	V/V
	OS4	HL[2:0] (CFG1 register D[5:3]) = 100	0.8416	0.8516	0.8616	V/V
	OS5	HL[2:0] (CFG1 register D[5:3]) = 101	0.7673	0.7773	0.7873	V/V
	OS6	HL[2:0] (CFG1 register D[5:3]) = 110	0.6189	0.6289	0.6389	V/V
	OS7	HL[2:0] (CFG1 register D[5:3]) = 111	0.5603	0.5703	0.5803	V/V
Over-Scale Threshold Tempco				**±3**		**ppm/°C**
Over-Scale Amplifier Offset				±9		mV
Over-Scale Amplifier Offset Drift				**±10**		**µV/°C**
Under-Scale Thresholds		V_{LIM} = 5V, register-selectable ratio of V_{LIM}				
	US7	LL[2:0] (CFG1 register D[2:0]) = 111	0.0487	0.0547	0.0607	V/V
	US6	LL[2:0] (CFG1 register D[2:0]) = 110	0.04478	0.05078	0.05678	V/V
	US5	LL[2:0] (CFG1 register D[2:0]) = 101	0.04088	0.04688	0.05288	V/V
	US4	LL[2:0] (CFG1 register D[2:0]) = 100	0.03306	0.03906	0.04506	V/V
	US3	LL[2:0] (CFG1 register D[2:0]) = 011	0.02916	0.03516	0.04116	V/V
	US2	LL[2:0] (CFG1 register D[2:0]) = 010	0.02525	0.03125	0.03725	V/V
	US1	LL[2:0] (CFG1 register D[2:0]) = 001	0.01743	0.02343	0.02943	V/V
	US0	LL[2:0] (CFG1 register D[2:0]) = 000	0.01353	0.01953	0.02553	V/V
Under-Scale Threshold Tempco				**±3**		**ppm/°C**
Under-Scale Amplifier Offset				±9		mV
Under-Scale Amplifier Offset Drift				**±10**		**µV/°C**
Output Voltage Clamp						
Input Voltage Range		$V_{CLAMP} \le V_S$, V_S = +5V	1.25		4.95	V
Input Bias Current				±60		nA
V_{OUT} Clamp Point			V_{CLAMP} – 0.05	V_{CLAMP}	V_{CLAMP} + 0.05	V
Fault Monitor Circuit (External Comparators)						
INP_HI Comparator Threshold INN_HI Comparator Threshold		Fault Detect Mode Select = 0 (bridge fault); see CFG1 register		Smaller of (V_S – 1.2) or (0.65V_{FLT})		V
INP_LO Comparator Threshold INN_LO Comparator Threshold		Fault Detect Mode Select = 0 (bridge fault); see CFG1 register		Larger of (0.1V) or (0.35V_{FLT})		V
Fault Monitor Reference	V_{FLT}	Fault Monitor Reference; see CFG1 register, FLT REF bit sets V_{FLT}		V_S or V_{REF}		V
INP_HI Comparator Threshold INN_HI Comparator Threshold		Fault Detect Mode Select = 1 (common-mode fault); see CFG1 register		V_S – 1.2		V
INP_LO Comparator Threshold INN_LO Comparator Threshold		Fault Detect Mode Select = 1 (common-mode fault); see CFG1 register	70	100	130	mV
Comparator Hysteresis				7		mV
Comparator Input Offset Voltage				±10		mV
Fault Monitor Circuit (Internal Comparators)						
A1SAT_LO Comparator Threshold A2SAT_LO Comparator Threshold		Threshold is amplifier negative saturation voltage		100		mV
A1SAT_HI Comparator Threshold A2SAT_HI Comparator Threshold		Threshold is amplifier positive saturation voltage		V_S – 0.12		V
A3SAT_LO Comparator Threshold		Threshold is amplifier negative saturation voltage		50		mV
V_{IN1}, V_{IN2} Pull-up Current Sources						
Pull-Up Current Source	I_{PU}	Register-selectable	15	30	45	nA
Current Source Matching				±1.5	±7	nA
Current Source Tempco				**±5**		**pA/°C**

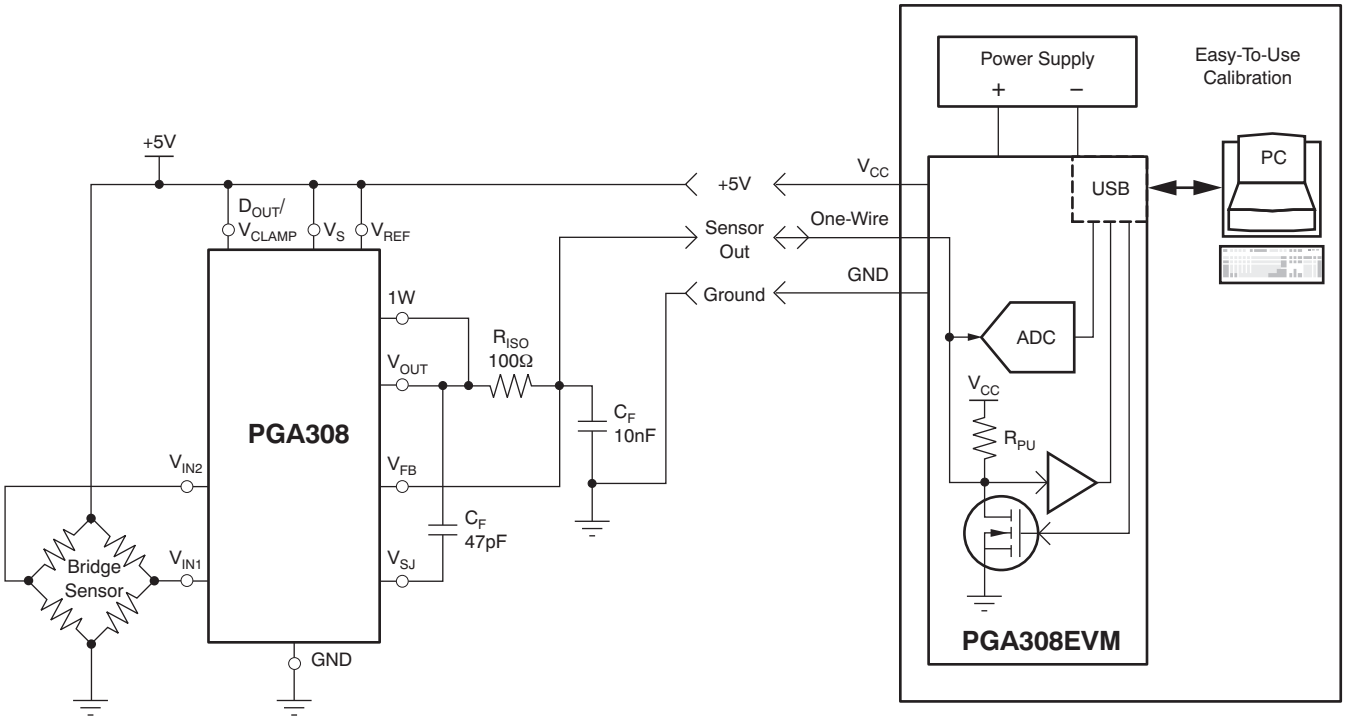
ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +5V, GND = 0V, D_{OUT}/V_{CLAMP} = +5V, and V_{REF} = +5V, unless otherwise noted.

PARAMETER		CONDITIONS	PGA308-Q1[1] MIN	TYP	MAX	UNIT
V_{REF}						
Input Range			1.8		V_S	V
Input Resistance				43		kΩ
Digital Interface						
One-Wire		Serial speed baud rate	4.8k		114k	bits/s
Logic Levels						
Logic Levels (1W pin)		Low			0.8	V
		High	2.0			V
		Hysteresis		100		mV
Output Low Level (1W pin)		Open drain, I_{SINK} = 4mA			0.5	V
Output Levels (D_{OUT}/V_{CLAMP})		Low, D_{OUT} mode selected, I_{SINK} = 4mA and V_S = +4.5V, or I_{SINK} = 2mA and V_S = +2.7V			0.4	V
		High, D_{OUT} mode selected, I_{SOURCE} = 4mA and V_S = +4.5V, or I_{SOURCE} = 2mA and V_S = +2.7V	V_S – 0.4			V
POWER SUPPLY						
Supply Voltage	V_S		2.7		5.5	V
OTP Program Voltage	V_{S-PGM}		4.5		5.5	V
Quiescent Current	I_Q	V_S = +5V, does not include I_{REF}		1.3	1.6	mA
Shutdown Supply Current	I_{SHDN}	V_S = +5V, does not include I_{REF} (8)		260		µA
POWER-ON RESET (POR)						
Power-Up Threshold		V_S rising		2.1		V
Power-Down Threshold		V_S falling		1.7		V
TEMPERATURE RANGE						
Specified Performance Range			–40		+125	°C
Operational-Degraded Performance Range			–40		+150	°C
Thermal Resistance						
MSOP-10, Junction-to-Ambient	θ_{JA}			150		°C/W

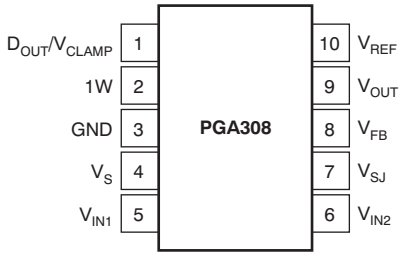
(8) I_{REF} current load is typically 100µA while in Shutdown mode. Although the output amplifier is disabled in Shutdown mode, RFO and RGO (180kΩ typical total) remain connected in series between V_{FB} and GND while in Shutdown mode. See Figure 37, *Detailed Block Diagram*, for more information.

TYPICAL THREE-WIRE APPLICATION CIRCUIT

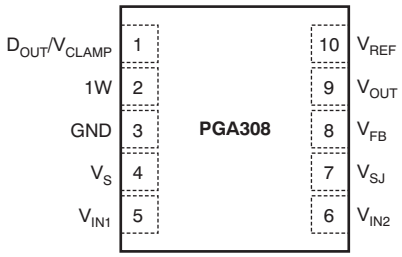


PIN CONFIGURATIONS

DGS PACKAGE
MSOP-10
(TOP VIEW)



DRK PACKAGE
3x4 DFN-10
(TOP VIEW)



PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	D_{OUT}/V_{CLAMP}	Dual-use pin: Output voltage clamp limit for V_{OUT} or programmable digital output. The output voltage clamp function is for use in multiple supply systems where the PGA308-Q1 may be at V_S = +5V and the system analog-to-digital converter (ADC) is powered at +3V. Setting V_{CLAMP} to +3.2V prevents over-voltage and latch-up on the system ADC input. V_{CLAMP} may be set through a resistor divider from V_S. If configured for digital output, the D_{OUT} function allows for configuration plus calibration of a sensor module either through the One-Wire interface (1W pin) or as a permanently configured module through the power-on reset (POR) OTP memory setting.
2	1W	One-Wire interface program pin. UART interface for digital calibration of the PGA308-Q1 over a single wire. Can be connected to V_{OUT} for a three terminal (V_S, GND, V_{OUT}) programmable sensor assembly.
3	GND	Ground.
4	V_S	+Voltage supply.
5	V_{IN1}	Signal input voltage 1. Connect to + or – output of the sensor bridge. Internal multiplexer can change connection internally to front-end PGA.
6	V_{IN2}	Signal input voltage 2. Connect to + or – output of the sensor bridge. Internal multiplexer can change connection internally to front-end PGA.
7	V_{SJ}	Output amplifier summing junction. Use for output amplifier compensation when driving large capacitive loads (> 200pF) and/or for using external gain setting resistors for the output amplifier.
8	V_{FB}	V_{OUT} feedback pin. Voltage feedback sense point for over-/under-scale limit circuitry. If internal gain set resistors for the output amplifier are used, this pin is also the voltage feedback sense point for the output amplifier. V_{FB} in combination with V_{SJ} allows for use of external filter and protection circuits without degrading the PGA308-Q1 V_{OUT} accuracy. V_{FB} must always be connected to either V_{OUT} or the point of feedback for V_{OUT} if external filtering is used.
9	V_{OUT}	Analog output voltage of conditioned sensor.
10	V_{REF}	Reference voltage input pin. V_{REF} is used for coarse offset adjust and Zero DAC. V_{REF} or V_S may be individually selected for over-/under-scale threshold reference and fault monitor comparator reference.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = V_{REF} = D_{OUT}/V_{CLAMP} = +5V, R_L = 10kΩ and C_L = 100pF connected to GND, unless otherwise noted. Gain format is presented: G = FE-PGA × Fine Gain × Output Gain.

FRONT-END PGA INPUT BIAS CURRENT WITH I_{PU} ENABLED vs TEMPERATURE

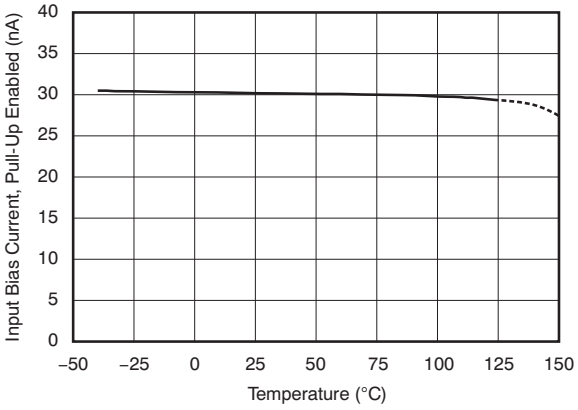


Figure 1.

FRONT-END PGA INPUT BIAS CURRENT WITH I_{PU} DISABLED vs TEMPERATURE

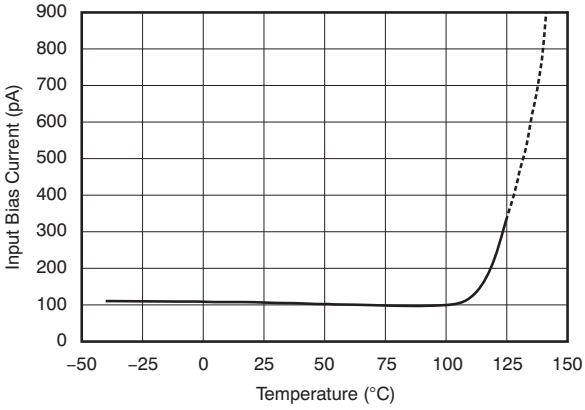


Figure 2.

COARSE OFFSET ADJUST ERROR vs TEMPERATURE

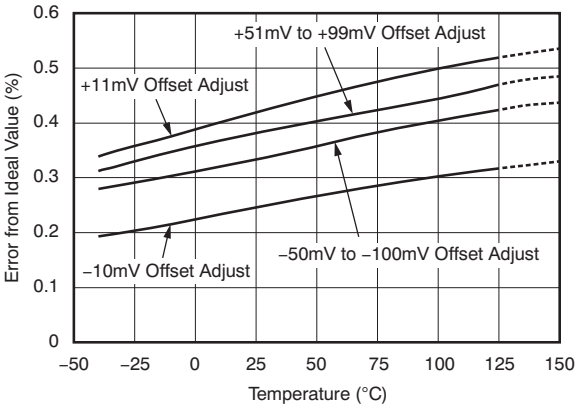


Figure 3.

FRONT-END PGA OFFSET VOLTAGE vs TEMPERATURE

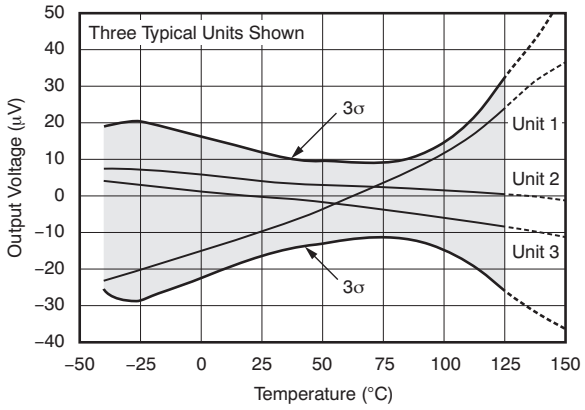


Figure 4.

0.1Hz TO 10Hz OUTPUT NOISE (G = 1600)

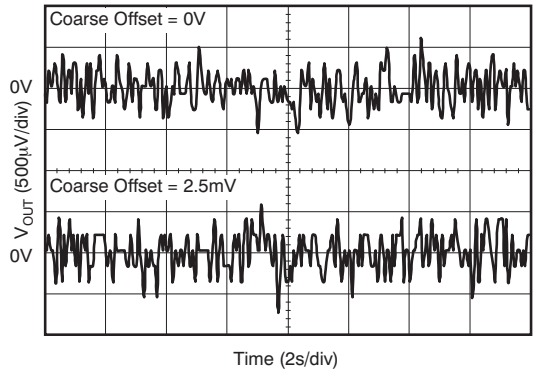


Figure 5.

INPUT-REFERRED FRONT-END NOISE vs FREQUENCY

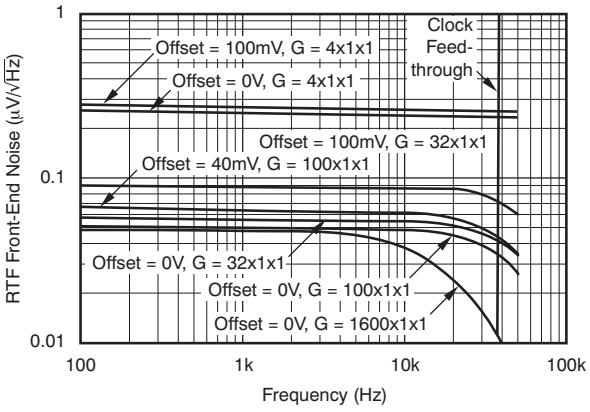


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_{REF} = D_{OUT}/V_{CLAMP} = +5V, R_L = 10kΩ and C_L = 100pF connected to GND, unless otherwise noted.

Gain format is presented: G = FE-PGA × Fine Gain × Output Gain.

OVER-SCALE TOTAL ERROR vs TEMPERATURE (5V Ref)

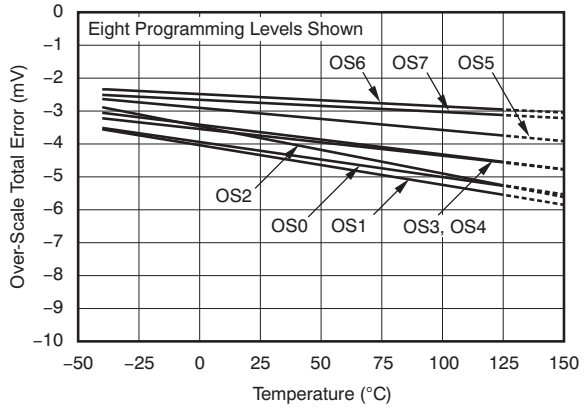


Figure 7.

UNDER-SCALE TOTAL ERROR vs TEMPERATURE (4V Ref)

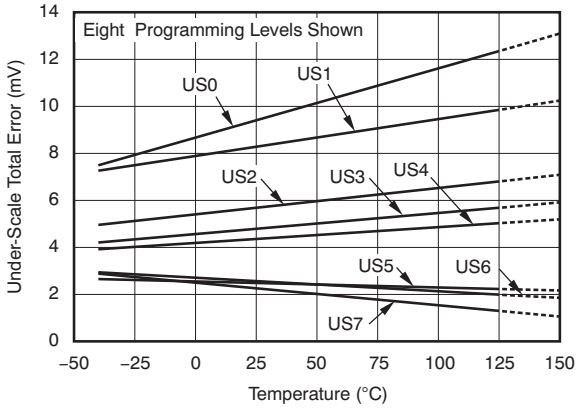


Figure 8.

ZERO DAC OFFSET ERROR vs TEMPERATURE

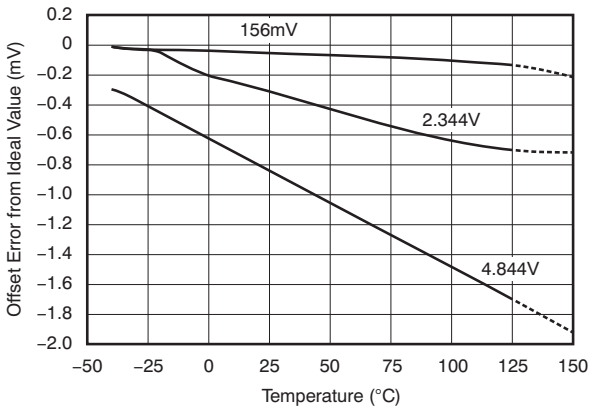


Figure 9.

COMMON-MODE REJECTION (RTI) vs FREQUENCY

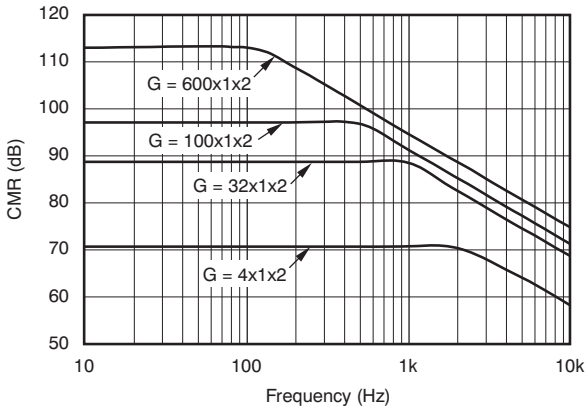


Figure 10.

POWER-SUPPLY REJECTION RATIO (RTI) vs FREQUENCY

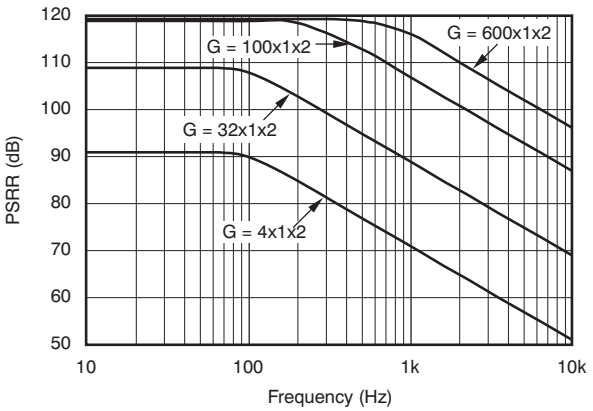


Figure 11.

GAIN vs FREQUENCY

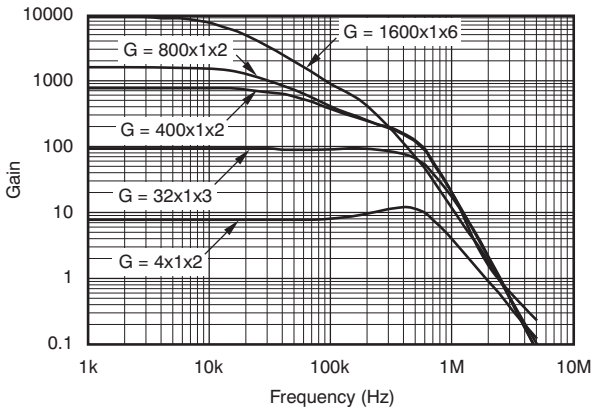


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_{REF} = D_{OUT}/V_{CLAMP} = +5V, R_L = 10kΩ and C_L = 100pF connected to GND, unless otherwise noted.

Gain format is presented: G = FE-PGA × Fine Gain × Output Gain.

V_{OUT} WITH V_{CLAMP} HIGH (4.94V) vs TEMPERATURE

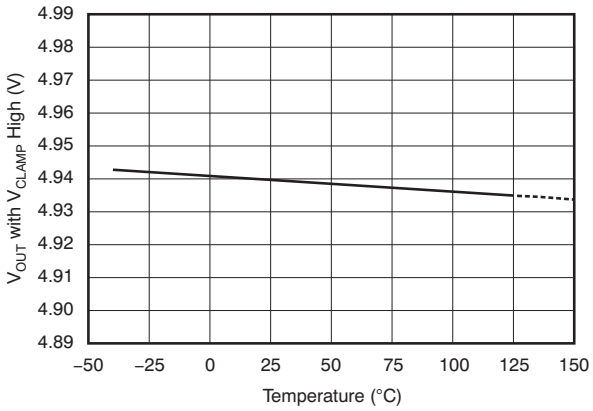


Figure 13.

V_{OUT} WITH V_{CLAMP} LOW (1.25V) vs TEMPERATURE

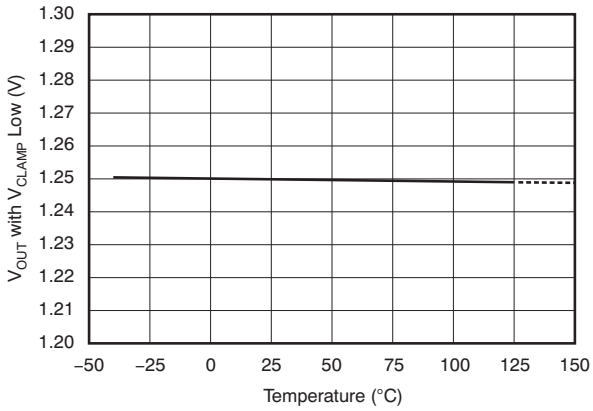


Figure 14.

COMMON-MODE OVER-VOLTAGE RECOVERY

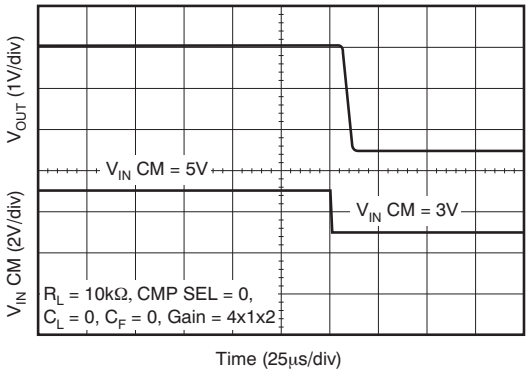


Figure 15.

V_{CLAMP} RESPONSE (No Cap Load, CMP SEL = 1)

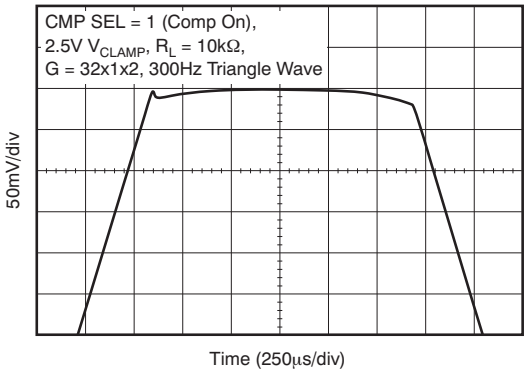


Figure 16.

V_{CLAMP} RESPONSE (No Cap Load, CMP SEL = 0)

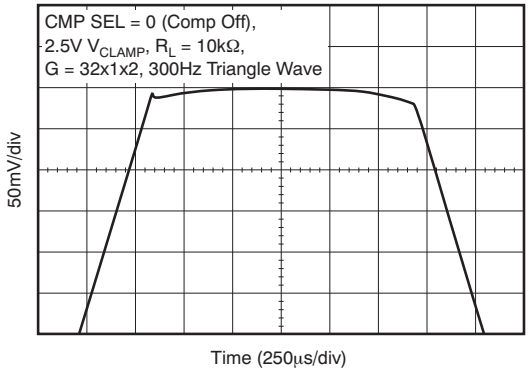


Figure 17.

V_{CLAMP} RESPONSE (C_L = 10nF, CMP SEL = 1)

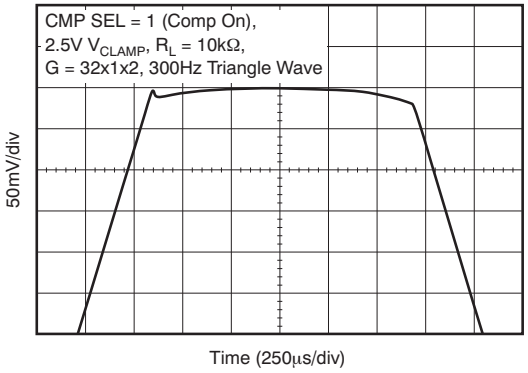


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_{REF} = D_{OUT}/V_{CLAMP} = +5V, R_L = 10kΩ and C_L = 100pF connected to GND, unless otherwise noted.

Gain format is presented: G = FE-PGA × Fine Gain × Output Gain.

V_{CLAMP} RESPONSE (C_L = 10nF, CMP SEL = 0)

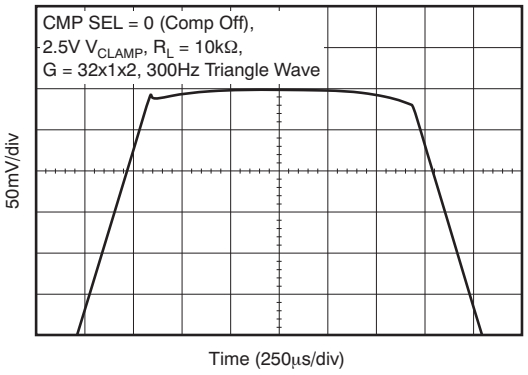


Figure 19.

OUTPUT VOLTAGE vs OUTPUT CURRENT

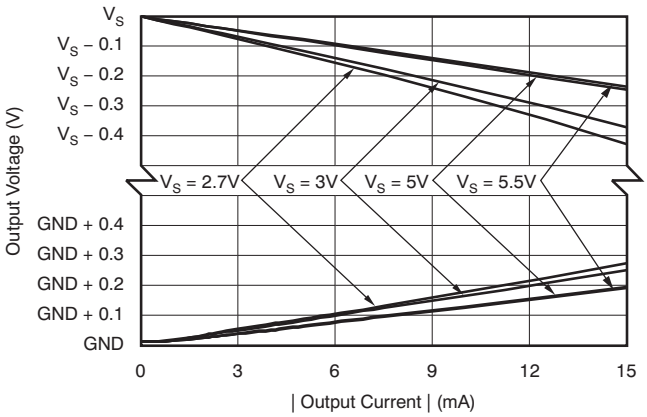


Figure 20.

QUIESCENT CURRENT vs TEMPERATURE

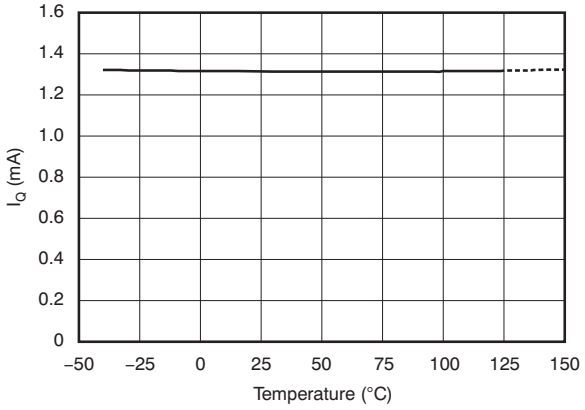


Figure 21.

OUTPUT AMPLIFIER OPEN-LOOP GAIN vs FREQUENCY (CMP SEL = 1)

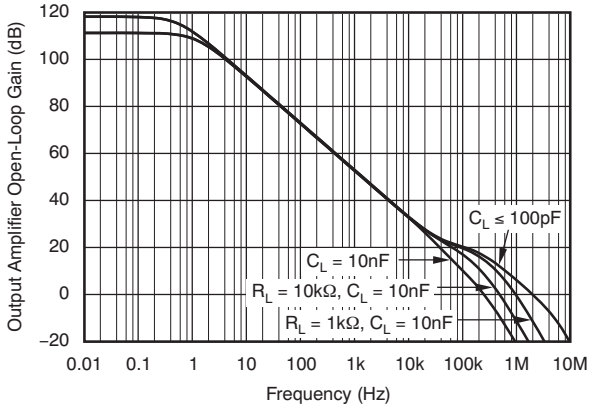


Figure 22.

OUTPUT AMPLIFIER OPEN-LOOP GAIN vs FREQUENCY (CMP SEL = 0)

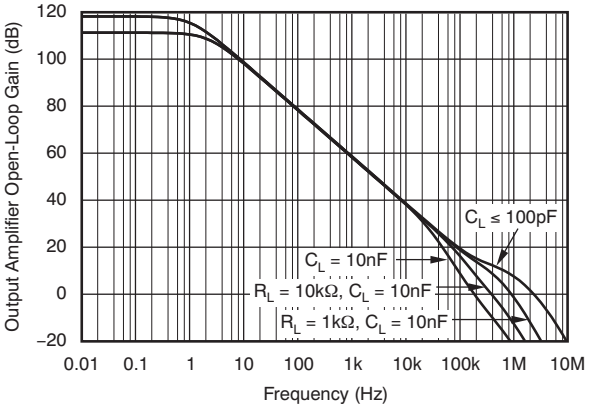


Figure 23.

OUTPUT AMPLIFIER OPEN-LOOP PHASE vs FREQUENCY (CMP SEL = 1)

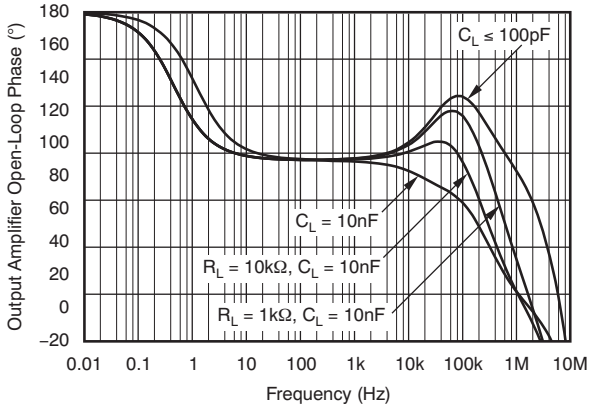


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_{REF} = D_{OUT}/V_{CLAMP} = +5V, R_L = 10kΩ and C_L = 100pF connected to GND, unless otherwise noted.

Gain format is presented: G = FE-PGA × Fine Gain × Output Gain.

OUTPUT AMPLIFIER OPEN-LOOP PHASE vs FREQUENCY (CMP SEL = 0)

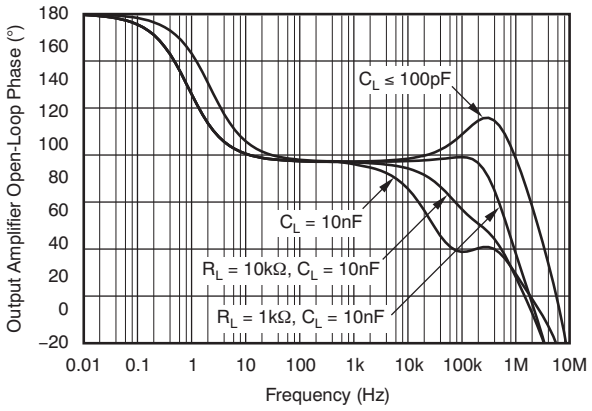


Figure 25.

CAPACITIVE LOAD DRIVE C_L = 1nF

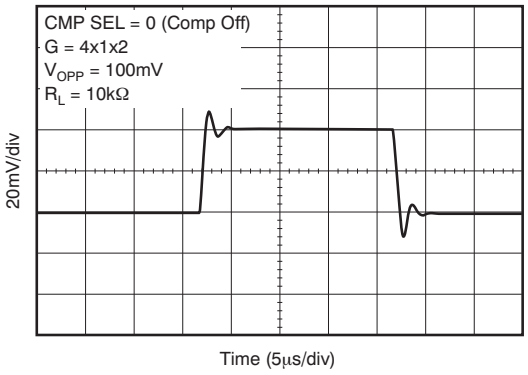


Figure 26.

CAPACITIVE LOAD DRIVE C_L = 10pF

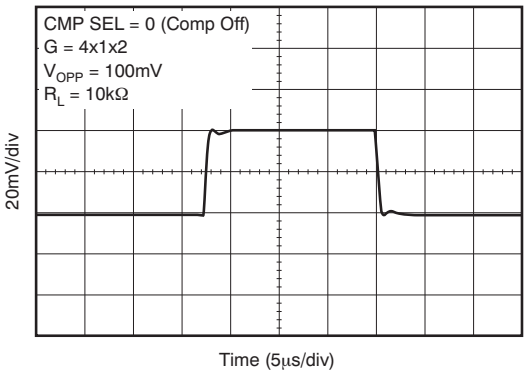


Figure 27.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

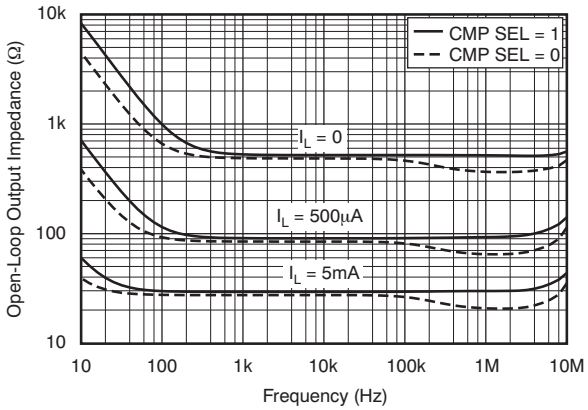


Figure 28.

SMALL-SIGNAL STEP RESPONSE CMP SEL = 1

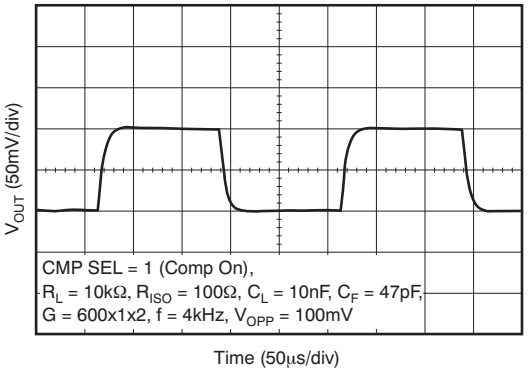


Figure 29.

LARGE-SIGNAL STEP RESPONSE CMP SEL = 1

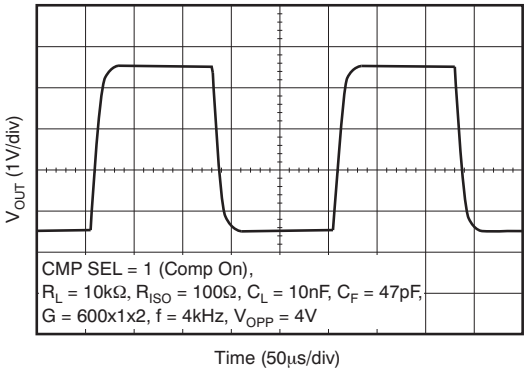


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_{REF} = D_{OUT}/V_{CLAMP} = +5V, R_L = 10kΩ and C_L = 100pF connected to GND, unless otherwise noted.

Gain format is presented: G = FE-PGA × Fine Gain × Output Gain.

SMALL-SIGNAL STEP RESPONSE
CMP SEL = 1

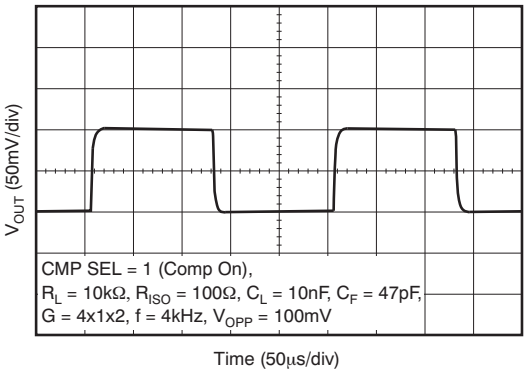


Figure 31.

LARGE-SIGNAL STEP RESPONSE
CMP SEL = 1

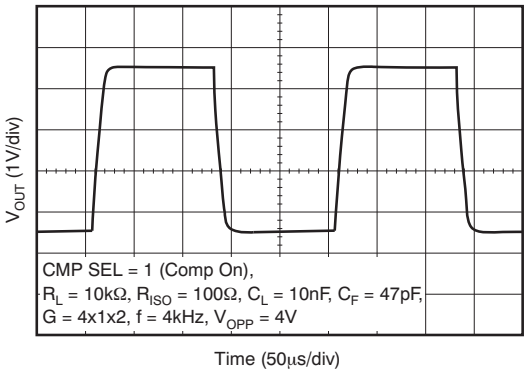


Figure 32.

SMALL-SIGNAL STEP RESPONSE
CMP SEL = 0

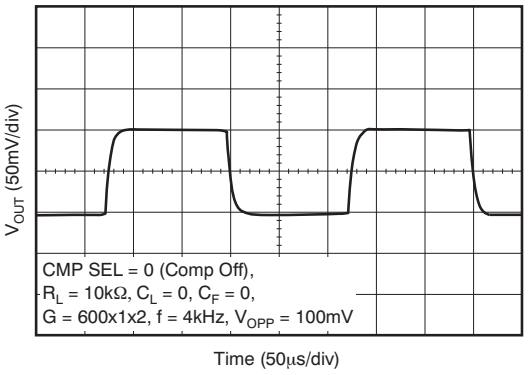


Figure 33.

LARGE-SIGNAL STEP RESPONSE
CMP SEL = 0

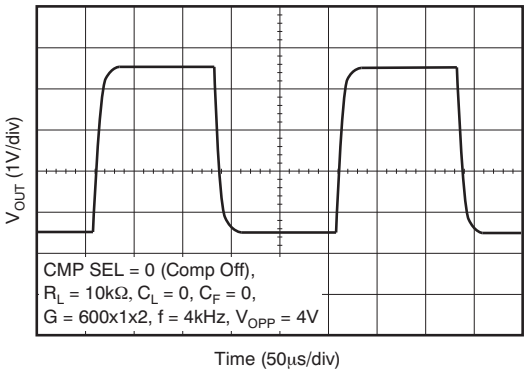


Figure 34.

SMALL-SIGNAL STEP RESPONSE
CMP SEL = 0

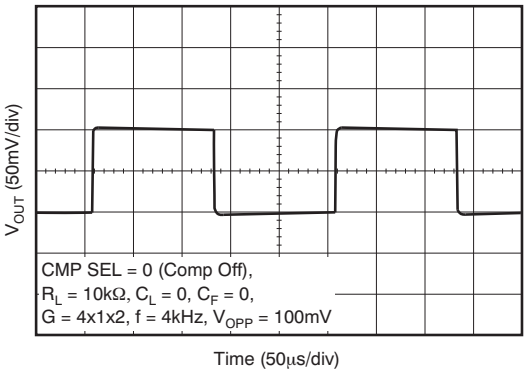


Figure 35.

LARGE-SIGNAL STEP RESPONSE
CMP SEL = 0

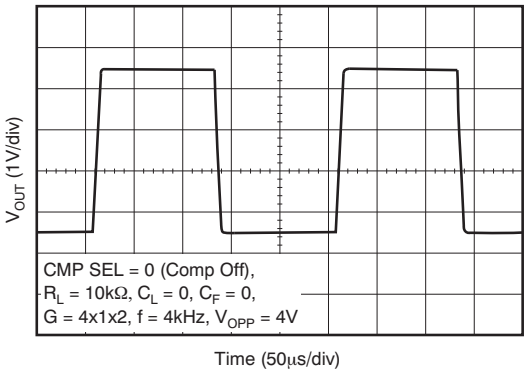


Figure 36.

FUNCTIONAL DESCRIPTION

OVERVIEW

The PGA308-Q1 is an ideal building block for resistive bridge sensor conditioning and general data acquisition. Digitally-programmable coarse offset, fine offset, and gain may be controlled in real time or permanently programmed into the PGA308-Q1.

SENSOR ERROR ADJUSTMENT RANGE

The PGA308-Q1 is designed to readily accommodate the following sensors:

$Span_{25°C}$: 0.08mV/V to 296mV/V

Initial Offset: 20mV/V

Span and offset are based on a bridge sensor excitation voltage of +5V, a PGA308-Q1 output voltage span of 4V (+0.5V to +4.5V), V_{REF} of +5V, and a V_{OUT}/V_{IN} gain up to 9600. For proper PGA308-Q1 setup, consider noise, small-signal bandwidth, V_{OUT}/V_{IN} gain, and required system error.

AMPLIFICATION SIGNAL PATH

The core of the PGA308-Q1 is a precision, low drift, and low noise front-end programmable gain amplifier (PGA). This front-end PGA has gain capabilities from x4 to x1600. The output amplifier has a gain range from ×2 to ×6. A fine gain adjust in front of the output amplifier offers a selectable ×0.33 to ×1.0 *attenuation factor*. This architecture yields a V_{OUT}/V_{IN} gain range for the PGA309 of ×2.67 to ×9600. Many applications use overall gains of ×1600 or less. The selection of gains in the front-end PGA and output amplifier, although capable of up to ×9600 overall gain, are intended to allow for gain distribution throughout the PGA308-Q1; this design enables optimum span and offset scaling from input to output. The polarity of the inputs can be switched through the input mux to accommodate sensors with unknown polarity output. Higher gains reduce bandwidth and require more analog filtering and/or system analog-to-digital converter (ADC) averaging to reject noise.

COARSE AND FINE OFFSET ADJUSTMENT

The sensor offset adjustment is done in two stages. The input-referred Coarse Offset Adjust DAC has a ±100mV offset adjustment range for a selected V_{REF} of +5V. Any residual input sensor offset is corrected and any desired V_{OUT} offset pedestal for zero-applied sensor strain input is set by a Fine Offset Adjust through the 16-bit Zero DAC that adds to the signal from the output of the front-end PGA.

VOLTAGE REFERENCE

The PGA308-Q1 V_{REF} pin provides input from a reference voltage. The reference voltage is used by the Coarse Offset Adjust and Zero DACs. The fault monitor circuitry trip points, as well as the over- and under-scale limits, can be selected to be referenced to either V_S or V_{REF}. This flexibility accommodates absolute or ratiometric mode designs.

FAULT MONITOR CIRCUIT SENSOR FAULT DETECTION

To detect sensor burnout and/or short, a set of four comparators (external fault comparators) are connected to the inputs of the front-end PGA. There are two fault-detect modes of operation for these comparators.

Common-Mode Fault

If either of the inputs are taken outside of the common-mode range of the amplifier [greater than (V_S – 1.2V), or less than 100mV], then the corresponding comparator sets a sensor fault flag that can be programmed to drive the PGA308-Q1 V_{OUT} to within 100mV (I_{OUT} < 4mA) of either V_S (or V_{CLAMP} if V_{CLAMP} is used) or ground. This level is well above the set over-scale limit level or well below the set under-scale limit level. The state of the fault condition can be read in digital form in the ALRM register. If the over-scale/under-scale limiting is disabled, the PGA308-Q1 output voltage is also driven within 100mV (I_{OUT} < 4mA) of either V_S (or V_{CLAMP} if V_{CLAMP} is used) or ground, depending on the selected fault polarity (high or low).

Bridge Fault

To assist in identifying mis-wiring, or open- or short-circuit conditions, the PGA308-Q1 provides bridge fault monitoring. For bridge fault detection, either V_S or V_{REF} (whichever is used for bridge excitation) can be chosen as V_{FLT}. If either of the inputs are taken to less than the larger of either 100mV or $0.35V_{FLT}$, then a fault is signaled. Also, if either of the inputs is taken to greater than the smaller of (V_S – 1.2V) or $0.65V_{FLT}$, then a fault is signaled. This fault detection allows for operation with bridge differential voltages of up to 30% of the bridge excitation voltage. The corresponding comparator sets a sensor fault flag that can be programmed to drive the PGA308-Q1 V_{OUT} to within 100mV (I_{OUT} < 4mA) of either V_S (or V_{CLAMP} if V_{CLAMP} is used) or ground. This level is well above the set over-scale limit level or well below the

set under-scale limit level. If over-scale/under-scale limiting is disabled, the PGA308-Q1 output voltage is driven within 100mV (I_{OUT} < 4mA) of either V_S or ground, depending on the selected fault polarity (high or low).

Additional Fault Detection

There are five additional fault detect comparators (internal fault comparators) that help detect subtle PGA308-Q1 front-end violations that could result in linear voltages at V_{OUT} and be interpreted as valid states. These comparators are especially useful during factory calibration and setup.

Alarm Register

Each of nine fault conditions sets a corresponding bit in the Alarm register. The state of the fault condition can be read digitally from the Alarm register.

OVER-SCALE AND UNDER-SCALE LIMITS

The over-scale and under-scale limit circuitry provides a programmable upper and lower clip limit for the PGA308-Q1 output voltage. When combined with the fault monitor circuitry, system diagnostics can be performed to determine if a conditioned sensor is defective, or if the process being monitored by the sensor is out of range. The selected PGA308-Q1 V_{LIM} is divided down by a precision resistor string to form the over- and under-scale trip points. These resistor ratios are extremely accurate and produce no significant initial or temperature errors. An over-scale amplifier driven by the over-scale threshold limits (clips) the maximum PGA308-Q1 output, V_{OUT}. Similarly, an under-scale amplifier driven by the under-scale threshold limits (clips) the minimum PGA308-Q1 output, V_{OUT}. The reference for the trip points, V_{LIM}, is register-selectable for either V_{REF} or V_S.

D_{OUT}/V_{CLAMP} PIN

The dual-use D_{OUT}/V_{CLAMP} pin functions either as a V_{OUT} clamp or as a digital push-pull output. The voltage clamp function provides an output voltage clamp, which is external-resistor programmable. In mixed-voltage systems, where the PGA308-Q1 may run from +5V with its output scaled for 0.1V to 2.9V, V_{CLAMP} can be set to 3.0V to prevent an over-voltage lock-up/latch-up condition on a 3V system ADC or microcontroller input. When programmed as a digital output this pin can be used for sensor module configuration. The value may be pre-programmed in the one-time programmable (OTP) banks, or controlled through the One-Wire interface (1W pin).

DIGITAL INTERFACE: ONE-WIRE PROGRAM PROTOCOL

The PGA308-Q1 can be configured through a single-wire, UART-compatible interface (1W pin). It is possible to connect this single-wire communication pin to the V_{OUT} pin in true three-terminal modules (V_S, ground, and sensor out) and continue to allow for calibration and configuration programming.

All communication transactions start with an initialization byte transmitted by the controller. This byte (55h) sets the baud rate used for the communication transaction. The baud rate is sensed during the initialization byte of every transaction, and is used throughout the entire transaction. Each transaction may use a different baud rate, if desired. Baud rates of 4.8k to 114k bits/second are supported.

Each communication consists of several bytes of data. Each byte consists of 10-bit periods. The first bit is the start bit and is always '0'. When idle, the 1W pin should always be high. The second through ninth bits are the eight data bits for the byte and are transferred LSB first. The 10th bit is the stop bit and is always '1'.

The second byte is a command/address byte. The last bit in this byte indicates either a read or write at the address selected by the address pointer portion of the byte. Additional data transfer occurs after the command/address byte. The number of bytes and direction of data transfer depend on the command byte. For a read sequence, the PGA308-Q1 waits for a 2-bit delay (unless programmed otherwise) after the completion of the command/address byte before beginning to transmit. This wait allows time for the controller to ensure that the PGA308-Q1 is able to control the One-Wire interface. The first byte transmitted by the PGA308-Q1 is the least significant byte of the register and the second byte will be the most significant byte of the register.

The recommended circuit implementation is to use a pull-up resistor and/or current source with an open drain (or open collector) output connected to the 1W pin, which is also an open drain output. The single wire can be driven high by the controller during transmit from the controller, but some form of pull-up is required to allow the signal to go high during receive because the PGA308-Q1 1W pin can only pull the output low.

Timeout on the One-Wire Interface

The PGA308-Q1 includes a timeout mechanism. If synchronization between the controller and the PGA308-Q1 is lost for any reason, the timeout mechanism allows the One-Wire interface to reset communication. The timeout period is set to approximately 28ms (typical). If the timeout period expires between the initialization byte and the command byte, between the command byte and any data byte, or between any data bytes, the PGA308-Q1 resets the One-Wire interface circuitry so that it expects an initialization byte. Every time that a byte is transmitted on the single wire interface, this timeout period restarts.

POWER-ON SEQUENCE

The PGA308-Q1 provides circuitry to detect when the power supply is applied to the PGA308-Q1 and resets the internal registers to a known power-on reset (POR) state. This reset also occurs whenever the supply is invalid so that the PGA308-Q1 is set to a known state when the supply becomes valid again. The threshold for this circuit is approximately 1.7V to 2.1V. After the power supply becomes valid, the PGA308-Q1 waits for approximately 25ms, during which V_{OUT} is disabled, and then attempts to read the data from the last valid OTP memory bank. If the memory bank has the proper checksum, then the PGA308-Q1 RAM is loaded with the OTP data and V_{OUT} enabled. If the checksum is invalid, V_{OUT} is set to disabled. Unless disabled by the OWD bit in Configuration Register 2 (CFG2), the One-Wire interface can always communicate to the PGA308-Q1 and override the contents of the current RAM in use by setting the appropriate SWL[2:0] bits in the Software Control Register (SFTC). For applications that require *instant-on* for V_{OUT}, the NOW bit in the CFG2 register can be set to '1', which eliminates the 25ms disable of V_{OUT} on power-up.

ONE-WIRE OPERATION WITH 1W CONNECTED TO V_{OUT}

In some sensor applications, it is desired to provide the end user of the sensor module with three pins: V_S, GND, and Sensor Out. It is also desired in these applications to digitally calibrate the sensor module after its final assembly of sensor and electronics. The PGA308-Q1 has a mode that allows the One-Wire interface pin (1W) to be tied directly to the PGA308-Q1 output pin (V_{OUT}).

To calibrate the PGA308-Q1 in Three-Wire configuration, program the internal registers and measure the resulting V_{OUT}. To do this while V_{OUT} is connected to 1W requires the ability to enable and disable V_{OUT}. Thus, the 1W/V_{OUT} line operates in a multiplexed mode where 1W is used as a bidirectional digital interface while V_{OUT} is disabled, and V_{OUT} drives the line as a conditioned sensor output voltage when it is enabled.

The PGA308-Q1 also provides a mode in which the output amplifier can be enabled for a set time period and then disabled again to allow sharing of the 1W pin with the V_{OUT} connection. This action is accomplished by writing a value to bits OEN[7:0] in the One-Wire Enable Control register (OENC). Any non-zero value enables the output. This non-zero value is decremented every 10ms until it becomes zero. When this value becomes zero, V_{OUT} is disabled and a 1s timeout begins waiting for bus activity on the digital interface (1W pin). As long as there is activity on the 1W pin, the 1s timeout is continually reset. After 1s of no bus activity, the PGA308-Q1 checks for a correct checksum. If the checksum is correct, the PGA308-Q1 runs with the values that currently exist in RAM. If the checksum is not valid, the PGA308-Q1 checks for written bank select registers in OTP in the order of BANK SEL4, BANK SEL3, BANK SEL2 then BANK SEL1. The highest bank select register containing valid programmed data is read. The value read from this register points to one of the seven OTP banks, which is then loaded into RAM.

OTP MEMORY BANKS

There are four one-time programmable (OTP) bank selection registers: BANK SEL1, BANK SEL2, BANK SEL3, and BANK SEL4. Bank selection may be set four times by programming the BANK SELx registers in order (1, 2, 3, 4). The default OTP bank used on POR is the location stored in the last programmed BANK SELx register. Therefore, if programmed, BANK SEL4 always has priority over lower-numbered bank select registers.

The PGA308-Q1 contains seven OTP user memory banks. All seven of these banks may be independently programmed. However, the default bank at POR can be set only four times. The seven possible OTP user memory banks allow an end product with a microcontroller interface between the end-user and the PGA308-Q1 to select from up to seven factory pre-programmed configurations. It also provides total user flexibility for any other configuration through software communication over the One-Wire interface (1W pin). This flexibility allows no-scrap recovery from miscalibration situations.

PGA308-Q1 TRANSFER FUNCTION

Equation 1 shows the mathematical expression that is used to compute the output voltage, V_{OUT}. This equation can also be rearranged algebraically to solve for different terms. For example, during calibration, this equation is rearranged to solve for V_{IN}.

$$V_{OUT} = \left[\left(\text{mux\_sign} \bullet V_{IN} + V_{Coarse\_Offset}\right) \bullet GI + V_{Zero\_DAC}\right] \bullet GD \bullet GO \quad (1)$$

Where:

mux_sign: This term changes the polarity of the input signal; value is ±1

V_{IN}: The input signal for the PGA308-Q1; $V_{IN}1 = V_{INP}$, $V_{IN}2 = V_{INN}$

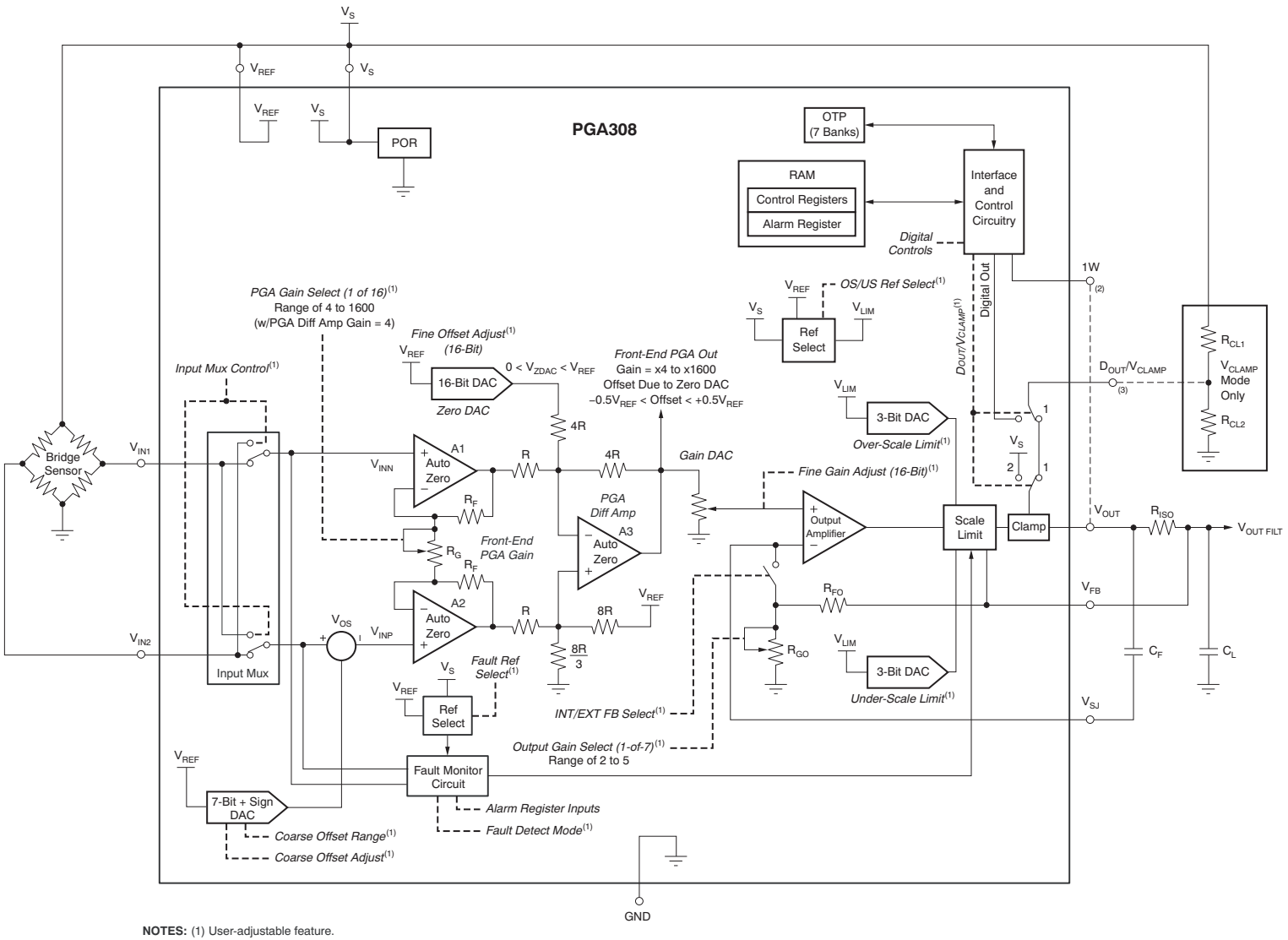
V_{Coarse_Offset}: The coarse offset DAC output voltage

GI: Input stage gain

V_{Zero_DAC}: Zero DAC output voltage

GD: Gain DAC

GO: Output stage gain



NOTES: (1) User-adjustable feature.
(2) Optional connection; see the *One-Wire Operation with 1W Connected to VOUT* section for more information.
(3) Optional connection; see the PGA308 User's Guide for more information.

Figure 37. Detailed Block Diagram

REVISION HISTORY

Changes from Original (March 2012) to Revision A	Page
• Changed Removed External Sensor Output Sensitivity from Electrical Characteristics table and added it to the table notes.	4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PGA308AQDGSRQ1	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JAAQ
PGA308AQDGSRQ1.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JAAQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF PGA308-Q1 :

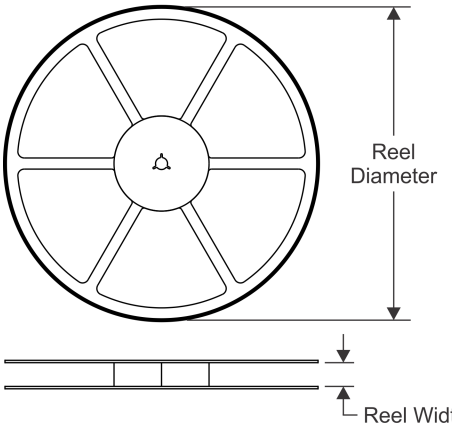
- Catalog : PGA308

NOTE: Qualified Version Definitions:

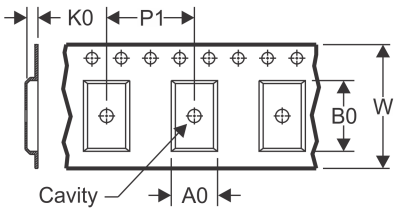
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

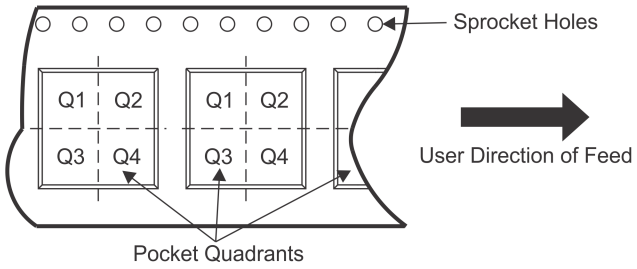


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

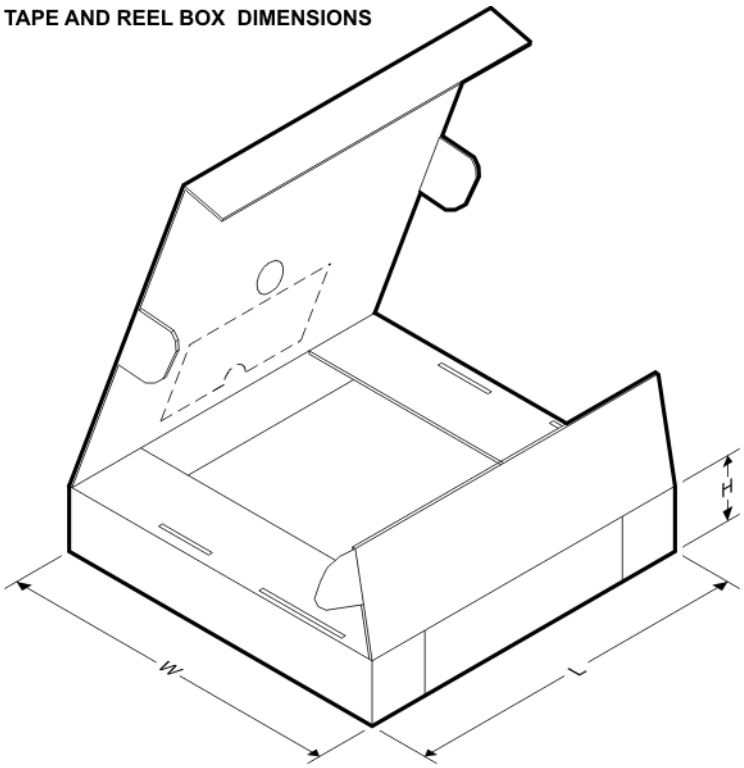
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA308AQDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

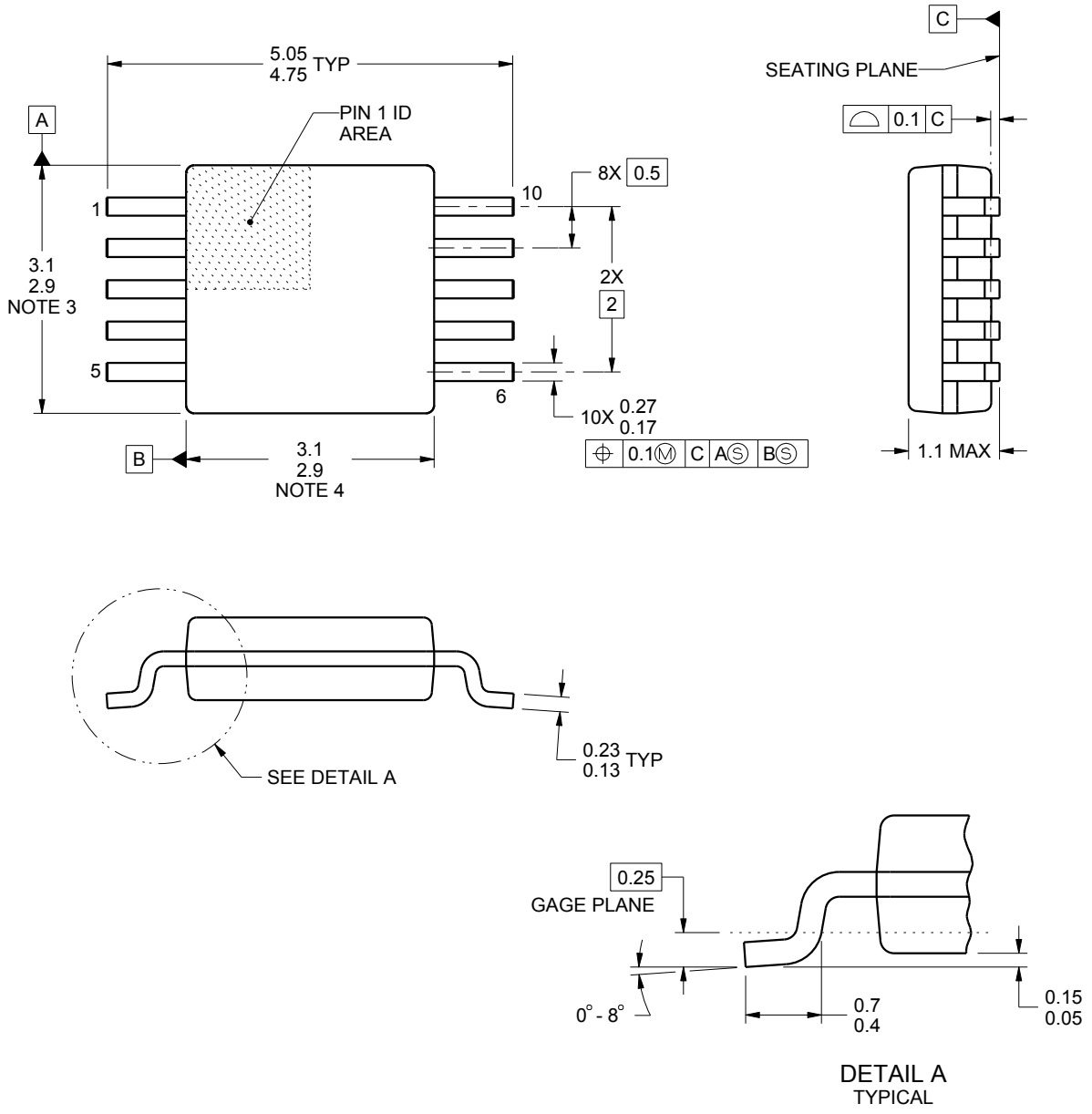
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA308AQDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

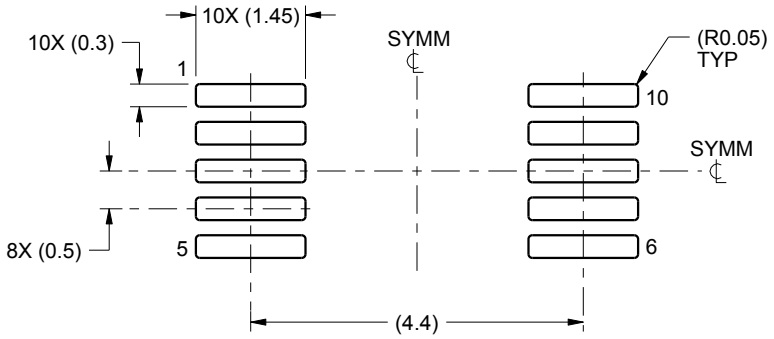
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

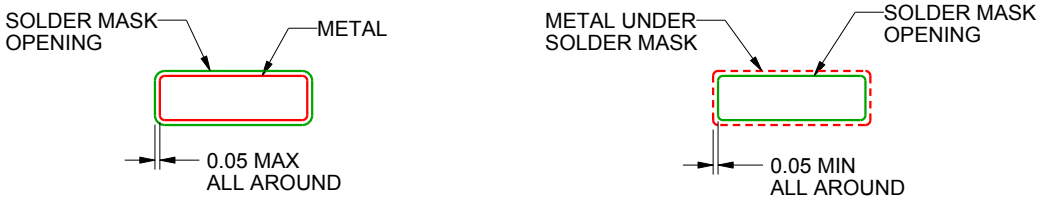


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

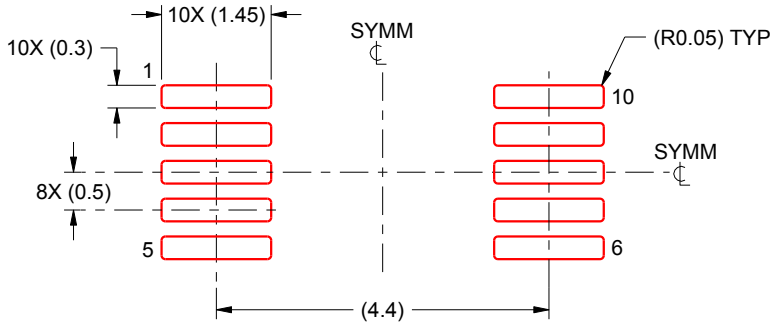


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月