电压输出可编程传感器调节器

查询样片: PGA309-HT

特性

- 完整的桥式传感器调节器
- 电压输出：成比例或绝对值
- 数字计算：无电位器/传感器调整
- 传感器误差补偿
  - 跨度、偏移和温度漂移
- 低误差、时间稳定
- 传感器线性化电路
- 温度感测：内部或外部
- 校准查询表逻辑
  - 使用外部 **EEPROM**（小外形尺寸晶体管 **(SOT)23-5** 封装）
- 过量程/欠量程限制
- 传感器故障检测
- **+2.7V** 至 **+5.5V** 工作电压范围
- 小型薄型小尺寸 **(TSSOP)-16** 封装

应用范围

- 桥式传感器
- 远程 **4-20mA** 发射器
- 应变、负载和衡器
- 车载传感器

支持极端温度环境下的应用

- 受控基线
- 同一组装和测试场所
- 同一制造场所
- 极端（**-55°C** 至 **150°C**）温度范围内可用 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性
- 德州仪器 **(TI)** 高温产品利用高度优化的硅（芯片）解决方案，此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大幅提高性能。 在最大额定温度下，器件可连续正常运行 **1000** 小时。

评估工具

- 硬件设计人员套件 **(PGA309EVM)**
  - **PGA309 +** 传感器的温度评估
  - **PGA309** 完全编程
  - 传感器补偿分析工具

(1) 可定制工作温度范围

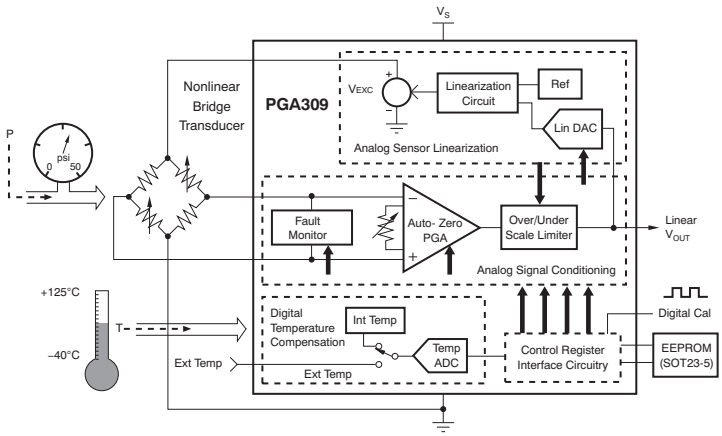
说明

PGA309 是为电桥传感器设计的可编程模拟信号调节器。 模拟信号路径可以放大传感器信号，并通过外加应力（压力、应变等）为零、跨度、零漂移、跨度漂移和传感器线性化误差提供数字校准。 通过 1 线数字串行接口或 2 线行业标准连接进行校准。 校准参数存储在外部非易失性存储器（通常为 SOT23-5），无需手动修整并可以实现长期稳定性。

全部模拟信号路径包含一个 2 x 2 输入复用器 (mux)，自动归零可编程增益仪表放大器，线性化电路，电压基准，内部振荡器，控制逻辑和一个输出放大器。 可编程电平位移对传感器直流偏移做出补偿。

PGA309 的内核是精密、低漂移、无 1/f 噪声前端 PGA（可编程增益放大器）。 前端 PGA + 输出放大器的总体增益可在 2.7V/V 至 1152V/V 之间进行调节。可通过输入复用器来切换输入的极性，以使传感器适应未知的极性输出。 故障监控电路检测并发出传感器烧断、过载、和系统故障状态信号。

要获得参考应用信息，请参阅商用器件《PGA309 用户指南》（文献号：SBOU024），此文件可从www.ti.com 内下载。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 150°C	TSSOP-16 (PW)	PGA309ASPWT	PGA309AS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		PGA309	UNIT
Supply Voltage, V_{SD}, V_{SD}		+7.0	V
Input Voltage, V_{IN1}, V_{IN2}(2)		–0.3 to V_{SA} +0.3	V
Input Current, V_{FB}, V_{OUT}		±150	mA
Input Current		±10	mA
Output Current Limit		50	mA
Storage Temperature Range		–60 to +150	°C
Operating Temperature Range		–55 to +150	°C
Junction Temperature		+170	°C
ESD Ratings	Human Body Model (HBM)	4	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

THERMAL INFORMATION

THERMAL METRIC(1)		PGA309-HT	UNITS
		PW	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	95.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	28.1	
θ_{JB}	Junction-to-board thermal resistance(4)	41.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	40.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：ZHCA543）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_J = –55°C to +150°C.**
At T_J = +25°C, V_{SA}= V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNIT
Front-End PGA + Output Amplifier					
V_{OUT}/V_{IN} Differential Signal Gain Range(1)	Fine gain adjust = 1		8 to 1152		V/V
	Front-End PGA Gains: 4, 8, 16, 23.27, 32, 42.67, 64, 128				
	Output Amplifier gains: 2, 2.4, 3, 3.6, 4.5, 6, 9				
Input Voltage Noise Density	f = 1kHz		210		nV/√Hz
V_{OUT} Slew Rate			0.5		V/µs
V_{OUT} Settling Time (0.01%)	V_{OUT}/V_{IN} Differential gain = 8, R_L = 5kΩ || 200pF		6		µs
V_{OUT} Settling Time (0.01%)	V_{OUT}/V_{IN} Differential gain = 191, R_L = 5kΩ || 200pF		4.1		µs
V_{OUT} Nonlinearity			0.002		%FSR
External Sensor Output Sensitivity	V_{SA} = V_{SD} = V_{EXC} = +5V		1 to 245		mV/V
Front-End PGA					
Auto-Zero Internal Frequency			7		kHz
Offset Voltage (RTI)(2)	**Coarse offset adjust disabled**		**±3**	**±70**	**µV**
vs Supply Voltage, V_{SA}			±2		µV/V
vs Common-Mode Voltage	G_F = Front-End PGA gain		1500/G_F	6500/G_F	µV/V
Linear Input Voltage Range(3)		**0.2**		**V_{SA} – 1.5**	**V**
Input Bias Current			0.1	1.5	nA
Input Impedance: Differential			30 || 6		GΩ || pF
Input Impedance: Common-Mode			50 || 20		GΩ || pF
Input Voltage Noise	0.1Hz to 10Hz, G_F = 128		4		μV_{PP}
PGA Gain					
Gain Range Steps	4, 8, 16, 23.27, 32, 42.67, 64, 128		4 to 128		V/V
Initial Gain Error	**G_F = 4 to 42**		**0.2**	**±1.3**	**%**
	G_F = 64		**0.25**	**±1.3**	**%**
	G_F = 128		**0.3**	**±1.6**	**%**
vs Temperature			**10**		**ppm/°C**
Output Voltage Range			**0.05 to V_{SA} – 0.1**		**V**
Bandwidth	Gain = 4		400		kHz
	Gain = 128		60		kHz
Coarse Offset Adjust (RTI of Front-End PGA)					
Range	±(14)(V_{REF})(0.00085)	±56	±59.5	±64	mV
vs Temperature			**0.004**		**%/°C**
Drift	±14 steps, 4-bit + sign		4		mV
Fine Offset Adjust (Zero DAC) (RTO of the Front-End PGA)(2)					
Programming Range		0		V_{REF}	V
Output Voltage Range		0.1		V_{SA} – 0.1	V
Resolution	65,536 steps, 16-bit DAC		73		µV
Integral Nonlinearity			20		LSB
Differential Nonlinearity			0.5		LSB
Gain Error			0.1		%
Gain Error Drift			10		ppm/°C
Offset			5		mV
Offset Drift			10		µV/°C

(1) PGA309 total differential gain from input (V_{IN1} – V_{IN2}) to output (V_{OUT}). V_{OUT} / (V_{IN1} – V_{IN2}) = (Front-end PGA gain) × (Output Amplifier gain) × (Gain DAC).
(2) RTI = Referred-to-input. RTO = referred to output.
(3) Linear input range is the allowed min/max voltage on the V_{IN1} and V_{IN2} pins for the input PGA to continue to operate in a linear region. The allowed common-mode and differential voltage depends on gain and offset settings. Refer to the *Gain Scaling* section for more information.

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_J = –55°C to +150°C.**
At T_J = +25°C, V_{SA}= V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309			UNIT
		MIN	TYP	MAX	
Output Fine Gain Adjust (Gain DAC)					
Range			0.33 to 1		V/V
Resolution	65,536 steps, 16-bit DAC		10		µV/V
Integral Nonlinearity			20		LSB
Differential Nonlinearity			0.5		LSB
Output Amplifier					
Offset Voltage (RTI of Output Amplifier)(4)			3		mV
vs Temperature			**5**		**µV/°C**
vs Supply Voltage, V_{SA}			30		µV/V
Common-Mode Input Range		**0**		**V_S – 1.5**	**V**
Input Bias Current			100		pA
Amplifier Internal Gain					
Gain Range Steps	2, 2.4, 3, 3.6, 4.5, 6, 9		2 to 9		V/V
Initial Gain Error	**2, 2.4, 3.6**		**0.25**	**±1.1**	**%**
	4.5		**0.3**	**±1.3**	**%**
	6		**0.4**	**±1.6**	**%**
	9		**0.6**	**±2.0**	**%**
vs Temperature	**2, 2.4, 3.6**		**5**		**ppm/°C**
	4.5		**5**		**ppm/°C**
	6		**15**		**ppm/°C**
	9		**30**		**ppm/°C**
Output Voltage Range(5)	**R_L = 10kΩ**	**0.1**		**4.9**	**V**
Open-Loop Gain			115		dB
Gain-Bandwidth Product			2		MHz
Phase Margin	Gain = 2, C_L = 200pF		45		deg
Output Resistance	AC Small-signal, open-loop, f = 1MHz, I_O = 0		675		Ω
Over- and Under-Scale Limits	V_{REF} = 4.096				
Over-Scale Thresholds	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '000'		0.9708		
	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '001'		0.9610		
	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '010'		0.9394		
	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '011'		0.9160		
	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '100'		0.9102		
	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '101'		0.7324		
	Ratio of V_{REF}, Register 5—bits D5, D4, D3 = '110'		0.5528		
Over-Scale Comparator Offset		+6	+60	+114	mV
Over-Scale Comparator Offset Drift			+0.37		mV/°C
Under-Scale Thresholds	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '111'		0.0605		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '110'		0.0547		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '101'		0.0507		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '100'		0.0449		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '011'		0.0391		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '010		0.0352		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '001'		0.0293		
	Ratio of V_{REF}, Register 5—bits D2, D1, D0 = '000'		0.0254		
Under-Scale Comparator Offset		−7	−50	+93	mV
Under-Scale Comparator Offset Drift			−0.15		mV/°C

(4) RTI = Referred-to-input. RTO = referred to output.
(5) Unless limited by the over/under-scale setting.

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_J = –55°C to +150°C.**

At T_J = +25°C, V_{SA}= V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNIT
Fault Monitor Circuit					
INP_HI, INN_HI Comparator Threshold	See (6)		V_{SA} − 1.2 or V_{EXC} − 0.1		V
INP_LO, INN_LO Comparator Threshold		40	100		mV
A1SAT_HI, A2SAT_HI Comparator Threshold			V_{SA} − 0.12		V
A1SAT_LO, A2SAT_LO Comparator Threshold			V_{SA} − 0.12		V
A3_VCM Comparator Threshold			V_{SA} − 1.2		V
Comparator Hysteresis			20		mV
Internal Voltage Reference					
V_{REF1}	Register 3, bit D9 = 1	2.43	2.5	2.53	V
		2.18		**2.7**	**V**
V_{REF1} Drift vs Temperature			**+10**		**ppm/°C**
V_{REF2} I_{PU}	Register 3, bit D9 = 0	4.0	4.096	4.14	V
		3.85		**4.22**	**V**
V_{REF2} Drift vs Temperature			**+10**		**ppm/°C**
Input Current REF_{IN}/REF_{OUT}	Internal V_{REF} disabled		100		µA
Output Current REF_{IN}/REF_{OUT}	V_{SA} > 2.7V for V_{REF} = 2.5V		1		mA
	V_{SA} > 4.3V for V_{REF} = 4.096V		1		mA
Temperature Sense Circuitry (ADC)					
Internal Temperature Measurement	Register 6, bit D9 = 1				
Accuracy			±2		°C
Resolution	12-Bit + sign, twos complement data format		±0.0625		°C
Temperature Measurement Range		−55		+150	°C
Conversion Rate	R_1, R_0 = '11', 12-bit + sign resolution		24		ms
Temperature ADC					
External Temperature Mode	Temp PGA + Temp ADC		1 to 8		V/V
Gain Range Steps	G_{PGA} = 1, 2, 4, 8	GND −0.2		V_{SA} +0.2	V
Analog Input Voltage Range					
Temperature ADC Internal REF (2.048V)	Register 6, bit D8 = 1				
Full-Scale Input Voltage	(+Input) − (−Input)		±2.048/G_{PGA}		V
Differential Input Impedance			2.8/G_{PGA}		MΩ
Common-Mode Input Impedance	G_{PGA} = 1		3.5		MΩ
	G_{PGA} = 2		3.5		MΩ
	G_{PGA} = 4		1.8		MΩ
	G_{PGA} = 8		0.9		MΩ
Resolution	R1, R0 = '00', ADC2X = '0', conversion time = 8ms		11		Bits + Sign
	R1, R0 = '01', ADC2X = '0', conversion time = 32ms		13		Bits + Sign
	R1, R0 = '10', ADC2X = '0', conversion time = 64ms		14		Bits + Sign
	R1, R0 = '11', ADC2X = '0', conversion time = 128ms		15		Bits + Sign
Integral Nonlinearity			0.004		%
Offset Error	G_{PGA} = 1		1.2		mV
	G_{PGA} = 2		0.7		mV
	G_{PGA} = 4		0.5		mV
	G_{PGA} = 8		0.4		mV
Offset Drift	G_{PGA} = 1		1.2		µV/°C
	G_{PGA} = 2		0.6		µV/°C
	G_{PGA} = 4		0.3		µV/°C
	G_{PGA} = 8		0.3		µV/°C

(6) When V_{EXC} is enabled, a minimum reference selector circuit becomes the reference for the comparator threshold. This minimum reference selector circuit uses V_{EXC} − 100mV and V_{SA} − 1.2V and compares the V_{INX} pin to the lower of the two references. This configuration ensures accurate fault monitoring in conditions where V_{EXC} might be higher or lower than the input CMR of the PGA input amplifier relative to V_{SA}.

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_J = –55°C to +150°C.**
At T_J = +25°C, V_{SA}= V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

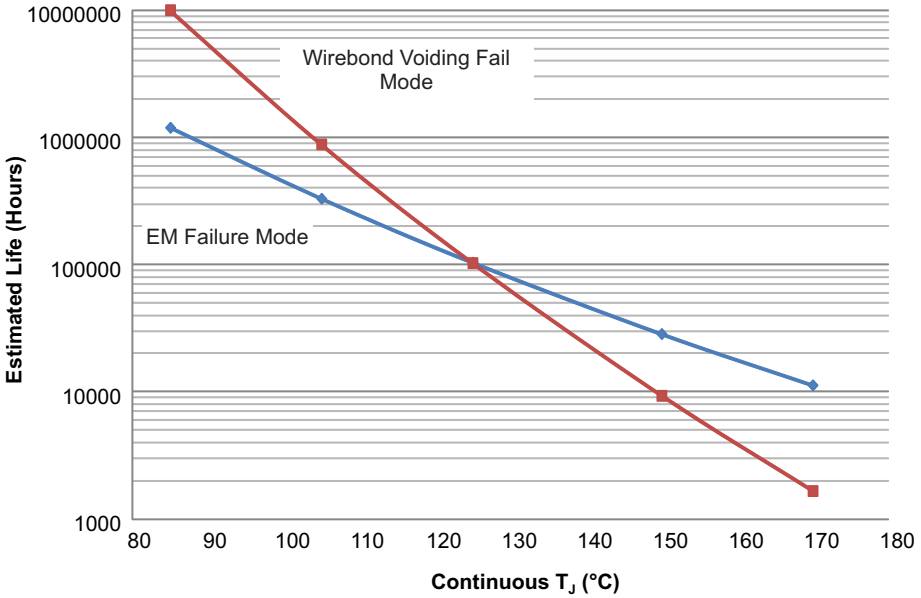
PARAMETER	CONDITIONS	PGA309			UNIT
		MIN	TYP	MAX	
Temperature ADC. *continued*					
Offset vs V_{SA}	G_{PGA} = 1		800		µV/V
	G_{PGA} = 2		400		µV/V
	G_{PGA} = 4		200		µV/V
	G_{PGA} = 8		150		µV/V
Gain Error			0.05	0.50	%
Gain Error Drift			5	50	ppm/°C
Noise	All gains		< 1		LSB
Gain vs V_{SA}			80		ppm/V
Common-Mode Rejection	At dc and G_{PGA} = 8		105		dB
	At dc and G_{PGA} = 1		100		dB
Temp ADC Ext. REF (V_{REFT} = V_{REF}, V_{EXC}, or V_{SA})	Register 6, bit D8 = 0				
Full-Scale Input Voltage	(+Input) − (−Input)		$\pm V_{REFT}/G_{PGA}$		V
Differential Input Impedance			$2.4/G_{PGA}$		MΩ
Common-Mode Input Impedance	G_{PGA} = 1		8		MΩ
	G_{PGA} = 2		8		MΩ
	G_{PGA} = 4		8		MΩ
	G_{PGA} = 8		8		MΩ
Resolution	R1, R0 = ‘00’, ADC2X = ‘0’, conversion time = 6ms		11		Bits + Sign
	R1, R0 = ‘01’, ADC2X = ‘0’, conversion time = 24ms		13		Bits + Sign
	R1, R0 = ‘10’, ADC2X = ‘0’, conversion time = 50ms		14		Bits + Sign
	R1, R0 = ‘11’, ADC2X = ‘0’, conversion time = 100ms		15		Bits + Sign
Integral Nonlinearity			0.01		%
Offset Error	G_{PGA} = 1		2.5		mV
	G_{PGA} = 2		1.25		mV
	G_{PGA} = 4		0.7		mV
	G_{PGA} = 8		0.3		mV
Offset Drift	G_{PGA} = 1		1.5		µV/°C
	G_{PGA} = 2		1.0		µV/°C
	G_{PGA} = 4		0.7		µV/°C
	G_{PGA} = 8		0.6		µV/°C
Gain Error			−0.2		%
Gain Error Drift			2		ppm/°C
Gain vs V_{SA}			80		ppm/V
Common-Mode Rejection	At dc and G_{PGA} = 8		100		dB
	At dc and G_{PGA} = 1		85		dB
External Temperature Current Excitation I_{TEMP}	Register 6, bit D11 = 1				
Current Excitation		5.8	7	8	µA
		5.2		**8.3**	**µA**
Temperature Drift			5		nA/°C
Voltage Compliance			V_{SA} −1.2		V

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_J = –55°C to +150°C.**
At T_J = +25°C, V_{SA}= V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309			UNIT
		MIN	TYP	MAX	
Linearization Adjust and Excitation Voltage (V_{EXC})					
Range 0	Register 3, bit D11 = 0				
Linearization DAC Range	With respect to V_{FB}		−0.166 to +0.166		V/V
Linearization DAC Resolution	±127 steps, 7-bit + sign		1.307		mV/V
V_{EXC} Gain	With respect to V_{REF}		0.83		V/V
Gain Error Drift			25		ppm/°C
Range 1	Register 3, bit D11 = 1				
Linearization DAC Range	With respect to V_{FB}		−0.124 to +0.124		V/V
Linearization DAC Resolution	±127 steps, 7-bit + sign		0.9764		mV/V
V_{EXC} Gain	With respect to V_{REF}		0.52		V/V
Gain Error Drift			25		ppm/°C
V_{EXC} Range Upper Limit	I_{EXC} = 5mA		V_{SA} −0.5		V
$I_{EXC\ SHORT}$	Short-circuit V_{EXC} output current		50		mA
Digital Interface					
Two-Wire Compatible	Bus speed	1		400	kHz
One-Wire	Serial speed baud rate	4.8K		38.4K	Bits/s
Maximum Lookup Table Size(7)			17 x 3 x 16		Bits
Two-Wire Data Rate	PGA309 to EEPROM (SCL frequency)		65		kHz
Logic Levels					
Input Levels (SDA, SCL, PRG, TEST)	Low			0.2 • V_{SD}	V
(SDA, SCL, PRG, TEST)	High	0.7 • V_{SD}			V
(SDA, SCL)	Hysteresis		0.1 • V_{SD}		V
Pull-Up Current Source (SDA, SCL)		**55**	**85**	**135**	**µA**
Pull-Down Current Source (TEST)		**10.5**	**25**	**50**	**µA**
Output LOW Level (SDA, SCL, PRG)	Open drain, I_{SINK} = 5mA			0.4	V
Power Supply					
$V_{SA,}$ V_{SD}		2.7		5.5	V
I_{SA} + I_{SD}, Quiescent Current	V_{SA} = V_{SD} = +5V, without bridge load		1.2	1.6	mA
Power-On Reset (POR)					
Power-Up Threshold	**V_S rising**		**2.2**	**2.7**	**V**
Power-Down Threshold	V_S falling		1.7		V
Temperature Range					
Specified Performance Range		–55		+150	°C

(7) Lookup table allows multislope compensation over temperature. Lookup table has access to 17 calibration points consisting of three adjustment values (Tx, Temperature, ZMx, Zero DAC, GMx, Gain DAC) that are stored in 16-bit data format (17x3x16 = Lookup table size).



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

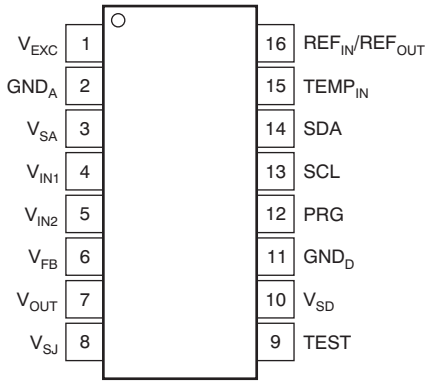
(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

(4) This device is qualified for 1000 hours of continuous operation at maximum rated temperature.

Figure 1. PGA309-HT Operating Life Derating Chart

PIN CONFIGURATION

PW PACKAGE
TSSOP-16
(TOP VIEW)



PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	V_{EXC}	Bridge sensor excitation. Connect to bridge if linearization and/or internal reference for bridge excitation is to be used.
2	GND_A	Analog ground. Connect to analog ground return path for V_{SA}. Should be same as GND_D.
3	V_{SA}	Analog voltage supply. Connect to analog voltage supply. To be within 200mV of V_{SD}.
4	V_{IN1}	Signal input voltage 1. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to Front-End PGA.
5	V_{IN2}	Signal input voltage 2. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to Front-End PGA.
6	V_{FB}	V_{OUT} feedback pin. Voltage feedback sense point for over/under-scale limit circuitry. When internal gain set resistors for the output amplifier are used, this is also the voltage feedback sense point for the output amplifier. V_{FB} in combination with V_{SJ} allows for ease of external filter and protection circuits without degrading the PGA309 V_{OUT} accuracy. V_{FB} must always be connected to either V_{OUT} or the point of feedback for V_{OUT}, if external protection is used.
7	V_{OUT}	Analog output voltage of conditioned sensor.
8	V_{SJ}	Output amplifier summing junction. Use for output amplifier compensation when driving large capacitive loads (> 100pF) and/or for using external gain setting resistors for the output amplifier.
9	TEST	Test/External controller mode pin. Pull to GND_D in normal mode.
10	V_{SD}	Digital voltage supply. Connect to digital voltage supply. To be within 200mV of V_{SA}.
11	GND_D	Digital ground. Connect to digital ground return path for V_{SD}. Should be same as GND_A.
12	PRG	Single-wire interface program pin. UART-type interface for digital calibration of the PGA309 over a single wire. Can be connected to V_{OUT} for a three-lead (V_S, GND, V_{OUT}) digitally-programmable sensor assembly.
13	SCL	Clock input/output for Two-Wire, industry-standard compatible interface for reading and writing digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface.
14	SDA	Data input/output for Two-Wire, industry-standard compatible interface for reading and writing digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface.
15	$TEMP_{IN}$	External temperature signal input. PGA309 can be configured to read a bridge current sense resistor as an indicator of bridge temperature, or an external temperature sensing device such as diode junction, RTD, or thermistor. This input can be internally gained by 1, 2, 4, or 8. In addition, this input can be read differentially with respect to V_{GNDA}, V_{EXC}, or the internal/external V_{REF}. There is also an internal, register-selectable, 7μA current source (I_{TEMP}) that can be connected to $TEMP_{IN}$ as an RTD, thermistor, or diode excitation source.
16	REF_{IN}/REF_{OUT}	Reference input/output pin. As an output, the internal reference (selectable as 2.5V or 4.096V) is available for system use on this pin. As an input, the internal reference may be disabled and an external reference can then be applied as the reference for the PGA309.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

V_{REF} vs TEMPERATURE

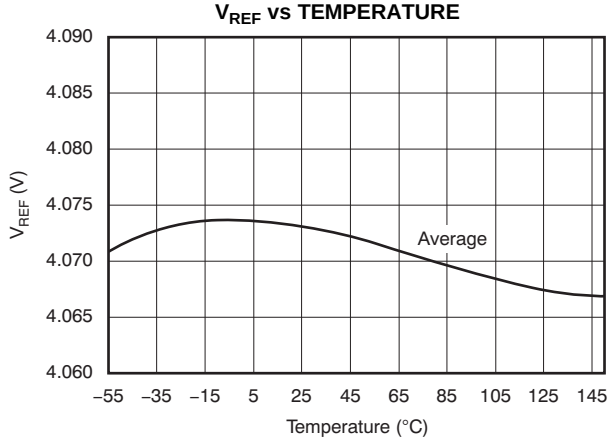


Figure 2.

I_B CURRENT vs TEMPERATURE

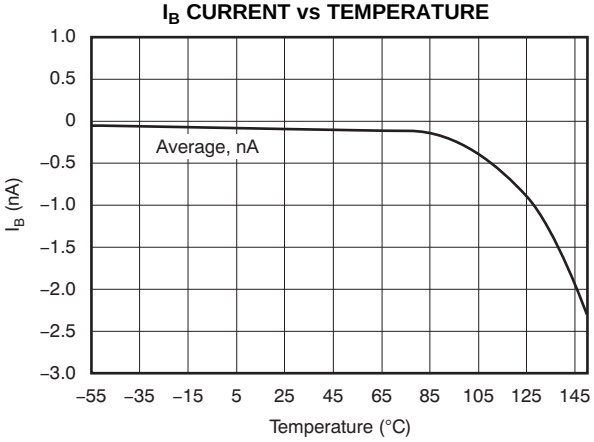


Figure 3.

I_{TEMP} CURRENT vs TEMPERATURE

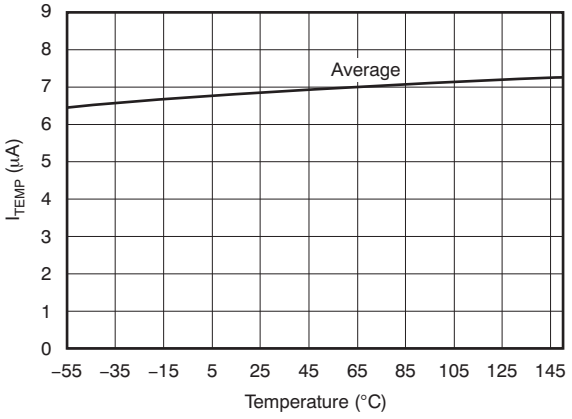


Figure 4.

COMMON-MODE REJECTION RATIO vs FREQUENCY

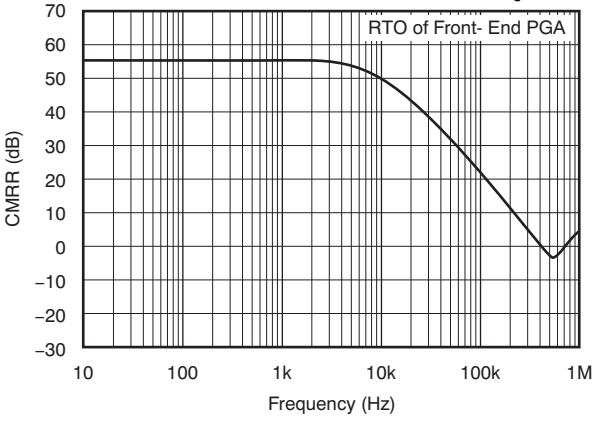


Figure 5.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

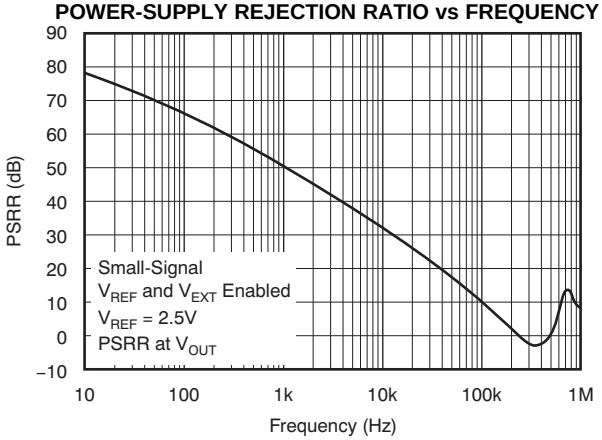


Figure 6.

CLOSED−LOOP GAIN vs FREQUENCY

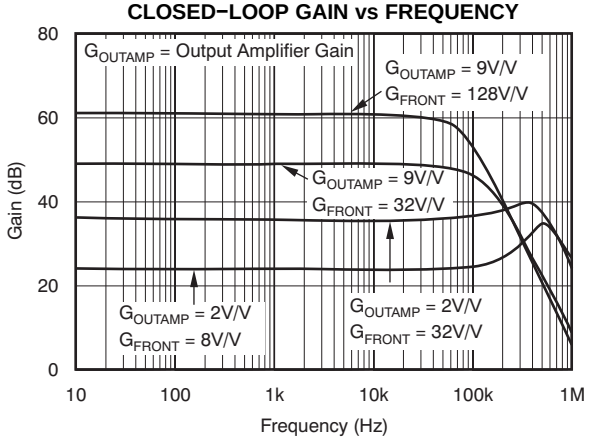


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

V_{OUT} SWING TO RAIL vs I_{LOAD}

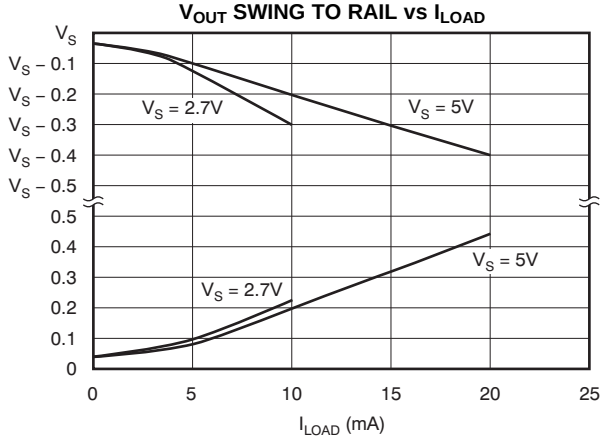


Figure 8.

I_Q vs TEMPERATURE

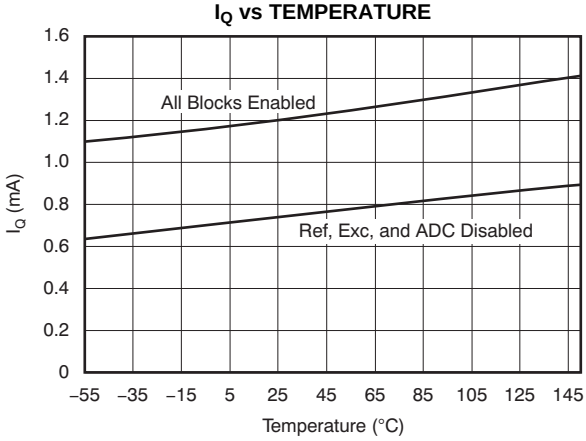


Figure 9.

TEMPERATURE ADC ERROR (INTERNAL MODE)

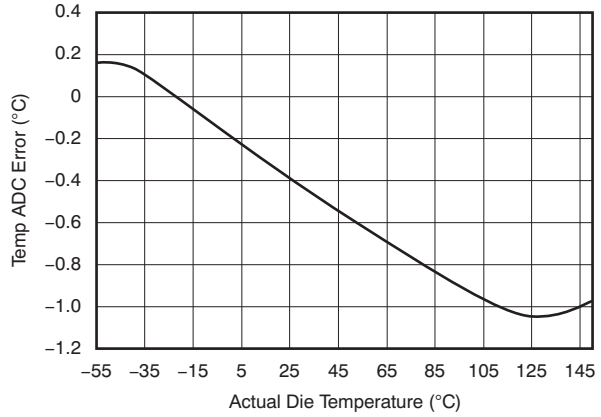


Figure 10.

TEMPERATURE ADC ERROR (EXTERNAL MODES)

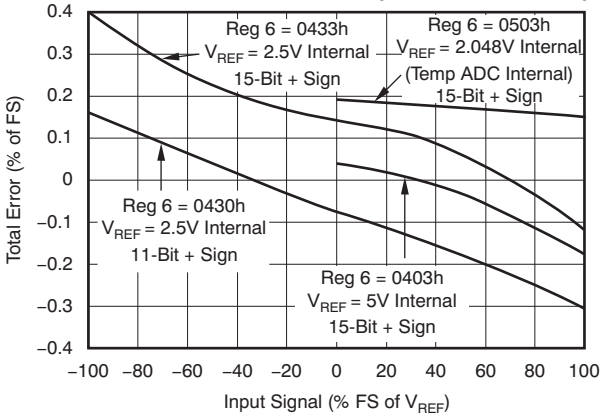


Figure 11.

V_{REF} NOISE (0.1Hz TO 10Hz)

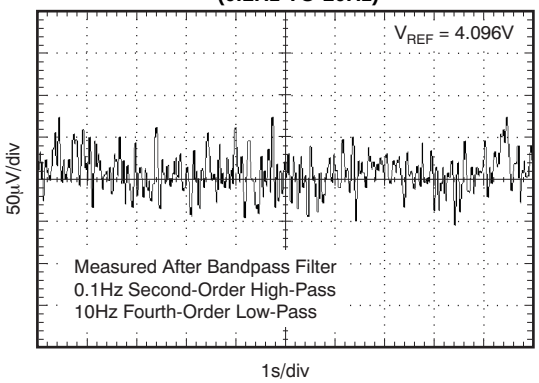


Figure 12.

V_{OUT} NOISE (0.1Hz TO 10Hz PEAK-TO-PEAK NOISE)

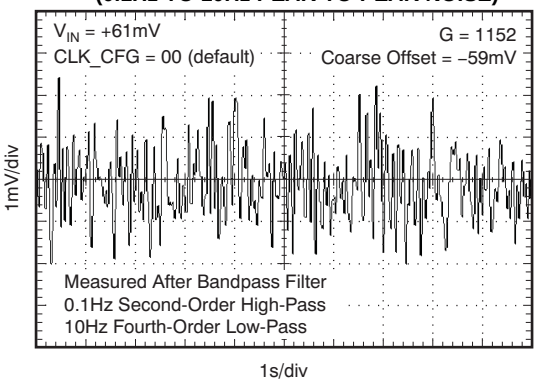


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY

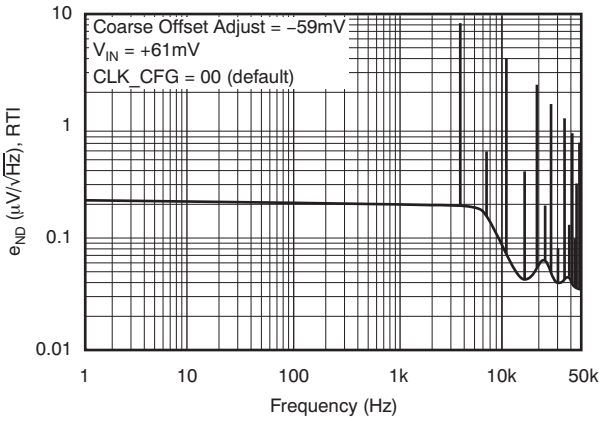


Figure 14.

INPUT VOLTAGE NOISE DENSITY

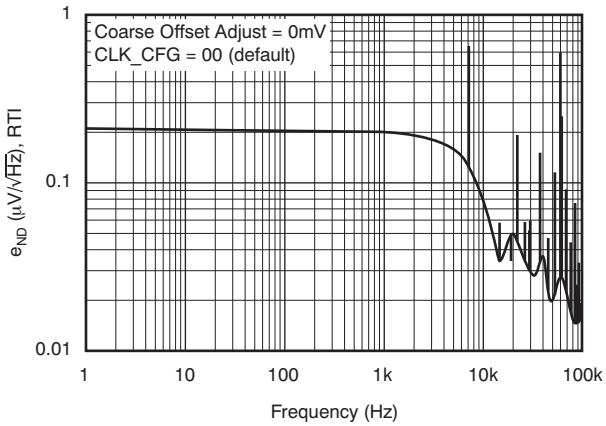


Figure 15.

LARGE-SIGNAL STEP RESPONSE

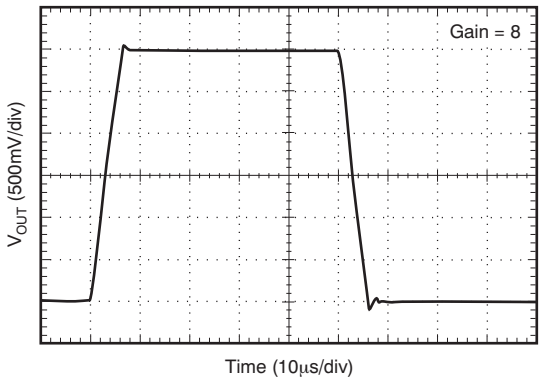


Figure 16.

LARGE-SIGNAL STEP RESPONSE

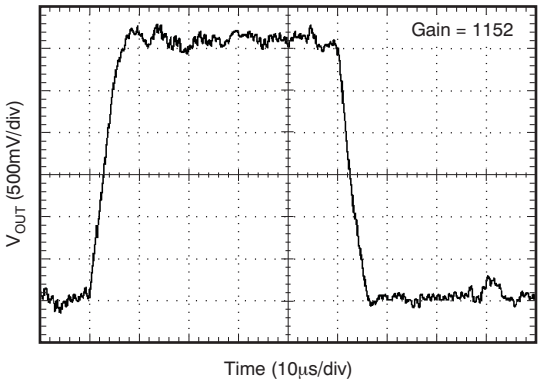


Figure 17.

SMALL-SIGNAL STEP RESPONSE

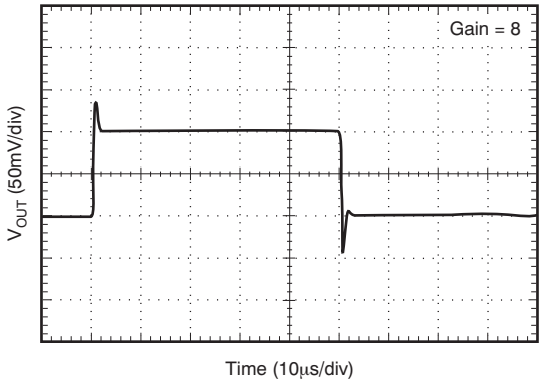


Figure 18.

SMALL-SIGNAL STEP RESPONSE

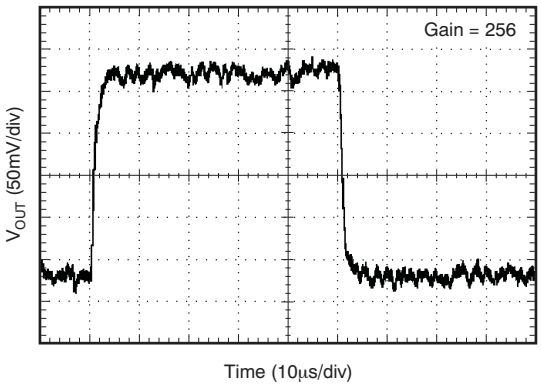


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

CAPACITIVE LOAD DRIVE

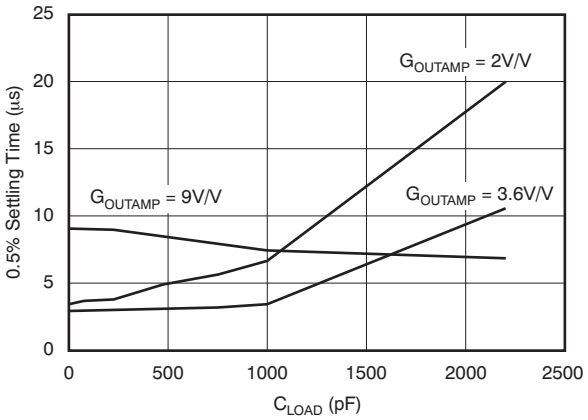


Figure 20.

OVERVOLTAGE RECOVERY

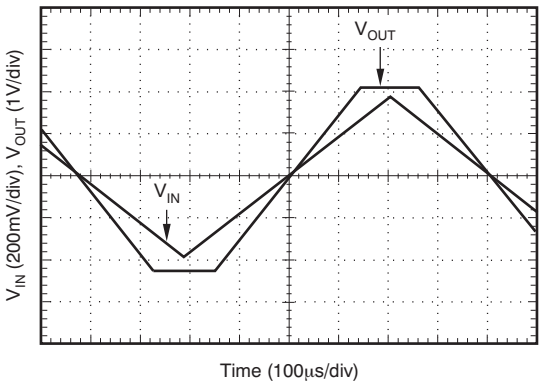


Figure 21.

OUTPUT AMPLIFIER OPEN-LOOP GAIN/PHASE vs FREQUENCY

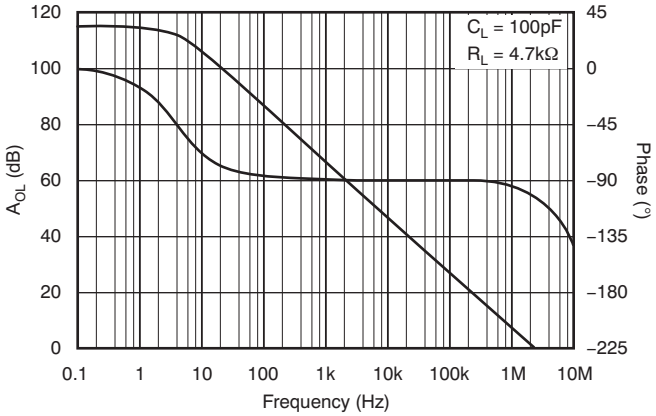


Figure 22.

ZERO DAC TYPICAL ERROR vs CODE

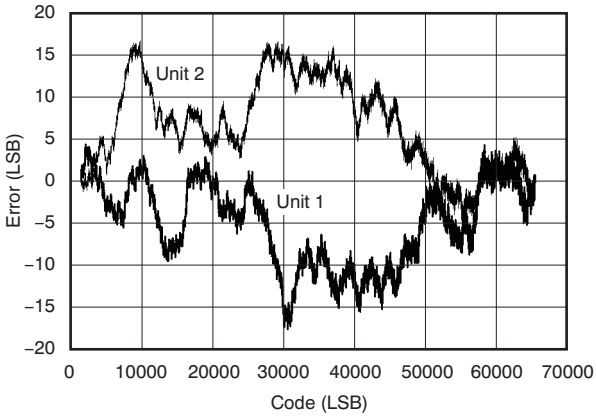


Figure 23.

GAIN DAC TYPICAL ERROR vs CODE

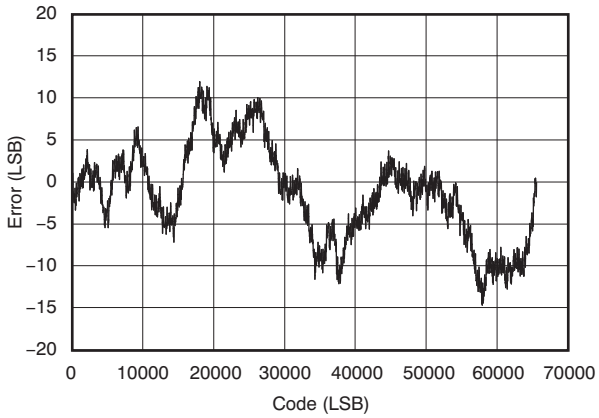


Figure 24.

FUNCTIONAL DESCRIPTION

OVERVIEW

The PGA309 is a programmable analog signal conditioner designed for resistive bridge sensor applications. It is a complete signal conditioner with bridge excitation, initial span and offset adjustment, temperature adjustment of span and offset, internal/external temperature measurement capability, output over-scale and under-scale limiting, fault detection, and digital calibration. The PGA309, in a calibrated sensor module, can reduce errors to the level approaching the bridge sensor repeatability. See Figure 25 for a block diagram of the PGA309. Following is a brief overview of each major function.

SENSOR ERROR ADJUSTMENT RANGE

The adjustment capability of the PGA309 is summarized in Table 1.

Table 1. PGA309 Adjustment Capability

FSS (full-scale sensitivity)	1mV/V to 245mV/V
Span TC	Over ±3300ppmFS/°C(1)
Span TC nonlinearity	≥ 10%
Zero offset	±200%FS(2)
Zero offset TC	Over ±3000ppmFS/°C(2)
Zero offset TC nonlinearity	≥ 10%
Sensor impedance	Down to 200Ω(3)

1. Depends on the temperature sensing scheme.
2. Combined coarse and fine offset adjust.
3. Lower impedance possible by using a dropping resistor in series with the bridge.

GAIN SCALING

The core of the PGA309 is the precision low-drift and no 1/f noise Front-End PGA. The overall gain of the Front-End PGA + Output Amplifier can be adjusted from 2.7V/V to 1152V/V. The polarity of the inputs can be switched through the 2x2 input mux to accommodate sensors with unknown polarity output.

The Front-End PGA provides initial coarse signal gain using a no 1/f noise, auto-zero instrumentation amplifier. The fine gain adjust is accomplished by the 16-bit attenuating Gain Digital-to-Analog Converter (Gain DAC). This Gain DAC is controlled by the data in the Temperature Compensation Lookup Table driven by the Temperature Analog-to-Digital Converter (Temp ADC). In order to compensate for second-order and higher drift nonlinearity, the span drift can be fitted to piecewise linear curves during calibration with the coefficients stored in an external nonvolatile EEPROM lookup table.

Following the fine gain adjust stage is the Output Amplifier that provides additional programmable gain. Two key output amplifier connections, V_{FB} and V_{SJ}, are brought out on the PGA309 for application flexibility. These connections allow for an accurate conditioned signal voltage while also providing a means for PGA309 output overvoltage and large capacitive loading for RFI/EMI filtering required in many end applications.

OFFSET ADJUSTMENT

The sensor offset adjustment is performed in two stages. The input-referred Coarse Offset Adjust DAC has approximately a ±60mV offset adjustment range for a selected V_{REF} of 5V. The fine offset and the offset drift are canceled by the 16-bit Zero DAC that sums the signal with the output of the front-end instrumentation amplifier. Similar to the Gain DAC, the input digital values of the Zero DAC are controlled by the data in the Temperature Compensation Lookup Table, stored in external EEPROM, driven by the Temp ADC. The programming range of the Zero DAC is 0V to V_{REF} with an output range of 0.1V to V_{SA} – 0.1V.

VOLTAGE REFERENCE

The PGA309 contains a precision low-drift voltage reference (selectable for 2.5V or 4.096V) that can be used for external circuitry through the REF_{IN}/REF_{OUT} pin. This same reference is used for the Coarse Offset Adjust DAC, Zero DAC, Over/Under-Scale Limits and sensor excitation/linearization through the V_{EXC} pin. When the internal reference is disabled, the REF_{IN}/REF_{OUT} pin should be connected to an external reference or to V_{SA} for ratiometric-scaled systems.

SENSOR EXCITATION AND LINEARIZATION

A dedicated circuit with a 7-bit + sign DAC for sensor voltage excitation and linearization is provided on the PGA309. This block scales the reference voltage and sums it with a portion of the PGA309 output to compensate the positive or negative bow-shaped nonlinearity exhibited by many sensors over their applied pressure range. Sensors not requiring linearization can be connected directly to the supply (V_{SA}) or to the V_{EXC} pin with the Linearization DAC (Lin DAC) set to zero.

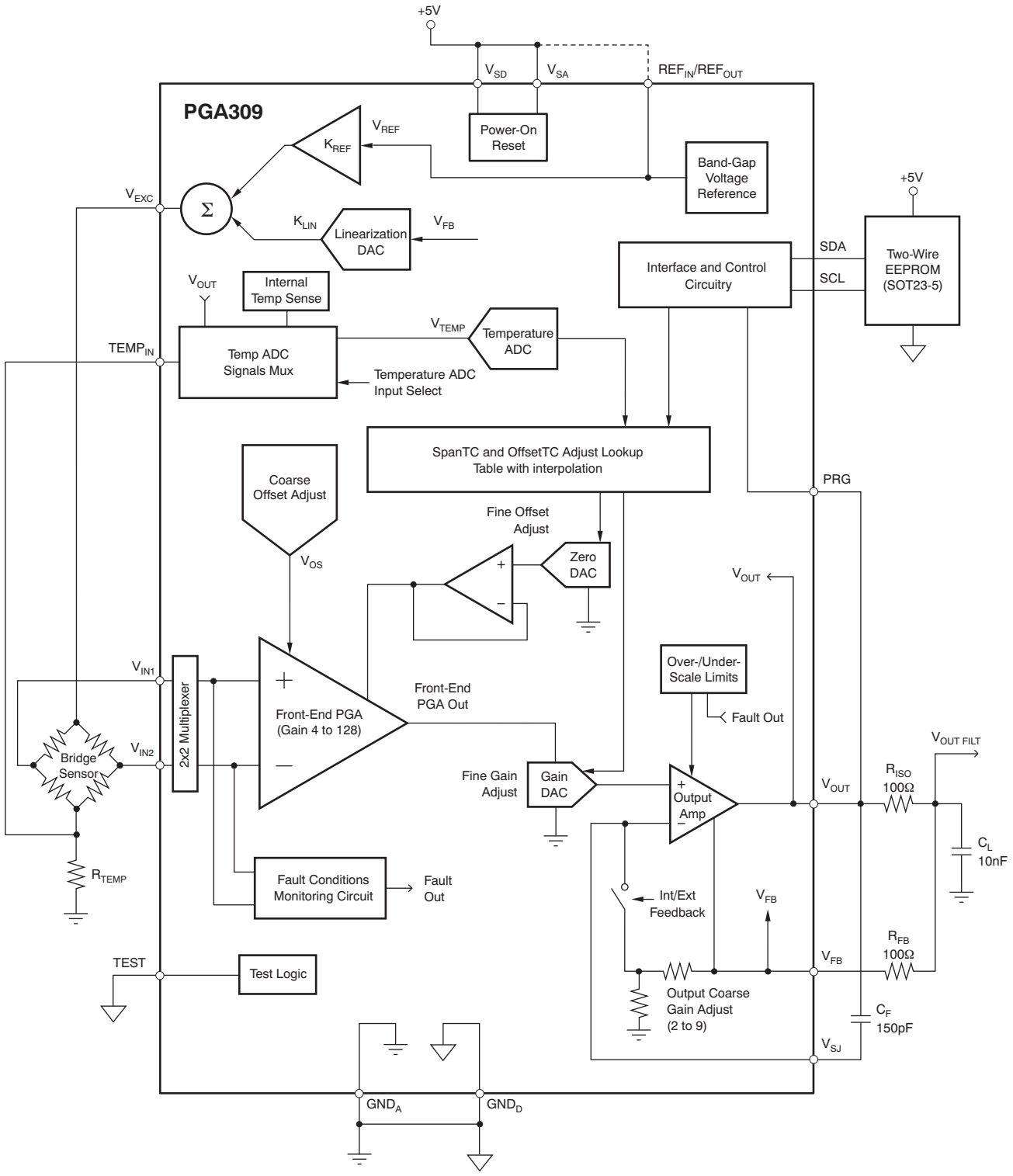


Figure 25. Simplified Diagram of the PGA309 in a Typical Configuration

ADC FOR TEMPERATURE SENSING

The temperature sense circuitry drives the compensation for the sensor span and offset drift. Either internal or external temperature sensing is possible. The temperature can be sensed in one of the following ways:

- Bridge impedance change (excitation current sense, in the positive or negative part of the bridge), for sensors with large temperature coefficient of resistance (TCR > 0.1%/°C).
- On-chip PGA309 temperature, when the chip is located sufficiently close to the sensor.
- External diode, thermistor, or RTD placed on the sensor membrane. An internal 7μA current source may be enabled to excite these types of temperature sensors.

The temperature signal is digitized by the onboard Temp ADC. The output of the Temp ADC is used by the control digital circuit to read the data from the Lookup Table in an external EEPROM, and set the output of the Gain DAC and the Zero DAC to the calibrated values as temperature changes.

An additional function provided through the Temp ADC is the ability to read the V_{OUT} pin back through the Temp ADC input mux. This provides flexibility for a digital output through either One-Wire or Two-Wire interface, as well as the possibility for an external microcontroller to perform real-time custom calibration of the PGA309.

EXTERNAL EEPROM AND TEMPERATURE COEFFICIENTS

The PGA309 uses an industry-standard Two-Wire external EEPROM (typically, a SOT23-5 package). A 1k-bit (minimum) EEPROM is needed when using all 17 temperature coefficients. Larger EEPROMs may be used to provide space for a serial number, lot code, or other data.

The first part of the external EEPROM contains the configuration data for the PGA309, with settings for:

- Register 3—Reference Control and Linearization
- Register 4—PGA Coarse Offset and Gain/Output Amplifier Gain
- Register 5—PGA Configuration and Over/Under-Scale Limit
- Register 6—Temp ADC Control

This section of the EEPROM contains its own individual checksum (Checksum1).

The second part of the external EEPROM contains up to 17 temperature index values and corresponding temperature coefficients for the Zero DAC and Gain DAC adjustments with measured temperature, and also contains its own checksum (Checksum2). The PGA309 lookup logic contains a linear interpolation algorithm for accurate DAC adjustments between stored temperature indexes. This approach allows for a piecewise linear temperature compensation of up to 17 temperature indexes and associated temperature coefficients.

If either Checksum1, Checksum2, or both are incorrect, the output of the PGA309 is set to high-impedance.

FAULT MONITOR

To detect sensor burnout or a short, a set of four comparators are connected to the inputs of the Front-End PGA. If any of the inputs are taken to within 100mV of ground or V_{EXC}, or violate the input CMR of the Front-End PGA, then the corresponding comparator sets a sensor fault flag that causes the PGA309 V_{OUT} to be driven within 100mV of either V_{SA} or ground, depending upon the alarm configuration setting (Register 5—PGA Configuration and Over/Under-Scale Limit). This will be well above the set Over-Scale Limit level or well below the set Under-Scale Limit level. The state of the fault condition can be read in digital form in Register 8—Alarm Status Register. If the Over/Under-Scale Limit is disabled, the PGA309 output voltage will still be driven within 100mV of either V_{SA} or ground, depending upon the alarm configuration setting.

There are five other fault detect comparators that help detect subtle PGA309 front-end violations that could otherwise result in linear voltages at V_{OUT} that would be interpreted as valid states. These are especially useful during factory calibration and setup, and are configured through Register 5—PGA Configuration and Over/Under-Scale Limit. The respective status of each can also be read back through Register 8—Alarm Status Register.

OVER-SCALE AND UNDER-SCALE LIMITSE

The over-scale and under-scale limit circuitry combined with the fault monitor circuitry provides a means for system diagnostics. A typical sensor-conditioned output may be scaled for 10% to 90% of the system ADC range for the sensor normal operating range. If the conditioned pressure sensor is below 4%, it is considered under-pressure; if over 96%, it is considered over-pressure.

The PGA309 over/under-scale limit circuit can be programmed individually for under-scale and over-scale values that clip or limit the PGA309 output. From a system diagnostic view, 10% to 90% of ADC range is normal operation, less than 4% is under-pressure, and greater than 96% is over-pressure. If the fault detect circuitry is used, a detected fault will cause the PGA309 output to be driven to positive or negative saturation.

If this fault flag is programmed for high, then greater than 97% ADC range will be a fault; if programmed for low. then less than 3% ADC range will be a fault. In this configuration, the system software can be used to distinguish between over- or under-pressure condition, which indicates an out-of-control process, or a sensor fault.

POWER-UP AND NORMAL OPERATION

The PGA309 has circuitry to detect when the power supply is applied to the PGA309, and reset the internal registers and circuitry to an initial state. This reset also occurs when the supply is detected to be invalid, so that the PGA309 is in a known state when the supply becomes valid again. The rising threshold for this circuit is typically 2.2V and the falling threshold is typically 1.7V. After the power supply becomes valid, the PGA309 waits for approximately 25ms and then attempts to read the configuration data from the external EEPROM device.

If the EEPROM has the proper flag set in address locations 0 and 1, then the PGA309 continues reading the first part of the EEPROM; otherwise, the PGA309 waits for one second before trying again. If the PGA309 detects no response from the EEPROM, the PGA309 waits for one second and tries again; otherwise, the PGA309 tries to free the bus and waits for 25ms before trying to read the EEPROM again. If a successful read of the first part of the EEPROM is accomplished, (including valid Checksum1 data), the PGA309 triggers the Temp ADC to measure temperature. For 16-bit resolution results, the converter takes approximately 125ms to complete a conversion. Once the conversion is complete, the PGA309 begins reading the Lookup Table information from the EEPROM (second part) to calculate the settings for the Gain DAC and Zero DAC.

The PGA309 reads the entire Lookup Table so that it can determine if the checksum for the Lookup Table (Checksum2) is correct. Each entry in the Lookup Table requires approximately 500µs to read from the EEPROM. Once the checksum is determined to be valid, the calculated values for the Gain and Zero DACs are updated into their respective registers, and the output amplifier is enabled. The PGA309 then begins looping through this entire procedure, starting with reading the EEPROM configuration registers from the first part of the EEPROM, then starting a new conversion on the Temp ADC, which then triggers reading the Lookup Table data from the second part of the EEPROM. This loop continues indefinitely.

DIGITAL INTERFACE

There are two digital interfaces on the PGA309. The PRG pin uses a One-Wire, UART-compatible interface with bit rates from 4.8Kbits/s to 38.4Kbits/s. The SDA and SCL pins together form an industry standard Two-Wire interface at clock rates from 1kHz to 400kHz. The external EEPROM uses the Two-Wire interface. Communication to the PGA309 internal registers, as well as to the external EEPROM, for programming and readback can be conducted through either digital interface.

It is also possible to connect the One-Wire communication pin, PRG, to the V_{OUT} pin in true three-wire sensor modules and still allow for programming. In this mode, the PGA309 output amplifier may be enabled for a set time period and then disabled again to allow sharing of the PRG pin with the V_{OUT} connection. This allows for both digital calibration and analog readback during sensor calibration in a three-wire sensor module.

The Two-Wire interface has timeout mechanisms to prevent bus lockup from occurring. The Two-Wire master controller in the PGA309 has a mode that attempts to free up a stuck-at-zero SDA line by issuing SCL pulses, even when the bus is not indicated as idle after a timeout period has expired. The timeout will only apply when the master portion of the PGA309 is attempting to initiate a Two-Wire communication.

PGA309 TRANSFER FUNCTION

Equation 1 shows the mathematical expression that is used to compute the output voltage, V_{OUT}. This equation can also be rearranged algebraically to solve for different terms. For example, during calibration, this equation is rearranged to solve for V_{IN}.

$$V_{OUT} = \left[\left(mux\_sign \bullet V_{IN} + V_{Coarse\_Offset}\right) \bullet GI + V_{Zero\_DAC}\right] \bullet GD \bullet GO \quad (1)$$

Where:

mux_sign: This term changes the polarity of the input signal; value is ±1.

V_{IN}: The input signal for the PGA309; $V_{IN}1 = V_{INP}$, $V_{IN}2 = V_{INN}$.

V_{Coarse_Offset}: The coarse offset DAC output voltage.

GI: Input stage gain.

V_{Zero_DAC}: Zero DAC output voltage.

GD: Gain DAC.

GO: Output stage gain.

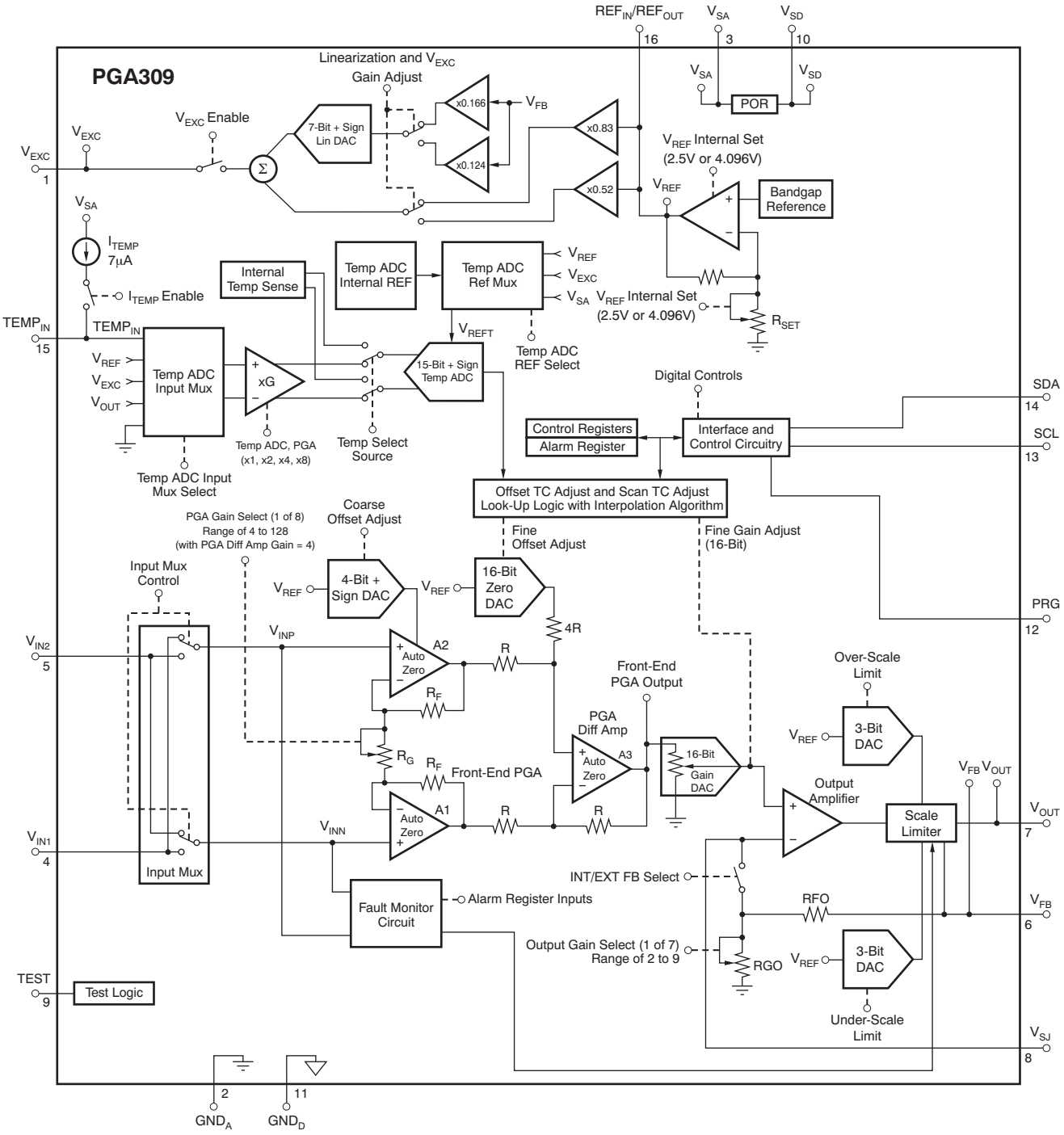


Figure 26. Detailed Block Diagram

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PGA309ASPWT	Active	Production	TSSOP (PW) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	PGA 309AS

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF PGA309-HT :

- Catalog : PGA309

NOTE: Qualified Version Definitions:

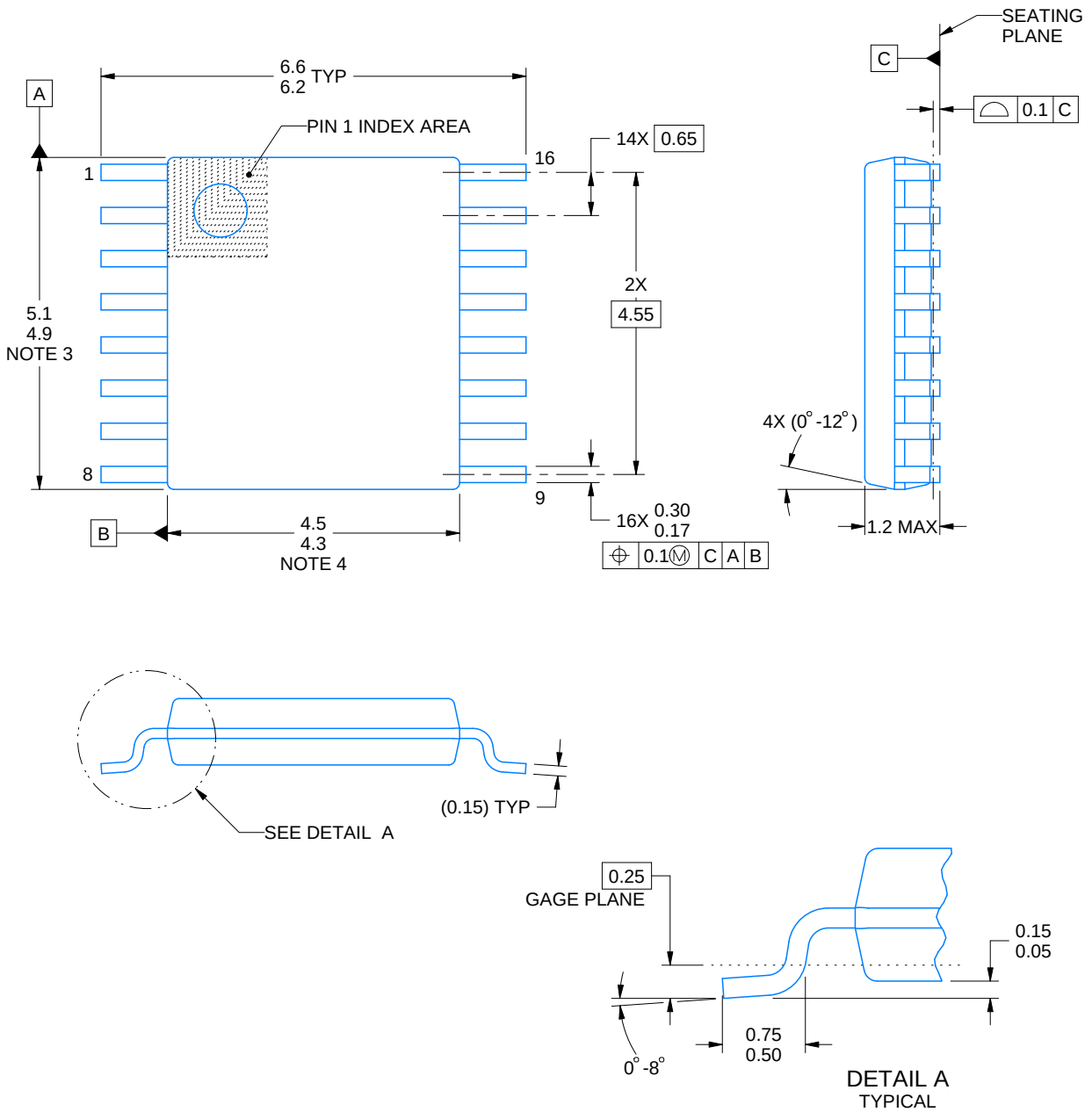
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

PW0016A

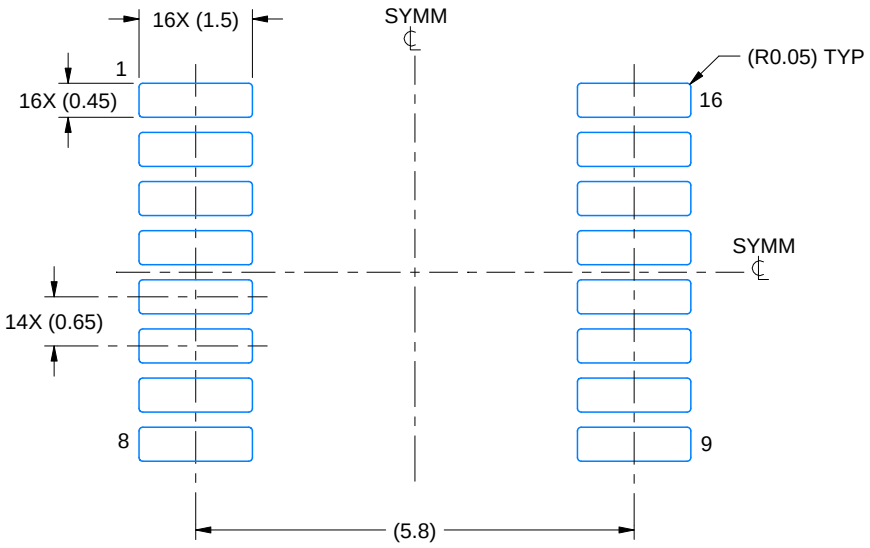
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

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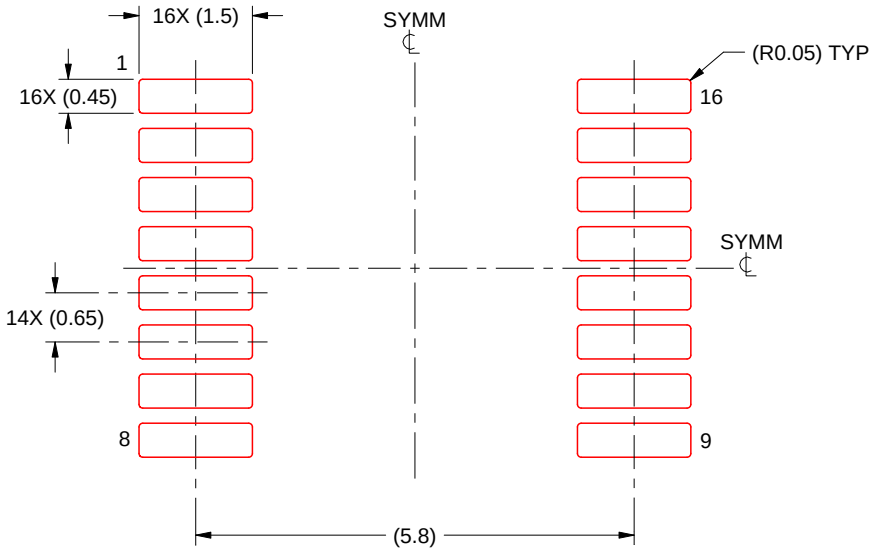
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月