TPS22933 具有自动选择功能和低压降稳压器的三路输入电源多路复用器

1 特性

- 三个集成负载开关，自动选择最高电平输入
- 集成 3.6V 固定电压低压降 (LDO) 稳压器
- 提供开关控制式和始终开启式两种 LDO 输出
- 采用 1.5mm × 1.5mm µQFN 封装
- 输入电压范围：2.5V 至 12V
- 低导通电阻 (r_{ON})
  - V_{IN} = 5.0V 时，r_{ON} = 2.4Ω
  - V_{IN} = 4.2V 时，r_{ON} = 2.6Ω
- 50mA 的最大持续电流
- 低阈值控制输入 (EN)
- 切换时间：18µs（典型值）

2 应用范围

- 智能电话
- 全球卫星定位 (GPS) 设备
- 数码摄像机
- 便携式工业设备
- 便携式医疗设备
- 便携式媒体播放器
- 便携式仪表

3 说明

TPS22933 器件是一款具有自动输入选择功能和低压降线性稳压器的三路输入电源多路复用器，同时兼具小尺寸和低 r_{ON} 特性。此器件包含三个 P 沟道金属氧化物半导体场效应晶体管 (MOSFET)，它们的工作输入电压范围为 2.5V 到 12V。TPS22933 能够自动选择电平最高的输入（从 BAT、USB 和 DC_IN 三者中选择）并将其提供给 LDO。LOUT 是 LDO 始终开启的输出。通过使能功能（EN 引脚），可以对 VOUT 进行开关控制，接通快速放电电阻，而且能够直接连接低电压控制信号。

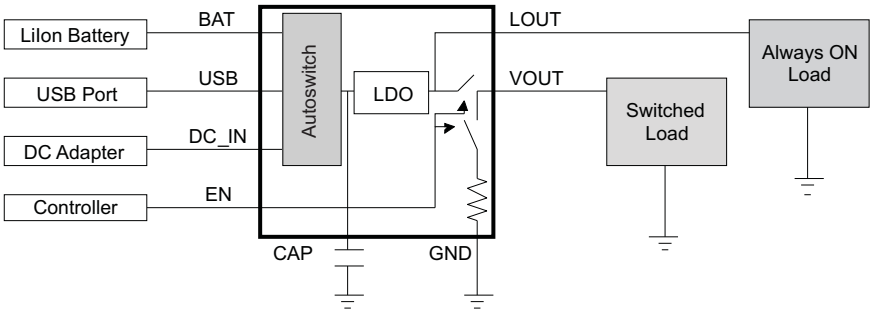
TPS22933 采用小型、节省空间的 8 引脚 µQFN 封装，并可在 -40°C 至 85°C 温度范围内的自然通风条件下额定运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS22933	UQFN (8)	1.50mm x 1.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



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4 修订历史记录

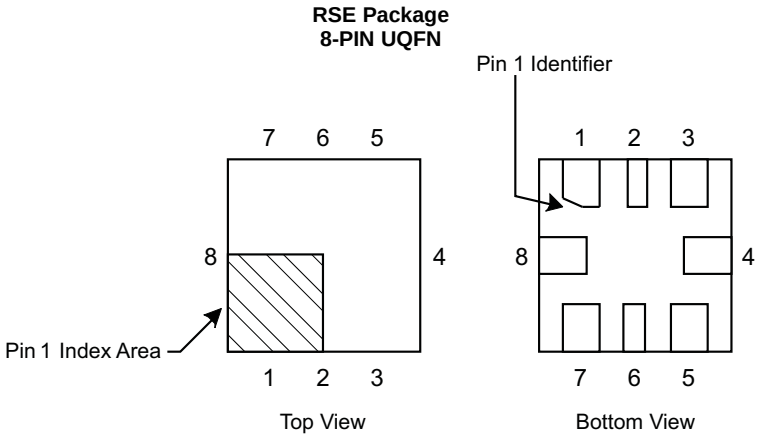
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (October 2011) to Revision A **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 说明* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

S

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BAT	I	Source Voltage 1 (Battery)
2	USB	I	Source Voltage 2 (V+ USB)
3	DC_IN	I	Source Voltage 3 (DC Adapter)
4	GND	—	Ground
5	EN	I	VOUT Enable (Cannot be left floating)
6	CAP	O	Capacitor for LDO
7	VOUT	O	Switched LDO Output
8	LOUT	O	Always on LDO Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VIN	Input voltage	BAT, USB, DC_IN	–0.3	14	V
VOUTPUT	Output voltage	VOUT, LOUT	–0.3	6	V
VEN	Input voltage	EN	–0.3	6	V
IMAX	Maximum continuous switch current			75	mA
IPLS	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle			100	mA
T_A	Operating free-air temperature		–40	85	°C
T_{lead}	Maximum lead temperature (10-s soldering time)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	BAT, USB, DC_IN	2.5		12	V
V_{EN}		EN	0		5.5	V
V_{IH}	EN pin High-level input voltage, (EN > V_{IH} Min, VOUT = LDO Output)	BAT = 2.5 V to 5.5 V, USB, DC_IN = 2.5 V to 12 V	1.15		5.5	V
V_{IL}	EN pin Low-level input voltage, (EN< V_{IL} Max, VOUT = pulldown)	BAT = 2.5 V to 5.5 V, USB, DC_IN = 2.5 V to 12 V	0		0.6	V
$I_{OUT-LOUT}$	LOUT Current	V_{BAT} = 4.2 V OR V_{USB} = 5 V OR V_{DC_IN} = 5 V, EN = 3.4 V, $I_{OUT-VOUT}$ = 0 mA			50	mA
$I_{OUT-VOUT}$	VOUT Current	V_{BAT} = 4.2 V OR V_{USB} = 5 V OR V_{DC_IN} = 5 V, EN = 3.4 V, $I_{OUT-LOUT}$ = 0 mA			50	mA
$I_{OUT-TOTAL}$	LOUT + VOUT current	V_{BAT} = 4.2 V OR V_{USB} = 5 V OR V_{DC_IN} = 5 V, EN = 3.4 V			50	mA
CAP	LDO Capacitor (on CAP pin)		20 (1)			nF
	LOUT Capacitor			1		µF
	VOUT Capacitor			1		µF

(1) Refer to *Application and Implementation*.

6.4 Thermal Information

THERMAL METRIC (1)		TPS22933 RSE (UQFN) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

BAT = 2.5 V to 12.0 V, USB = 2.5 V to 12.0 V, DC_IN = 2.5 V to 12.0 V, T_A = –40ºC to +85ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1) (2) (3)	T_A	MIN	TYP(4)	MAX	UNIT
I_{IN-BAT}	Operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 3 V, V_{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	µA
	Quiescent current	I_{OUT} = 0, V_{BAT} = 4.2 V, V_{USB} = 5 V, V_{DC_IN} = 3 V, EN = 3.4 V			0.7	2	
I_{IN-USB}	Operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 5 V, V_{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	µA
	Quiescent current	I_{OUT} = 0, V_{BAT} = 4.2V, V_{USB} = 5V, V_{DC_IN} = 5.5V, EN = 3.4 V			0.7	2	
I_{IN-DC_IN}	Operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 3 V, V_{DC_IN} = 5 V, EN = 3.4 V	Full		9.2	15	µA
	Quiescent current	I_{OUT} = 0, V_{BAT} = 4.2V, V_{USB} = 5.5V, V_{DC_IN} = 5V, EN = 3.4 V			0.7	2	
I_{IN-USB}	Hi-Voltage operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 12 V, V_{DC_IN} = 5 V, EN = 3.4 V	Full		10.8	20	µA
I_{IN-DC_IN}	Hi-Voltage operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 5 V, V_{DC_IN} = 12 V, EN = 3.4 V	Full		10.8	20	µA
R_{ON}	ON resistance (USB to CAP, BAT to CAP, DC_IN to CAP)	V_{IN} = 5.0 V, I_{OUT} = 10 mA	25ºC		2.4	3.3	Ω
			Full			3.5	
		V_{IN} = 4.2 V, I_{OUT} = 10 mA	25ºC		2.6	3.5	Ω
			Full			4	
		V_{IN} = 2.5 V, I_{OUT} = 10 mA	25ºC		3.8	5	Ω
			Full			6	
R_{ONVOUT}	ON resistance (LDO output to VOUT)	V_{IN} = 4.2 V, $I_{OUT-VOUT}$ = 10 mA	25ºC		1.3	2.5	Ω
			Full			3	
R_{PD}	Output pulldown resistance	V_{IN} = 4.2 V, V_{EN} = 0 V, I(into VOUT) = 10 mA	25ºC		63.8	120	Ω
I_{EN}	EN input leakage	V_{EN} = 1.6 V to 5.5 V or GND	Full			1	µA
$V_{DO-VOUT}$	Dropout voltage VOUT (5) (6)	I_{OUT} = 10 mA	Full		0.11		V
$V_{DO-LOUT}$	Dropout voltage LOUT	I_{OUT} = 10 mA(5) (6)	Full		0.1		V
V_{LOUT}	Always on LDO output voltage (LOUT pin)	V_{IN} < 3.4 V, I_{OUT} = 10 mA, V_{EN} = 1.8 V	Full		V_{IN} – $V_{DO-LOUT}$		V
		V_{IN} > 4 V, I_{OUT} = 10 mA, V_{EN} = 1.8 V	Full	3.42	3.6	3.78	
V_{VOUT}	Switched LDO output voltage (VOUT pin)	V_{IN} < 3.4 V, I_{OUT} = 10 m A, V_{EN} = 1.8 V	Full		V_{IN} – $V_{DO-VOUT}$		V
		V_{IN} > 4 V, I_{OUT} = 10 mA, V_{EN} = 1.8 V	Full	3.39	3.57	3.75	
V_{CO}	Changeover voltage	V_{BAT} = 4.2 V, V_{USB} = 4.0 V rising to 4.4 V	Full		0.15		V
t_{CO}	Changeover time	VBAT=4.2 V, V_{USB} = 4.0 V rising to 4.4 V, CAP = 0.01 µF, I_{OUT} = 10 mA	25ºC		18		µs
			Full			50	
t_{OFF}	VOUT OFF-time	EN high to low, C(VOUT) = 1 µF, VOUT load = 360 Ω	Full		32		µs
t_{ON}	VOUT ON-time	EN low to high, C(VOUT) = open, VOUT load = 360 Ω	Full		65		µs

(1) V_{IN} is defined as the highest voltage present on the BAT, USB and DC_IN pins.
(2) One of the voltages on BAT, USB and DC_IN must be > VIN (Min), others can be 0 V.
(3) V_{BAT}, V_{USB} and V_{DC_IN} refer to the voltages on BAT, USB and DC_IN respectively. OUT, IOUT-VOUT and IOUT-LOUT refer to the currents for the combined output current for VOUT and LOUT, the current on VOUT and the current on LOUT respectively.
(4) TYP is 25ºC, BAT = 4.2-V, USB = 0-V, DC_IN = 0-V.
(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: V_{IN} – $V_{DROPOUT}$.
(6) Dropout voltage is measured at the VIN that causes the output to drop to 100mV below its nominal voltage. For VOUT, the voltage drop across the output switch is included (10mA × R_{ONVOUT}).

6.6 Typical Characteristics

Table 1. Performance Graphs and Plots

Type	Description	Figure
Graph	RON versus VIN (BAT, USB, DC_IN) 25°C	Figure 1
Graph	RON versus VIN (Any input)	Figure 2
Graph	Quiescent Current versus Input Voltage (Any input)	Figure 3
Graph	Operating Current versus Input Voltage (Any Input)	Figure 4
Scope Plot	t_{OFF} (VIN = 4.2 V, C(VOUT) = 1 uF, 25°C)	Figure 5
Scope Plot	t_{OFF} (VIN = 4.2 V, C(VOUT) = open, 25°C)	Figure 6
Scope Plot	t_{ON} (VIN = 4.2 V, C(VOUT) = 1 uF, 25°C)	Figure 7
Scope Plot	t_{ON} (VIN = 4.2 V, C(VOUT) = open, 25°C)	Figure 8
Graph	LOUT and VOUT versus Temperature at VIN = 4.2 V	Figure 9
Graph	LOUT and VOUT versus IOUT (VIN = 4.2 V, Temp = 25°C)	Figure 10
Graph	LOUT Dropout Voltage versus Temperature (VIN = 2.5 V)	Figure 11
Graph	VOUT Dropout Voltage versus Temperature (VIN = 2.5 V)	Figure 12
Graph	Output Pulldown Resistance (R_{PD}) versus Temperature (10 mA into VOUT)	Figure 13

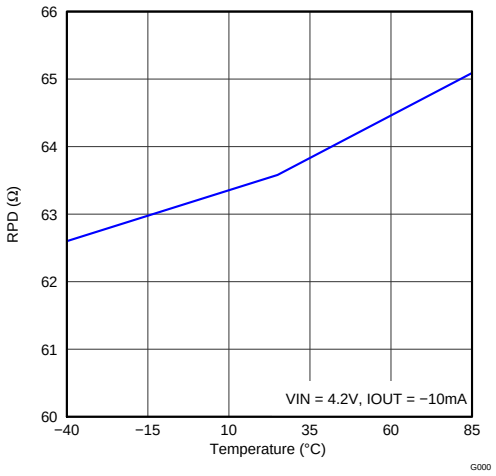


Figure 1. RPD vs Temperature

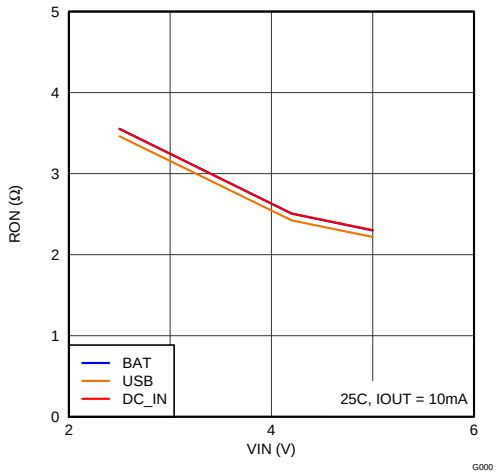


Figure 2. R_{ON} vs VIN (Typical)

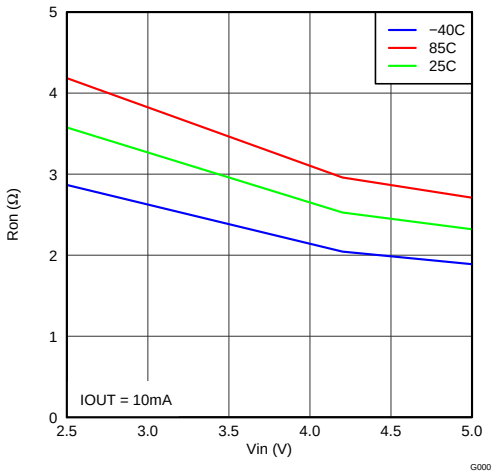


Figure 3. R_{ON} vs VIN

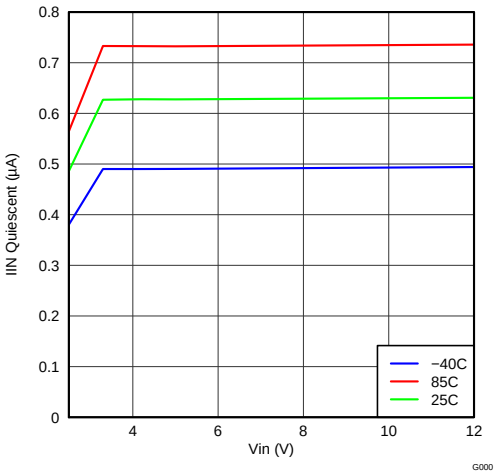


Figure 4. I_{IN} (Quiescent) vs VIN

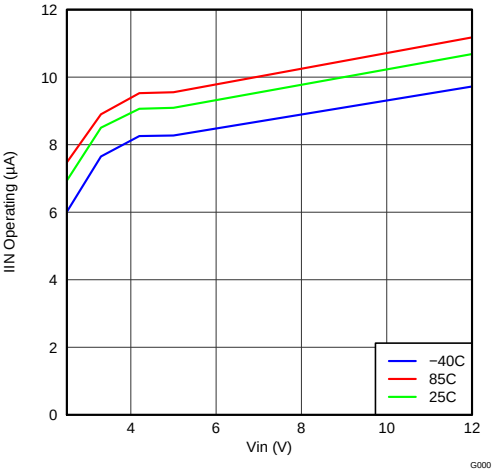


Figure 5. I_{IN} (Operating) vs VIN

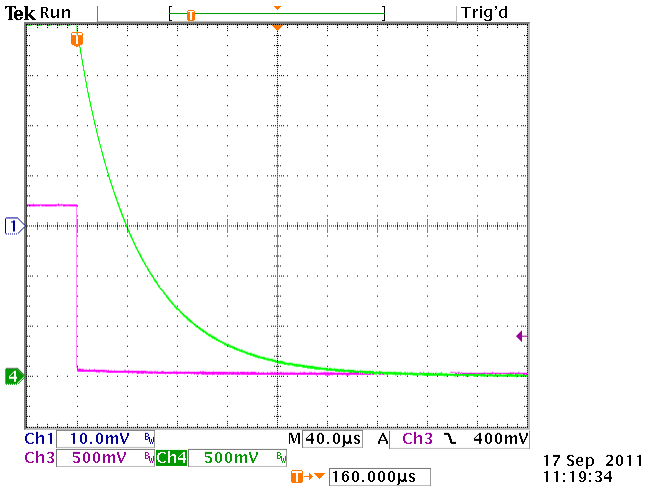


Figure 6. VOUT t_{OFF} (1 µF on VOUT)

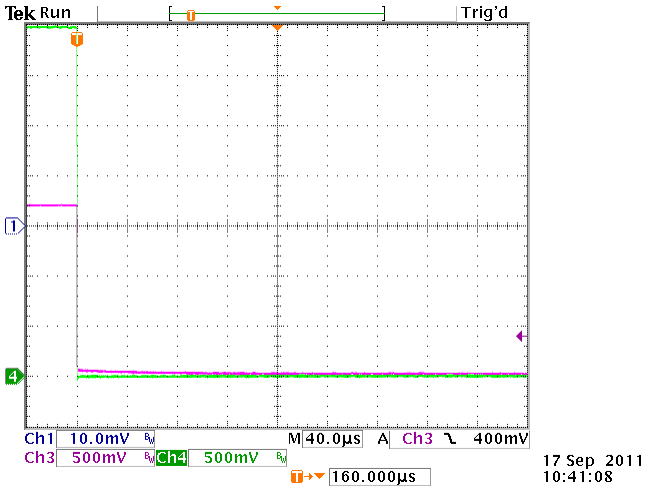


Figure 7. VOUT t_{OFF} (No Capacitor on VOUT)

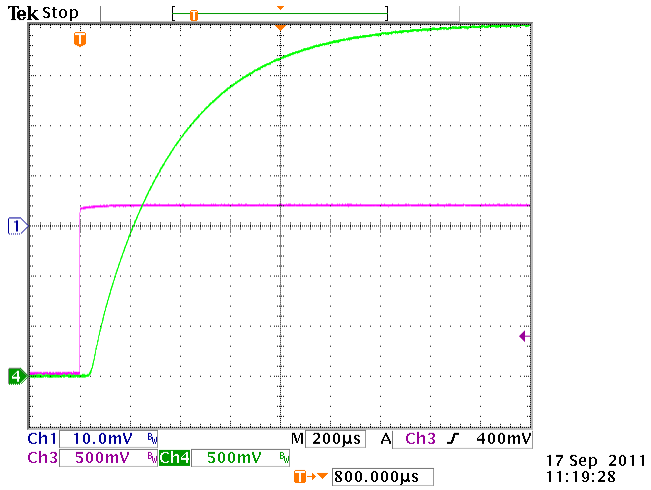


Figure 8. VOUT t_{ON} (1 µF on VOUT)

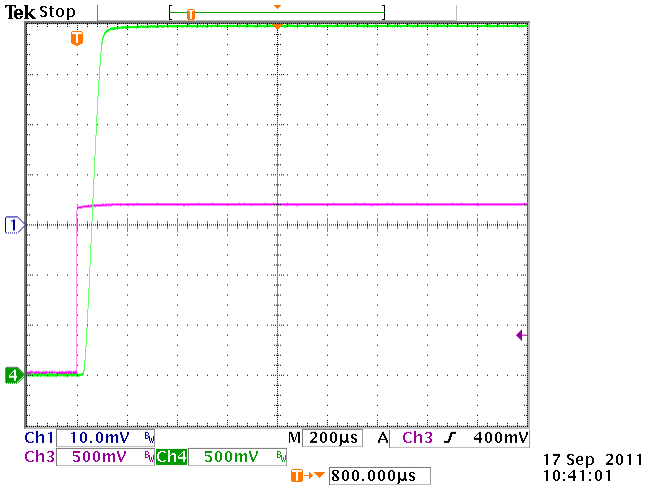


Figure 9. VOUT t_{ON} (No Capacitor on VOUT)

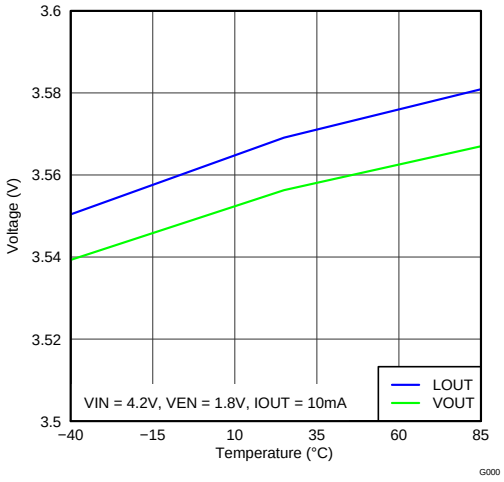


Figure 10. LOUT-VOUT vs Temperature VIN 4.2 V

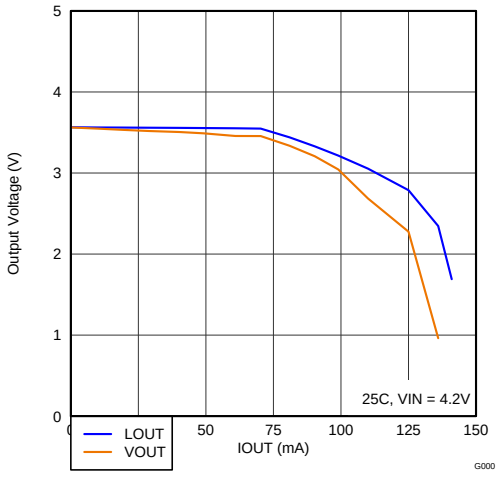


Figure 11. LOUT-VOUT vs IOUT

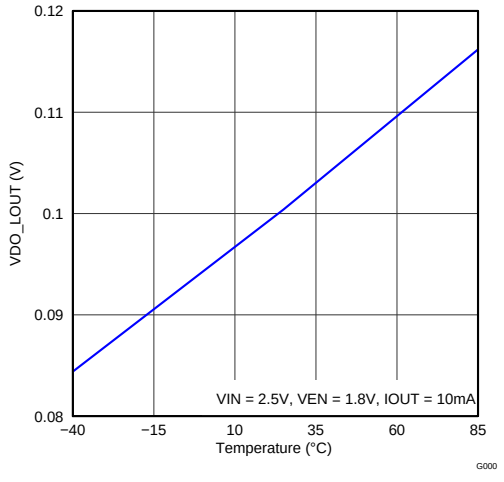


Figure 12. VDOLOUT vs Temperature VIN 2.5 V

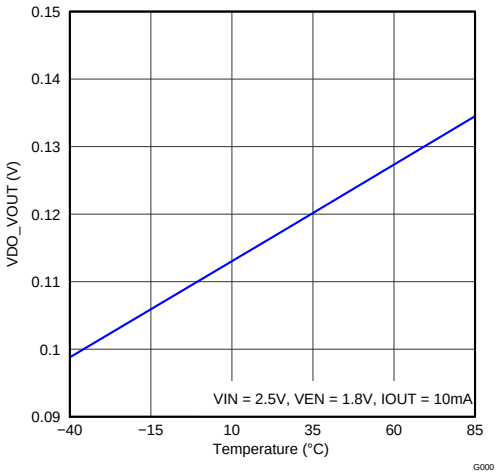


Figure 13. VDOVOUT vs Temperature VIN 2.5 V

7 Parametric Measurement Information

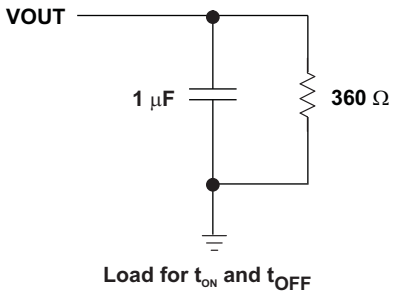


Figure 14. Test Circuit and t_{ON} / t_{OFF} Waveforms

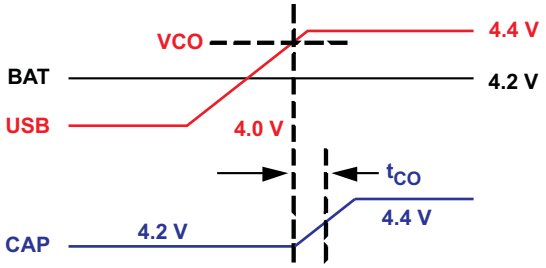


Figure 15. Switchover Timing

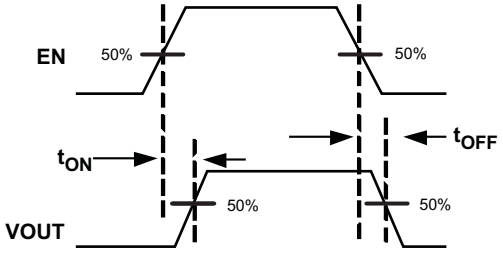


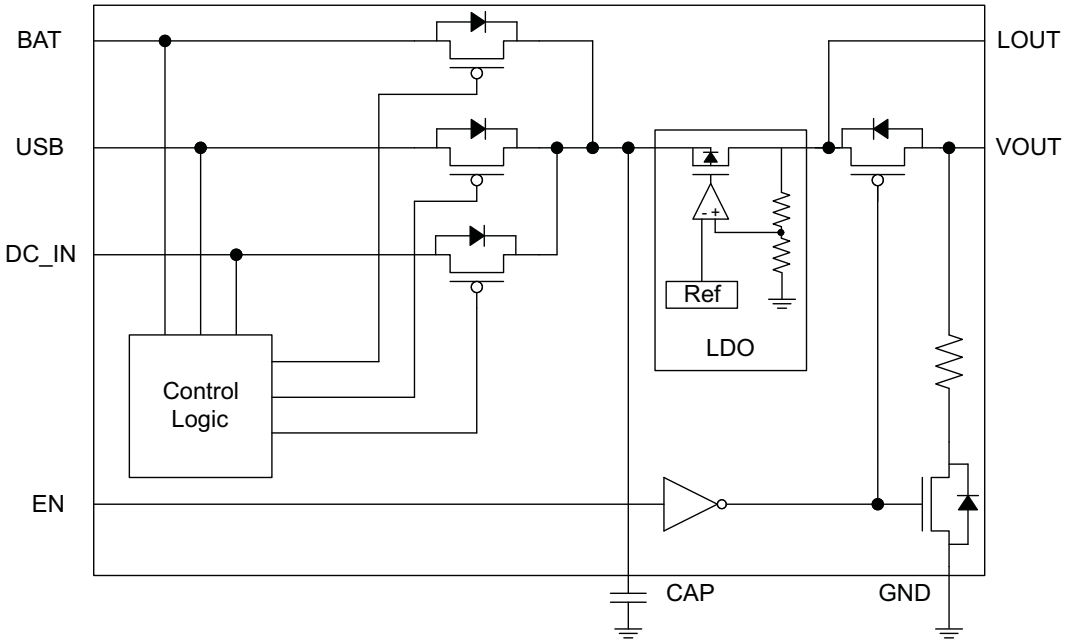
Figure 16. VOUT Enable Timing

8 Detailed Description

8.1 Overview

The TPS22933 is a triple-input power multiplexer with auto-input selection and a low dropout linear regulator. The device contains three P-channel MOSFETs that can operate over an input voltage range of 2.5 V to 12 V. The TPS22933 automatically selects the highest voltage level (from BAT, USB, and DC_IN) and enables that input to source the LDO. LOUT is an always-on output from the LDO, but VOUT can be switched on and off using the EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON and OFF Control

The EN pin controls the state of the VOUT switch and VOUT pulldown switch. EN has no control over LOUT. Asserting EN enables the VOUT switch and disables the Quick Output Discharge (QOD) switch. Deasserting EN disables the VOUT switch and enables the QOD switch. EN is active high and has a low threshold, making it capable of interfacing with low voltage signals. The EN pin is compatible with standard GPIO Logic threshold and can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

8.3.2 Power Changeover

The TPS22933 LDO is powered by the highest level input. When input voltages change, the TPS22933 may change which input powers the LDO. During initial power up, the input that reaches the highest value first will power the LDO. Once that decision is made, changing between input sources is based on VCO. When an input source becomes VCO over the input currently supplying power to the LDO, changeover will occur and the new, higher input will power the LDO.

8.4 Device Functional Modes

Table 2 and Table 3 show the behavior of the device with various voltage conditions for the inputs and enable pin.

Table 2. Function Table

EN	LDO TO LOUT	LDO TO VOUT	VOUT TO GND
L	ON	OFF	ON
H	ON	ON	OFF

Table 3. Input Selection Table (V1 > V2 > V3)

BAT	USB	DC_IN	LDO SUPPLY
V1	V2 or V3	V2 or V3	BAT
V2 or V3	V1	V2 or V3	USB
V2 or V3	V2 or V3	V1	DC_IN
V1	V1	V1	See (1)

(1) Whichever source achieves the highest level the fastest will supply the LDO.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 LDO Capacitor (for CAP Pin)

An optional capacitor on the CAP pin helps stabilize the integrated LDO. Take care in capacitor sizing to reduce inrush currents. The voltage on the CAP pin will follow the highest input. Since the max input voltage is 12 V, the capacitor voltage rating must be higher than 12 V.

9.1.2 Using the CAP Pin as a Power Output

Figure 17 shows three power inputs multiplexed to source only through the CAP pin. In this case, the LDO outputs are not used (EN is tied low). The highest of the inputs is chosen to drive the voltage at the CAP pin.

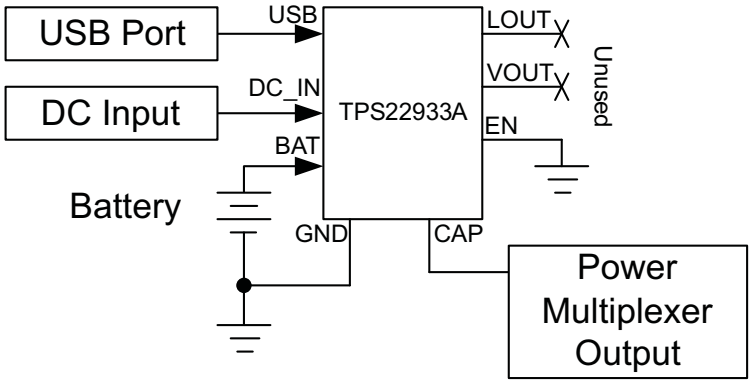


Figure 17. Using the CAP Pin as a Multiplexer Output

9.2 Typical Application

Figure 18 shows three power inputs multiplexed to source the LDO. The LDO always on output (LOUT) is tied to an MSP430. The MSP430 then determines when to enable the switched output (VOUT) by driving the EN pin.

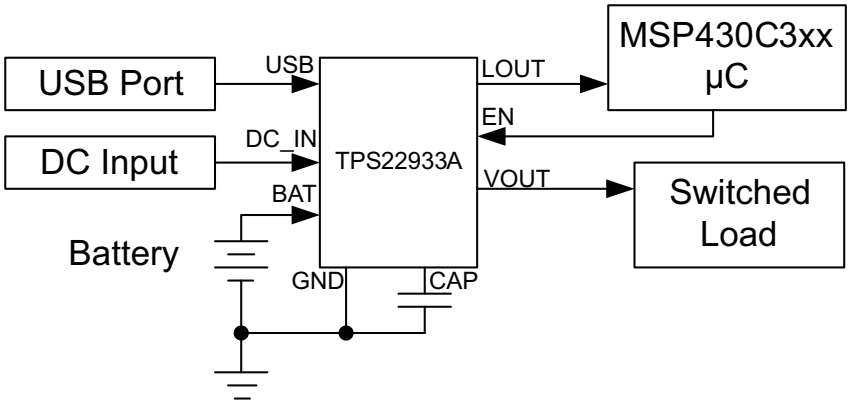


Figure 18. Application Example

Typical Application (continued)

9.2.1 Design Requirements

Table 4 lists the design parameters for TPS22933.

Table 4. Design Parameters

INPUT	VOLTAGE
USB Port	5.0V
DC Input	5.0V
Battery	4.2V

9.2.2 Detailed Design Procedure

Initial power up:
DC_IN = 0 V; USB = 0 V; EN = 0 V
BAT is applied at 4.2 V
LDO power comes from BAT
LOUT = 3.6 V; CAP = 4.2 V; VOUT = 0 V

USB power is connected at 5 V, BAT remains 4.2 V and DC_IN remains 0 V
LDO power is changed from BAT to USB in t_{CO}

LOUT = 3.6 V; CAP = 5 V; VOUT = 0 V

DC_IN power is connected at 5.0 V, BAT remains 4.2 V and USB remains 5 V
No change in LDO power

LOUT = 3.6 V; CAP = 5 V; VOUT = 0 V

EN = VIH, BAT remains 4.2 V, USB remains 5 V and DC_IN remains 5 V
LOUT = 3.6 V, CAP = 5 V; VOUT = 3.6 V

USB power is removed, BAT remains 4.2 V and DC_IN remains 5 V
LDO power is changed from USB to DC_IN

LOUT = 3.6 V; CAP = 5 V; VOUT = 3.6 V

DC_IN power is removed, BAT remains 4.2 V and USB remains 0 V:
LDO power is changed from DC_IN to BAT

LOUT = 3.6 V; CAP = 4.2 V; VOUT = 3.6 V

9.2.3 Application Curve

Figure 19 shows the device behavior in the last step of the design procedure, when DC_IN power is removed and the LDO is powered by the battery. The capacitor on the CAP pin discharges as DC_IN is removed but then charges to the battery voltage when the input is automatically switched. LOUT remains a constant 3.6 V throughout this power switching.

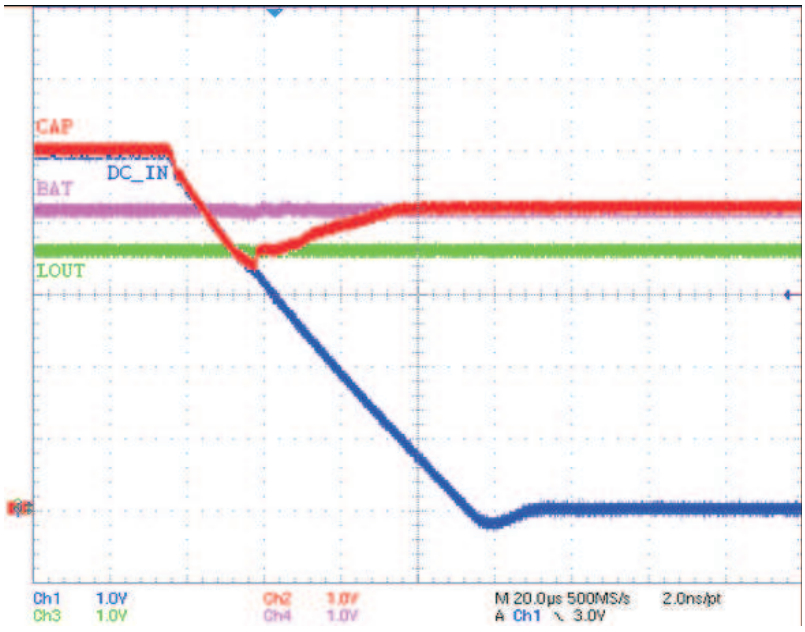


Figure 19. DC_IN Removed, BAT Powers LDO (LOUT = 3.6 V)

10 Power Supply Recommendations

The device is designed to operate with an input voltage range of 2.5 V to 12 V. This supply must be well regulated and placed as close to the device terminals as possible.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for BAT, USB, DC_IN, LOUT, VOUT, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

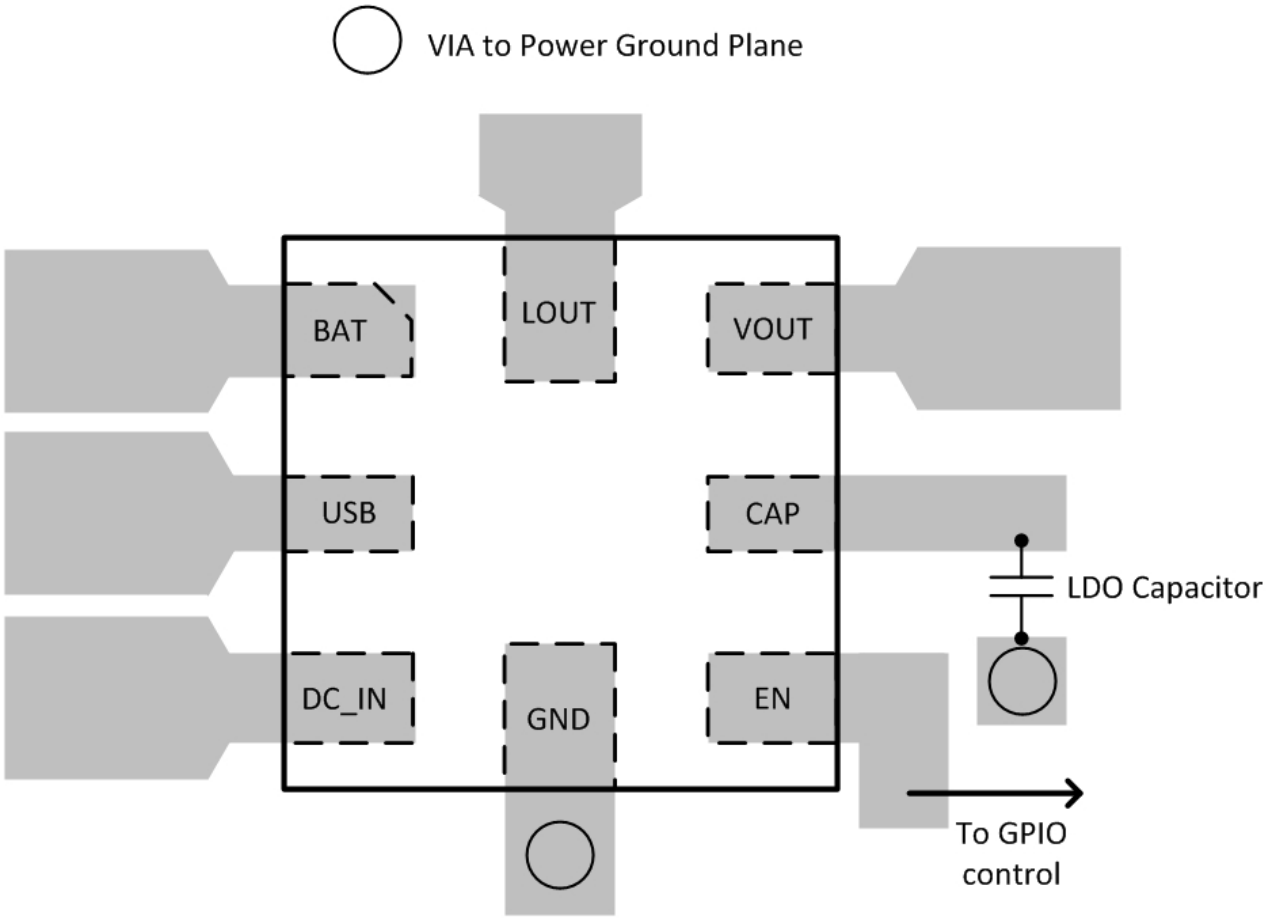


Figure 20. TPS22933 Layout Example

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

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12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22933ARSER	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q
TPS22933ARSER.B	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q
TPS22933ARSET	Active	Production	UQFN (RSE) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q
TPS22933ARSET.B	Active	Production	UQFN (RSE) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

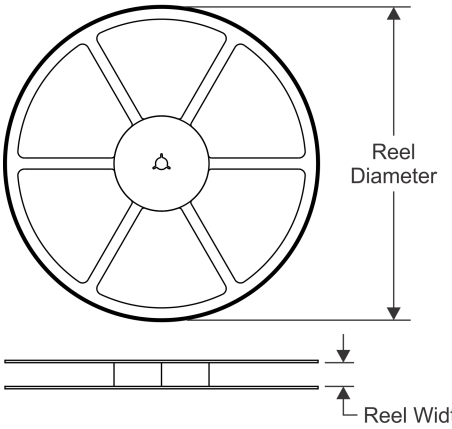
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

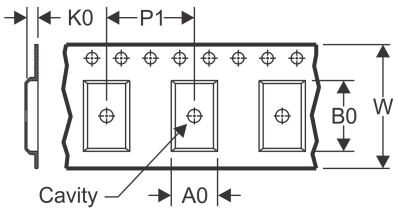
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

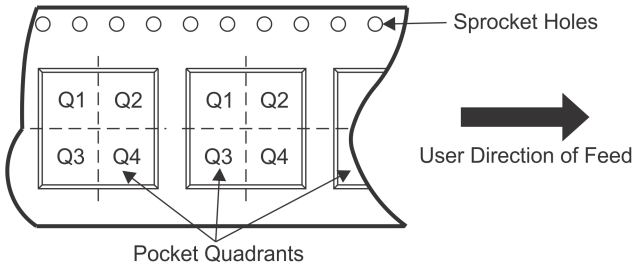


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

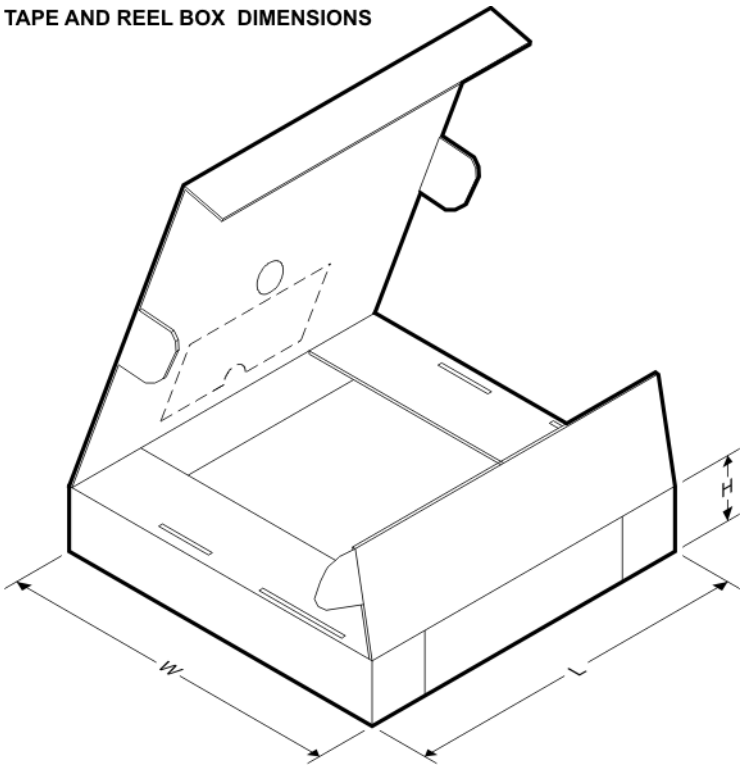
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22933ARSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22933ARSET	UQFN	RSE	8	250	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

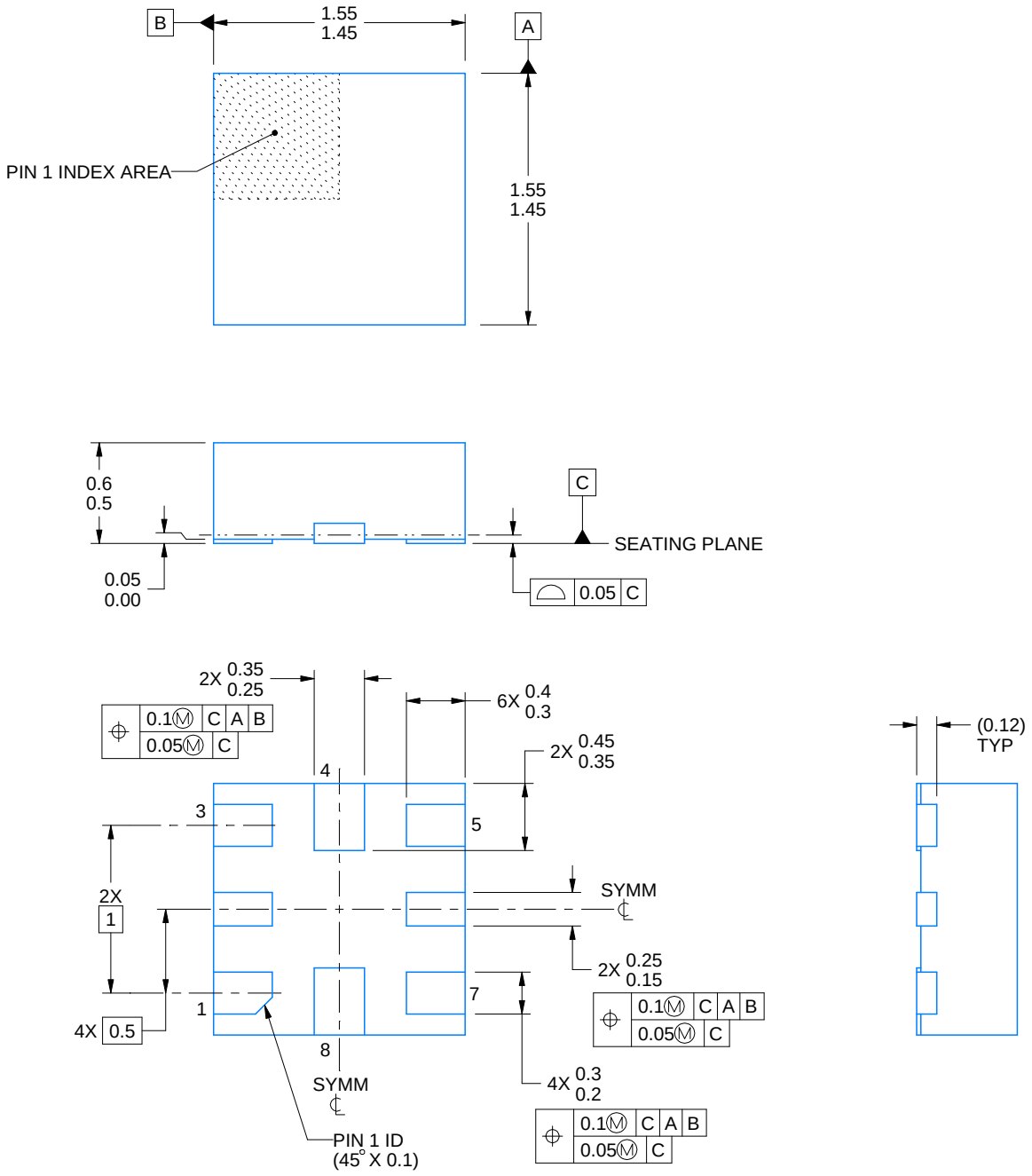
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22933ARSER	UQFN	RSE	8	3000	202.0	201.0	28.0
TPS22933ARSET	UQFN	RSE	8	250	202.0	201.0	28.0

RSE0008A

PACKAGE OUTLINE

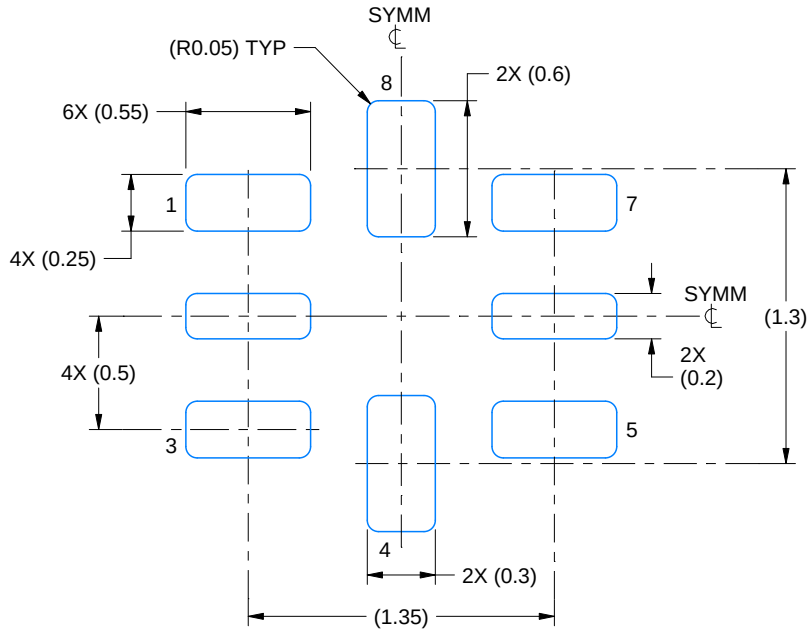
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

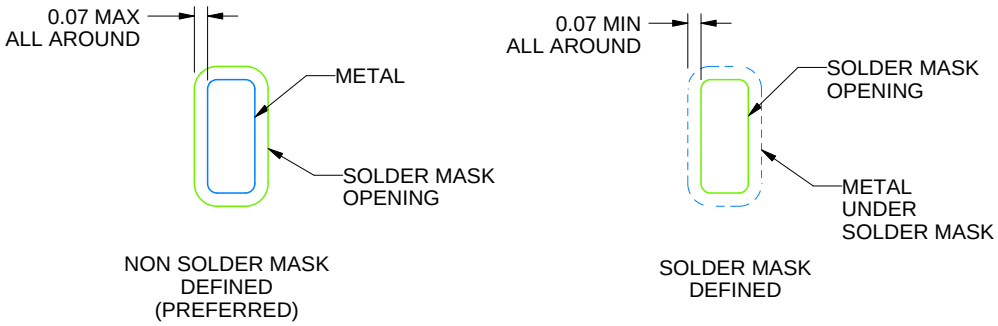


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

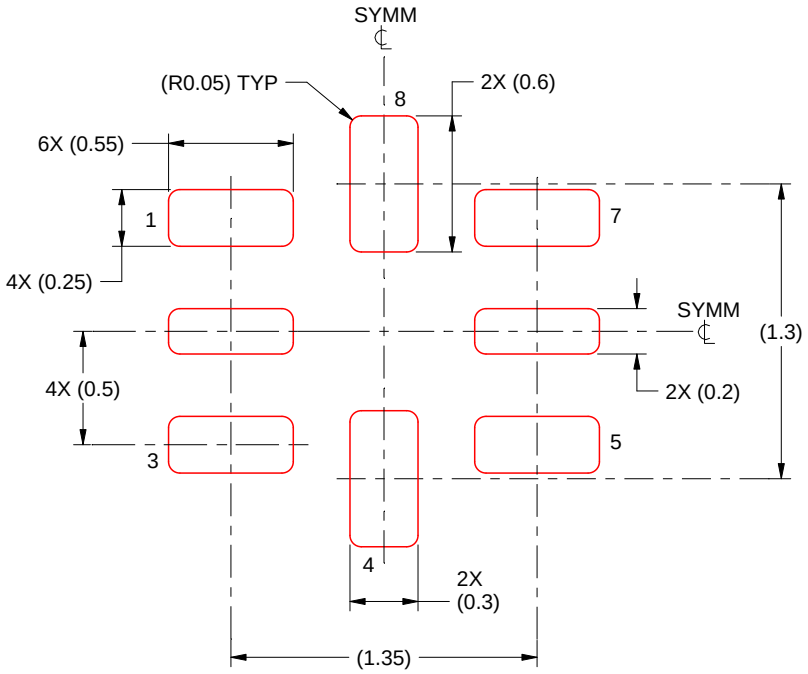


SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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