具有反向电流阻断功能的 TPS22948 5.5V、240mA 限流负载开关

1 特性

- 输入工作电压范围 (V_{IN})：
  2.5V 至 5.5V
- 输出电流限制 (I_{LIMIT})：
  240mA（典型值）
- 热关断 (TSD)
- 导通电阻 (R_{ON})：
  300mΩ（典型值）
- 慢速开通时序可限制浪涌电流（典型值）：
  - 开通时间 (t_{ON})：
    6.6mV/µs 时为 820us
- 常开的反向电流阻断 (RCB)：
  - 导通状态激活电流 (I_{RCB})：
    –200mA（典型值）
- 故障指示 (FLT)
- 智能 ON 引脚下拉电阻 ($R_{PD,ON}$)：
  - ON V_{IH} (I_{ON})：25nA（最大值）
  - ON V_{IL} ($R_{PD,ON}$)：500kΩ（典型值）
- 低功耗：
  - 导通状态 (I_Q)：50uA（典型值）
  - 关断状态 (I_{SD})：0.3uA（典型值）

2 应用

- 个人电子产品
- 机顶盒
- HDMI 输出端口
- 笔记本电脑、台式计算机
- 扩展坞

3 说明

TPS22948 器件是一款小型单通道负载开关，能够通过输出电流限制、反向电流阻断和热关断来提供强大的故障情况保护。

开关导通状态由数字输入控制，此输入可与低压控制信号直接连接。首次加电时，此器件使用智能下拉电阻来保持 ON 引脚不悬空，直到系统定序完成。故意将该引脚驱动为高电平 (>VIH) 之后，便会断开智能下拉电阻，以防止不必要的功率损耗。

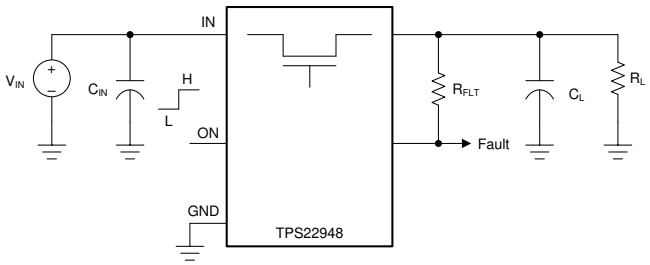
TPS22948 采用标准 SC-70 封装，工作温度范围为 –40°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS22948	SC-70 (6)	2.1mm x 2.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

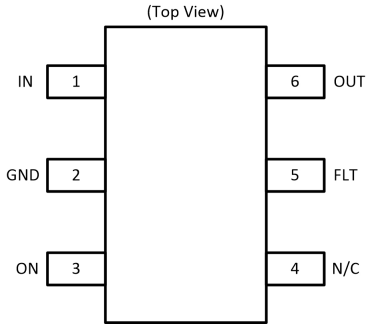
4 修订历史记录

Changes from Original (March 2019) to Revision A **Page**

- 将“预告信息”更改成了“生产数据” ... 1
- 首次公开发布 ... 1

5 Pin Configuration and Functions

DCK Package
6-Pin SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input
2	GND	–	Device ground
3	ON	I	Active high switch control input. Do not leave floating.
4	N/C	–	No connect pin, leave floating or GND
5	FLT	O	Open-drain output, pulled low during thermal shutdown or reverse current-conditions.
6	OUT	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–0.3	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range	–0.3	6	V
V_{FLT}	Maximum FLT Pin Voltage	–0.3	6	V
I_{MAX}	Maximum Output Current	Internally Limited		A
T_J	Junction temperature	Internally Limited		°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	2.5		5.5	V
V_{OUT}	Output Voltage Range	0		5.5	V
V_{IH}	ON Pin High Voltage Range	1		5.5	V
V_{IL}	ON Pin Low Voltage Range	0		0.35	V
I_{OUT}	Output Current Range	0		130	mA
C_{OUT} (1)	Output Capacitance		18		nF
T_A	Ambient temperature	–40		125	°C

(1) The recommended output capacitance is the capacitance placed next to the output of the device that will provide optimal hard short performance across different load cable lengths.

6.4 Thermal Information

THERMAL METRIC(1)		TPS22948 DCK (SC-70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	213.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	50.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless otherwise noted, the characteristics in the following table applies at 5 V with a load of C_L = 0.1 µF, R_L = 100 Ω. Typical Values are at 25°C.

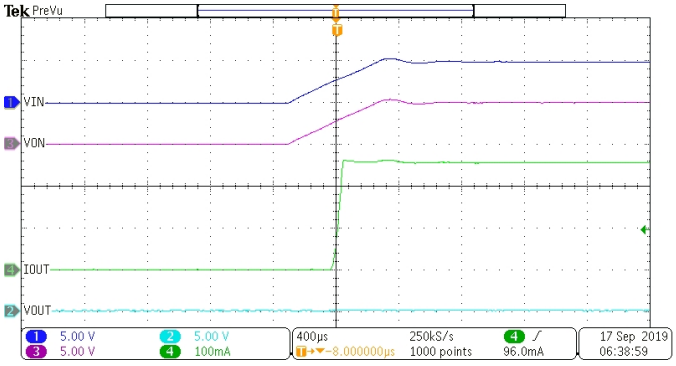
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Input Supply (VIN)								
$I_{Q, VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, VOUT = Open		-40°C to 125°C		50	85	µA
$I_{SD, VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, VOUT = GND		-40°C to 125°C		0.3	5	µA
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	I_{OUT} = -50 mA		25°C		300	350	mΩ
				-40°C to 85°C			450	
				-40°C to 125°C			500	
Output Current Limit (ILIM)								
I_{LIM}	Output Current Limit			-40°C to 125°C	130	240	350	mA
t_{LIM}	Current Limit Response Time	Output hard short ($I_{OUT} > I_{LIM}$)		-40°C to 125°C		2		µs
Reverse Current Blocking (RCB)								
V_{RCB}	Activation Threshold	V_{OUT} Rising; $V_{OUT} > V_{IN}$		-40°C to 125°C		60		mV
	Release Threshold	V_{OUT} Falling; $V_{OUT} > V_{IN}$		-40°C to 125°C		44		mV
t_{RCB}	Response Time	$V_{OUT} = V_{IN}$ + 1V		-40°C to 125°C		3		µs
$I_{Q, RCB}$	RCB Quiescent Current (VIN)	$V_{ON} \leq V_{IL}$ $V_{OUT} - V_{IN}$ = 1V	$V_{ON} \leq V_{IL}$ $V_{OUT} - V_{IN}$ = 1V	-40°C to 125°C			15	µA
Fault Indication (FLT)								
$V_{OL, FLT}$	Output Low Voltage	I_{FLT} = 1 mA		-40°C to 125°C			0.1	V
$t_{DG,FLT}$	Fault Delay Time	$V_{ON} \geq V_{IH}$		-40°C to 125°C		10		µs
I_{FLT}	Off State Leakage	$V_{ON} \leq V_{IL}$		-40°C to 125°C			25	nA
Enable Pin (ON)								
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$		-40°C to 85°C		500		kΩ
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$		-40°C to 125°C			25	nA
Thermal Shutdown (TSD)								
TSD	Thermal Shutdown	Rising		N/A	130	150	170	°C
		Falling (Hysteresis)		N/A	100	120	140	°C

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 5 V and 25°C

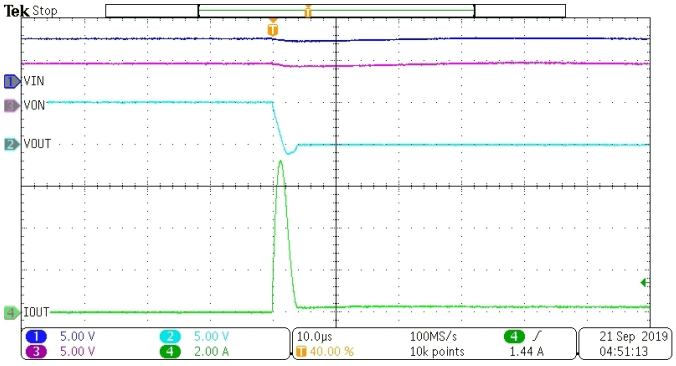
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	C_L = 18 nF, R_L = 100 Ω		820		µs
t_R	Output Rise Time	C_L = 18 nF, R_L = 100 Ω		600		µs
SR_{ON}	Turn ON Slew Rate	C_L = 18 nF, R_L = 100 Ω		6.6		mV/µs
t_{OFF}	Turn OFF Time	C_L = 18 nF, R_L = 100 Ω		15		µs
t_{FALL}	Output Fall Time	C_L = 18 nF, R_L = 100 Ω		6.9		µs

6.7 Typical Characteristics



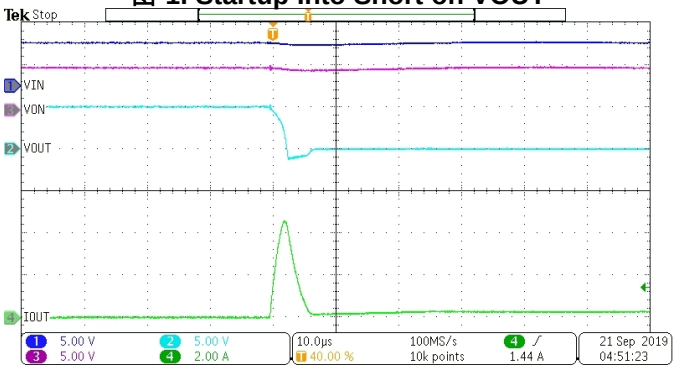
V_{IN} = 5 V T_A = 25 °C V_{OUT} = 0 V

图 1. Startup Into Short on VOUT



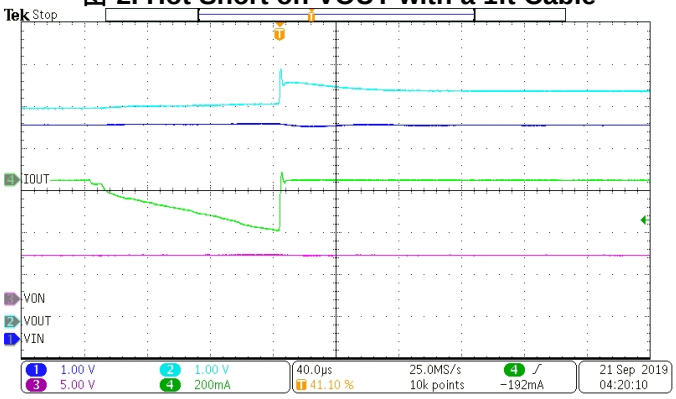
V_{IN} = 5 V T_A = 25 °C C_{OUT} = 18 nF

图 2. Hot Short on VOUT with a 1ft Cable



V_{IN} = 5 V T_A = 25 °C C_{OUT} = 18 nF

图 3. Hot Short on VOUT with a 3ft Cable



V_{IN} = 5 V T_A = 25 °C

图 4. Reverse Current Blocking Behavior

7 Parameter Measurement Information

7.1 Timing Waveform Diagram

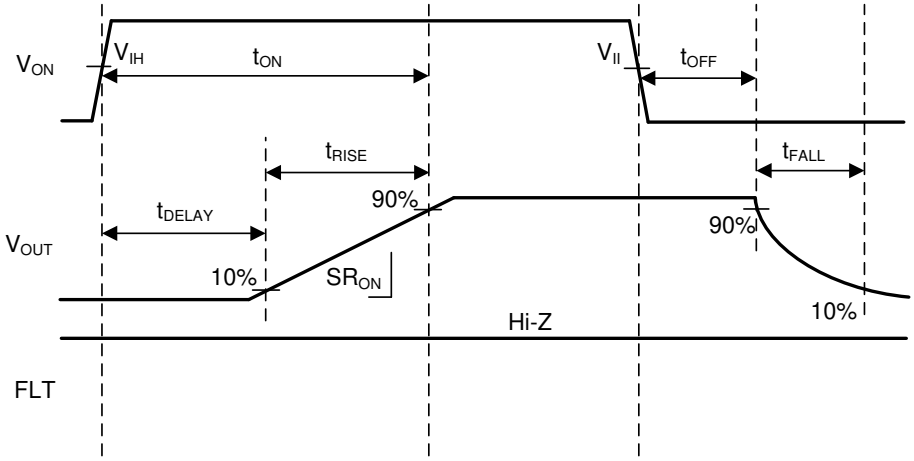


图 5. Timing Waveforms

8 Detailed Description

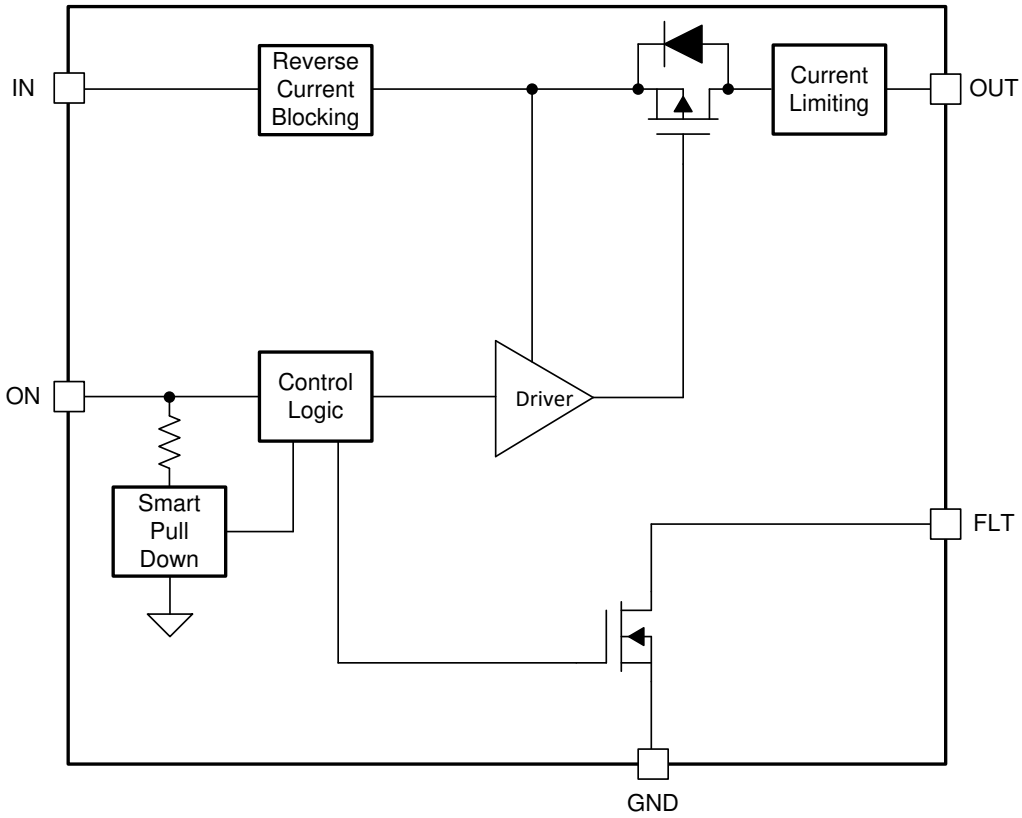
8.1 Overview

The TPS22948 device is a 5.5-V, 240-mA current limited load switch in a 6-pin SC-70 package. The 300-mΩ P-channel FET is used to switch power from input to output with minimal voltage drop across the device.

The TPS22948 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, and driver eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22948 load switch also provides protection features such as reverse current blocking, output current limiting and thermal shutdown.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a smart pull down is used to keep the ON pin from floating until system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the smart pull down is disconnected to prevent unnecessary power loss. See 表 1 when the ON pin smart pull down is active.

表 1. Smart-ON Pull Down

VON	Pull Down
≤ V_{IL}	Connected
≥ V_{IH}	Disconnected

8.3.2 Fault Indication (FLT)

The FLT pin is an open drain output that acts as a status indication for the device. It is pulled low during thermal shutdown or reverse-current events. The behavior of the FLT pin is shown in 图 6.

8.3.3 Current Limiting (V_{SC})

The TPS22948 responds to overcurrent conditions by limiting its output current to the ILIM level shown in 图 6.

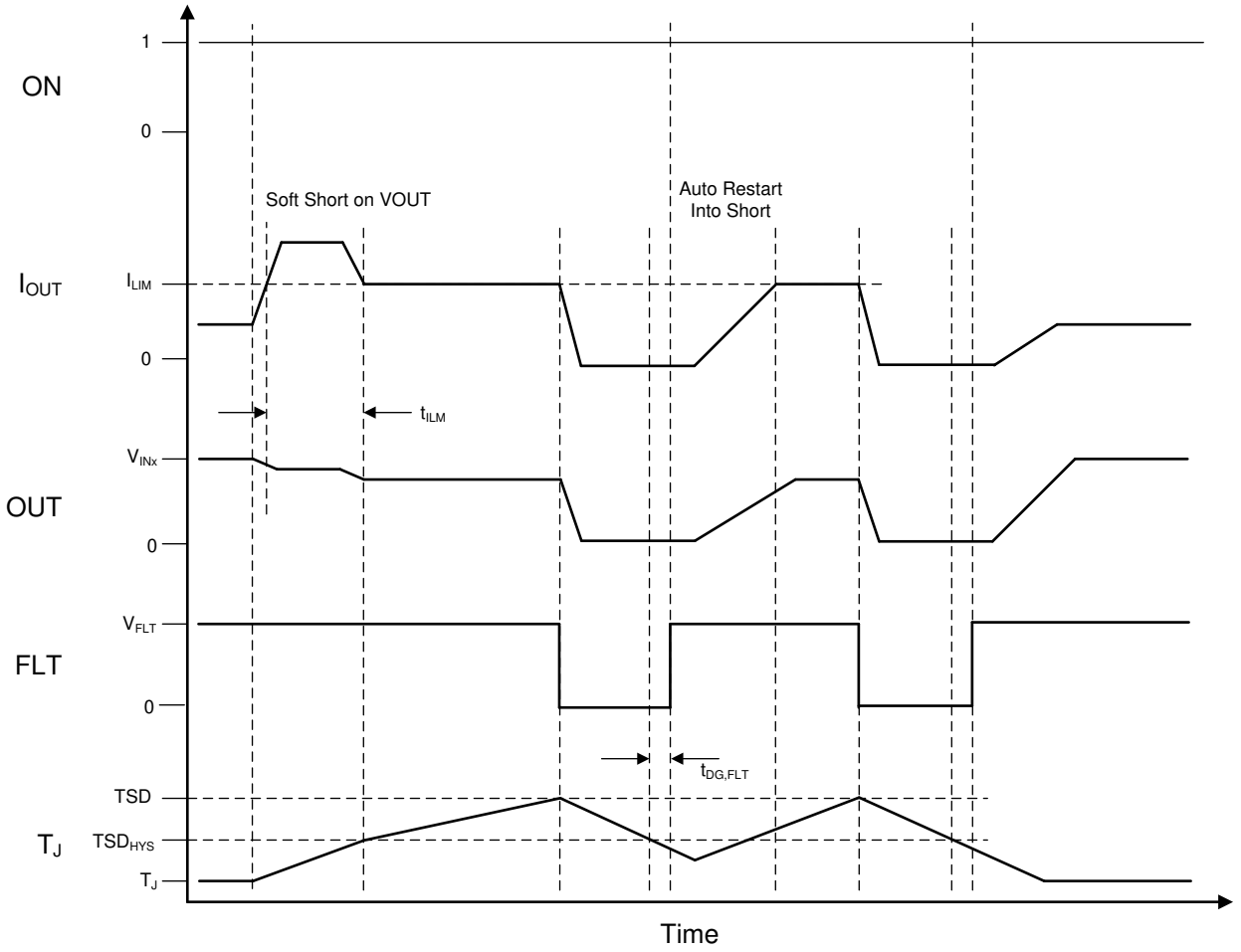


图 6. TPS22948 Current Limiting Behavior

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output and the ON pin is toggled high, turning the device on. The output voltage is held near zero potential with respect to ground and the TPS22948 ramps the output current to I_{LIM}. The TPS22948 device will limit the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and the device turns itself off. The device remains off until the junction temperature has lowered by TSD_{HYS}, and the device will turn itself back on. This will cycle until the overload condition is removed.

The second condition is when a short circuit, partial short circuit, or transient overload occurs after the device has been fully powered on. The device responds to the overcurrent condition within time t_{LIM} (see 图 7), and before this time, the current is able to exceed I_{LIM}. In the case of a fast transient, the current-sense amplifier is overdriven and momentarily disables the internal power FET. The current-sense amplifier recovers and limits the output current to I_{LIM}. Similar to the previous case, the TPS22948 limits the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and begins thermally cycling on and off.

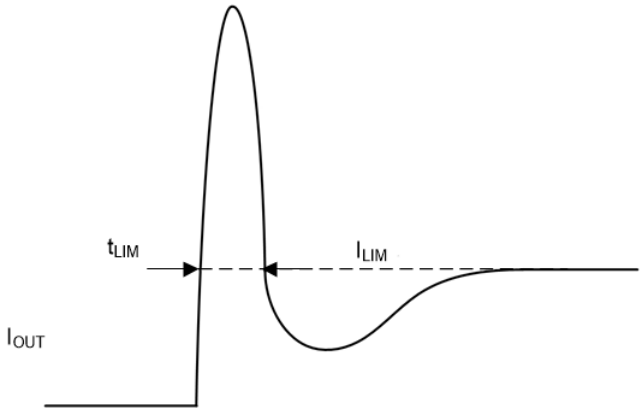


图 7. Transient Current Limit Waveform

8.3.4 Reverse Current Blocking (RCB)

In a scenario where the device is enabled and VOUT is greater than VIN, there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold is exceeded (about 200 mA), there is a delay time (t_{RCB}) before the switch turns off to stop the current flow. The switch will remain off and block reverse current as long as the reverse voltage condition exists. Once VOUT has dropped below the release voltage threshold (V_{RCB}) the device will turn back on. When the ON pin is pulled low, the device will constantly block reverse current.

8.4 Device Functional Modes

表 2 describes the connection of the VOUT pin depending on the state of the ON pin.

表 2. VOUT Connection

ON	TPS22919 VOUT
L	Open
H	VIN

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22948 device can be used to power downstream modules.

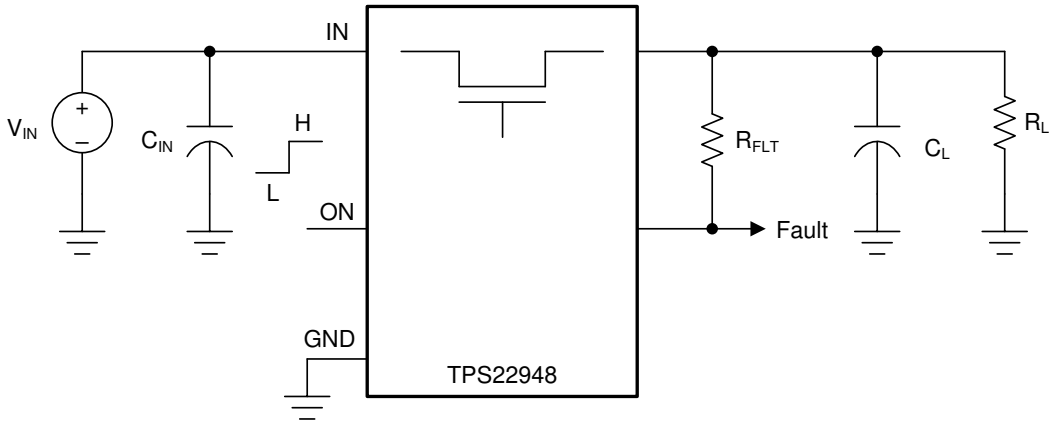


图 8. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in 表 3 as the design parameters:

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	5 V
Load Current / Resistance (R_L)	1 kΩ
Load Capacitance (C_L)	10 µF
Maximum Inrush Current (I_{INRUSH})	100 mA

Although the load capacitance is 10 µF, this is assumed to be at the end of a cable or closer to the load. An 18nF capacitance close to the output of the device is recommended for optimal performance during short circuit conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use 公式 1 to find the maximum output capacitance for a given inrush current requirement.

$$C_L = I_{INRUSH} \times t_R \div (0.8 \times V_{IN})$$

where

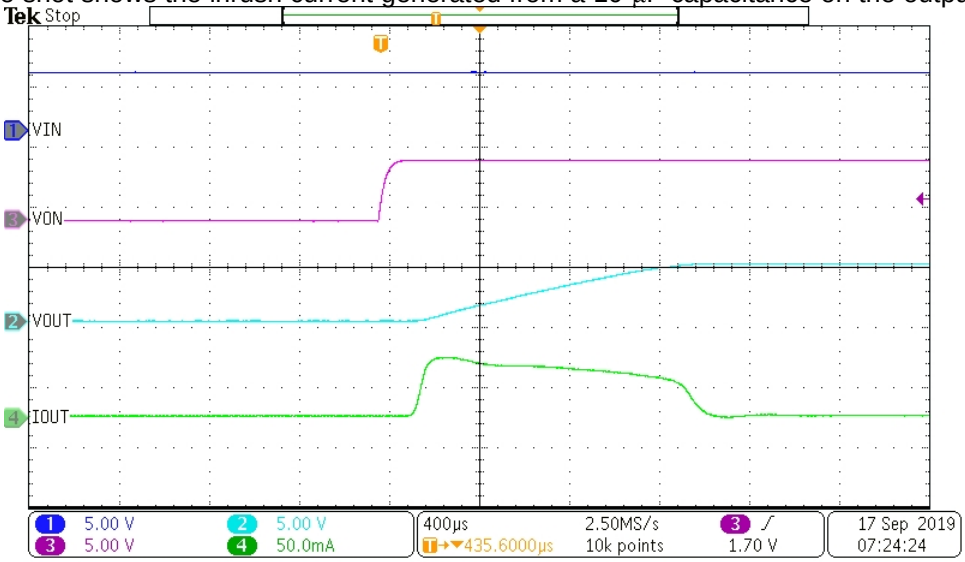
- C_L = capacitance on VOUT (µF)
- I_{INRUSH} = maximum acceptable inrush current (A)
- t_R = rise time of the TPS22948 (µs)

- V_{IN} = input voltage (V) (1)

Based on 公式 1, the maximum output capacitance that limits the inrush current to 100 mA is 12.5 µF. Therefore, the desired 10-µF load capacitance will not exceed the inrush current design requirement during turn on.

9.2.3 Application Curves

The below scope shot shows the inrush current generated from a 10-µF capacitance on the output.



A.

VIN = 5 V CL = 10 µF

图 9. TPS22948 Inrush Current Control with Slow Rise Time

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 2.5 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input. A 18nF capacitance close to the output of the device is recommended for optimal performance during short circuit conditions.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

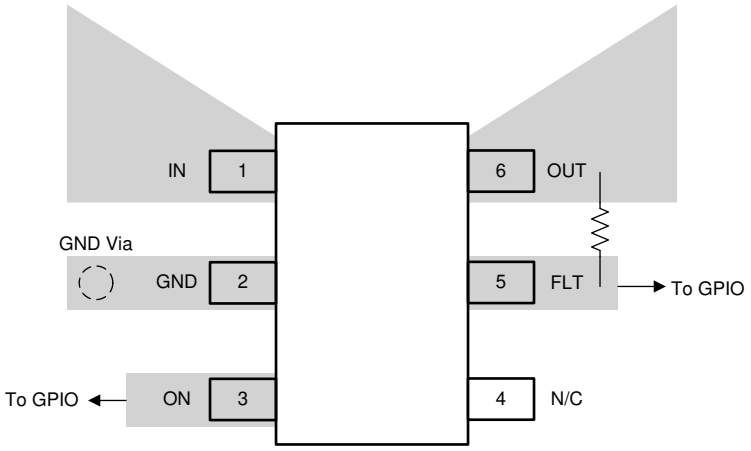


图 10. Recommended Board Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 商标

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22948DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	1CT
TPS22948DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

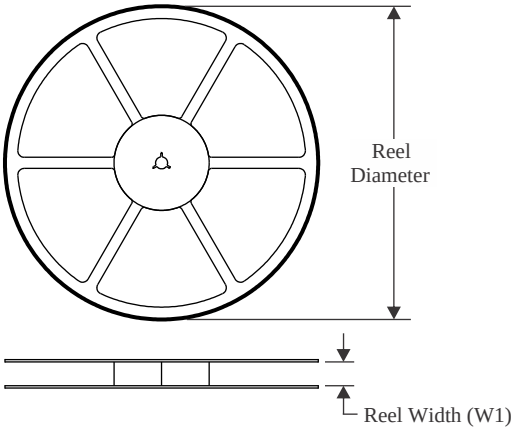
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

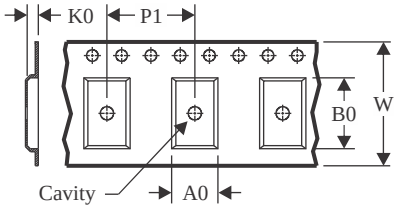
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

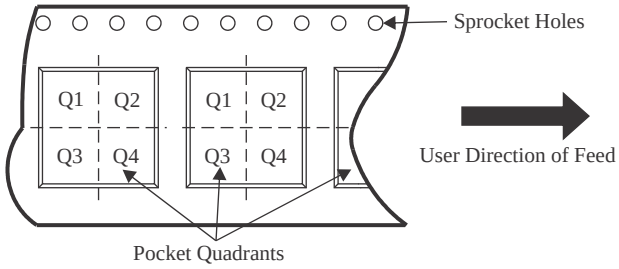


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

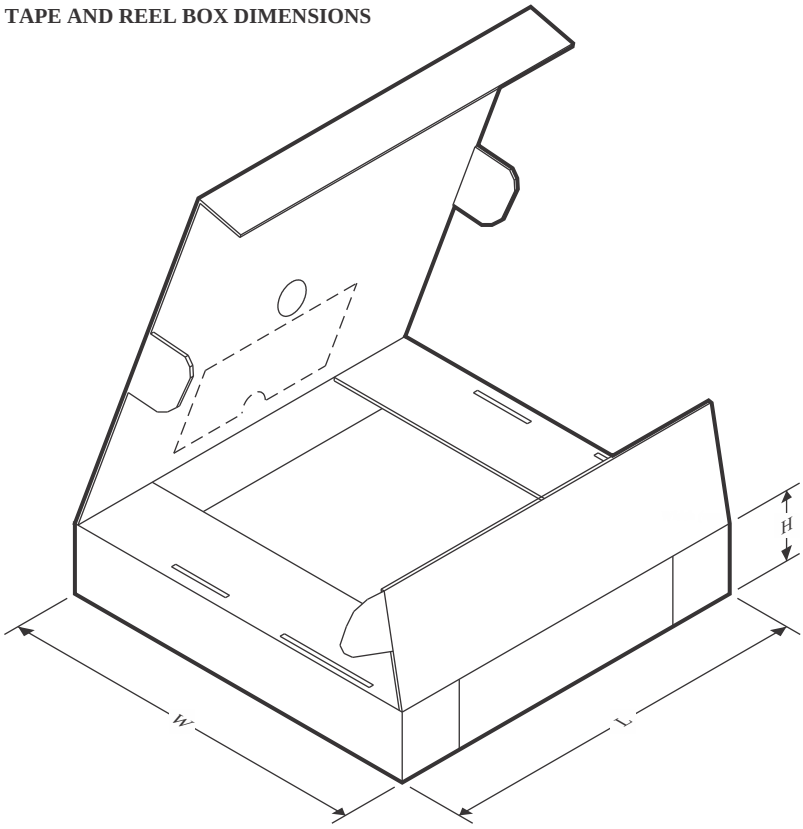
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22948DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS22948DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

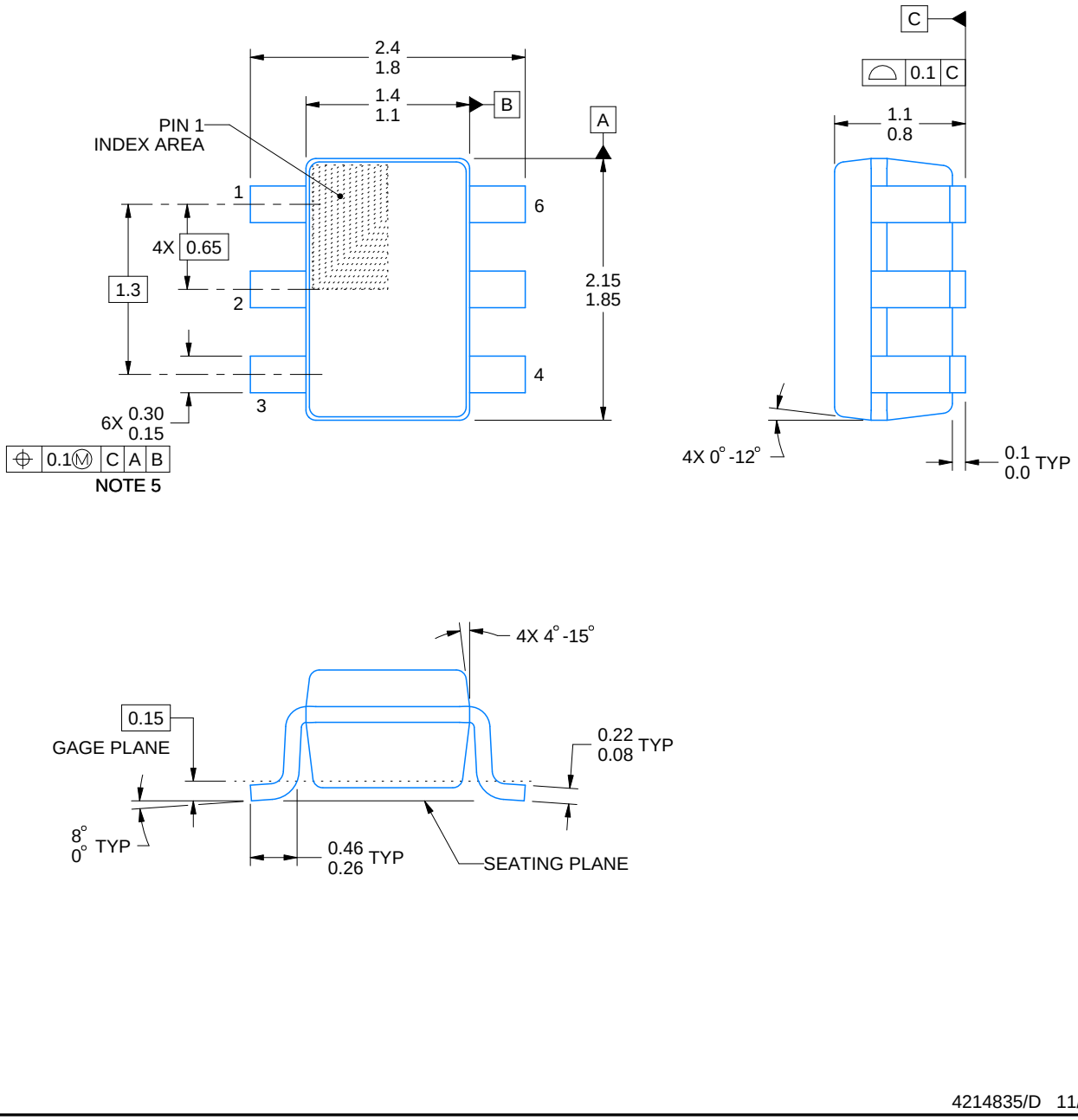
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22948DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TPS22948DCKR	SC70	DCK	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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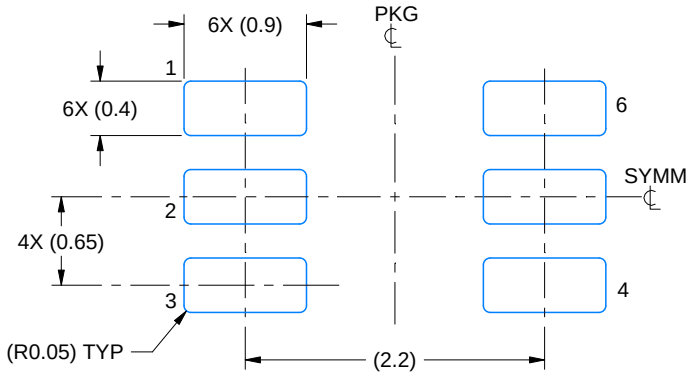
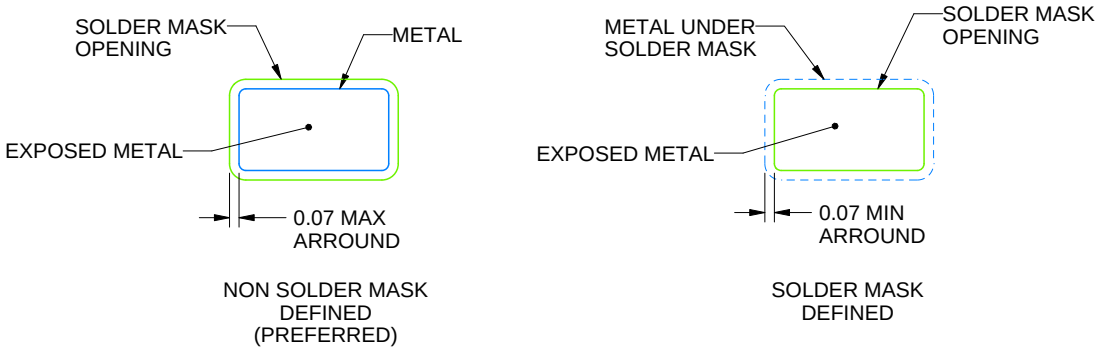
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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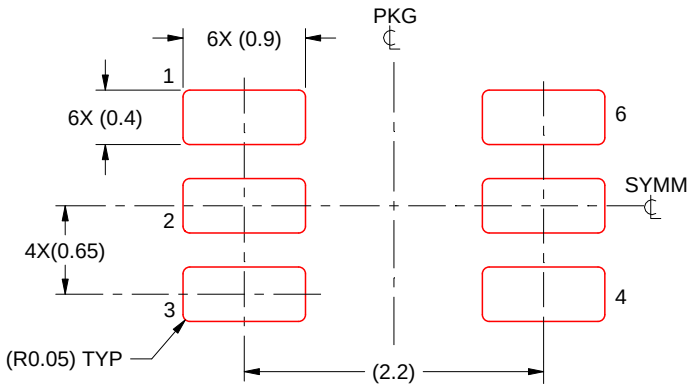
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月