



TPS22961 3.5V, 6A, 超低电阻负载开关

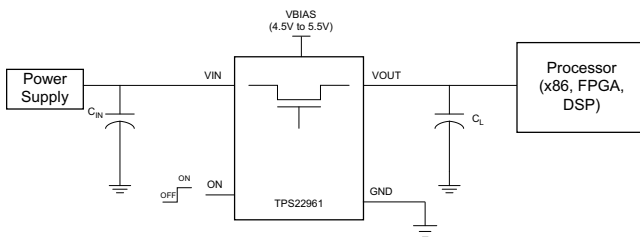
1 特性

- 集成单通道负载开关
- VBIAS 电压范围: 3V 至 5.5V
- 输入电压范围: 0.8V 至 3.5V
- 超低 R_{ON} 电阻
 - $V_{IN} = 1.05V$ ($V_{BIAS} = 5V$) 时, $R_{ON} = 4.4m\Omega$
- 6A 最大持续开关电流
- 低静态电流小于 $1\mu A$ (最大值)
- 低控制输入阈值支持使用 1.2V/1.8V/2.5V/3.3V 逻辑器件
- 受控转换率
 - $V_{IN} = 1.05V$ 时 ($V_{BIAS} = 5V$), $t_R = 4.2\mu s$
- 快速输出放电 (QOD)
- 带有散热垫的小外形尺寸无引线 (SON) 8 端子封装
- 静电放电 (ESD) 性能经测试符合 JESD 22 规范
 - 2kV 人体放电模式 (HBM) 和 1kV 器件充电模型 (CDM)

2 应用范围

- Ultrabook™/笔记本电脑
- 台式机
- 服务器
- 机顶盒
- 电信系统
- 平板电脑

4 简化电路原理图



典型应用: 驱动用于处理器的高电流内核电源轨

3 说明

TPS22961 是一款小型, 超低 R_{ON} , 单通道负载开关, 此开关具有受控开启功能。此器件包含一个可在 0.8V 至 3.5V 输入电压范围内运行的 N 通道金属氧化物半导体场效应晶体管 (MOSFET), 并且支持最大 6A 的持续电流。

器件的超低 R_{ON} 和高电流处理能力的组合使得此器件非常适合于驱动具有非常严格压降耐受的处理器的电源轨。器件的快速上升时间使得电源轨可以在器件被启用时迅速接通, 从而减少配电响应时间。此开关可由 ON 端子单独控制, 此端子能够与微控制器或低压离散逻辑电路生成的低压控制信号直接对接。通过集成一个 260Ω 下拉电阻器, 在开关关闭时实现快速输出放电 (QOD), 此器件进一步减少总体解决方案尺寸。

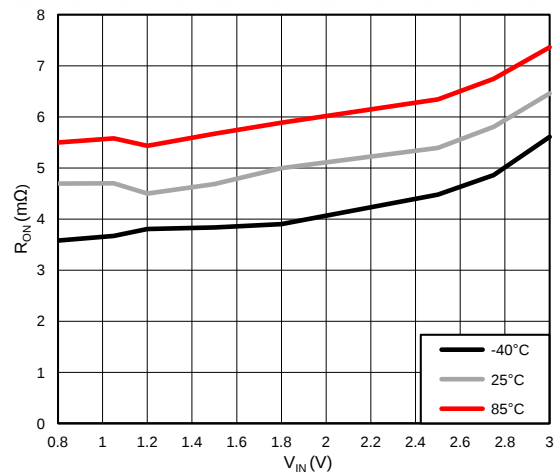
TPS22961 采用小型, 节省空间的 $3mm \times 3mm$ 8 端子小外形尺寸无引线 (SON) 封装 (DNY), 此类封装具有可实现高功率耗散的集成散热垫。器件在自然通风环境下的额定运行温度范围为 $-40^\circ C$ 至 $85^\circ C$ 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸
TPS22961	WS0N (8)	$3.00mm \times 3.00mm$

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

R_{ON} 与 V_{IN} 之间的关系 ($V_{BIAS} = 5V$, $I_{OUT} = -200mA$)



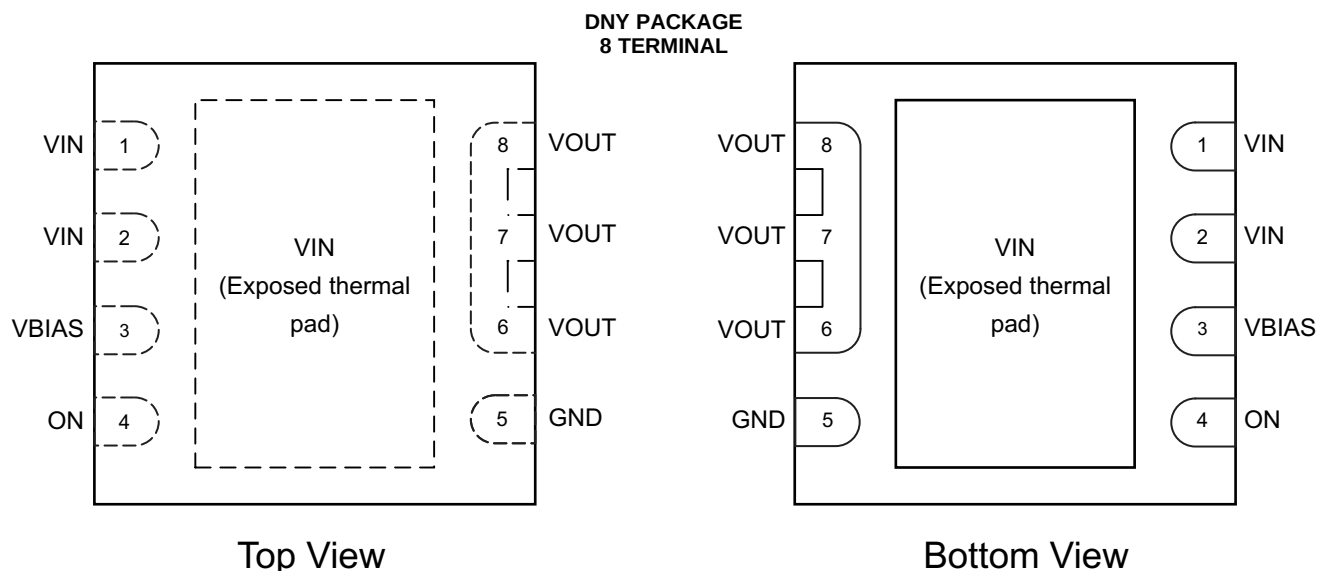
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5 修订历史记录

Changes from Revision A (February 2014) to Revision B	Page
• Fixed caption error in Filtered Output curve.	18
Changes from Original (February 2014) to Revision A	Page
• 完整版的最初发布版本。	1

6 Terminal Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1, 2	I	Switch input. Place ceramic bypass capacitor(s) between this terminal and GND. See Detailed Description section for more information.
VIN	Exposed thermal Pad	I	Switch input. Place ceramic bypass capacitor(s) between this terminal and GND. See Detailed Description section for more information.
VBIAS	3	I	Bias voltage. Power supply to the device.
ON	4	I	Active high switch control input. Do not leave floating.
GND	5	–	Ground.
VOUT	6, 7, 8	O	Switch output. Place ceramic bypass capacitor(s) between this terminal and GND. See Detailed Description section for more information.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	–0.3	4	V
V _{BIAS}	Bias voltage range	–0.3	6	V
V _{OUT}	Output voltage range	–0.3	4	V
V _{ON}	ON pin voltage range	–0.3	6	V
I _{MAX}	Maximum Continuous Switch Current		6	A
I _{PLS}	Maximum Pulsed Switch Current, pulse < 300 μs, 2% duty cycle		8	A
T _A	Operating free-air temperature range	–40	85	°C
T _J	Maximum junction temperature		125	°C

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{STG}	Storage temperature range	–65	150	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
V _{ESD} ⁽¹⁾	Human-Body Model (HBM) ⁽²⁾		2	kV
	Charged-Device Model (CDM) ⁽³⁾		1	kV

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input voltage range		0.8	V _{BIAS} – 1.95	V
V _{BIAS}	Bias voltage range		3	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range			V _{IN}	V
V _{IH, ON}	High-level voltage, ON	V _{BIAS} = 3 V to 5.5 V	1.2	5.5	V
V _{IL, ON}	Low-level voltage, ON	V _{BIAS} = 3 V to 5.5 V	0	0.5	V
C _{IN}	Input Capacitor		1 ⁽¹⁾		μF

- (1) Refer to [Detailed Description](#) section.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22961	UNIT
		DNY	
		8 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	44.6	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	44.4	
θ _{JB}	Junction-to-board thermal resistance	17.6	
ψ _{JT}	Junction-to-top characterization parameter	0.4	
ψ _{JB}	Junction-to-board characterization parameter	17.4	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	1.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics, $V_{BIAS} = 5.0\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (full) and $V_{BIAS} = 5.0\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = 3\text{ V}$, $V_{ON} = V_{BIAS} = 5.0\text{ V}$	Full		0.6	1	μA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full		0.6	1	μA
$I_{SD, VIN}$	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full	$V_{IN} = 3.0\text{ V}$	0.0009	0.1	μA
				$V_{IN} = 2.5\text{ V}$	0.0008	0.1	
				$V_{IN} = 2.0\text{ V}$	0.0007	0.1	
				$V_{IN} = 1.05\text{ V}$	0.0007	0.1	
				$V_{IN} = 0.8\text{ V}$	0.0006	0.1	
I_{ON}	ON terminal input leakage current	$V_{ON} = 5.5\text{ V}$	Full			0.1	μA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 5.0\text{ V}$	$V_{IN} = 3.0\text{ V}$	25°C	6.5	8	$\text{m}\Omega$
				Full		8.8	
			$V_{IN} = 2.5\text{ V}$	25°C	5.3	6.3	$\text{m}\Omega$
				Full		7.2	
			$V_{IN} = 2.0\text{ V}$	25°C	4.8	5.8	$\text{m}\Omega$
				Full		6.7	
			$V_{IN} = 1.05\text{ V}$	25°C	4.4	5.3	$\text{m}\Omega$
				Full		6.2	
			$V_{IN} = 0.8\text{ V}$	25°C	4.3	5.3	$\text{m}\Omega$
				Full		6.1	
R_{PD}	Output pulldown resistance	$V_{IN} = 5.0\text{ V}$, $V_{ON} = 0\text{ V}$, $V_{OUT} = 1\text{ V}$	Full		260	300	Ω

7.6 Electrical Characteristics, $V_{BIAS} = 3.0\text{ V}$

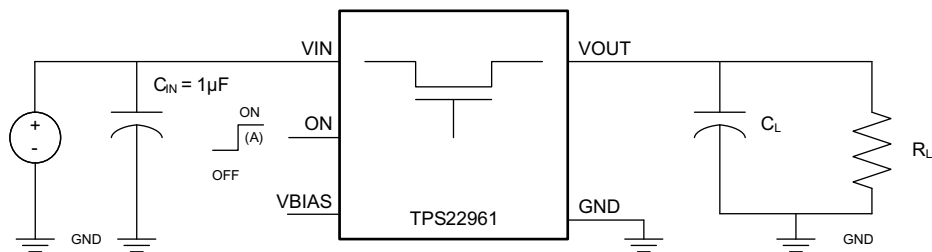
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (full) and $V_{BIAS} = 3.0\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = 1\text{ V}$, $V_{ON} = V_{BIAS} = 3.0\text{ V}$	Full		0.3	1	μA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full		0.3	1	μA
$I_{SD, VIN}$	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	Full	$V_{IN} = 1.05\text{ V}$	0.001	0.1	μA
				$V_{IN} = 0.8\text{ V}$	0.0008	0.1	
I_{ON}	ON terminal input leakage current	$V_{ON} = 5.5\text{ V}$	Full			0.1	μA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 3.0\text{ V}$	$V_{IN} = 1.05\text{ V}$	25°C	6.7	8.4	$\text{m}\Omega$
				Full		9.2	
			$V_{IN} = 0.8\text{ V}$	25°C	5.8	7.0	$\text{m}\Omega$
				Full		7.9	
R_{PD}	Output pull-down resistance	$V_{IN} = 3\text{ V}$, $V_{ON} = 0\text{ V}$, $V_{OUT} = 1\text{ V}$	Full		260	300	Ω

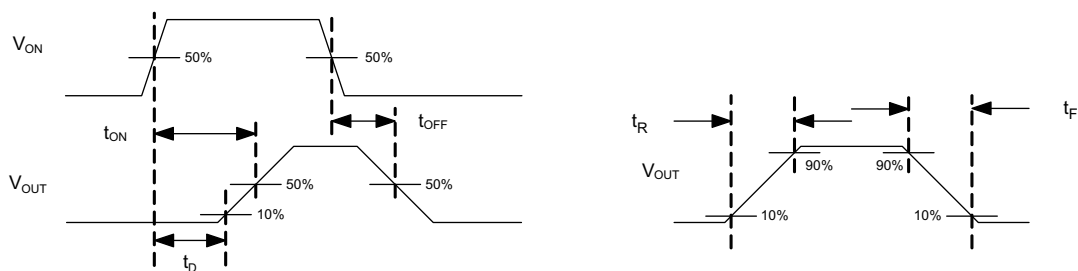
7.7 Switching Characteristics

Refer to the timing test circuit in [Figure 1](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN} = 2.5 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF	10.0			μs
t _{OFF}	Turn-off time		3.5			
t _R	V _{OUT} rise time		6.3			
t _F	V _{OUT} fall time		2.0			
t _D	Delay time		8.1			
V _{IN} = 1.05 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	L = 2.2 μH (DCR = 0.33 Ω), C = 2 x 22 μF (Refer to Typical Application Powering Rails Sensitive to Ringing and Overvoltage due to Fast Rise Time and Figure 31)	8.1	11.3	17.3	μs
t _{OFF}	Turn-off time		13700			
t _R	V _{OUT} rise time		5	9.5	12.5	
t _F	V _{OUT} fall time		44200			
t _D	Delay time		6.7	9.3	12.5	
V _{IN} = 0.8 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF	9.7			μs
t _{OFF}	Turn-off time		6.0			
t _R	V _{OUT} rise time		3.2			
t _F	V _{OUT} fall time		1.8			
t _D	Delay time		8.1			
V _{IN} = 1.05 V, V _{ON} = 5 V, V _{BIAS} = 3.0 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF	19.1			μs
t _{OFF}	Turn-off time		4.7			
t _R	V _{OUT} rise time		9.0			
t _F	V _{OUT} fall time		2.0			
t _D	Delay time		15.6			
V _{IN} = 0.8 V, V _{ON} = 5 V, V _{BIAS} = 3.0 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF	19.0			μs
t _{OFF}	Turn-off time		5.4			
t _R	V _{OUT} rise time		7.0			
t _F	V _{OUT} fall time		1.9			
t _D	Delay time		15.7			



Timing Test Circuit

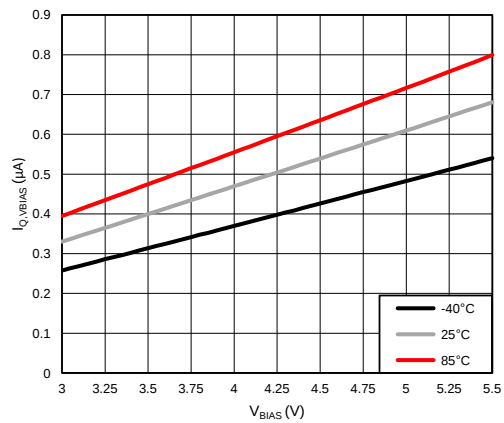


Timing Waveforms

(A) Rise and fall times of the control signal is 100ns.

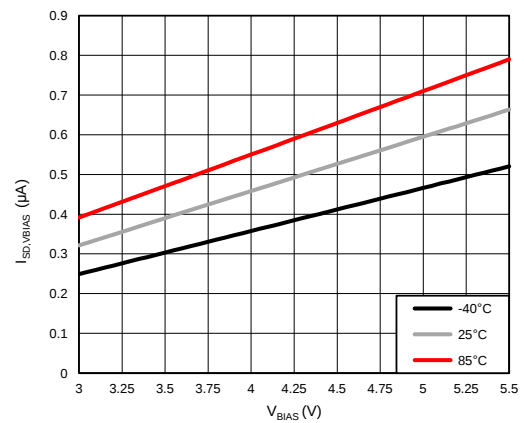
Figure 1. Switching Characteristics Measurement Setup and Definitions

7.8 Typical Characteristics



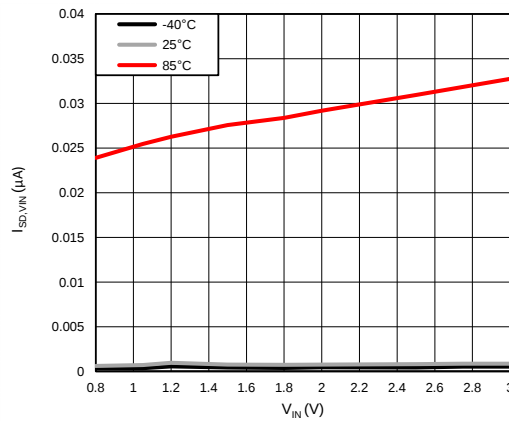
$V_{IN} = 1.05\text{ V}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = 0\text{ A}$

Figure 2. $I_{Q,VBIAS}$ vs V_{BIAS}



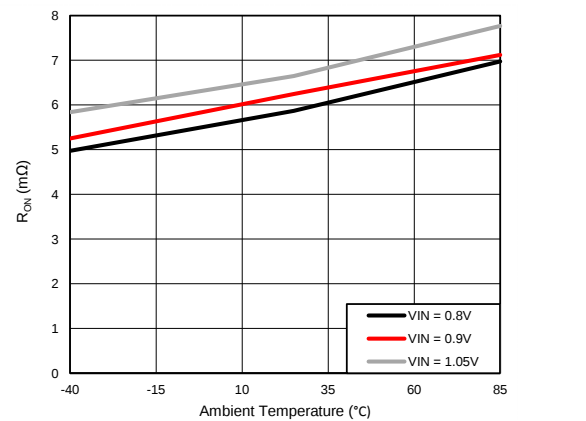
$V_{ON} = 0\text{ V}$ $V_{OUT} = 0\text{ V}$

Figure 3. $I_{SD,VBIAS}$ vs V_{BIAS}



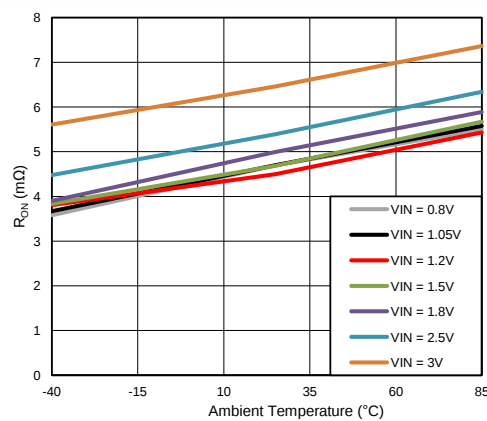
$V_{BIAS} = 5\text{ V}$ $V_{ON} = 0\text{ V}$ $V_{OUT} = 0\text{ V}$

Figure 4. $I_{SD,VIN}$ vs V_{IN}



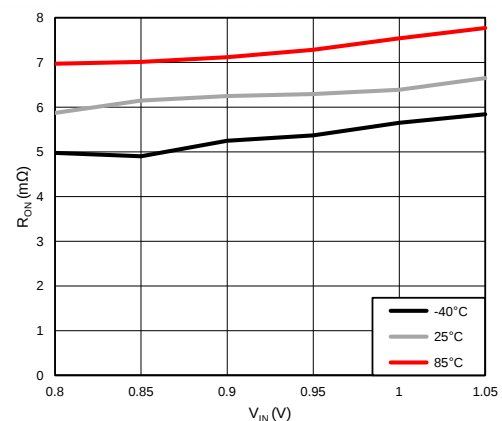
$V_{BIAS} = 3\text{ V}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = -200\text{ mA}$

Figure 5. R_{ON} vs Ambient Temperature



$V_{BIAS} = 5\text{ V}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = -200\text{ mA}$

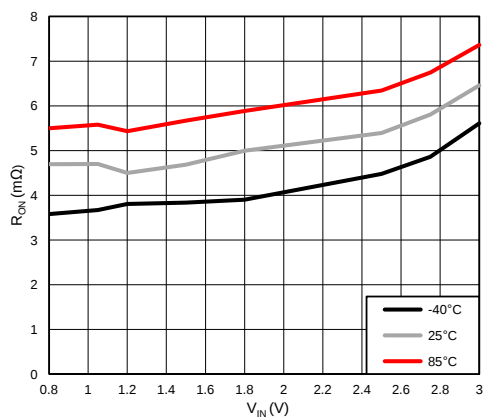
Figure 6. R_{ON} vs Ambient Temperature



$V_{BIAS} = 3\text{ V}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = -200\text{ mA}$

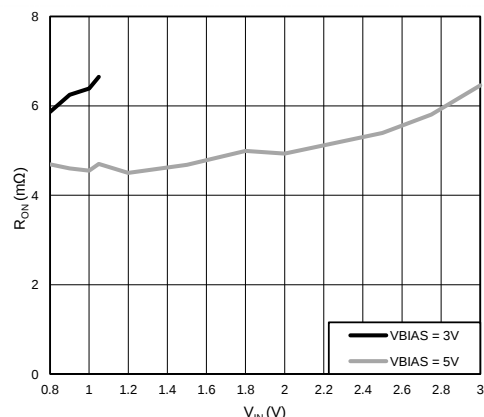
Figure 7. R_{ON} vs V_{IN}

Typical Characteristics (continued)



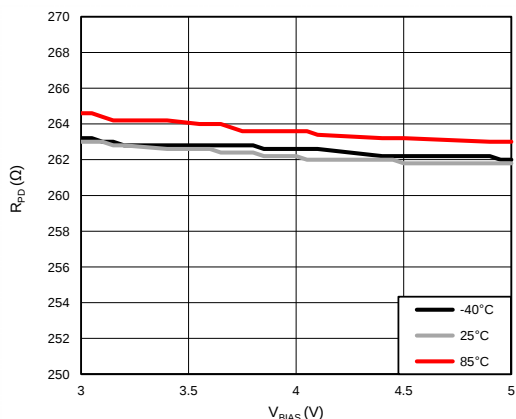
$V_{BIAS} = 5\text{ V}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = -200\text{ mA}$

Figure 8. R_{ON} vs V_{IN}



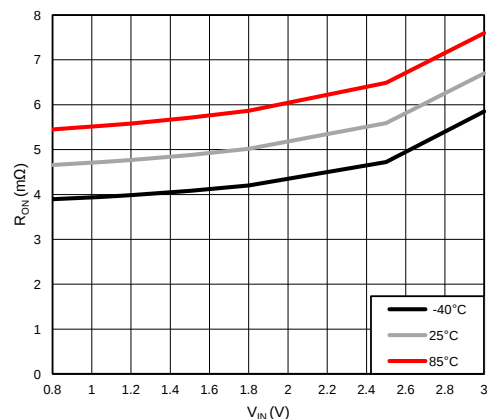
$T_A = 25^\circ\text{C}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = -200\text{ mA}$

Figure 9. R_{ON} vs V_{IN}



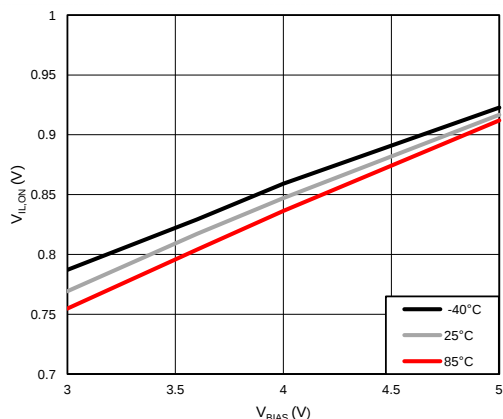
$V_{ON} = 0\text{ V}$ $V_{IN} = 1.05\text{ V}$ $V_{OUT} = 1\text{ V}$

Figure 10. R_{PD} vs V_{BIAS}



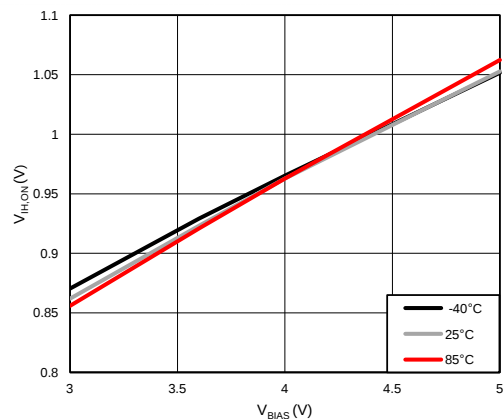
$V_{BIAS} = 5\text{ V}$ $V_{ON} = 5\text{ V}$ $I_{OUT} = -6\text{ A}$

Figure 11. R_{ON} vs V_{IN} at 6A load



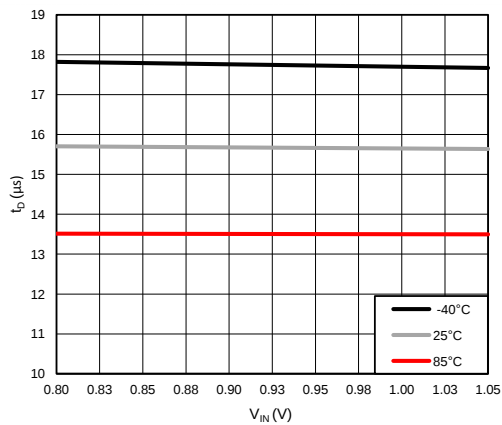
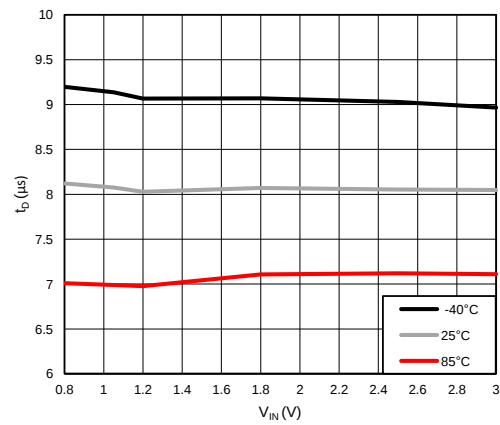
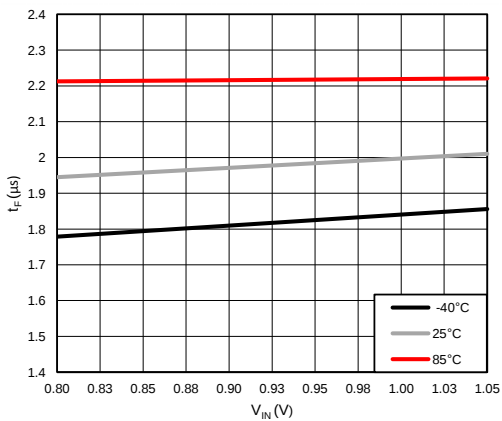
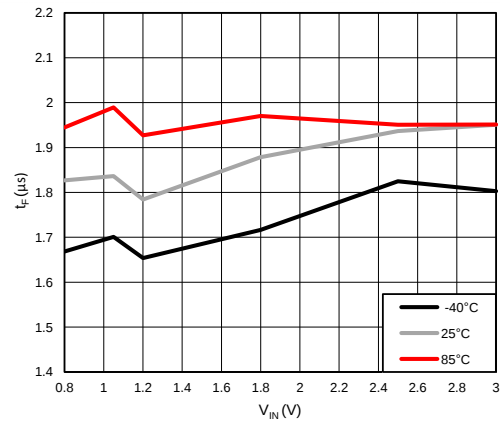
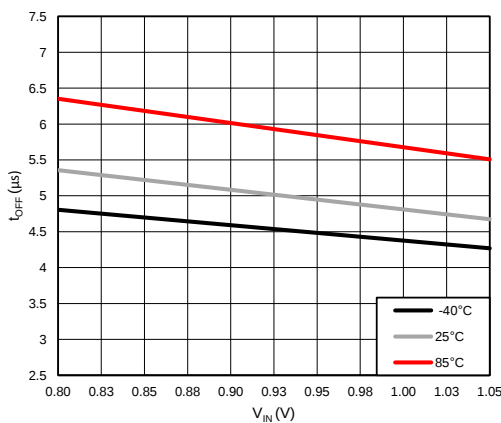
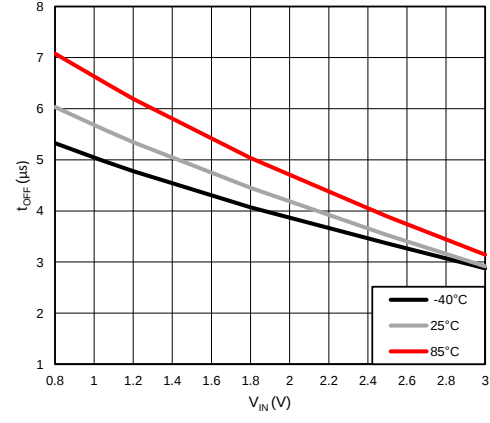
$V_{IN} = V_{BIAS} - 2\text{ V}$

Figure 12. $V_{IL,ON}$ vs V_{BIAS}

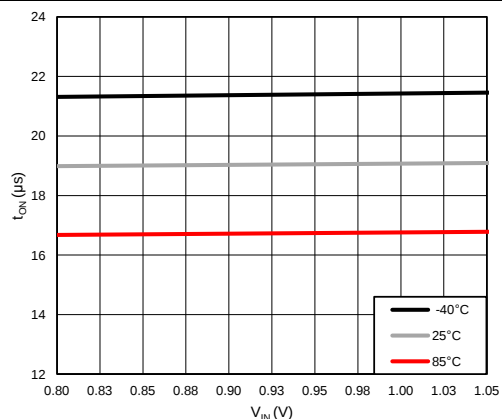


$V_{IN} = V_{BIAS} - 2\text{ V}$

Figure 13. $V_{IH,ON}$ vs V_{BIAS}

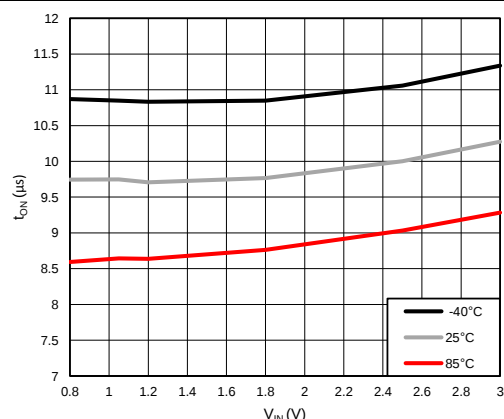
Typical Characteristics (continued)

 $V_{BIAS} = 3\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$
Figure 14. t_D vs V_{IN}

 $V_{BIAS} = 5\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$
Figure 15. t_D vs V_{IN}

 $V_{BIAS} = 3\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$
Figure 16. t_F vs V_{IN}

 $V_{BIAS} = 5\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$
Figure 17. t_F vs V_{IN}

 $V_{BIAS} = 3\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$
Figure 18. t_{OFF} vs V_{IN}

 $V_{BIAS} = 5\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$
Figure 19. t_{OFF} vs V_{IN}

Typical Characteristics (continued)



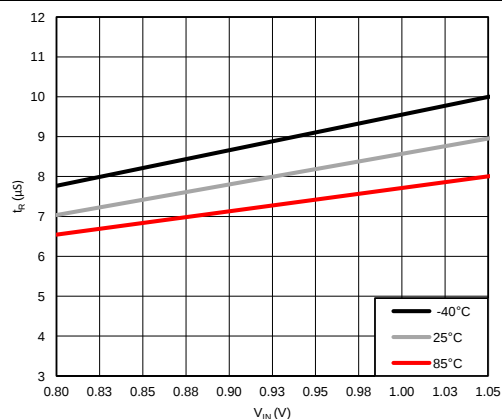
$V_{BIAS} = 3\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$

Figure 20. t_{ON} vs V_{IN}



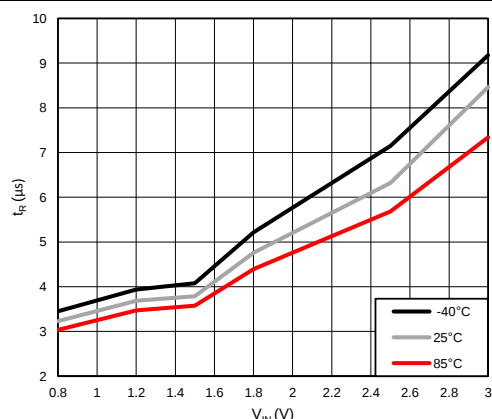
$V_{BIAS} = 5\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$

Figure 21. t_{ON} vs V_{IN}



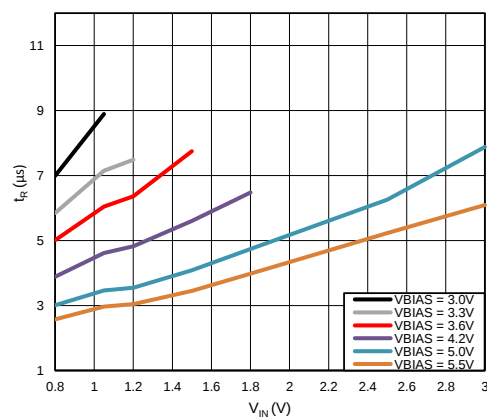
$V_{BIAS} = 3\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$

Figure 22. t_R vs V_{IN}



$V_{BIAS} = 5\text{ V}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$

Figure 23. t_R vs V_{IN}



$T_A = 25^\circ\text{C}$ $R_L = 10\ \Omega$ $C_L = 0.1\ \mu\text{F}$

Figure 24. t_R vs V_{IN} for Various V_{BIAS}

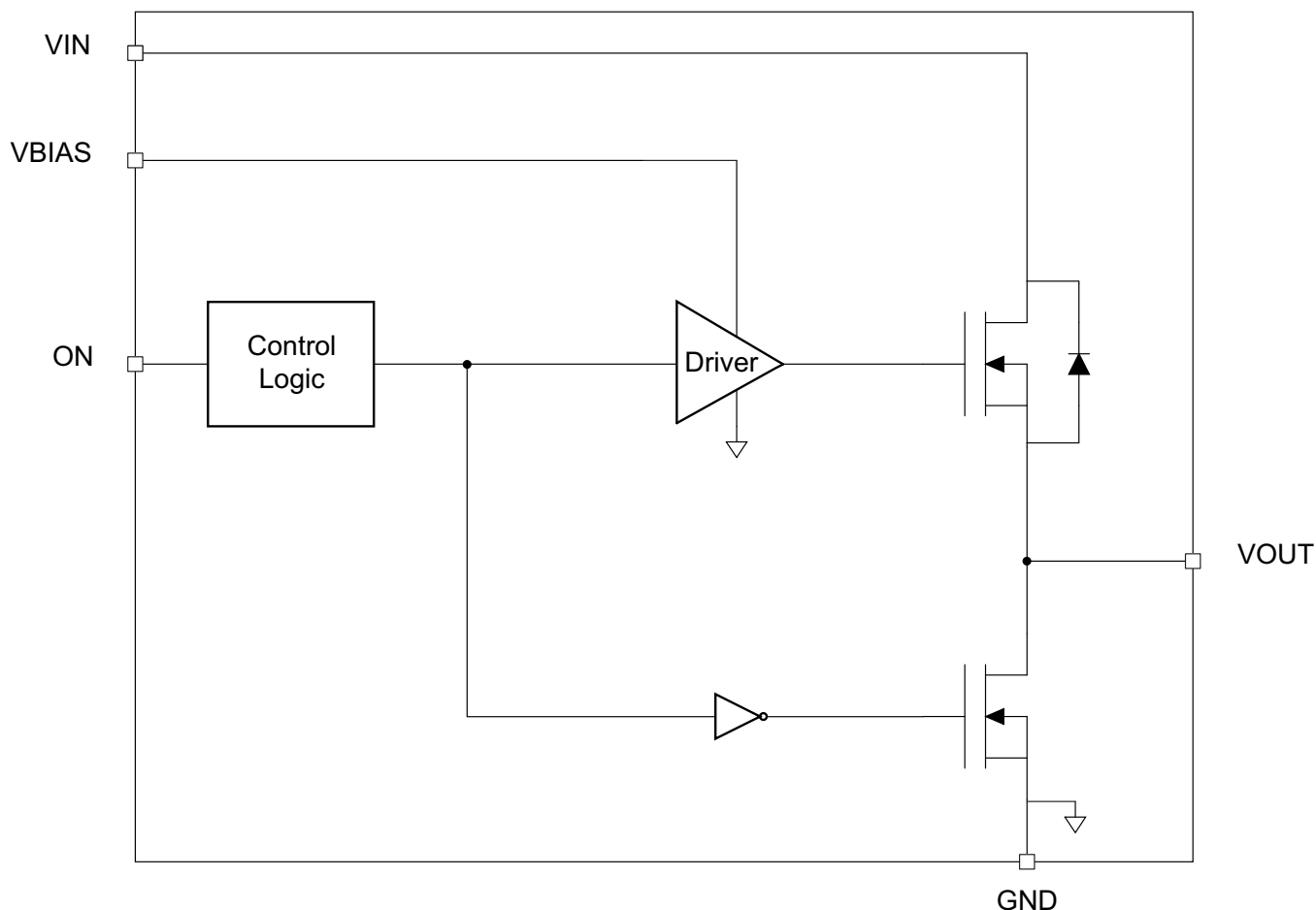
8 Detailed Description

8.1 Overview

The device is a 3.5 V, 6 A load switch in a 8-terminal SON package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device at very high currents.

The device has a controlled, yet quick, fixed slew rate for applications that require quick turn-on response. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On/off Control

The ON terminal controls the state of the load switch, and asserting the terminal high (active high) enables the switch. The ON terminal is compatible with standard GPIO logic threshold and can be used with any microcontroller or discrete logic with 1.2 V or higher GPIO voltage. This terminal cannot be left floating and must be tied either high or low for proper functionality.

8.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1 μ F ceramic capacitor, C_{IN} , placed close to the terminals, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor 10 times higher than the output capacitor to avoid excessive voltage drop.

8.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents.

8.3.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq (V_{BIAS} - 1.95 \text{ V})$. For example, in order to have $V_{IN} = 3.5 \text{ V}$, V_{BIAS} must be 5.5 V. The device will still be functional if $V_{IN} > (V_{BIAS} - 1.95 \text{ V})$ but it will exhibit R_{ON} greater than what is listed in the [Electrical Characteristics, \$V_{BIAS} = 5.0 \text{ V}\$](#) table. See [Figure 25](#) for an example of a typical device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS} .

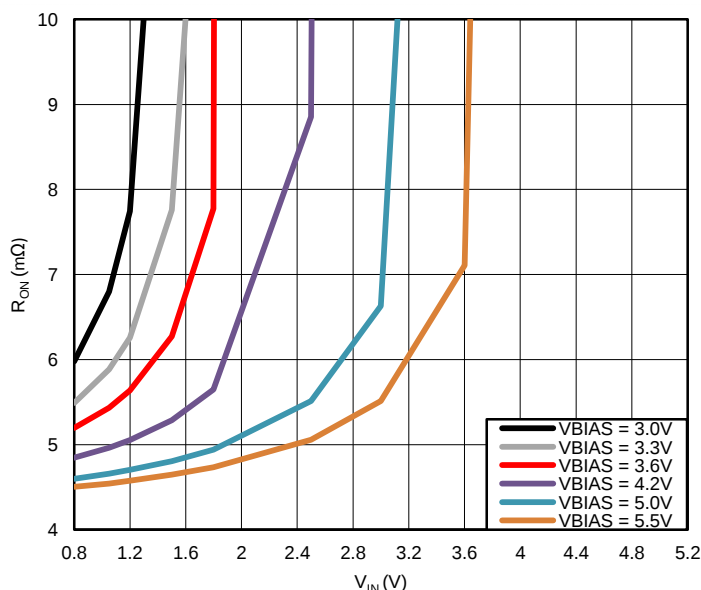


Figure 25. R_{ON} vs V_{IN} ($V_{IN} > V_{BIAS}$)

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

9.2 Typical Application

9.2.1 Typical Application Powering a Downstream Module

This application demonstrates how the TPS22961 can be used to power downstream modules.

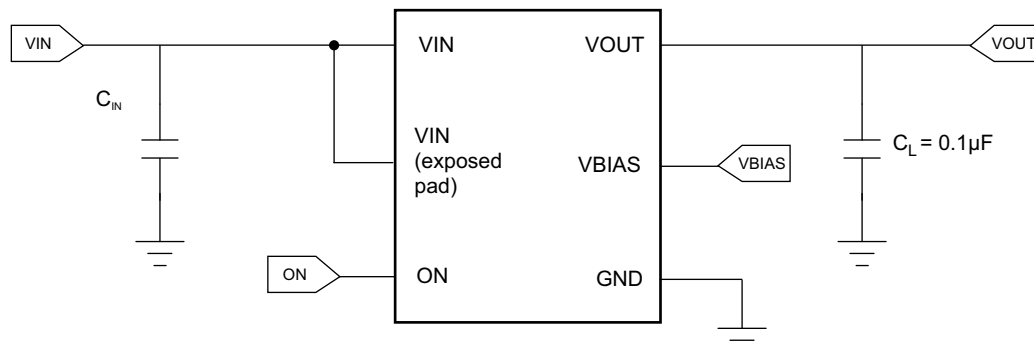


Figure 26. Typical Application Schematic for Powering a Downstream Module

9.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V _{IN}	1.05 V
V _{BIAS}	5.0 V
Load current	6 A

9.2.1.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current

9.2.1.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use [Equation 1](#) to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.2.1.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use [Equation 2](#):

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (2)$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

9.2.1.2.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use [Equation 3](#).

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (3)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22961)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See [Thermal Information](#) section. This parameter is highly dependent upon board layout.

9.2.1.3 Application Curves

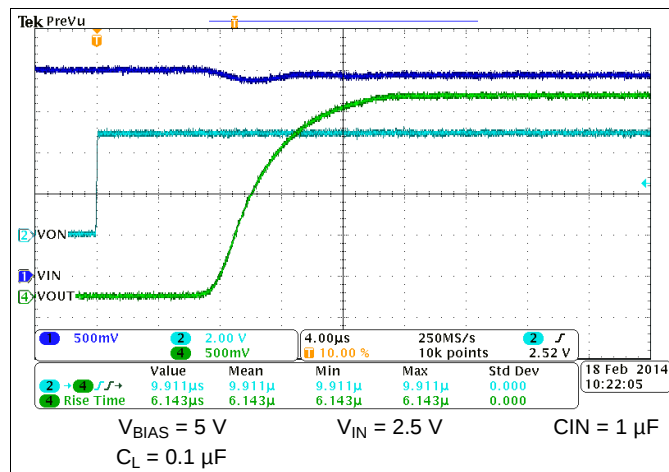


Figure 27. t_R at V_{BIAS} = 5 V

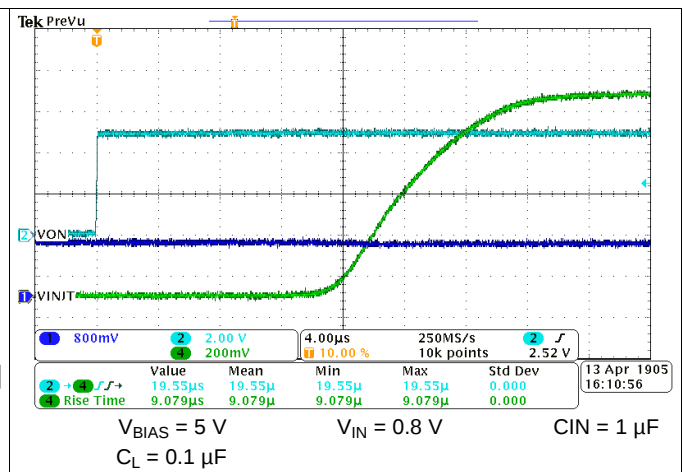


Figure 28. t_R at V_{BIAS} = 5 V

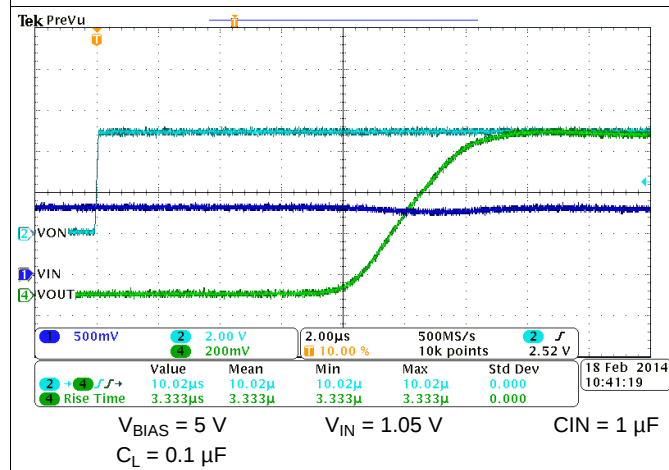


Figure 29. t_R at V_{BIAS} = 3 V

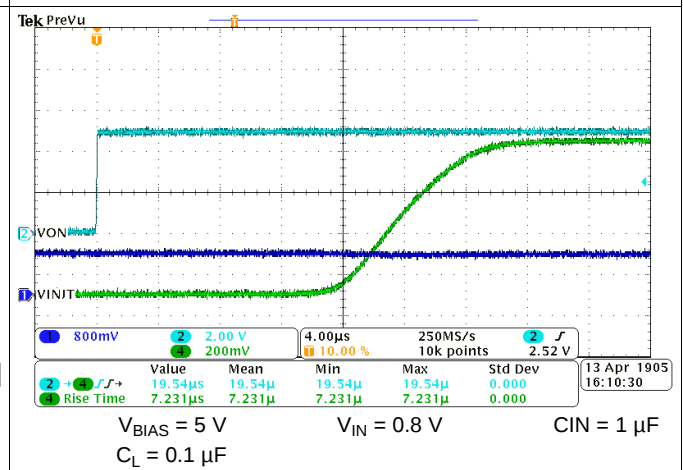


Figure 30. t_R at V_{BIAS} = 3 V

9.2.2 Typical Application Powering Rails Sensitive to Ringing and Overvoltage due to Fast Rise Time

This application demonstrates how the TPS22961 can be used to power rails sensitive to ringing and overvoltage that can often happen due to fast rise times.

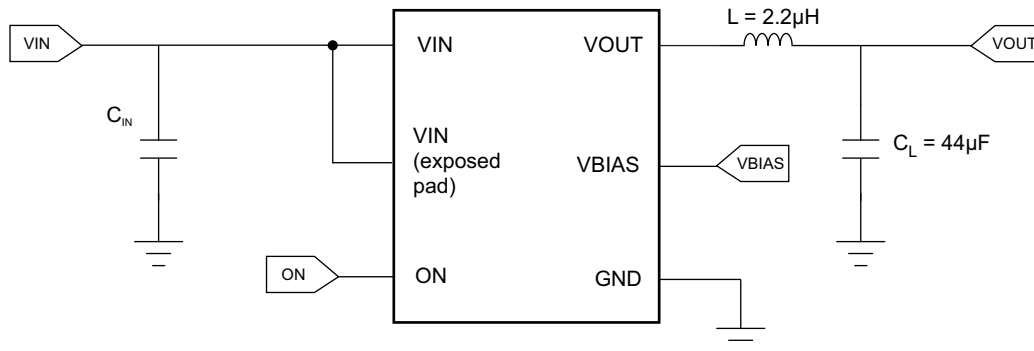


Figure 31. Typical Application Schematic for Powering Rails Sensitive to Ringing

9.2.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05 V
V_{BIAS}	5.0 V
Acceptable percent overshoot (ρ)	3.2%
Maximum settling time (t_{SETTLE})	40 μ s

9.2.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Acceptable percent overshoot
- Maximum allowed settling time for the power rail

9.2.2.2.1 Picking Proper Inductor and Capacitor to Meet Voltage Overshoot Requirements

To determine the value of L and C_L in the circuit, the damping factor associated with the acceptable percent overshoot must be calculated. To calculate the damping factor (ε), use [Equation 4](#).

$$\varepsilon = \frac{-\ln \rho}{\sqrt{\pi^2 + (\ln \rho)^2}} \quad (4)$$

where

- ε = damping factor of the LC filter
- ρ = allowable percent overshoot for the power rail

Use the damping factor calculated in Equation 4 to determine the inductance (L), the DCR of the inductor (R_{DCR}), and capacitance (C_L) to achieve the percent overshoot. This will be an iterative process to determine the optimal combination of L and C_L with standard value components available. Use Equation 5 to determine the combination of L, R_{DCR} , and C_L that is needed to satisfy damping factor calculated from Equation 4.

$$\varepsilon = \frac{R_{DCR}}{2} \times \sqrt{\frac{C_L}{L}} \quad (5)$$

where

- ε = damping factor of the LC filter
- R_{DCR} = DCR of the inductor
- C_L = the capacitance of the filter
- L = the inductor of the filter

To determine the setting time (within 5% of steady state value) of the filter, use Equation 6.

$$t_{SETTLE} \approx \frac{3 \times \sqrt{L \times C_L}}{\varepsilon} \quad (6)$$

where

- t_{SETTLE} = settling time of filter to within 5% of steady state value
- ε = damping factor of the LC filter
- C_L = the capacitance of the filter
- L = the inductor of the filter

The combination of damping factor (ε) and filter settling time (t_{SETTLE}) will bound the values for L, R_{DCR} , and C_L that can be used to meet the design constraints in Table 2.

9.2.2.3 Application Curves

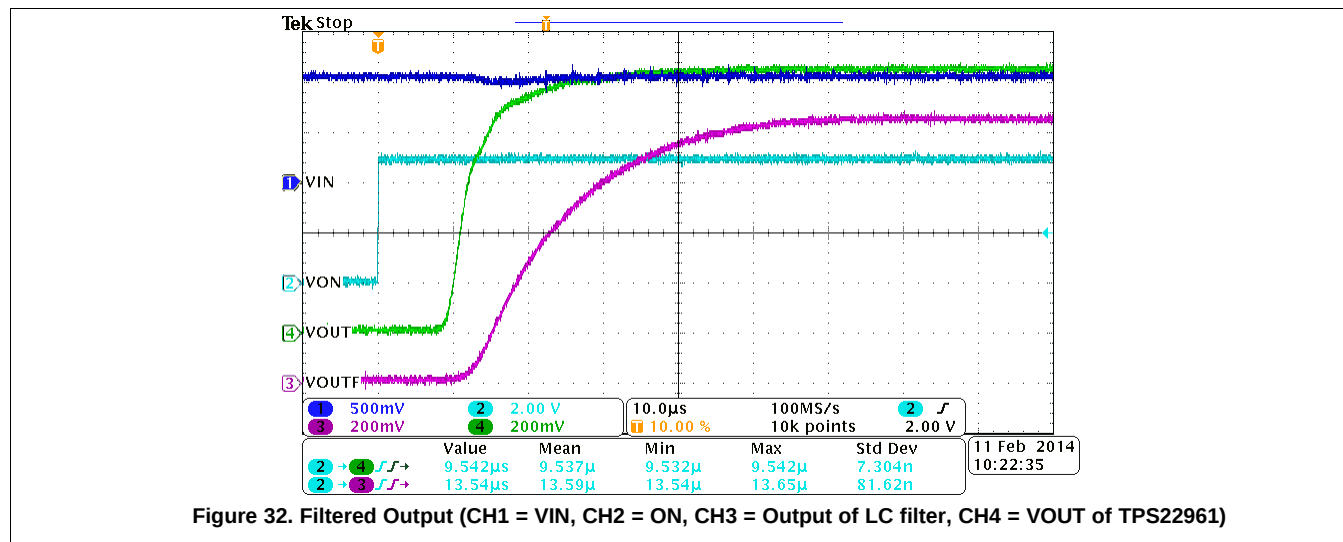


Figure 32. Filtered Output (CH1 = VIN, CH2 = ON, CH3 = Output of LC filter, CH4 = VOUT of TPS22961)

10 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 3 V to 5.5 V and VIN range of 0.8 V to 3.5 V. This supply must be well regulated and placed as close to the TPS22961 as possible. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic, tantalum, or ceramic capacitor of 10 μF may be sufficient.

11 Layout

11.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The VIN terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- μ F ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device terminals as possible.
- The VOUT terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device terminals as possible.
- The VBIAS terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1- μ F ceramic with X5R or X7R dielectric.

11.2 Layout Example

○ VIA to Power Ground Plane

⊃ VIA to VIN Plane

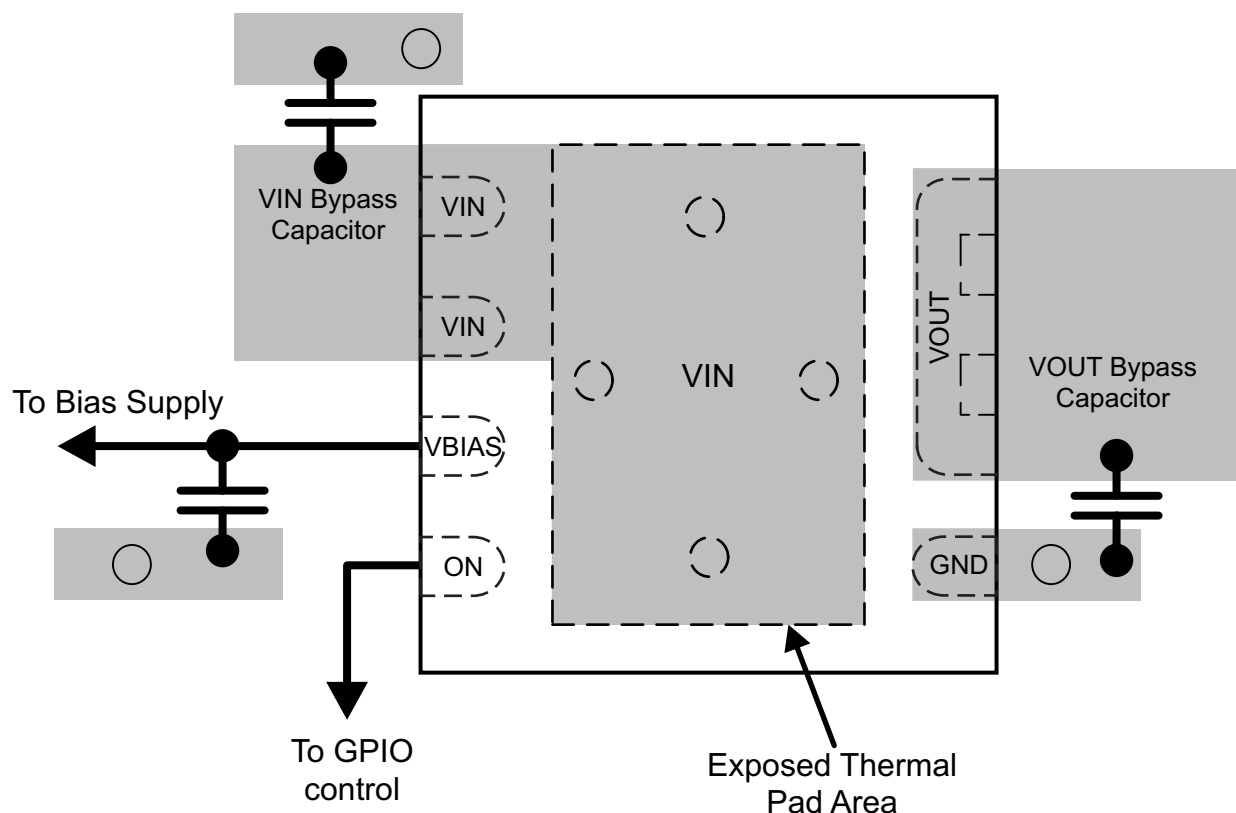


Figure 33. Recommended Board Layout

12 器件和文档支持

12.1 商标

Ultrabook is a trademark of Intel.

12.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22961DNYR	Active	Production	WSO (DNY) 8	3000 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 85	961A1
TPS22961DNYR.B	Active	Production	WSO (DNY) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	
TPS22961DNYT	Active	Production	WSO (DNY) 8	250 SMALL T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 85	961A1
TPS22961DNYT.B	Active	Production	WSO (DNY) 8	250 SMALL T&R	-	Call TI	Call TI	-40 to 85	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

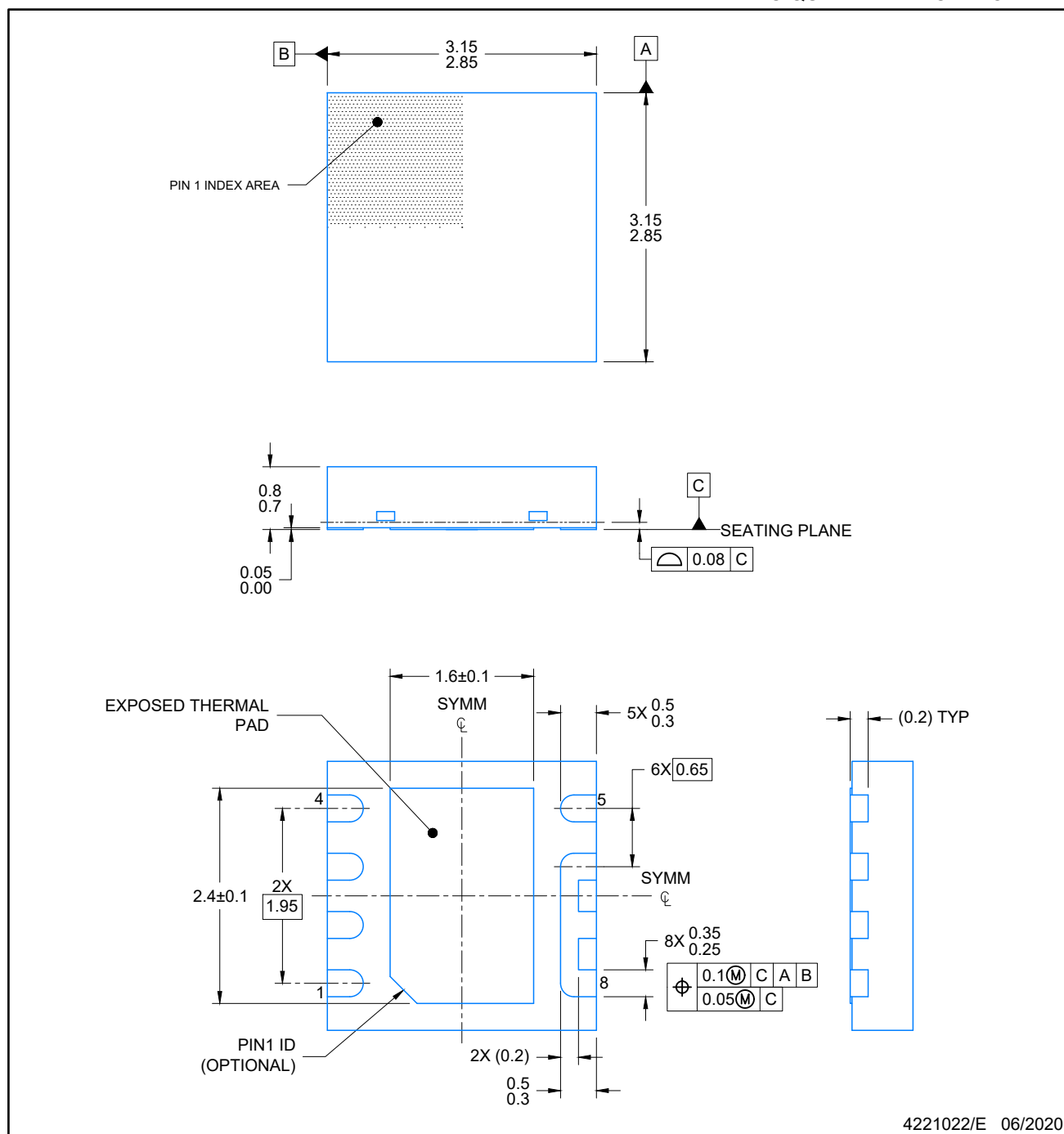
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PACKAGE OUTLINE

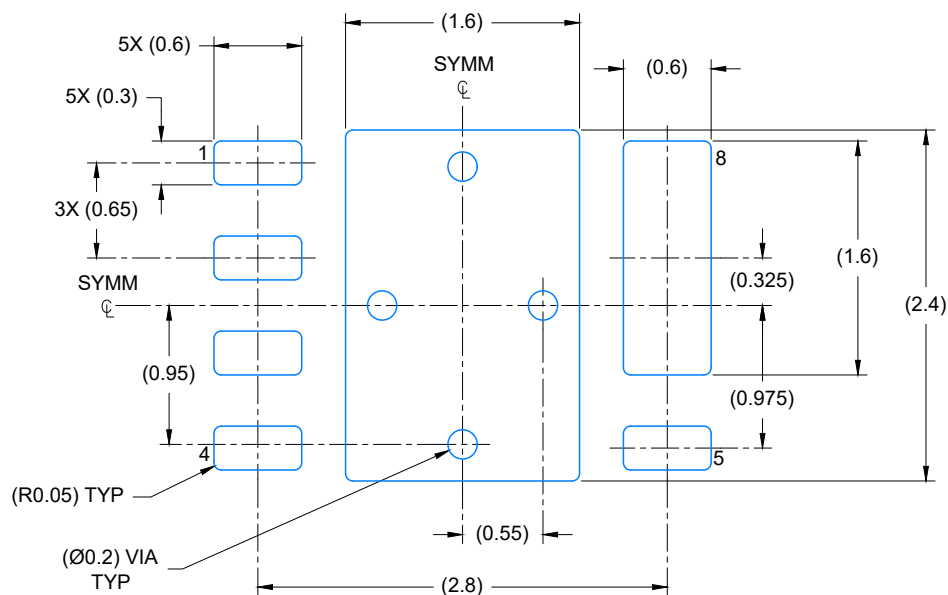
WSN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

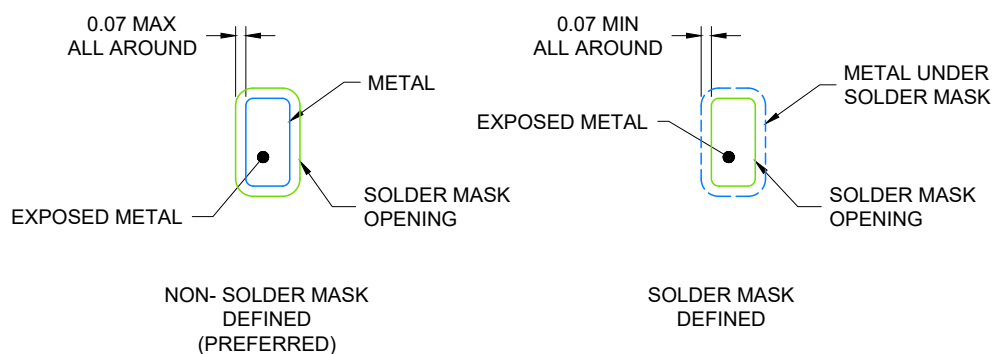


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

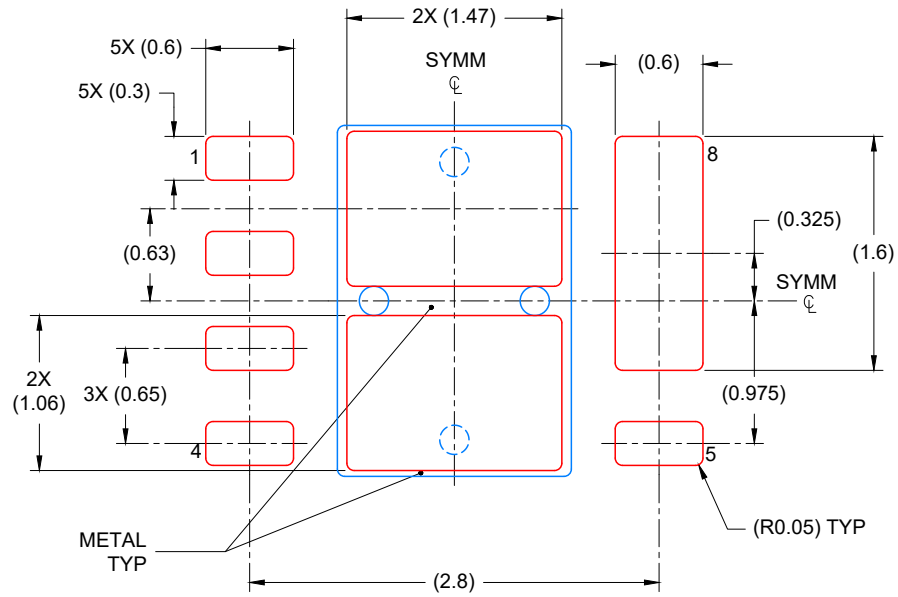


SOLDER MASK DETAILS

4221022/E 06/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 81% PRINTED COVERAGE BY AREA
 SCALE: 20X

4221022/E 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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