24位模数转换器

查询样品: **ADS1243-HT**

特性

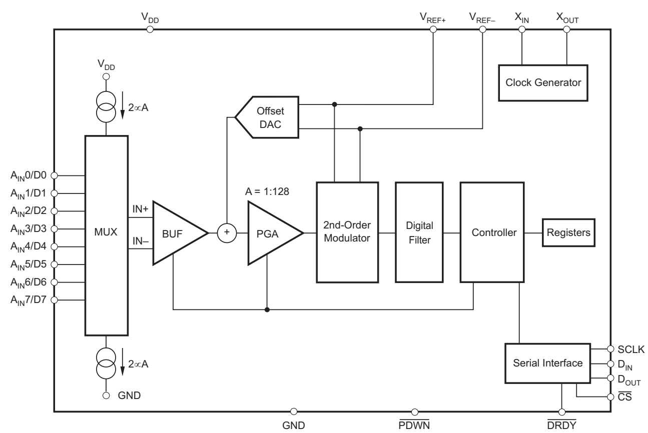
- **24**位无丢码
- 同步**50Hz**和**60Hz**抑制
（最小**–90 dB**）
- **0.0025%** 积分非线性**(INL)**
- 可编程增益放大器**(PGA)**增益从**1**到**128**
- 单循环建立
- 可编程数据输出速率
- **0.1V**至**0.5V**外部差分基准
- 片载校准
- 与**SPI™**兼容
- **2.7V**至**5.25V**电源范围
- **600μW**功率耗散
- 最多**8**个输入通道
- 最多**8**个数据**I/O**

应用范围

- 潜孔打钻
- 高温环境
- 振动**/**模式分析
- 多通道数据采集
- 声学**/**动态应变仪
- 压力传感器

支持极端温度环境下的应用

- 受控基线
- 一个组装**/**测试场所
- 一个制造场所
- 可在极端温度范围 **(–55°C/210°C)** 下工作(1)
- 延长的产品使用寿命周期
- 延长产品的变更通知周期
- 产品可追溯性
- 德州仪器的高温产品
使用高度优化的硅（芯片）解决方案，
此方案提升设计和制造工艺
以大大提高拓展温度范围内的性能
。 所有器件可在最大额定温度下连续运行**1000**小时。



(1) 可定制温度范围

说明

ADS1243是一款高精度，宽动态范围，Δ-Σ，模数(A/D)转换器，此转换器的运行电压为2.7V至5.25V并具有24位分辨率。 此Δ-Σ，A/D转换器能提供最高24位的无丢码性能并且其有效分辨率为21位。

此输入通道是复用的。 可选择内部缓冲来为到变频器的直接连接或者低水平电压信号提供一个非常高的输入阻抗。 提供的熔断电流可用于检测开式或者短接传感器。 一个8位模数转换器(DAC)提供一个FSR（满刻度范围）50%的偏差校正。

此可编程增益放大器(PGA)提供1到128间的可选增益（128增益时的有效分辨率为19位）。 A/D转换由一个二级Δ-Σ调制器和一个可提供同步50Hz和60Hz陷波的可编程有限脉冲响应(FIR)滤波器来完成的。 此基准输入是差分的并可被用于比例转换。

English Data Sheet: SBAS525

此串口与串行外设接口(SPI)兼容。 提供最多8位数据I/O用于输入或者输出。 ADS1243设计用于智能发送器，工业过程控制，称量台，套色版和便携式仪器中的高分辨率测量应用。

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	JD	ADS1243SJD	ADS1243SJD
	KGD	ADS1243SKGD1	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE	UNIT
V_{DD} to GND	–0.3 to 6	V
Input Current	100, Momentary	mA
Input Current	10, Continuous	mA
A_{IN}	GND – 0.5 to V_{DD} + 0.5	V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3	V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3	V
Maximum Junction Temperature	215	°C
Operating Temperature Range	–55 to 210	°C
Storage Temperature Range	–65 to 100	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	HKJ package			8.1	°C/W

DIGITAL CHARACTERISTICS

V_{DD} 2.7 V to 5.25 V

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input/Output									
Logic Family				CMOS			CMOS		
Logic Level	V_{IH}		0.8 • VDD		V_{DD}	0.8 • VDD		V_{DD}	V
	V_{IL} (1)		GND		0.2 • VDD	GND		0.2 • VDD	V
	V_{OH}	I_{OH} = 1 mA	V_{DD} – 0.4			V_{DD} – 0.4			V
	V_{OL}	I_{OL} = 1 mA	GND		GND + 0.4	GND		GND + 0.4	V
Input Leakage	I_{IH}	V_I = V_{DD}			10			10	µA
	I_{IL}	V_I = 0	–10			–10			µA
Master Clock Rate: f_{OSC}			1		5	1		5	MHz
Master Clock Period: t_{OSC}		1/f_{OSC}	200		1000	200		1000	ns

(1) V_{IL} for X_{IN} is GND to GND + 0.05 V.

ELECTRICAL CHARACTERISTICS: V_{DD} = 5 V

All specifications V_{DD} = 5 V, f_{MOD} = 19.2 kHz, PGA = 1, Buffer ON, f_{DATA} = 15 Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = 2.5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT (A_{IN}0 – A_{IN}7)								
Analog Input Range	Buffer OFF	GND – 0.1		V_{DD} + 0.1	GND – 0.1		V_{DD} + 0.1	V
	Buffer ON	GND + 0.05		V_{DD} – 1.5	GND + 0.05		V_{DD} – 1.5	V
Full-Scale Input Range	(In+) – (In–), See Block Diagram, RANGE = 0			±V_{REF}/PGA			±V_{REF}/PGA	V
	RANGE = 1			±V_{REF}/ (2 ● PGA)			±V_{REF}/ (2 ● PGA)	V
Differential Input Impedance	Buffer OFF		5/PGA			12/PGA		MΩ
	Buffer ON		5			8		GΩ
Bandwidth, f_{DATA} = 3.75 Hz	–3 dB		1.65					Hz
Bandwidth, f_{DATA} = 7.50 Hz	–3 dB		3.44					Hz
Bandwidth, f_{DATA} = 15 Hz	–3 dB		14.6					Hz
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	1		128	
Input Capacitance			9			25		pF
Input Leakage Current	Modulator OFF, T = 25°C		5			6		pA
Burnout Current Sources			2					μA
OFFSET DAC								
Offset DAC Range	RANGE = 0		±V_{REF} / (2 ● PGA)			±V_{REF} / (2 ● PGA)		V
	RANGE = 1		±V_{REF} / (4 ● PGA)			±V_{REF} / (4 ● PGA)		V
Offset DAC Monotonicity		8			8			Bits
Offset DAC Gain Error			±10			±15		%
Offset DAC Gain Error Drift			1			2.2		ppm/°C
SYSTEM PERFORMANCE								
Resolution	No Missing Codes	24			24			Bits
Integral Nonlinearity	End Point Fit			±0.0015			±0.0018	% of FS
Offset Error (1)			7.5			15		ppm of FS
Offset Drift (1)			0.02			0.04		ppm of FS/°C
Gain Error (1)			0.005			0.100		%
Gain Error Drift (1)			0.5			1.118		ppm°°C
Common-Mode Rejection	at DC	100			94			dB
	f_{CM} = 60 Hz, f_{DATA} = 15 Hz		130			100		dB
	f_{CM} = 50 Hz, f_{DATA} = 15 Hz		120			100		dB
Normal-Mode Rejection	f_{SIG} = 50 Hz, f_{DATA} = 15 Hz		100			95		dB
	f_{SIG} = 60 Hz, f_{DATA} = 15 Hz		100			95		dB
Output Noise		See Typical Characteristics						
Power-Supply Rejection	at DC, dB = –20 log(ΔV_{OUT} /V_{DD}) (2)	80	95		79	95		dB
VOLTAGE REFERENCE INPUT								
Reference Input Range	REF IN+, REF IN–	0		V_{DD}	0		V_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–), RANGE = 0	0.1	2.5	2.6	0.1	2.5	2.6	V
	RANGE = 1	0.1		V_{DD}	0.1		V_{DD}	V
Common-Mode Rejection	at DC		120			98		dB
Common-Mode Rejection	f_{VREFCM} = 60 Hz, f_{DATA} = 15 Hz		120			95		dB

(1) Calibration can minimize these errors.
(2) ΔV_{OUT} is a change in digital result.

ELECTRICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

All specifications V_{DD} = 5 V, f_{MOD} = 19.2 kHz, PGA = 1, Buffer ON, f_{DATA} = 15 Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = 2.5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Bias Current[3]	V_{REF} = 2.5 V		1.3			10		µA
POWER-SUPPLY REQUIREMENTS								
Power-Supply Voltage	V_{DD}	4.75		5.25	4.75		5.25	V
Current	PGA = 1, Buffer OFF		240	375		250	480	µA
	PGA = 128, Buffer OFF		450	800		630	940	µA
	PGA = 1, Buffer ON		290	425		350	585	µA
	PGA = 128, Buffer ON		960	1400		1200	2050	µA
	SLEEP Mode		60			80		µA
	Read Data Continuous Mode		230			350		µA
	$\overline{\text{PDWN}}$		0.5			10		nA
Power Dissipation	PGA = 1, Buffer OFF		1.2	1.9		1.3	2.52	mW

(3) 12-pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: V_{DD} = 3 V

All specifications V_{DD} = 3 V, f_{MOD} = 19.2 kHz, PGA = 1, Buffer ON, f_{DATA} = 15 Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = 1.25 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$)									
Analog Input Range		Buffer OFF	GND – 0.1		V_{DD} + 0.1	GND – 0.1		V_{DD} + 0.1	V
		Buffer ON	GND + 0.05		V_{DD} – 1.5	GND + 0.05		V_{DD} – 1.5	V
Full-Scale Input Voltage Range		(In+) – (In–), See Block Diagram, RANGE = 0			$\pm V_{REF}$/PGA			$\pm V_{REF}$/PGA	V
		RANGE = 1			$\pm V_{REF}$/(2 • PGA)			$\pm V_{REF}$/(2 • PGA)	V
Input Impedance		Buffer OFF		5/PGA			10/PGA		MΩ
		Buffer ON		5			8		GΩ
Bandwidth	f_{DATA} = 3.75 Hz	–3 dB		1.65					Hz
	f_{DATA} = 7.50 Hz	–3 dB		3.44					Hz
	f_{DATA} = 15 Hz	–3 dB		14.6					Hz
Programmable Gain Amplifier		User-Selectable Gain Ranges	1		128	1		128	
Input Capacitance				9			25		pF
Input Leakage Current		Modulator OFF, T = 25°C		5			6		pA
Burnout Current Sources				2					µA
OFFSET DAC									
Offset DAC Range		RANGE = 0		$\pm V_{REF}$/(2 ● PGA)			$\pm V_{REF}$/(2 ● PGA)		V
		RANGE = 1		$\pm V_{REF}$/(4 ● PGA)			$\pm V_{REF}$/(4 ● PGA)		V
Offset DAC Monotonicity			8			8			Bits
Offset DAC Gain Error				±10			±12		%
Offset DAC Gain Error Drift				1			2		ppm/°C
SYSTEM PERFORMANCE									
Resolution		No Missing Codes	24			24			Bits
Integral Nonlinearity		End Point Fit			±0.0015			±0.0025	% of FS
Offset Error[1]				75			40		ppm of FS

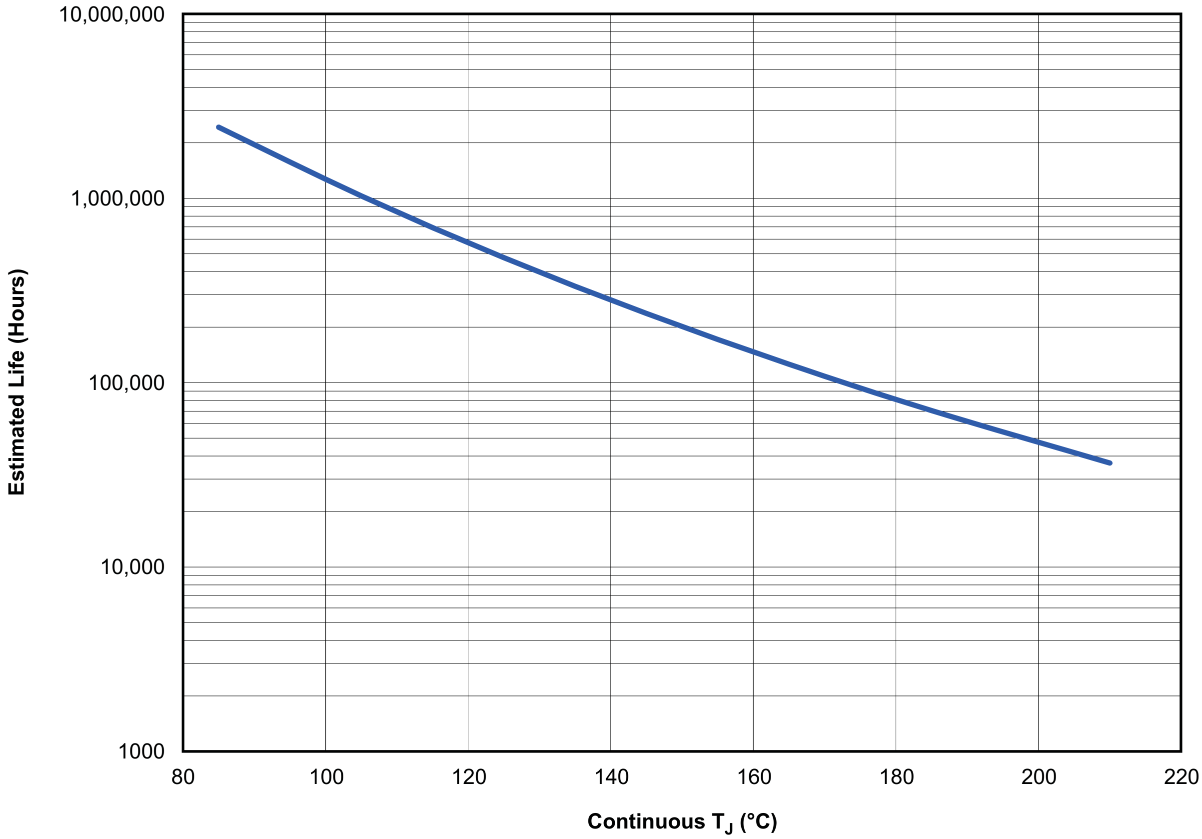
(1) Calibration can minimize these errors.

ELECTRICAL CHARACTERISTICS: V_{DD} = 3 V (continued)

All specifications V_{DD} = 3 V, f_{MOD} = 19.2 kHz, PGA = 1, Buffer ON, f_{DATA} = 15 Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = 1.25 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Offset Drift(1)			0.02			0.20		ppm of FS/°C
Gain Error(1)			0.005			0.1		%
Gain Error Drift(1)			0.5			1.118		ppm/°C
Common-Mode Rejection	at DC	100			87			dB
	f_{CM} = 60 Hz, f_{DATA} = 15 Hz		130			98		dB
	f_{CM} = 50 Hz, f_{DATA} = 15 Hz		120			95		dB
Normal-Mode Rejection	f_{SIG} = 50 Hz, f_{DATA} = 15 Hz		100			90		dB
	f_{SIG} = 60 Hz, f_{DATA} = 15 Hz		100			90		dB
Output Noise			See Typical Characteristics					
Power-Supply Rejection	at DC, dB = –20 log(ΔV_{OUT} /V_{DD})(2)	80	95		75	90		dB
VOLTAGE REFERENCE INPUT								
Reference Input Range	REF IN+, REF IN–	0		V_{DD}	0		V_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–), RANGE = 0	0.1	1.25	1.30	0.1	1.25	1.30	V
	RANGE = 1	0.1		V_{DD}	0.1		2.6	V
Common-Mode Rejection	at DC		120			95		dB
Common-Mode Rejection	f_{VREFCM} = 60 Hz, f_{DATA} = 15 Hz		120			93		dB
Bias Current(3)	V_{REF} = 1.25 V		1.3			8		µA
POWER-SUPPLY REQUIREMENTS								
Power-Supply Voltage	V_{DD}	2.7		3.3	2.7		3.3	V
Current	PGA = 1, Buffer OFF		190	375		200	480	µA
	PGA = 128, Buffer OFF		460	700		600	940	µA
	PGA = 1, Buffer ON		240	375		350	585	µA
	PGA = 128, Buffer ON		870	1325		1200	1800	µA
	SLEEP Mode		75			110		µA
	Read Data Continuous Mode		113			250		µA
	$\overline{PDWN}$ = 0		0.5			7.5		nA
Power Dissipation	PGA = 1, Buffer OFF		0.6	1.2		0.66	1.58	mW

(2) ΔV_{OUT} is a change in digital result.
(3) 12-pF switched capacitor at f_{SAMP} clock frequency.



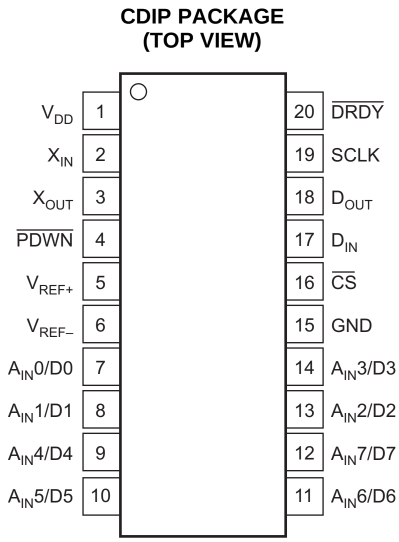
(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. ADS1243-HT Operating Life Derating Chart

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_{DD}	Power Supply
2	X_{IN}	Clock Input
3	X_{OUT}	Clock Output, used with crystal or ceramic resonator.
4	$\overline{PDWN}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
5	V_{REF+}	Positive Differential Reference Input
6	V_{REF-}	Negative Differential Reference Input
7	$A_{IN}0/D0$	Analog Input 0/Data I/O 0
8	$A_{IN}1/D1$	Analog Input 1/Data I/O 1
9	$A_{IN}4/D4$	Analog Input 4/Data I/O 4
10	$A_{IN}5/D5$	Analog Input 5/Data I/O 5
11	$A_{IN}6/D6$	Analog Input 6/Data I/O 6
12	$A_{IN}7/D7$	Analog Input 7/Data I/O 7
13	$A_{IN}2/D2$	Analog Input 2/Data I/O 2
14	$A_{IN}3/D3$	Analog Input 3/Data I/O 3
15	GND	Ground
16	$\overline{CS}$	Active LOW, Chip Select
17	D_{IN}	Serial Data Input, Schmitt Trigger
18	D_{OUT}	Serial Data Output
19	SCLK	Serial Clock, Schmitt Trigger
20	$\overline{DRDY}$	Active LOW, Data Ready

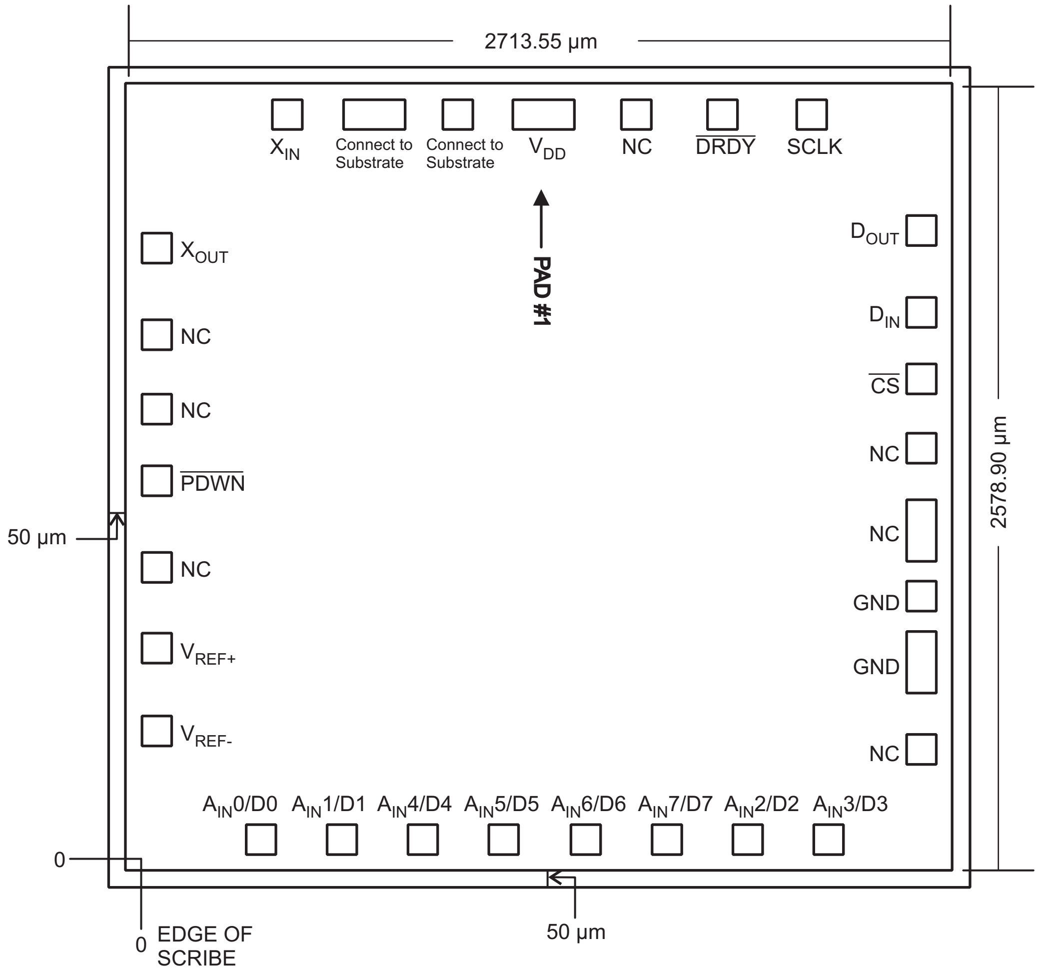
BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils	Silicon with backgrind	GND	AlCu

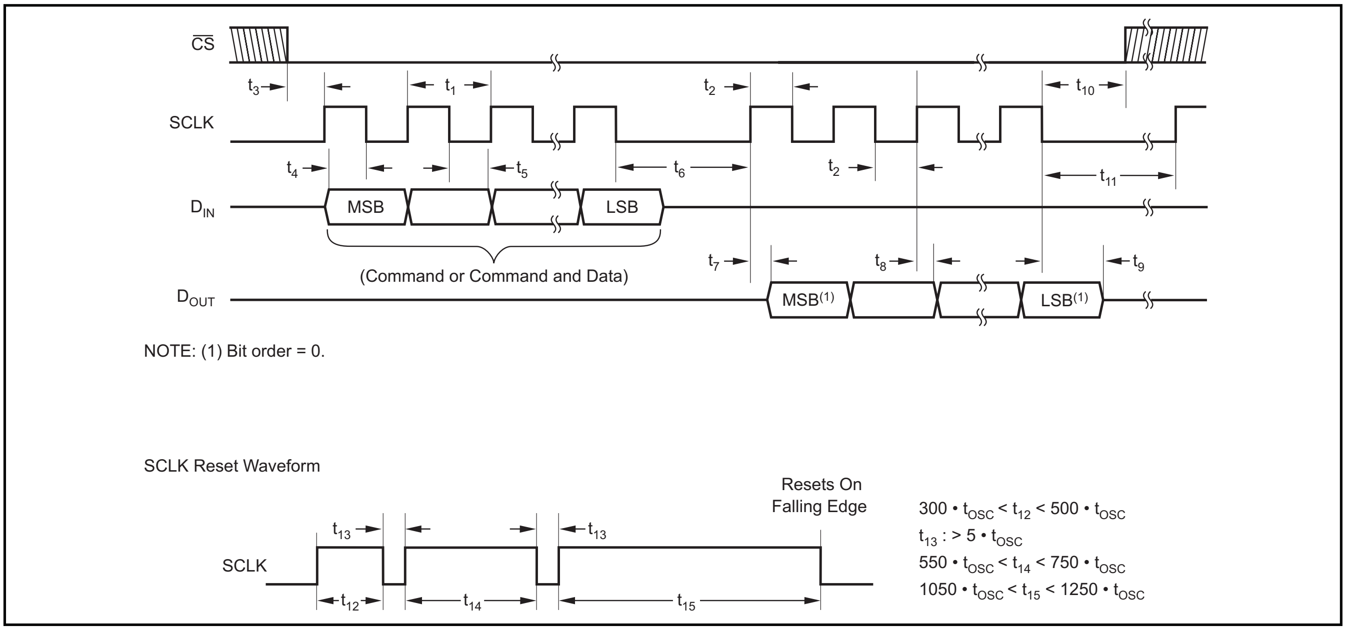
Table 1. Bond Pad Coordinates in Microns(1)

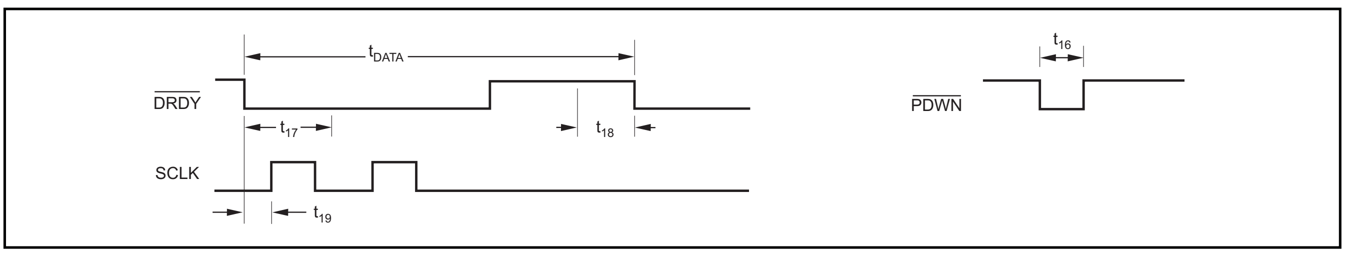
DISCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
V_{DD}	1	1268.55	2471.55	1478.15	2572.55
Connect to substrate	2	1030.45	2471.55	1132.45	2572.55
Connect to substrate	3	692.45	2471.55	902.05	2572.55
X_{IN}	4	450.05	2471.55	552.05	2572.55
X_{OUT}	5	6.45	2016.65	107.45	2118.65
NC	6	6.45	1721.75	107.45	1823.75
NC	7	6.45	1468.60	107.45	1570.60
$\overline{PDWN}$	8	6.45	1224.80	107.45	1326.80
NC	9	6.45	929.95	107.45	1031.95
V_{REF+}	10	6.45	655.20	107.45	757.20
V_{REF-}	11	6.45	373.25	107.45	475.25
$A_{IN}0/D0$	12	361.15	3.55	462.15	105.55
$A_{IN}1/D1$	13	636.45	3.55	737.45	105.55
$A_{IN}4/D4$	14	911.70	3.55	1012.70	105.55
$A_{IN}5/D5$	15	1186.85	3.55	1287.85	105.55
$A_{IN}6/D6$	16	1466.25	3.55	1567.25	105.55
$A_{IN}7/D7$	17	1742.50	3.55	1843.50	105.55
$A_{IN}2/D2$	18	2017.60	3.55	2118.60	105.55
$A_{IN}3/D3$	19	2292.75	3.55	2393.75	105.55
NC	20	2608.70	310.50	2709.70	412.50
GND	21	2608.75	553.25	2709.75	762.85
GND	22	2608.70	832.20	2709.70	934.20
NC	23	2608.75	1001.60	2709.75	1211.20
NC	24	2608.70	1335.65	2709.70	1437.65
$\overline{CS}$	25	2608.70	1571.45	2709.70	1673.45
D_{IN}	26	2608.70	1797.90	2709.70	1899.90
D_{OUT}	27	2608.70	2076.55	2709.70	2178.55
SCLK	28	2234.80	2471.55	2336.80	2572.55
$\overline{DRDY}$	29	1931.10	2471.55	2033.10	2572.55
NC	30	1637.90	2471.55	1739.90	2572.55

(1) For signal descriptions see the Pin Assignments table.


2713.55 µm
XIN
Connect to Substrate
Connect to Substrate
VDD
NC
DRDY
SCLK
PAD #1
XOUT
NC
NC
PDWN
NC
VREF+
VREF-
DOUT
DIN
CS
NC
NC
GND
GND
NC
2578.90 µm
50 µm
AIN0/D0
AIN1/D1
AIN4/D4
AIN5/D5
AIN6/D6
AIN7/D7
AIN2/D2
AIN3/D3
0
0
EDGE OF SCRIBE
50 µm

TIMING DIAGRAMS





TIMING REQUIREMENTS

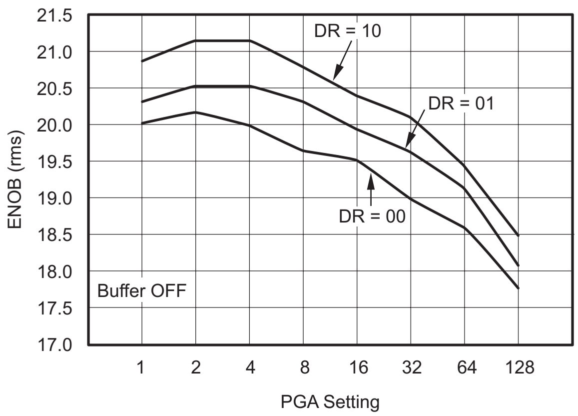
PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
t_1	SCLK Period		4		t_{OSC} Periods
				3	$\overline{DRDY}$ Periods
t_2	SCLK Pulse Width, HIGH and LOW		200		ns
t_3	$\overline{CS}$ low to first SCLK Edge; Setup Time(1)		0		ns
t_4	D_{IN} Valid to SCLK Edge; Setup Time		50		ns
t_5	Valid D_{IN} to SCLK Edge; Hold Time		50		ns
t_6	Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT}: RDATA, RDATAC, RREG, WREG		50		t_{OSC} Periods
t_7(2)	SCLK Edge to Valid New D_{OUT}			50	ns
t_8(2)	SCLK Edge to D_{OUT}, Hold Time		0		ns
t_9	Last SCLK Edge to D_{OUT} Tri-State NOTE: DOUT goes tri-state immediately when CS goes HIGH.		6	10	t_{OSC} Periods
t_{10}	$\overline{CS}$ LOW time after final SCLK edge.	Read from the device	0		t_{OSC} Periods
		Write to the device	8		t_{OSC} Periods
t_{11}	Final SCLK edge of one command until first edge SCLK of next command:	RREG, WREG, DSYNC, SLEEP, RDATA, RDATAC, STOPC	4		t_{OSC} Periods
		SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL	2		$\overline{DRDY}$ Periods
		SELFCAL	4		$\overline{DRDY}$ Periods
		RESET (also SCLK Reset)	16		t_{OSC} Periods
t_{16}	Pulse Width		4		t_{OSC} Periods
t_{17}	Allowed analog input change for next valid conversion.			5000	t_{OSC} Periods
t_{18}	DOR update, DOR data not valid.		4		t_{OSC} Periods
t_{19}	First SCLK after DRDY goes LOW:	RDATAC Mode	10		t_{OSC} Periods
		Any other mode	0		t_{OSC} Periods

(1) $\overline{CS}$ may be tied LOW.
(2) Load = 20 pF|| 10 kΩ to GND.

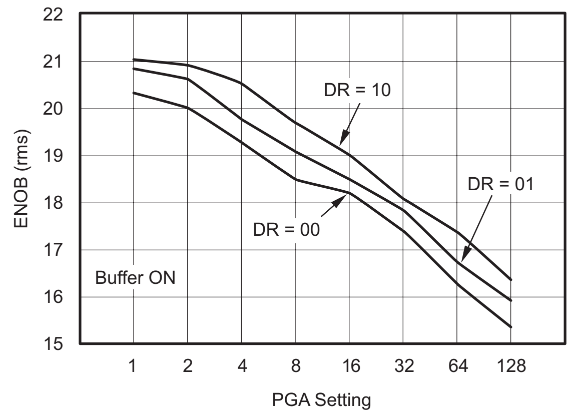
TYPICAL CHARACTERISTICS

All specifications V_{DD} = 5 V, f_{OSC} = 2.4576 MHz, PGA = 1, f_{DATA} = 15 Hz, and V_{REF} ≡ (REF IN+) – (REF IN–) = 2.5 V, unless otherwise specified.

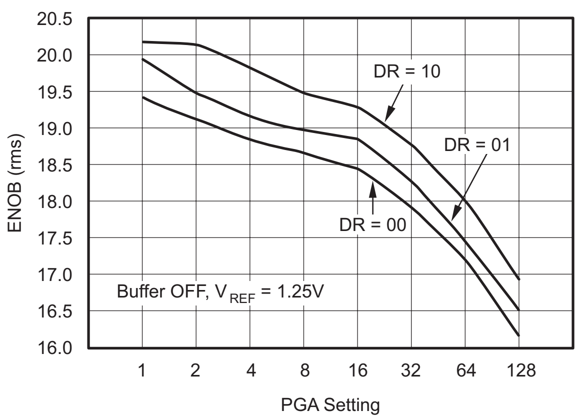
EFFECTIVE NUMBER OF BITS vs PGA SETTING



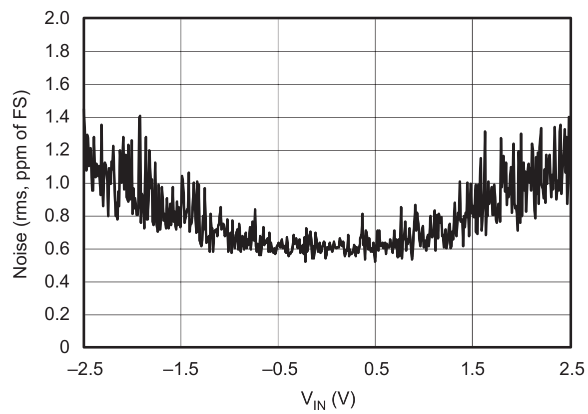
EFFECTIVE NUMBER OF BITS vs PGA SETTING



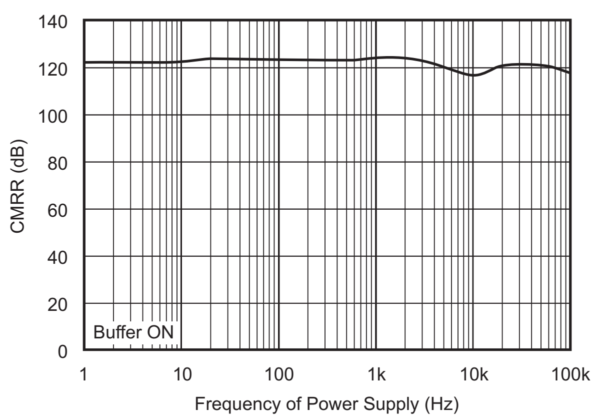
EFFECTIVE NUMBER OF BITS vs PGA SETTING



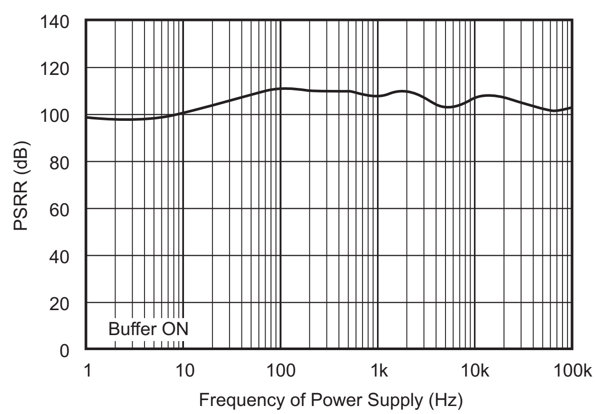
NOISE vs INPUT SIGNAL



COMMON-MODE REJECTION RATIO vs FREQUENCY



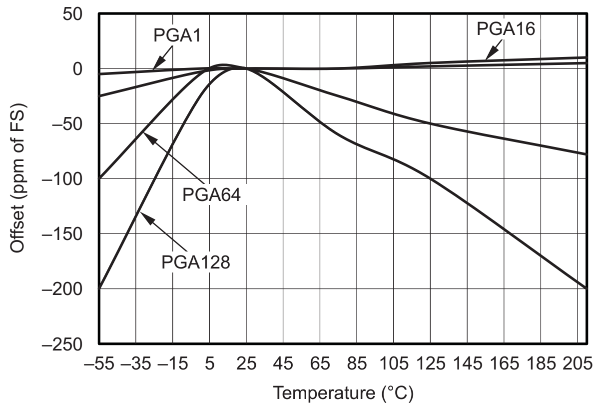
POWER SUPPLY REJECTION RATIO vs FREQUENCY



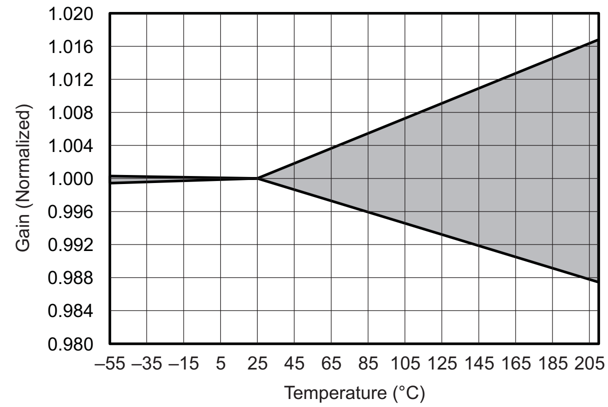
TYPICAL CHARACTERISTICS (continued)

All specifications V_{DD} = 5 V, f_{OSC} = 2.4576 MHz, PGA = 1, f_{DATA} = 15 Hz, and V_{REF} ≡ (REF IN+) – (REF IN–) = 2.5 V, unless otherwise specified.

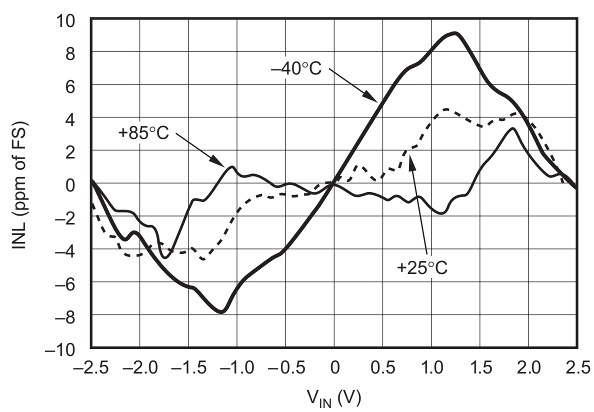
OFFSET vs TEMPERATURE (Cal AT 25°C)



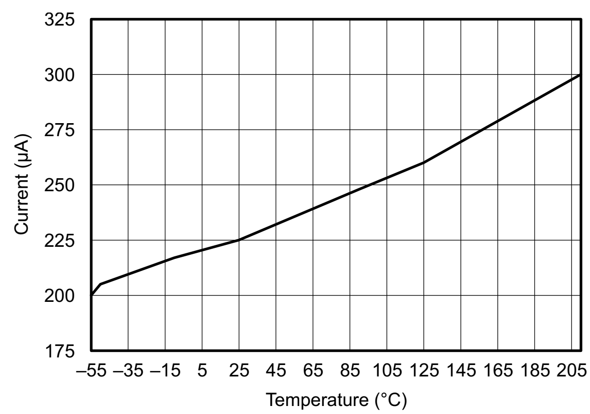
GAIN vs TEMPERATURE (Cal AT 25°C)



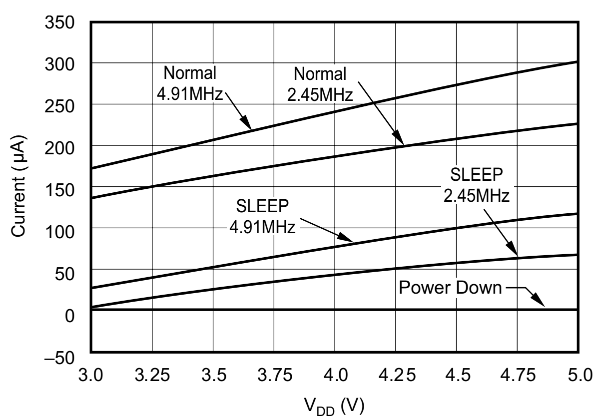
INTEGRAL NONLINEARITY vs INPUT SIGNAL



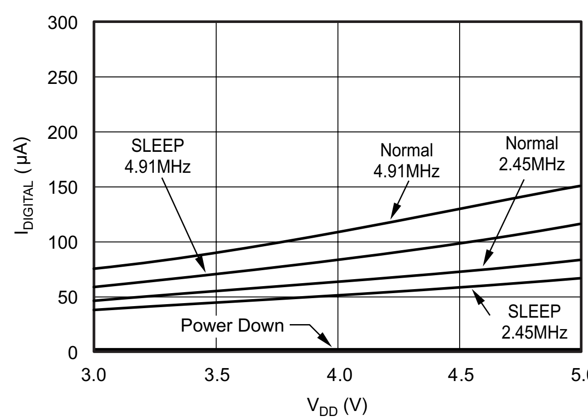
CURRENT vs TEMPERATURE



CURRENT vs VOLTAGE



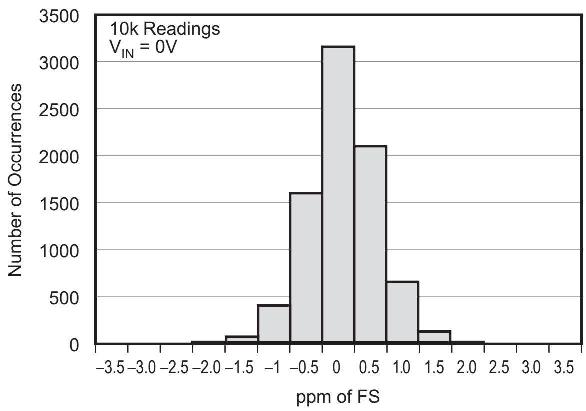
SUPPLY CURRENT vs SUPPLY



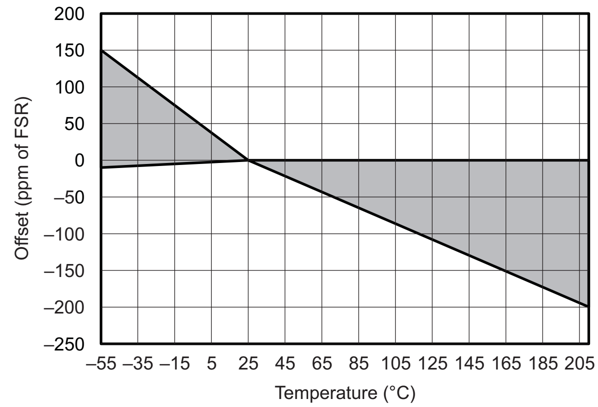
TYPICAL CHARACTERISTICS (continued)

All specifications V_{DD} = 5 V, f_{OSC} = 2.4576 MHz, PGA = 1, f_{DATA} = 15 Hz, and V_{REF} ≡ (REF IN+) – (REF IN–) = 2.5 V, unless otherwise specified.

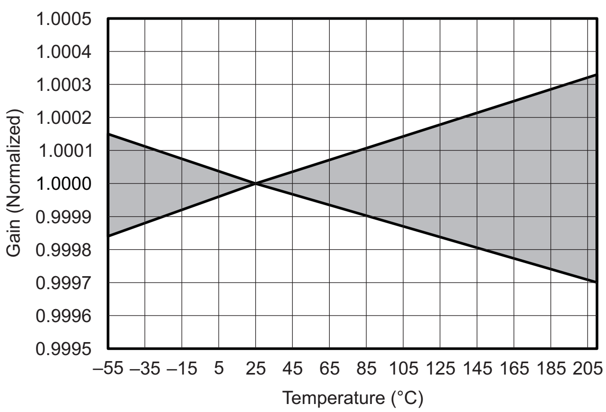
NOISE HISTOGRAM



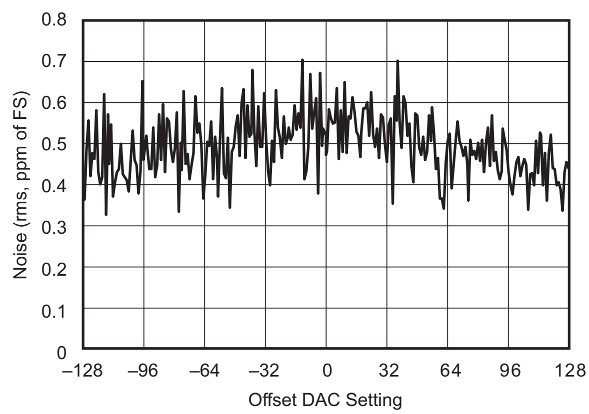
OFFSET DAC OFFSET vs TEMPERATURE (Cal AT 25°C)



OFFSET DAC GAIN vs TEMPEARTURE (Cal AT 25°C)



OFFSET DAC NOISE vs SETTING



OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 2. For example, if $A_{IN}0$ is selected as the positive differential input channel, any other channel can be selected as the negative terminal for the differential input channel. With this method, it is possible to have up to seven single-ended input channels or four independent differential input channels for the ADS1243.

The ADS1243 features a single-cycle settling digital filter that provides valid data on the first conversion after a new channel selection. In order to minimize the settling error, synchronize MUX changes to the conversion beginning, which is indicated by the falling edge of $\overline{DRDY}$. In other words, issuing a MUX change through the WREG command immediately after $\overline{DRDY}$ goes LOW minimizes the settling error. Increasing the time between the conversion beginning ($\overline{DRDY}$ goes LOW) and the MUX change command (t_{DELAY}) results in a settling error in the conversion data, as shown in Figure 3.

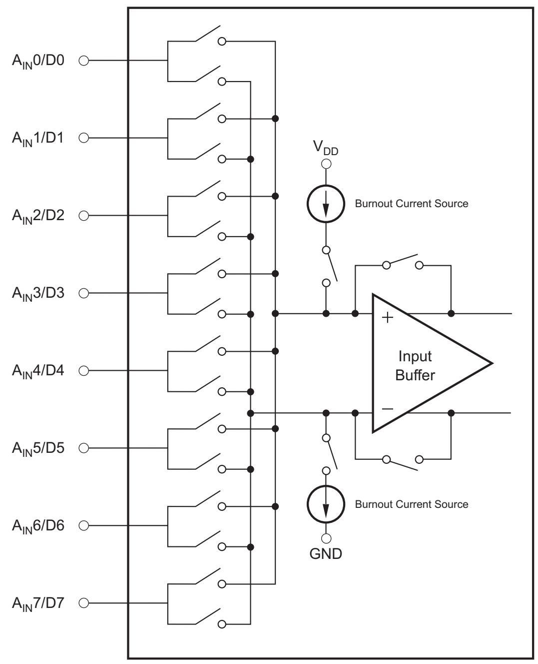


Figure 2. Input Multiplexer Configuration

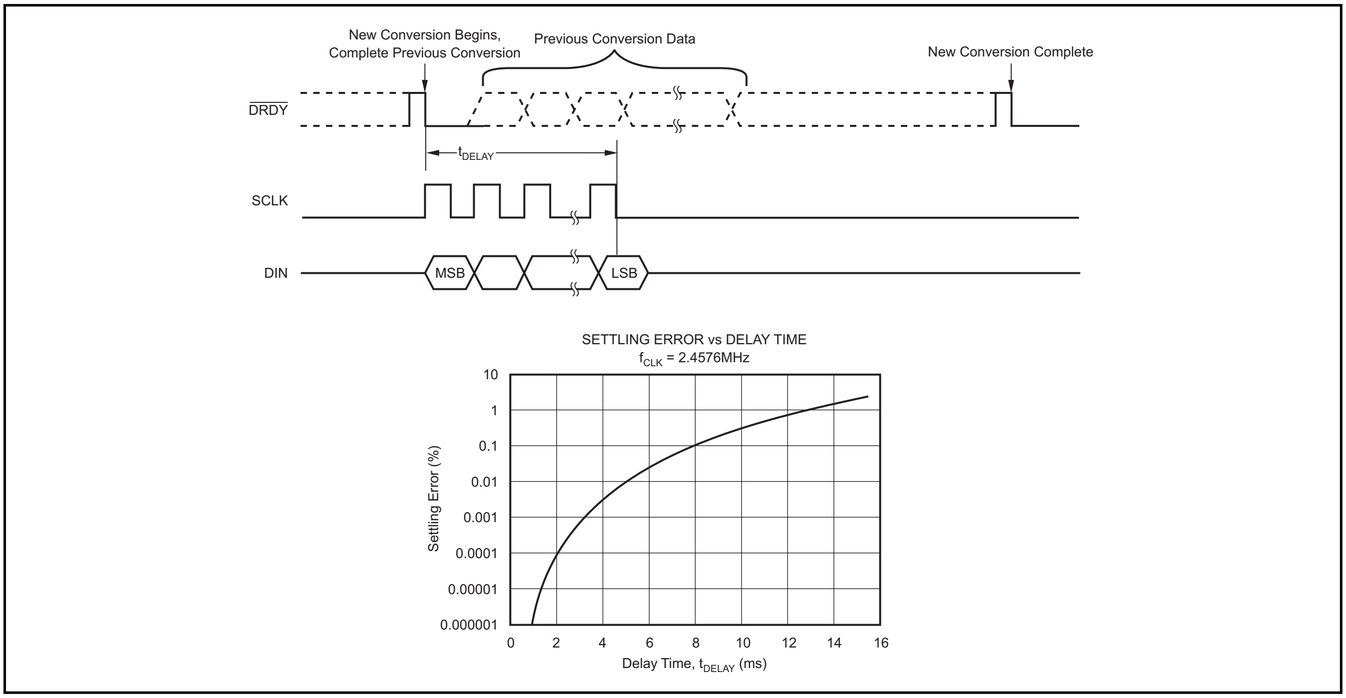


Figure 3. Input Multiplexer Configuration

BURNOUT CURRENT SOURCES

The Burnout Current Sources can be used to detect sensor short-circuit or open-circuit conditions. Setting the Burnout Current Sources (BOCS) bit in the SETUP register activates two 2μA current sources called burnout current sources. One of the current sources is connected to the converter's negative input and the other is connected to the converter's positive input.

Figure 4 shows the situation for an open-circuit sensor. This is a potential failure mode for many kinds of remotely connected sensors. The current source on the positive input acts as a pull-up, causing the positive input to go to the positive analog supply, and the current source on the negative input acts as a pull-down, causing the negative input to go to ground. The ADS1243 therefore outputs full-scale (7FFFFF Hex).

Figure 5 shows a short-circuited sensor. Since the inputs are shorted and at the same potential, the ADS1243 signal outputs are approximately zero. (Note that the code for shorted inputs is not exactly zero due to internal series resistance, low-level noise and other error sources.)

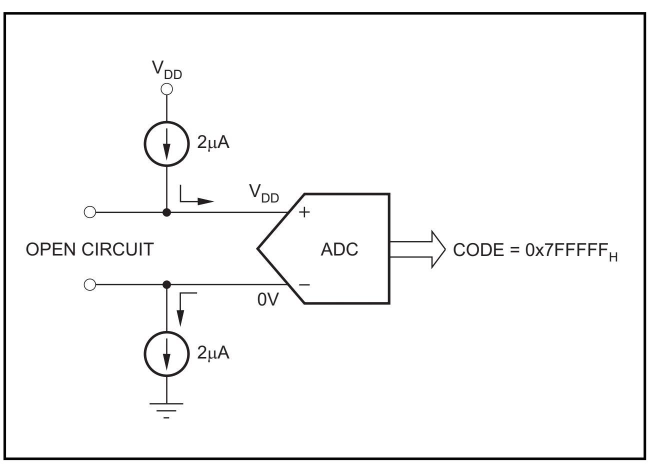


Figure 4. Burnout Detection While Sensor is Open-Circuited.

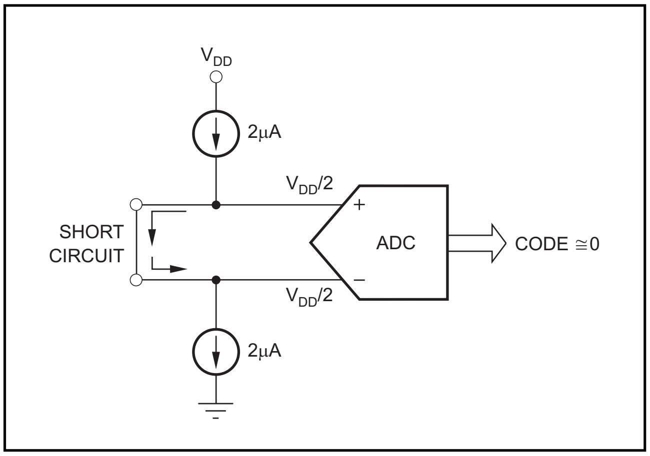


Figure 5. Burnout Detection While Sensor is Short-Circuited.

INPUT BUFFER

The input impedance of ADS1243 without the buffer enabled is approximately 5MΩ/PGA. For systems requiring very high input impedance, the ADS1243 provides a chopper-stabilized differential FET-input voltage buffer. When activated, the buffer raises the ADS1243 input impedance to approximately 5 GΩ.

The buffer's input range is approximately 50mV to V_{DD} – 1.5 V. The buffer's linearity will degrade beyond this range. Differential signals should be adjusted so that both signals are within the buffer's input range.

The buffer can be enabled using the BUFEN pin or the BUFEN bit in the ACR register. The buffer is on when the BUFEN pin is high and the BUFEN bit is set to one. If the BUFEN pin is low, the buffer is disabled. If the BUFEN bit is set to zero, the buffer is also disabled.

The buffer draws additional current when activated. The current required by the buffer depends on the PGA setting. When the PGA is set to 1, the buffer uses approximately 50 µA; when the PGA is set to 128, the buffer uses approximately 500µA.

PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5-V full-scale signal, the A/D converter can resolve down to 1 µV. With a PGA of 128 and a full-scale signal of 39 mV, the A/D converter can resolve down to 75 nV. V_{DD} current increases with PGA settings higher than 4.

OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA using the Offset DAC (ODAC) register. The ODAC register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the offset DAC does not reduce the performance of the A/D converter. For more details on the ODAC in the ADS1243, please refer to TI application report SBAA077 (available through the TI website).

MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the SETUP register, as shown in Table 2.

Table 2. Output Configuration

f_{OSC}	SPEED BIT	f_{MOD}	DR BITS			1st NOTCH FREQUENCY
			00	01	10	
2.4576 MHz	0	19,200 Hz	15 Hz	7.5 Hz	3.75 Hz	50/60 Hz
	1	9,600 Hz	7.5 Hz	3.75 Hz	1.875 Hz	25/30 Hz
4.9152 MHz	0	38,400 Hz	30 Hz	15 Hz	7.5 Hz	100/120 Hz
	1	19,200 Hz	15 Hz	7.5 Hz	3.75 Hz	50/60 Hz

CALIBRATION

The offset and gain errors can be minimized with calibration. The ADS1243 supports both self and system calibration.

Self-calibration of the ADS1243 corrects internal offset and gain errors and is handled by three commands: SELFCAL, SELFGAL, and SELFOCAL. The SELFCAL command performs both an offset and gain calibration. SELFGCAL performs a gain calibration and SELFOCAL performs an offset calibration, each of which takes two t_{DATA} periods to complete. During self-calibration, the ADC inputs are disconnected internally from the input pins. The PGA must be set to 1 prior to issuing a SELFCAL or SELFGCAL command. Any PGA is allowed when issuing a SELFOCAL command. For example, if using PGA = 64, first set PGA = 1 and issue SELFGCAL. Afterwards, set PGA = 64 and issue SELFOCAL. For operation with a reference voltage greater than (V_{DD} – 1.5) volts, the buffer must also be turned off during gain self-calibration to avoid exceeding the buffer input range.

System calibration corrects both internal and external offset and gain errors. While performing system calibration, the appropriate signal must be applied to the inputs. The system offset calibration command (SYSOCAL) requires a zero input differential signal (see Table 5). It then computes the offset that nullifies the offset in the system. The system gain calibration command (SYSGCAL) requires a positive full-scale input signal. It then computes a value to nullify the gain error in the system. Each of these calibrations takes two t_{DATA} periods to complete. System gain calibration is recommended for the best gain calibration at higher PGAs.

Calibration should be performed after power on, a change in temperature, or a change of the PGA. The RANGE bit (ACR bit 2) must be zero during calibration.

Calibration removes the effects of the ODAC; therefore, disable the ODAC during calibration, and enable again after calibration is complete.

At the completion of calibration, the $\overline{\text{DRDY}}$ signal goes low, indicating the calibration is finished. The first data after calibration should be discarded since it may be corrupt from calibration data remaining in the filter. The second data is always valid.

EXTERNAL VOLTAGE REFERENCE

The ADS1243 requires an external voltage reference. The selection for the voltage reference value is made through the ACR register.

The external voltage reference is differential and is represented by the voltage difference between the pins: $+V_{REF}$ and $–V_{REF}$. The absolute voltage on either pin, $+V_{REF}$ or $–V_{REF}$, can range from GND to V_{DD}. However, the following limitations apply:

- For V_{DD} = 5 V and RANGE = 0 in the ACR, the differential V_{REF} must not exceed 2.5 V.
- For V_{DD} = 5 V and RANGE = 1 in the ACR, the differential V_{REF} must not exceed 5 V.
- For V_{DD} = 3 V and RANGE = 0 in the ACR, the differential V_{REF} must not exceed 1.25 V.
- For V_{DD} = 3 V and RANGE = 1 in the ACR, the differential V_{REF} must not exceed 2.5 V.

CLOCK GENERATOR

The clock source for ADS1243 can be provided from a crystal, oscillator, or external clock. When the clock source is a crystal, external capacitors must be provided to ensure start-up and stable clock frequency. This is shown in both Figure 6 and Table 3. X_{OUT} is only for use with external crystals and it should not be used as a clock driver for external circuitry.

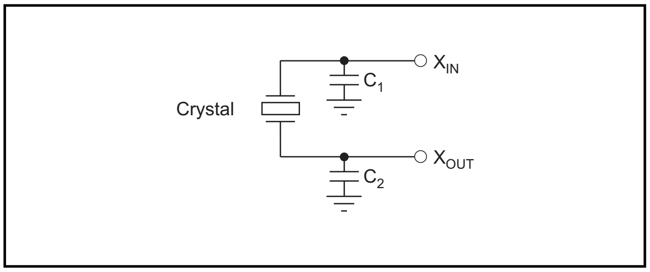


Figure 6. Crystal Connection.

Table 3. Recommended Crystals

CLOCK SOURCE	FREQUENCY	C_1	C_2	PART NUMBER
Crystal	2.4576	0-20 pF	0-20 pF	ECS, ECSD 2.45 – 32
Crystal	4.9152	0-20 pF	0-20 pF	ECS, ECSL 4.91
Crystal	4.9152	0-20 pF	0-20 pF	ECS, ECSD 4.91
Crystal	4.9152	0-20 pF	0-20 pF	CTS, MP 042 4M9182

DIGITAL FILTER

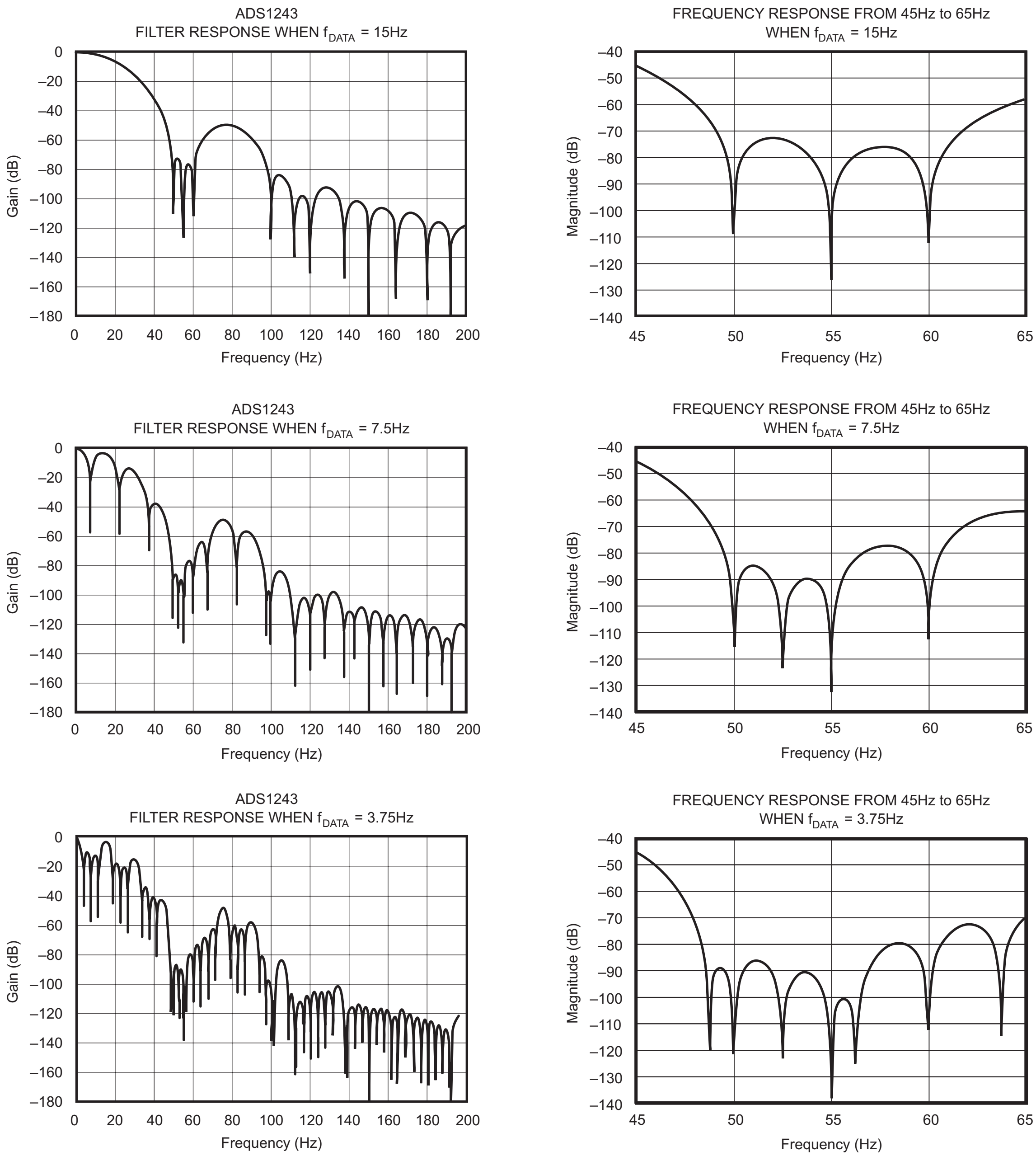
The ADS1243 has a 1279 tap linear phase Finite Impulse Response (FIR) digital filter that a user can configure for various output data rates. When a 2.4576-MHz crystal is used, the device can be programmed for an output data rate of 15 Hz, 7.5 Hz, or 3.75 Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference. Figure 7 shows the digital filter frequency response for data output rates of 15 Hz, 7.5 Hz, and 3.75 Hz.

If a different data output rate is desired, a different crystal frequency can be used. However, the rejection frequencies shift accordingly. For example, a 3.6864-MHz master clock with the default register condition has:

(3.6864 MHz/2.4576 MHz) ● 15 Hz = 22.5 Hz data output rate

and the first and second notch is:

1.5 ● (50 Hz and 60 Hz) = 75 Hz and 90 Hz



f_{OSC} = 2.4576MHz, SPEED = 0 or f_{OSC} = 4.9152MHz, SPEED = 1

DATA OUTPUT RATE	–3dB BANDWIDTH	ATTENUATION			
		f_{IN} = 50 ± 0.3Hz	f_{IN} = 60 ± 0.3Hz	f_{IN} = 50 ± 1Hz	f_{IN} = 60 ± 1Hz
15Hz	14.6Hz	–80.8dB	–87.3dB	–68.5dB	–76.1dB
7.5Hz	3.44Hz	–85.9dB	–87.4dB	–71.5dB	–76.2dB
3.75Hz	1.65Hz	–93.8dB	–88.6dB	–86.8dB	–77.3dB

Figure 7. Filter Frequency Responses

DATA I/O INTERFACE

The ADS1243 has eight pins that serve a dual purpose as both analog inputs and data I/O. These pins are configured through the IOCON, DIR, and DIO registers and can be individually configured as either analog inputs or data I/O. See Figure 8 for the equivalent schematic of an Analog/Data I/O pin.

The IOCON register defines the pin as either an analog input or data I/O. The power-up state is an analog input. If the pin is configured as an analog input in the IOCON register, the DIR and DIO registers have no effect on the state of the pin.

If the pin is configured as data I/O in the IOCON register, then DIR and DIO are used to control the state of the pin. The DIR register controls the direction of the data pin, either as an input or output. If the pin is configured as an input in the DIR register, then the corresponding DIO register bit reflects the state of the pin. Make sure the pin is driven to a logic one or zero when configured as an input to prevent excess current dissipation. If the pin is configured as an output in the DIR register, then the corresponding DIO register bit value determines the state of the output pin (0 = GND, 1 = V_{DD}).

It is still possible to perform A/D conversions on a pin configured as data I/O. This may be useful as a test mode, where the data I/O pin is driven and an A/D conversion is done on the pin.

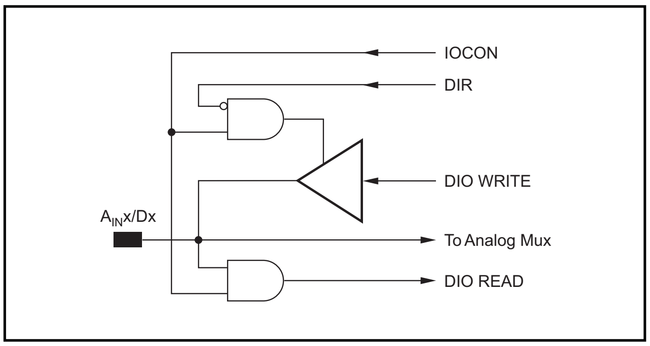


Figure 8. Analog/Data Interface Pin

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) allows a controller to communicate synchronously with the ADS1243. The ADS1243 operates in slave-only mode. The serial interface is a standard four-wire SPI ($\overline{CS}$, SCLK, D_{IN} and D_{OUT}) interface.

Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input must be externally asserted before communicating with the ADS1243. $\overline{CS}$ must stay LOW for the duration of the communication. Whenever $\overline{CS}$ goes HIGH, the serial interface is reset. $\overline{CS}$ may be hard-wired LOW.

Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock D_{IN} and D_{OUT} data. Make sure to have a clean SCLK to prevent accidental double-shifting of the data. If SCLK is not toggled within three $\overline{DRDY}$ pulses, the serial interface resets on the next SCLK pulse and starts a new communication cycle. A special pattern on SCLK resets the entire chip; see the RESET section for additional information.

Data Input (D_{IN}) and Data Output (D_{OUT})

The data input (D_{IN}) and data output (D_{OUT}) receive and send data from the ADS1243. D_{OUT} is high impedance when not in use to allow D_{IN} and D_{OUT} to be connected together and driven by a bidirectional bus. Note: the Read Data Continuous Mode (RDATAC) command should not be issued when D_{IN} and D_{OUT} are connected. While in RDATAC mode, D_{IN} looks for the STOPC or RESET command. If either of these 8-bit bytes appear on D_{OUT} (which is connected to D_{IN}), the RDATAC mode ends.

DATA READY ($\overline{DRDY}$) PIN

The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the internal data register. $\overline{DRDY}$ goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

The status of $\overline{DRDY}$ can also be obtained by interrogating bit 7 of the ACR register (address 2_H). The serial interface can operate in 3-wire mode by tying the $\overline{CS}$ input LOW. In this case, the SCLK, D_{IN}, and D_{OUT} lines are used to communicate with the ADS1243. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit of the microcontroller.

DSYNC OPERATION

Synchronization can be achieved through the DSYNC command. When the DSYNC command is sent, the digital filter is reset on the edge of the last SCLK of the DSYNC command. The modulator is held in RESET until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK following the DSYNC command.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1 V/10 ms. To ensure proper operation, the power supply should ramp monotonically.

ADS1243 REGISTERS

The operation of the device is set up through individual registers. Collectively, the registers contain all the information needed to configure the part, such as data format, multiplexer settings, calibration settings, data rate, etc. The 16 registers are shown in Table 4.

Table 4. Registers

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00_H	SETUP	ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0
01_H	MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02_H	ACR	$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0
03_H	ODAC	SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
04_H	DIO	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
05_H	DIR	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
06_H	IOCON	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
07_H	OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
08_H	OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
09_H	OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
$0A_H$	FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
$0B_H$	FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
$0C_H$	FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
$0D_H$	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
$0E_H$	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
$0F_H$	DOR0	DOR07	DOR16	FSR21	DOR04	DOR03	DOR02	DOR01	DOR00

DETAILED REGISTER DEFINITIONS

Setup

(Address 00_H) Setup Register

Reset Value = iiii0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0

bit 7–4 Factory Programmed Bits

bit 3 BOCS: Burnout Current Source

0 = Disabled (default)

1 = Enabled

bit 2–0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection

000 = 1 (default)

001 = 2

010 = 4

011 = 8

100 = 16

101 = 32

110 = 64

111 = 128

MUX

(Address 01_H) Multiplexer Control Register

Reset Value = 01_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

bit 7–4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select

0000 = $A_{IN}0$ (default)
0001 = $A_{IN}1$
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$
1111 = Reserved

bit 3–0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select

0000 = $A_{IN}0$
0001 = $A_{IN}1$ (default)
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$
1111 = Reserved

ACR

(Address 02_H) Analog Control Register

Reset Value = $X0_H$

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0

bit 7 $\overline{\text{DRDY}}$: Data Ready (Read Only)

This bit duplicates the state of the $\overline{\text{DRDY}}$ pin.

bit 6 U/B: Data Format

0 = Bipolar (default)
1 = Unipolar

U/$\overline{\text{B}}$	ANALOG INPUT	DIGITAL OUTPUT (Hex)
0	+FSR	0x7FFFFF
	Zero	0x000000
	–FSR	0x800000
1	+FSR	0xFFFFFF
	Zero	0x000000
	–FSR	0x000000

bit 5 SPEED: Modulator Clock Speed

0 = f_{MOD} = f_{OSC}/128 (default)

1 = f_{MOD} = f_{OSC}/256

bit 4 BUFEN: Buffer Enable

0 = Buffer Disabled (default)

1 = Buffer Enabled

bit 3 BIT ORDER: Data Output Bit Order

0 = Most Significant Bit Transmitted First (default)

1 = Least Significant Bit Transmitted First

Data is always shifted in or out MSB first.

bit 2 RANGE: Range Select

0 = Full-Scale Input Range equal to ±V_{REF} (default).

1 = Full-Scale Input Range equal to ±1/2 V_{REF}

NOTE: This allows reference voltages as high as V_{DD}, but even with a 5V reference voltage the calibration must be performed with this bit set to 0.

bit 1–0 DR1: DR0: Data Rate

(f_{OSC} = 2.4576MHz, SPEED = 0)

00 = 15 Hz (default)

01 = 7.5 Hz

10 = 3.75 Hz

11 = Reserved

ODAC

(Address 03) Offset DAC

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

bit 7 Sign

0 = Positive

1 = Negative

$$\text{Offset} = \frac{V_{REF}}{2 \bullet PGA} \bullet \left(\frac{OSET[6:0]}{127}\right) \quad RANGE = 0$$

$$\text{Offset} = \frac{V_{REF}}{4 \bullet PGA} \bullet \left(\frac{OSET[6:0]}{127}\right) \quad RANGE = 1$$

NOTE: The offset DAC must be enabled after calibration or the calibration nullifies the effects.

DIO

(Address 04_H) Data I/O

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIO 7	DIO 6	DIO 5	DIO 4	DIO 3	DIO 2	DIO 1	DIO 0

If the IOCON register is configured for data, a value written to this register appears on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register returns the value of the data I/O pins.

DIR

(Address 05_H) Direction Control for Data I/O

Reset Value = FF_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Each bit controls whether the corresponding data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

IOCON

(Address 06_H) I/O Configuration Register

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

bit 7-0 IO7: IO0: Data I/O Configuration

0 = Analog (default)

1 = Data

Configuring the pin as a data I/O pin allows it to be controlled through the DIO and DIR registers.

ORC0

(Address 07_H) Offset Calibration Coefficient

(Least Significant Byte)

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1

(Address 08_H) Offset Calibration Coefficient

(Middle Byte)

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2

(Address 09_H) Offset Calibration Coefficient

(Most Significant Byte)

Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0

(Address $0A_H$) Full-Scale Register

(Least Significant Byte)

Reset Value = 59_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1

(Address $0B_H$) Full-Scale Register
(Middle Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2

(Address $0C_H$) Full-Scale Register
(Most Significant Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DOR2

(Address $0D_H$) Data Output Register
(Most Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16

DOR1

(Address $0E_H$) Data Output Register
(Middle Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08

DOR0

(Address $0F_H$) Data Output Register
(Least Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

ADS1243 CONTROL COMMAND DEFINITIONS

The commands listed in Table IV control the operations of ADS1243. Some of the commands are stand-alone commands (for example, RESET) while others require additional bytes (for example, WREG requires the count and data bytes).

Operands:

- n = count (0 to 127)
- r = register (0 to 15)
- x = don't care

Table 5. Command Summary

COMMANDS	DESCRIPTION	OP CODE	2nd COMMAND BYTE
RDATA RDATAC STOPC RREG WREG SELFCAL SELFOCAL SELFGCAL SYSOCAL SYSGCAL WAKEUP DSYNC SLEEP RESET	Read Data	0000 0001 (01_H)	—
	Read Data Continuously	0000 0011 (03_H)	—
	Stop Read Data Continuously	0000 1111 ($0F_H$)	—
	Read from REG "rrrr"	0001 r r r r ($1x_H$)	xxxx_nnnn (# of regs-1)
	Write to REG "rrrr"	0101 r r r r ($5x_H$)	xxxx_nnnn (# of regs-1)
	Offset and Gain Self Cal	1111 0000 ($F0_H$)	—
	Self Offset Cal	1111 0001 ($F1_H$)	—
	Self Gain Cal	1111 0010 ($F2_H$)	—
	Sys Offset Cal	1111 0011 ($F3_H$)	—
	Sys GainCal	1111 0100 ($F4_H$)	—
	Wakup from SLEEP Mode	1111 1011 (FB_H)	—
	Sync $\overline{DRDY}$	1111 1100 (FC_H)	—
	Put in SLEEP Mode	1111 1101 (FD_H)	—
	Reset to Power-Up Values	1111 1110 (FE_H)	—
NOTE: The received data format is always MSB first; the data out format is set by the BIT ORDER bit in the ACR register.			

RDATA–Read Data

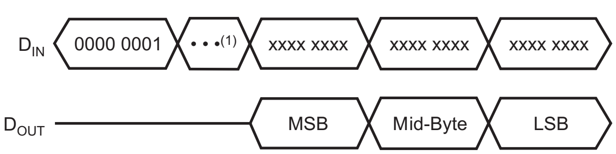
Description: Read the most recent conversion result from the Data Output Register (DOR). This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



(1) For wait time, refer to timing specification.

RDATAC–Read Data Continuous

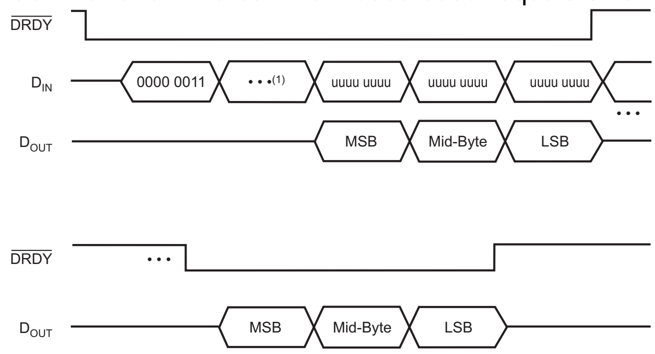
Description: Read Data Continuous mode enables the continuous output of new data on each $\overline{DRDY}$. This command eliminates the need to send the Read Data Command on each $\overline{DRDY}$. This mode may be terminated by either the STOPC command or the RESET command. Wait at least 10 f_{OSC} after $\overline{DRDY}$ falls before reading.

Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence: Command terminated when “uuuu uuuu” equals STOPC or RESET.



(1)For wait time, refer to timing specification.

STOPC–Stop Continuous

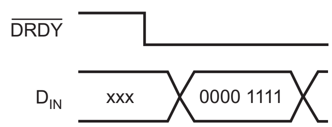
Description: Ends the continuous data output mode. Issue after $\overline{\text{DRDY}}$ goes LOW.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG–Read from Registers

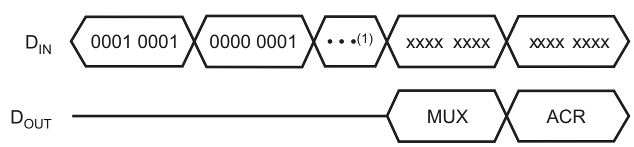
Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte count. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence: Read Two Registers Starting from Register 01_H (MUX)



(1)For wait time, refer to timing specification.

WREG–Write to Registers

Description: Write to the registers starting with the register address specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence: Write Two Registers Starting from 04_H (DIO)

SELFCAL–Offset and Gain Self Calibration

Description: Starts the process of self calibration. The Offset Calibration Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:

SELFOCAL–Offset Self Calibration

Description: Starts the process of self-calibration for offset. The Offset Calibration Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:

SELFGCAL–Gain Self Calibration

Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:

SYSOCAL–System Offset Calibration

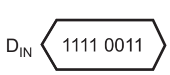
Description: Initiates a system offset calibration. The input should be set to 0V, and the ADS1243 computes the OCR value that compensates for offset errors. The Offset Calibration Register (OCR) is updated after this operation. The user must apply a zero input signal to the appropriate analog inputs. The OCR register is automatically updated afterwards.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL–System Gain Calibration

Description: Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the ADS1243 computes the FSR value that will compensate for gain errors. The FSR is updated after this operation. To initiate a system gain calibration, the user must apply a full-scale input signal to the appropriate analog inputs. FCR register is updated automatically.

Operands: None

Bytes: 1

Encoding: 1111 0100

Data Transfer Sequence: D_{IN} 1111 0100

WAKEUP

Description: Wakes the ADS1243 from SLEEP mode.

Operands: None

Bytes: 1

Encoding: 1111 1011

Data Transfer Sequence: D_{IN} 1111 1011

DSYNC–Sync $\overline{\text{DRDY}}$

Description: Synchronizes the ADS1243 to an external event.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence: D_{IN} 1111 1100

SLEEP–Sleep Mode

Description: Puts the ADS1243 into a low power sleep mode. To exit sleep mode, issue the WAKEUP command.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence: D_{IN} 1111 1101

RESET–Reset to Default Values

Description: Restore the registers to their power-up values. This command stops the Read Continuous mode.

Operands: None

Bytes: 1

Encoding: 1111 1110

Data Transfer Sequence: D_{IN} 1111 1110

APPLICATION INFORMATION

GENERAL-PURPOSE WEIGHT SCALE

Figure 9 shows a typical schematic of a general-purpose weight scale application using the ADS1243. In this example, the internal PGA is set to either 64 or 128 (depending on the maximum output voltage of the load cell) so that the load cell output can be directly applied to the differential inputs of ADS1243.

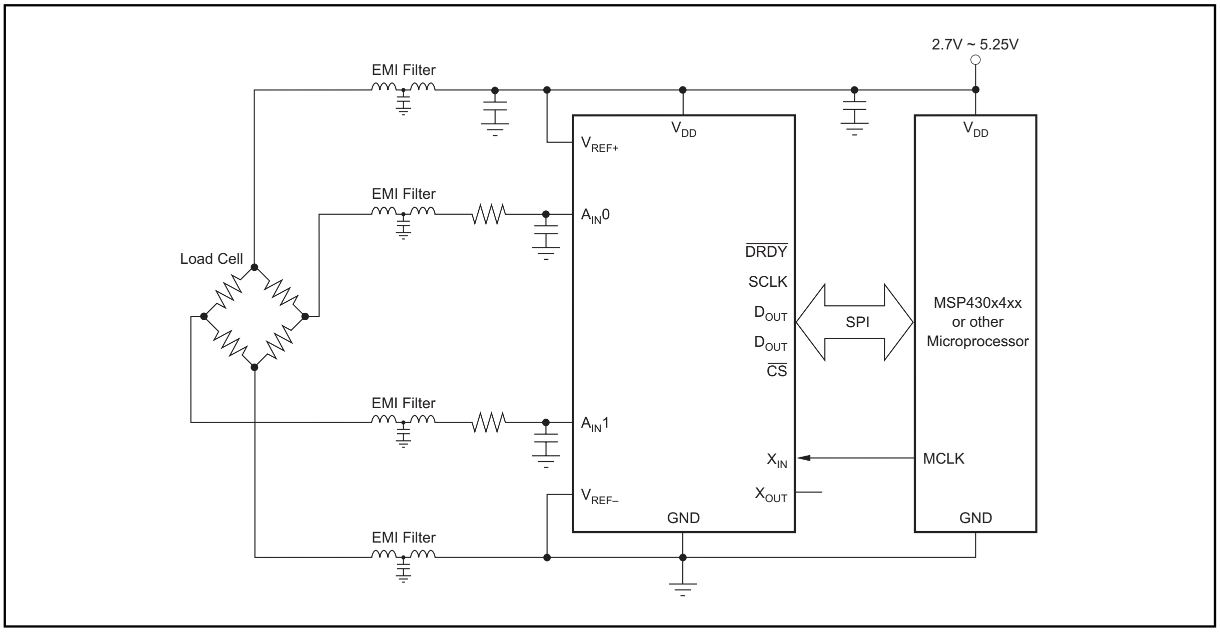


Figure 9. Schematic of a General-Purpose Weight Scale.

HIGH PRECISION WEIGHT SCALE

Figure 10 shows the typical schematic of a high-precision weight scale application using the ADS1243. The front-end differential amplifier helps maximize the dynamic range.

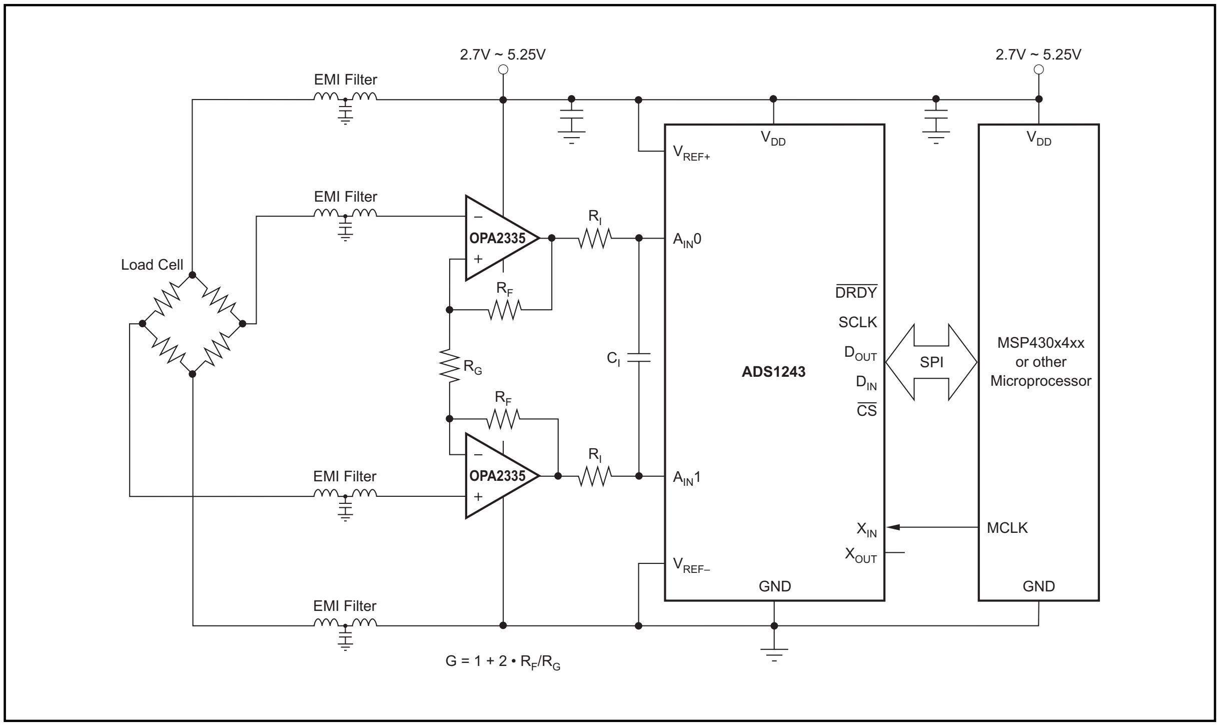


Figure 10. Block Diagram for a High-Precision Weight Scale.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Voltage – the voltage at any one analog input relative to GND.

Analog Input Differential Voltage –given by the following equation: (IN+) – (IN–). Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5-V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5 V. The negative full-scale output is produced when the differential is –2.5 V. In each case, the actual input voltages must remain within the GND to V_{DD} range.

Conversion Cycle –the term conversion cycle usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period.

Data Rate – The rate at which conversions are completed. See definition for f_{DATA}.

$$f_{DATA} = \frac{f_{OSC}}{128 \bullet 2^{SPEED} \bullet 1280 \bullet 2^{DR}}$$

SPEED = 0,1
DR = 0, 1, 2

$\mathbf{f_{OSC}}$ –the frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1243.

$\mathbf{f_{MOD}}$ – the frequency or speed at which the modulator of the ADS1243 is running. This depends on the SPEED bit as given by the following equation:

	SPEED = 0	SPEED = 1
mfactor	128	256

$$f_{MOD} = \frac{f_{osc}}{mfactor} = \frac{f_{osc}}{128 \bullet 2^{SPEED}}$$

PGA SETTING	SAMPLING FREQUENCY
1, 2, 4, 8	$f_{SAMP} = \frac{f_{OSC}}{mfactor}$
16	$f_{SAMP} = \frac{f_{OSC} \bullet 2}{mfactor}$
32	$f_{SAMP} = \frac{f_{OSC} \bullet 4}{mfactor}$
64, 128	$f_{SAMP} = \frac{f_{OSC} \bullet 8}{mfactor}$

$\mathbf{f_{SAMP}}$ – the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

$\mathbf{f_{DATA}}$ – the frequency of the digital output data produced by the ADS1243, f_{DATA} is also referred to as the Data Rate.

Full-Scale Range (FSR) – as with most A/D converters, the full-scale range of the ADS1243 is defined as the input, that produces the positive full-scale digital output minus the input, that produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5-V reference and is placed in a gain setting of 2, the full-scale range is: [1.25 V (positive full-scale) minus –1.25 V (negative full-scale)] = 2.5 V.

Least Significant Bit (LSB) Weight – this is the theoretical amount of voltage that the differential voltage at the analog input has to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSBWeight} = \frac{\text{Full-Scale Range}}{2^N - 1}$$

where N is the number of bits in the digital output.

t_{DATA} – the inverse of fDATA, or the period between each data output.

Table 6. Full-Scale Range versus PGA Setting

	5V SUPPLY ANALOG INPUT[1]			GENERAL EQUATIONS		
GAIN SETTING	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES[2]	PGA OFFSET RANGE	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES[2]	PGA SHIFT RANGE
1	5 V	±2.5 V	±1.25 V	RANGE = 0		
2	2.5 V	±1.25 V	±0.625 V	$\frac{V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{2 \bullet PGA}$	$\frac{\pm V_{REF}}{4 \bullet PGA}$
4	1.25 V	±0.625 V	±312.5 mV			
8	0.625 V	±312.5 mV	±156.25 mV			
16	312.5 mV	±156.25 mV	±78.125 mV	RANGE = 1		
32	156.25 mV	±78.125 mV	±39.0625 mV			
64	78.125 mV	±39.0625 mV	±19.531 mV			
128	39.0625 mV	±19.531 mV	±9.766 mV			

(1) With a 2.5-V reference.
(2) Refer to electrical specification for analog input voltage range.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1243SJD	Active	Production	CDIP SB (JD) | 20	19 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 210	ADS1243SJD
ADS1243SKGD1	Active	Production	XCEPT (KGD) | 0	121 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 210	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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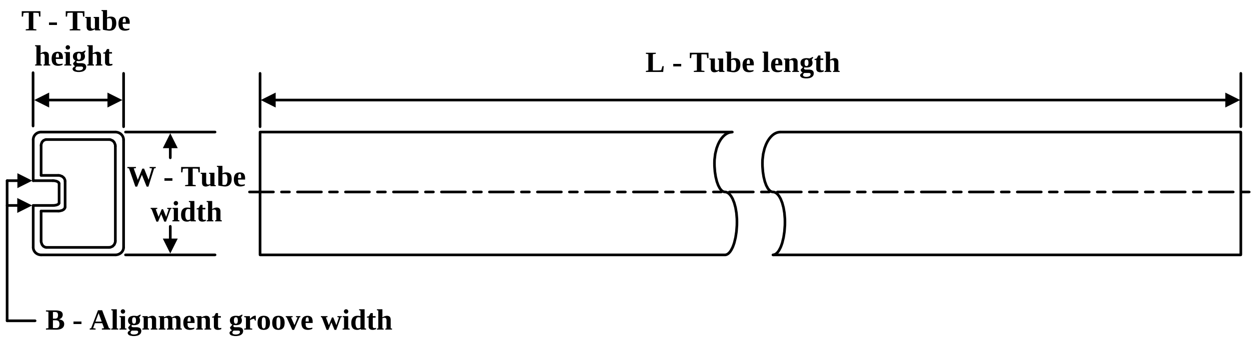
OTHER QUALIFIED VERSIONS OF ADS1243-HT :

- Catalog : ADS1243

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE

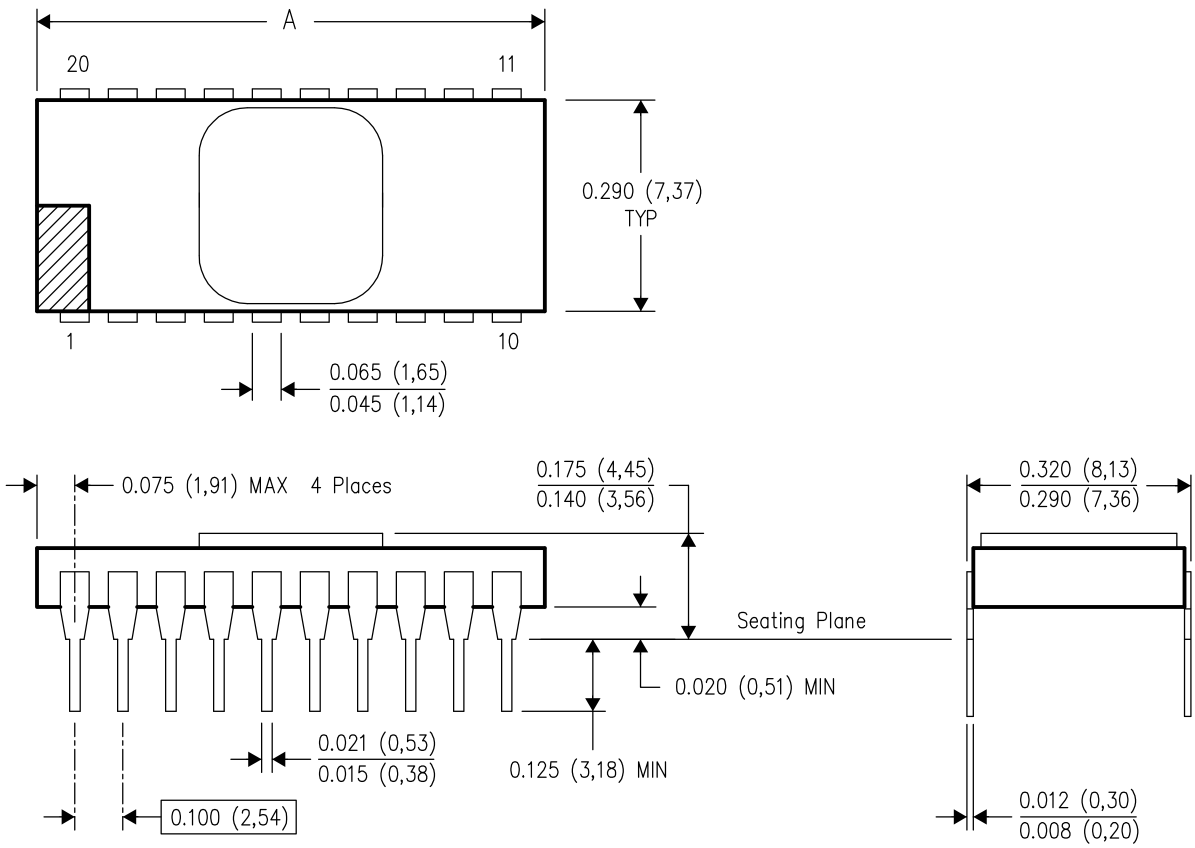


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1243SJD	JD	CDIP SB	20	19	506.98	15.24	12290	NA

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



PINS ** / DIM	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

重要通知和免责声明