ADS125H01 ±20V 输入、40kSPS、24 位 Δ-Σ ADC

1 特性

- ±20V 输入、24 位 Δ-Σ ADC
- 可编程数据速率：2.5SPS 至 40kSPS
- 高电压、1GΩ 输入阻抗 PGA：
  - 差分输入范围：高达 ±20V
  - 绝对输入范围：高达 ±15.5V
  - 可编程衰减和增益：
    - 0.125 至 128
- 高性能 ADC：
  - 噪声：45nVRMS（增益 = 128、20SPS）
  - CMRR：105dB
  - 50Hz 和 60Hz 抑制：95dB
  - 温漂：10nV/°C
  - 增益漂移：1ppm/°C
  - INL：2ppm
- 集成特性和诊断：
  - 内部振荡器
  - 信号和基准电压监控器
  - 循环冗余校验 (CRC)
- 电源：
  - AVDD：4.75V 至 5.25V
  - DVDD：2.7V 至 5.25V
  - HVDD：±5V 至 ±18V
- 工作温度：–40°C 至 +125°C
- 5mm × 5mm VQFN 封装

2 应用

- PLC 模拟输入模块：
  - 电压（±10V 或 0V 至 5V）
  - 电流（4mA 至 20mA，具有分流器）
- 数据采集 (DAQ)：
  - 高共模电压输入
  - 高侧电流测量
- 电池测试

3 说明

ADS125H01 是一款 ±20V 输入、24 位、Δ-Σ 模数转换器 (ADC)。该 ADC 具有低噪声可编程增益放大器 (PGA)、时钟振荡器以及信号或基准电压超范围监控器。

与分立式解决方案相比，该器件将宽输入电压范围、±18V 电源 PGA 和 ADC 集成到单个封装中，可将电路板面积减小多达 50%。

具有 0.125 至 128 的可编程衰减和增益（相当于 ±20V 至 ±20mV 的等效输入范围），因而无需外部衰减器或外部增益级。1GΩ 的最低输入阻抗可减小由传感器负载导致的误差。此外，由于具有低噪声和低漂移性能，因而可以直接连接到受高共模电压影响的应变仪桥和热电偶传感器。

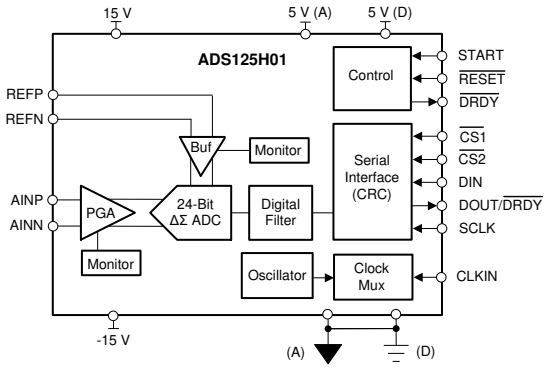
数字滤波器的可编程范围是从 2.5SPS 到 40kSPS。数据速率 ≤50SPS 或 60SPS 时，50Hz 和 60Hz 的线路周期噪声衰减可减小测量误差。在大多数数据速率下，滤波器可提供无延迟转换数据，从而在外部通道定序期间实现高数据吞吐量。

ADS125H01 采用 5mm × 5mm VQFN 封装，额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS125H01	VQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能模块图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2019) to Revision A (January 2021)	Page
• 将器件状态从“预告信息”更改为“量产数据”	1

5 Device Comparison Table

FEATURE	ADS125H01	ADS125H02
Resolution	24 bits	24 bits
Data rate	40 kSPS	40 kSPS
Analog input pins	2	3
Voltage reference	—	Yes
Temperature sensor	—	Yes
Auto-zero mode	—	Yes
Sinc2 filter mode	—	Yes
GPIO pins	—	4
Current sources	—	2

6 Pin Configuration and Functions

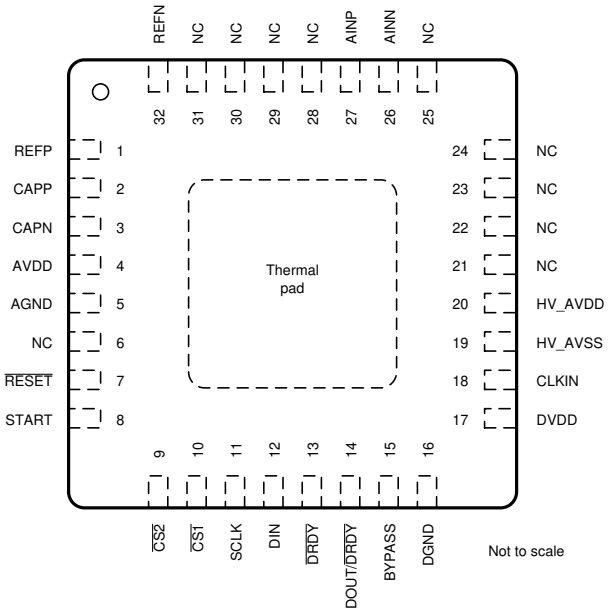


图 6-1. RHB Package, 32-Pin VQFN, Top View

表 6-1. Pin Functions

NO.	NAME	I/O	DESCRIPTION
1	REFP	Analog input	Positive reference input
2	CAPP	Analog output	PGA output P; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
3	CAPN	Analog output	PGA output N; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
4	AVDD	Analog	Low-voltage analog power supply
5	AGND	Analog	Analog ground; connect to the ADC ground plane
6	NC	—	No connection; electrically float or tie to AGND
7	$\overline{\text{RESET}}$	Digital input	Reset; active low
8	START	Digital input	Conversion start, active high
9	$\overline{\text{CS2}}$	Digital input	Serial interface chip-select 2 to select the PGA for communication
10	$\overline{\text{CS1}}$	Digital input	Serial interface chip-select 1 to select the ADC for communication
11	SCLK	Digital input	Serial interface shift clock
12	DIN	Digital input	Serial interface data input
13	$\overline{\text{DRDY}}$	Digital output	Data ready; active low
14	DOUT/$\overline{\text{DRDY}}$	Digital output	Serial interface data output or data-ready output, active low
15	BYPASS	Analog output	2-V subregulator output; connect a 1-µF capacitor to DGND
16	DGND	Digital	Digital ground; connect to the ADC ground plane
17	DVDD	Digital	Digital power supply
18	CLKIN	Digital input	External clock input; connect to DGND for internal oscillator operation
19	HV_AVSS	Analog	High-voltage negative analog power supply
20	HV_AVDD	Analog	High-voltage positive analog power supply
21 – 25	NC	—	No connection; electrically float or tie to AGND
26	AINN	Analog input	Negative analog input
27	AINP	Analog input	Positive analog input

表 6-1. Pin Functions (continued)

NO.	NAME	I/O	DESCRIPTION
28 – 31	NC	—	No connection; electrically float or tie to AGND
32	REFN	Analog input	Negative reference input
Thermal pad		—	Exposed thermal pad; connect to DGND; see the recommended PCB land pattern at the end of the document

7 Specifications

7.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	HV_AVDD to HV_AVSS	–0.3	38	V
	HV_AVSS to AGND	–19	0.3	
	AVDD to AGND	–0.3	6	
	DVDD to DGND	–0.3	6	
	AGND to DGND	–0.1	0.1	
Analog input voltage	AINP, AINN	HV_AVSS – 0.3	HV_AVDD + 0.3	V
	REFP, REFN	AGND – 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, START, $\overline{RESET}$, CLKIN, $\overline{DRDY}$, DOUT/ $\overline{DRDY}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to 10 mA in the event the analog input voltage exceeds HV_AVDD + 0.3 V or HV_AVSS – 0.3 V, or if the reference input exceeds AVDD + 0.3 V or AGND – 0.3 V, or if the digital input voltage exceeds DVDD + 0.3 V or DGND – 0.3 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-voltage analog power supplies	HV_AVDD to HV_AVSS	10		36	V
		HV_AVSS to AGND	–18		0	
		HV_AVDD to AGND(1)	5		36	
	Low-voltage analog power supply	AVDD to AGND	4.75	5	5.25	V
	Digital power supply	DVDD to DGND	2.7		5.25	V
SIGNAL INPUTS						
$V_{(AINx)}$	Absolute input voltage		See the *PGA Operating Range* section			
V_{IN}	Differential input voltage range(2)	$V_{IN} = V_{AINP} - V_{AINN}$	–20	$\pm V_{REF}$ / Gain	20	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Reference voltage input	$V_{REF} = V_{(REFP)} - V_{(REFN)}$	0.9		AVDD	V
$V_{(REFN)}$	Negative reference voltage		AGND – 0.05		$V_{(REFP)}$ – 0.9	V
$V_{(REFP)}$	Positive reference voltage		$V_{(REFN)}$ + 0.9		AVDD + 0.05	V
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
EXTERNAL CLOCK(3)						
f_{CLK}	Frequency	$f_{DATA} \leqslant$ 25.6 kSPS	1	7.3728	8	MHz
		f_{DATA} = 40 kSPS	1	10.24	10.75	
	Duty cycle		40%		60%	
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–45		125	°C

(1) HV_AVDD can be connected to AVDD if AVDD $\geqslant$ 5 V.
(2) The full available differential input voltage range is limited under certain conditions. See the *PGA Operating Range* section for details.
(3) Data rates scale with clock frequency.

7.4 Thermal Information

THERMAL METRIC(1)		ADS125H01 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	$V_{(AINx)}$ = 0 V, $T_A \leq$ 105°C	–15	±0.5	15	nA
	Absolute input current drift			20		pA/°C
	Differential input current	V_{IN} = 2.5 V		±0.1		nA
	Differential input current drift	V_{IN} = 2.5 V		10		pA/°C
	Differential input impedance		1	20		GΩ
PGA						
	Gain settings			0.125, 0.1875, 0.25, 0.5, 1, 2, 4, 8, 16, 32, 64,128		V/V
	Antialias filter frequency			230		kHz
PERFORMANCE						
	Resolution	No missing codes	24			Bits
e_n	Noise performance		See the *Noise Performance* section			
f_{DATA}	Data rate		2.5		40000	SPS
INL	Integral nonlinearity	Gain = 0.125 to 32		2	10	ppm_{FSR}
		Gain = 64, 128		4	12	
V_{OS}	Offset error(4)	T_A = 25°C	–30 – 300 / Gain	±10 + 100 / Gain	30 + 300 / Gain	µV
	Offset error drift	Gain = 0.125 to 8		150 / Gain	700 / Gain	nV/°C
		Gain = 16 to 128		10	50	
GE	Gain error(4)	T_A = 25°C, all gains	–0.7%	±0.1%	0.7%	
	Gain drift	All gains		1	4	ppm/°C
NMRR	Normal-mode rejection ratio(1)		See the *50-Hz and 60-Hz Normal-Mode Rejection* section			
CMRR	Common-mode rejection ratio(2)	Data rate = 20 SPS		130		dB
		Data rate = 400 SPS	90	105		
PSRR	Power-supply rejection ratio(3)	HV_AVDD, HV_AVSS		2	20	µV/V
		AVDD		20	60	
		DVDD		5	30	
VOLTAGE REFERENCE INPUTS						
	Absolute input current			±250		nA
	Input current vs reference voltage			15		nA/V
	Input current drift			0.2		nA/°C
	Effective input impedance	Differential		30		MΩ
PGA MONITORS						
	Input and output low threshold			HV_AVSS + 2		V
	Input and output high threshold			HV_AVDD – 2		V
REFERENCE MONITOR						
	Low voltage threshold			0.4	0.6	V
INTERNAL OSCILLATOR						
	Accuracy	$f_{DATA} \leq$ 25.6 kSPS	–2.5%	±0.5%	2.5%	
		f_{DATA} = 40 kSPS	–3.5%	±0.5%	3.5%	

7.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
		I_{OH} = 8 mA		0.75 × DVDD		
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × DVDD	V
		I_{OL} = –8 mA		0.2 × DVDD		
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD	V
V_{IL}	Low-level input voltage				0.3 × DVDD	V
	Input hysteresis			0.1		V
	Input leakage		–10		10	µA
POWER SUPPLY						
I_{HV_AVDD}, I_{HV_AVSS}	HV_AVDD, HV_AVSS supply current			1.1	1.8	mA
I_{AVDD}	AVDD supply current	$f_{DATA} \leq$ 25.6 kSPS		2.8	4.6	mA
		f_{DATA} = 40 kSPS		3.6		
I_{DVDD}	DVDD supply current	Internal oscillator active		0.5	0.7	mA
		f_{DATA} = 40 kSPS		0.7	1	
P_D	Power dissipation			49	79	mW

(1) Normal-mode rejection ratio performance is dependent on the digital filter configuration.
(2) Common-mode rejection ratio is specified at f_{IN} = 50 Hz and 60 Hz.
(3) Power-supply rejection ratio is specified at DC.
(4) Offset and gain errors are reduced to the level of noise by calibration.

7.6 Timing Requirements

over operating ambient temperature range and DVDD = 2.7 V to 5.25 V (unless otherwise noted)

		MIN	MAX	UNIT
SERIAL INTERFACE				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS1}$ or $\overline{CS2}$ falling edge	50		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	25		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns
$t_{c(SC)}$	SCLK period	97		ns
$t_{w(SCH)}$, $t_{w(SCL)}$	Pulse duration, SCLK high or low	40		ns
$t_{d(SCCS)}$	Delay time, last SCLK falling edge before $\overline{CS1}$ or $\overline{CS2}$ rising edge	50		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS1}$ or $\overline{CS2}$ high to reset interface	25		ns
RESET				
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	4		$1/f_{CLK}$
CONVERSION CONTROL				
$t_{w(STH)}$	Pulse duration, START high	4		$1/f_{CLK}$
$t_{w(STL)}$	Pulse duration, START low	4		$1/f_{CLK}$
$t_{su(STDR)}$	Setup time, START low or STOP command before $\overline{DRDY}$ falling edge to stop the next conversion (continuous-conversion mode)		100	$1/f_{CLK}$
$t_{h(DRSP)}$	Hold time, START low or STOP command after $\overline{DRDY}$ falling edge to continue the next conversion (continuous-conversion mode)	150		$1/f_{CLK}$

7.7 Switching Characteristics

over operating ambient temperature range and DVDD = 2.7 V to 5.25 V, and DOUT/$\overline{DRDY}$ load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE						
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		16			$1/f_{CLK}$
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS1}$ or $\overline{CS2}$ falling edge to DOUT/$\overline{DRDY}$ driven		0		50	ns
$t_{p(SCDO1)}$	Propagation delay time, SCLK rising edge to valid DOUT/$\overline{DRDY}$				40	ns
$t_{h(SCDO1)}$	Hold time, SCLK rising edge to invalid DOUT/$\overline{DRDY}$		0			ns
$t_{h(SCDO2)}$	Hold time, last SCLK falling edge to invalid DOUT/$\overline{DRDY}$ data output function		15			ns
$t_{p(SCDO2)}$	Propagation delay time, last SCLK falling edge to DOUT/$\overline{DRDY}$ data-ready function				110	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS1}$ or $\overline{CS2}$ rising edge to DOUT/$\overline{DRDY}$ high impedance				50	ns
RESET						
$t_{p(RSCN)}$	Propagation delay time, $\overline{RESET}$ rising edge or RESET command to conversion start		512			$1/f_{CLK}$
$t_{p(PRCM)}$	Propagation delay time, power-on threshold voltage to ADC communication			2^{16}		$1/f_{CLK}$
$t_{p(CMCN)}$	Propagation delay time, ADC communication to conversion start		512			$1/f_{CLK}$
CONVERSION CONTROL						
$t_{p(STDR)}$	Propagation delay time, START pin high or START command to $\overline{DRDY}$ high				2	$1/f_{CLK}$

7.8 Timing Diagrams

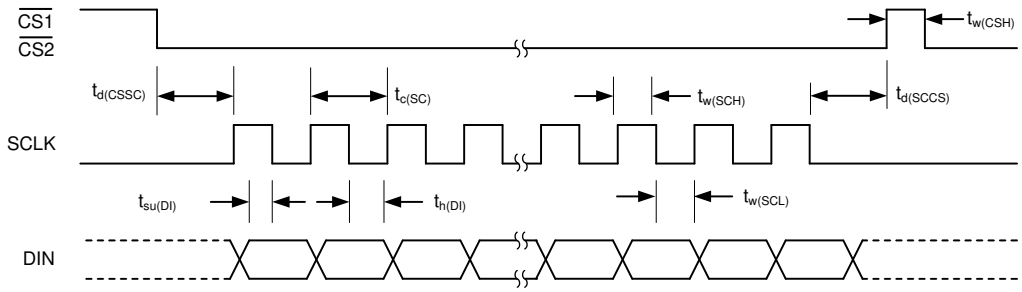
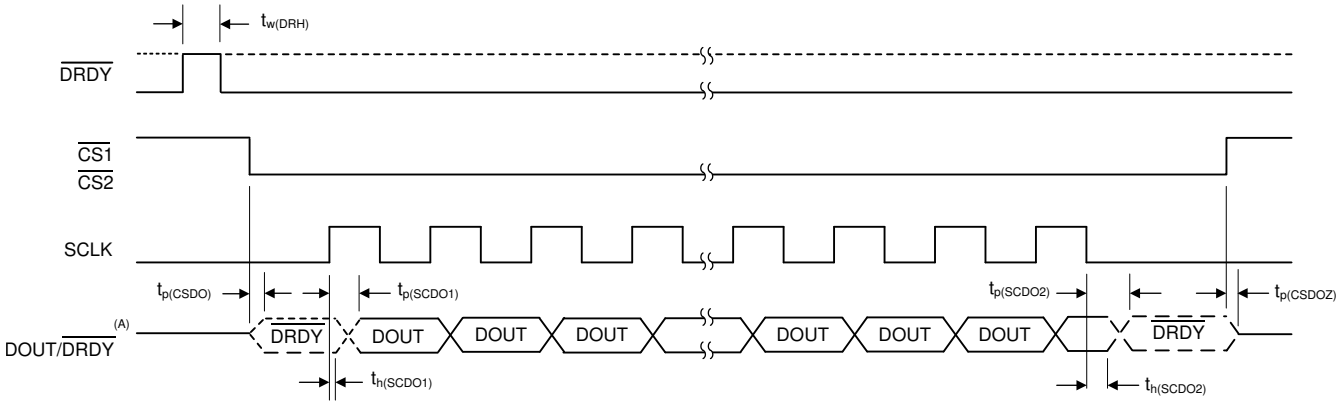


图 7-1. Serial Interface Timing Requirements



A. *$\overline{DRDY}$* indicates the data-ready function in the interval between $\overline{CS1}$ low and the first SCLK rising edge, and in the interval between the last SCLK falling edge of the command to $\overline{CS1}$ high. *DOUT* indicates the data output function during the data read operation.

图 7-2. Serial Interface Switching Characteristics

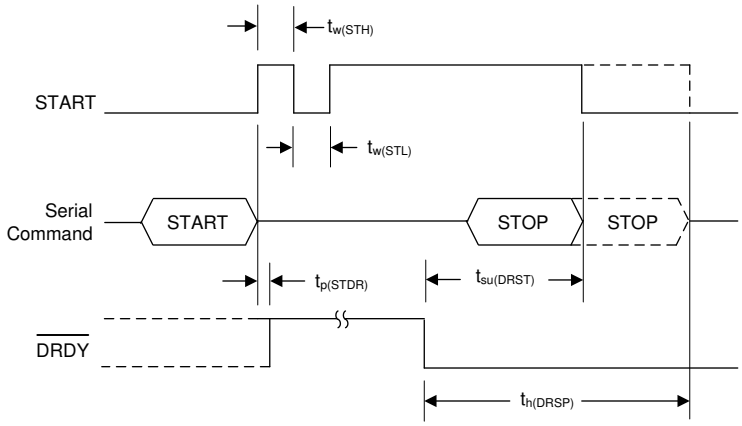


图 7-3. Conversion Control Timing Requirements

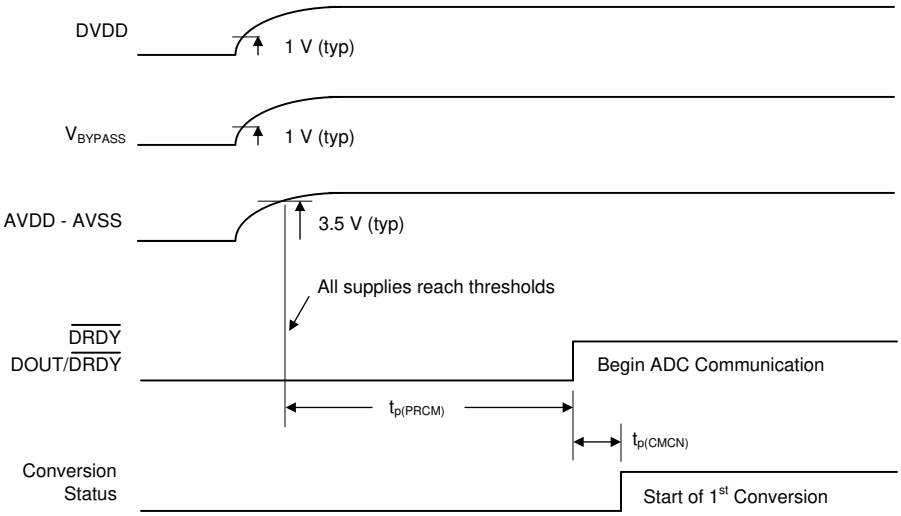


图 7-4. Power-Up Characteristics

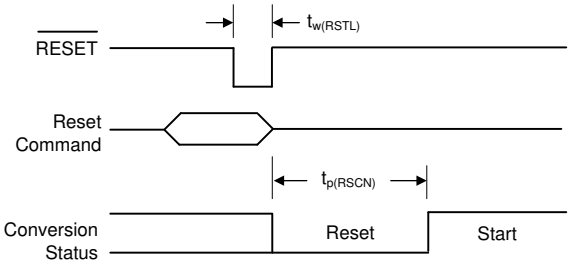


图 7-5. RESET Pin and Reset Command Timing Requirements

7.9 Typical Characteristics

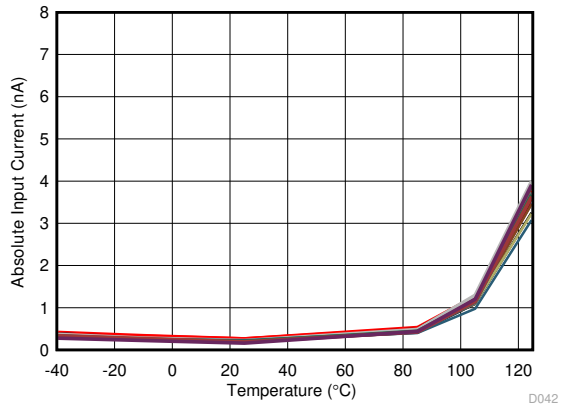
at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = – 15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

表 7-1. Table of Graphs

Analog Input Current	Absolute Input Current vs Temperature, $V_{(AINX)}$ = 0 V Differential Input Current vs Temperature, V_{IN} = 2.5 V	图 7-6 图 7-7
Noise	Distribution (Gain = 0.1875, Data Rate = 1.2 kSPS) Distribution (Gain = 32, Data Rate = 20 SPS)	图 7-8 图 7-9
Nonlinearity	vs Input Voltage (Gain = 0.125 to 2) vs Input Voltage (Gain = 4 to 128) Distribution (Gain = 0.125, 1, 32)	图 7-10 图 7-11 图 7-12
Offset Error	Drift Distribution (Gain = 0.125) Drift Distribution (Gain = 1) Drift Distribution (Gain = 32) Long-Term Drift (Gain = 0.1875) Long-Term Drift (Gain = 32)	图 7-13 图 7-14 图 7-15 图 7-16 图 7-17
Gain Error	Distribution (Gain = 0.125, 1, 32) Drift Distribution (Gain = 0.125, 1, 32) vs Temperature (Gain = 0.125 to 2) vs Temperature (Gain = 4 to 128) Long-Term Drift (Gain = 0.1875) Long-Term Drift (Gain = 32)	图 7-18 图 7-19 图 7-20 图 7-21 图 7-22 图 7-23
Reference Input Current	vs Reference Voltage (T_A = -40°C, 25°C, 85°C, 125°C)	图 7-24
Oscillator Frequency Error	vs Temperature Long-Term Drift	图 7-25 图 7-26
Power-Supply Rejection Ratio (PSRR)	vs Frequency (HV_AVDD and HV_AVSS) vs Frequency (AVDD and DVDD)	图 7-27 图 7-28
Common-Mode Rejection Ratio (CMRR)	vs Frequency	图 7-29
Operating Current	vs Temperature	图 7-30

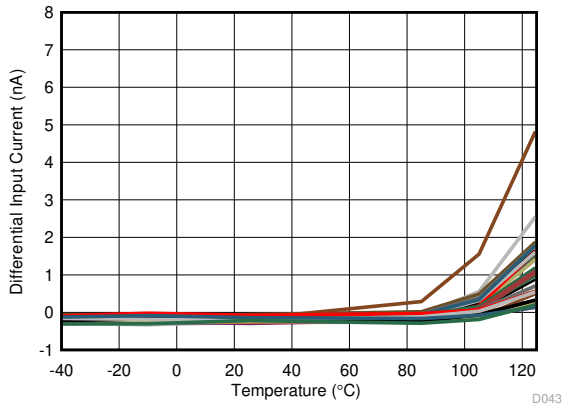
7.9 Typical Characteristics

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = – 15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



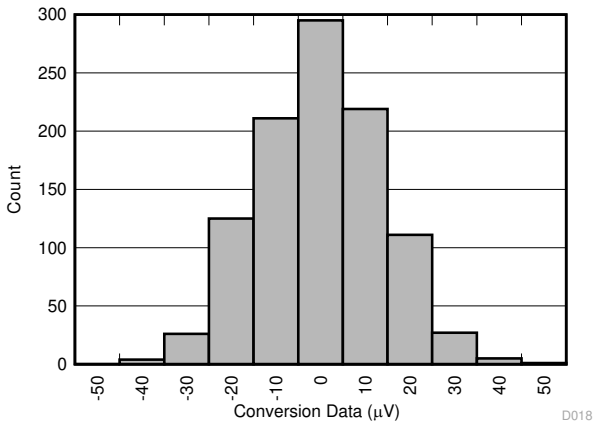
$V_{(AINx)}$ = 0 V

图 7-6. Absolute Analog Input Current vs Temperature



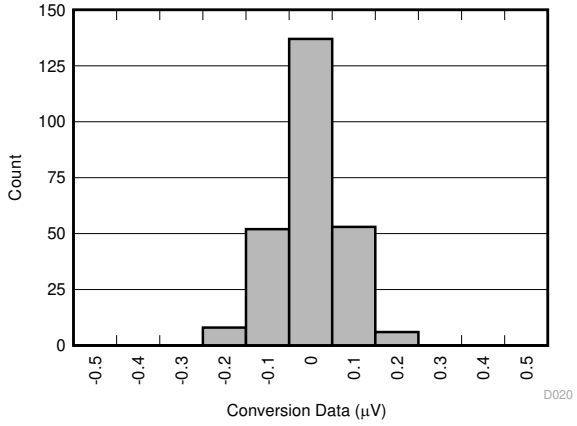
V_{IN} = 2.5 V

图 7-7. Differential Analog Input Current vs Temperature



Gain = 0.1875, data rate = 1200 SPS, sinc1 filter, calibrated offset, e_n = 13.6 μV_{RMS}

图 7-8. Conversion Data Distribution



Gain = 32, data rate = 20 SPS, FIR filter, calibrated offset, e_n = 0.076 μV_{RMS}

图 7-9. Conversion Data Distribution

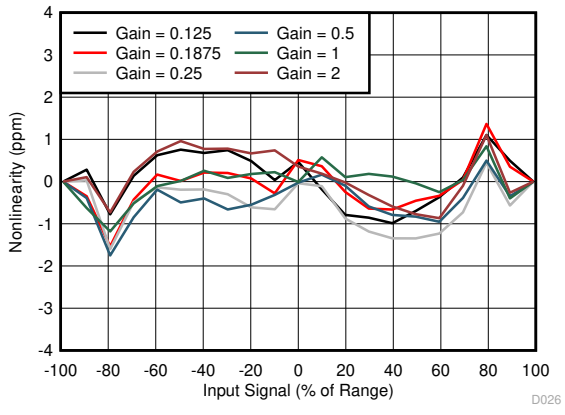


图 7-10. Nonlinearity vs Input Signal

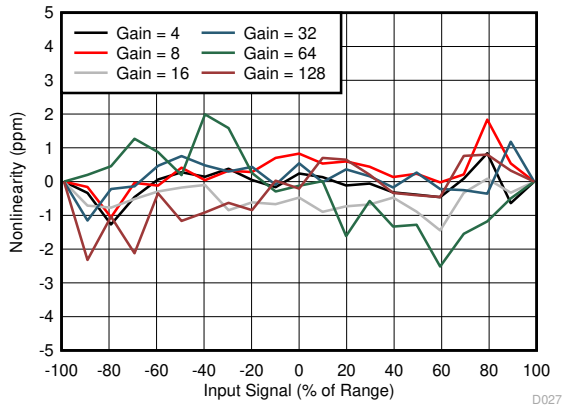


图 7-11. Nonlinearity vs Input Signal

7.9 Typical Characteristics (continued)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = – 15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

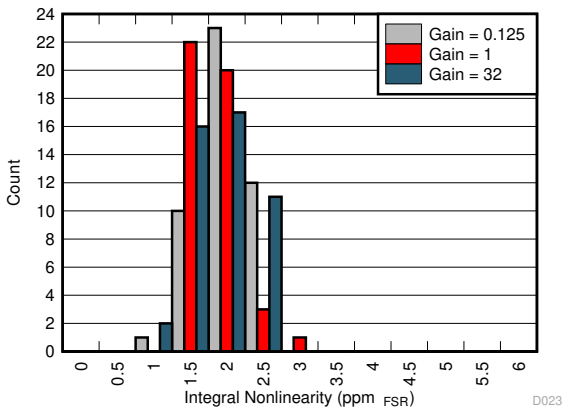
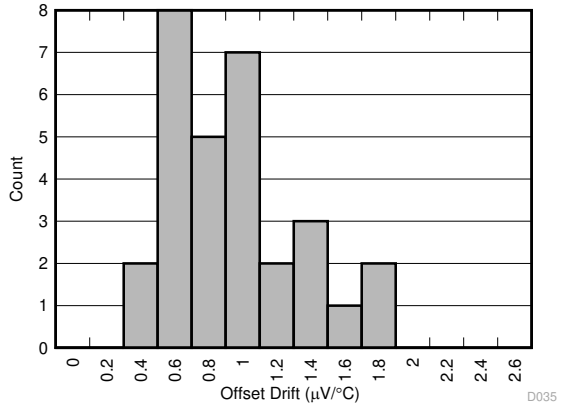
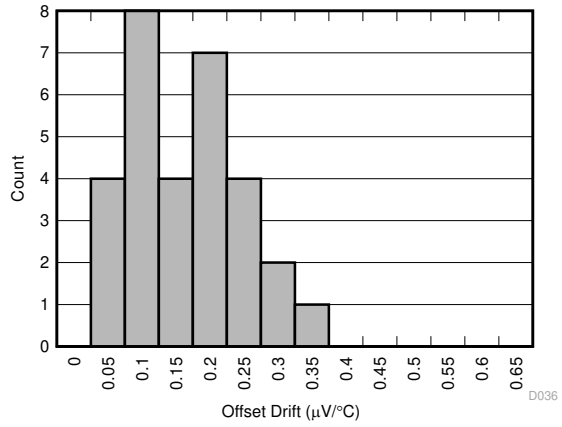


图 7-12. Nonlinearity Distribution



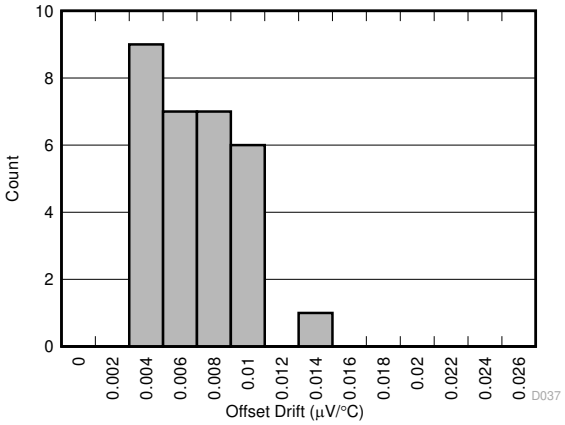
Gain = 0.125

图 7-13. Offset Error Drift Distribution



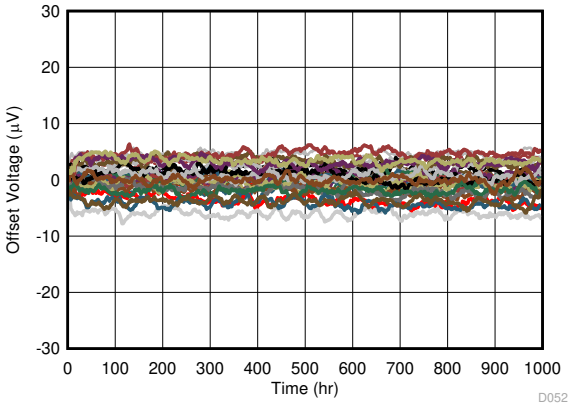
Gain = 1

图 7-14. Offset Error Drift Distribution



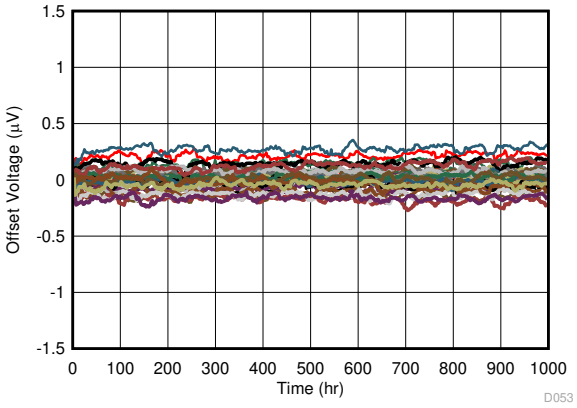
Gain = 32

图 7-15. Offset Error Drift Distribution



32 units, gain = 0.1875, after calibration

图 7-16. Offset Error Long-Term Drift



32 units, gain = 32, after calibration

图 7-17. Offset Error Long-Term Drift

7.9 Typical Characteristics (continued)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = – 15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

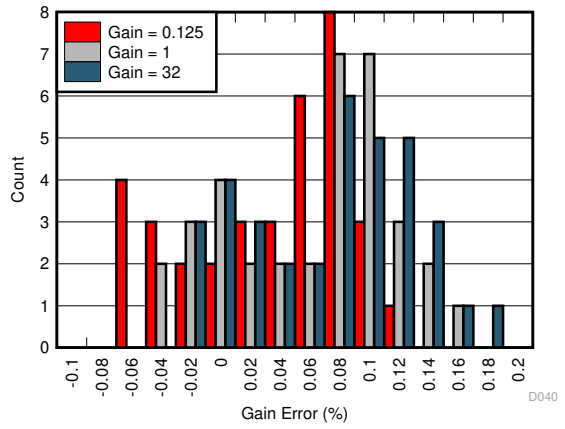


图 7-18. Gain Error Distribution

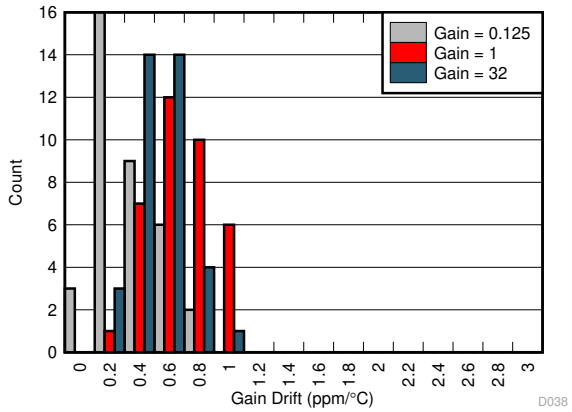
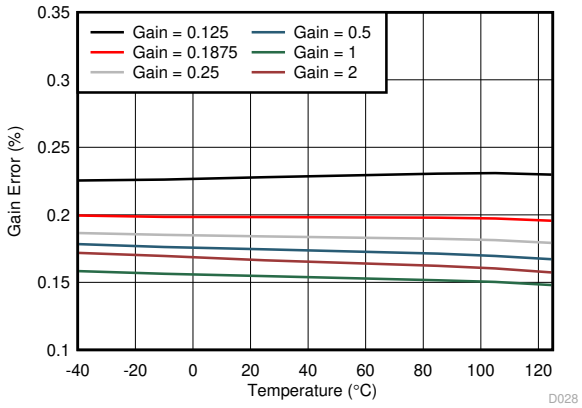
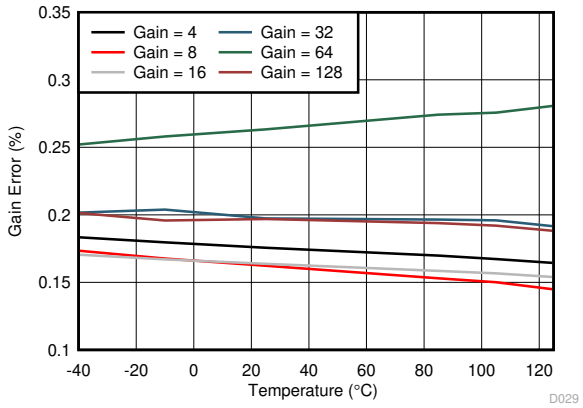


图 7-19. Gain Drift Distribution



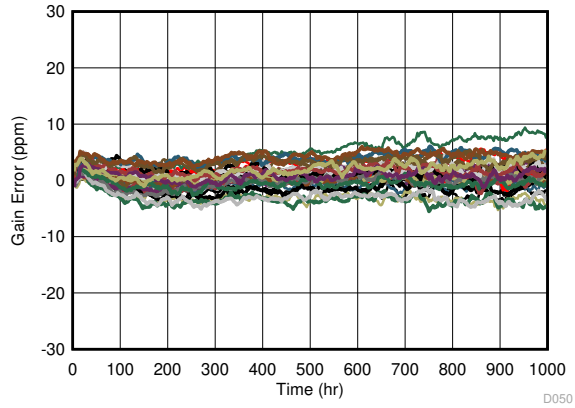
Gain = 0.125 to 2

图 7-20. Gain Error vs Temperature



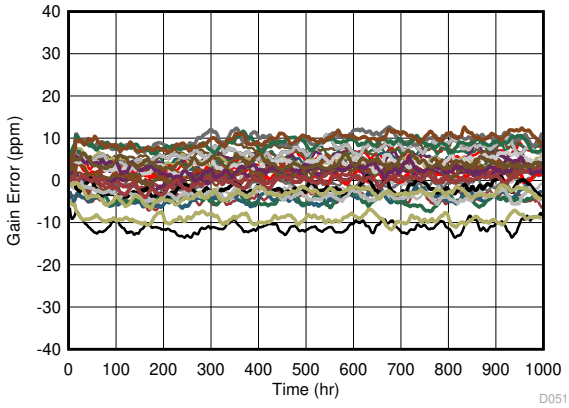
Gain = 4 to 128

图 7-21. Gain Error vs Temperature



32 units, gain = 0.1875, after calibration

图 7-22. Gain Long-Term Drift



32 units, gain = 32, after calibration

图 7-23. Gain Long-Term Drift

7.9 Typical Characteristics (continued)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = – 15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)

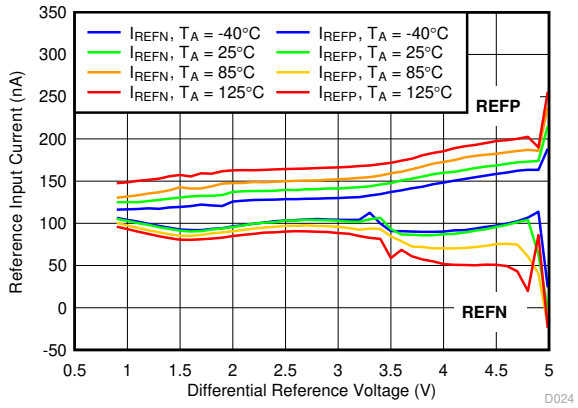
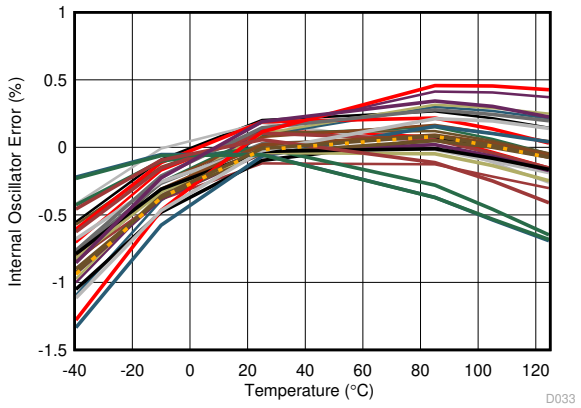
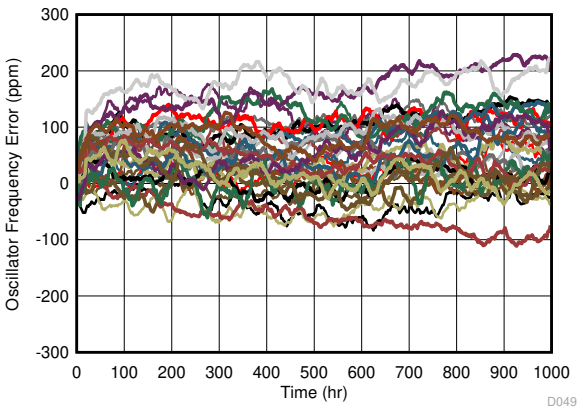


图 7-24. Reference Input Current vs Reference Voltage



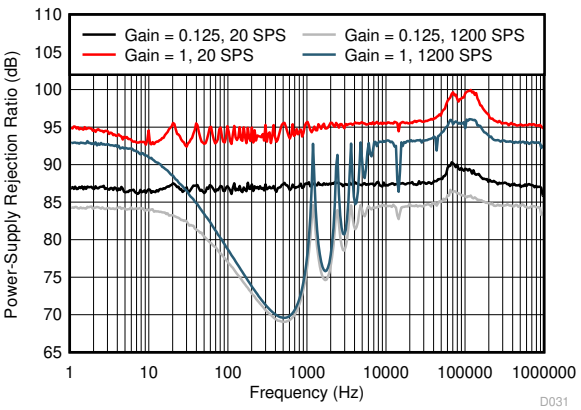
32 units

图 7-25. Oscillator Frequency Error vs Temperature



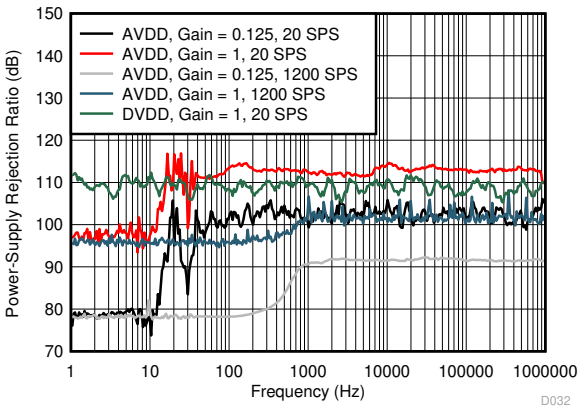
32 units, normalized data

图 7-26. Oscillator Frequency Long-Term Drift



HV_AVDD and HV_AVSS

图 7-27. PSRR vs Frequency



AVDD and DVDD

图 7-28. PSRR vs Frequency

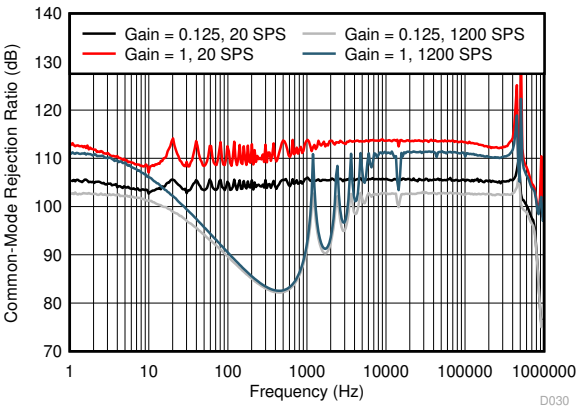
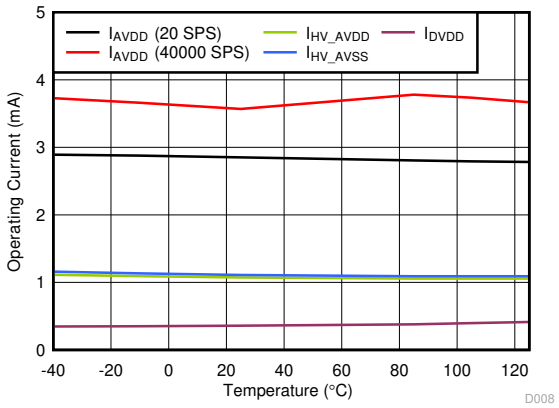


图 7-29. CMRR vs Frequency

7.9 Typical Characteristics (continued)

at T_A = 25°C, HV_AVDD = 15 V, HV_AVSS = – 15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 (unless otherwise noted)



All gains

图 7-30. Operating Current vs Temperature

8 Parameter Measurement Information

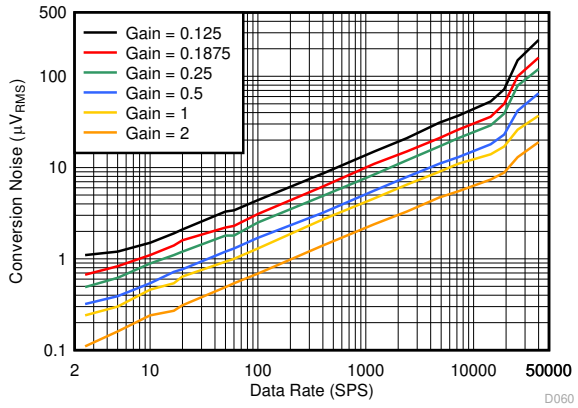
8.1 Noise Performance

Noise performance depends on the device configuration: data rate, input gain, and digital filter mode. Two significant factors affecting noise performance are data rate and input gain. Decreasing the data rate lowers the noise because the measurement bandwidth is reduced. Increasing the gain reduces noise (when noise is treated as an input-referred quantity) because the noise of the PGA is lower than that of the ADC. Noise performance also depends on the digital filter mode. As the digital filter order is increased, the bandwidth decreases, which results in lower noise.

图 8-1 shows noise data versus data rate as input-referred values (μV_{RMS}) in gains 0.125 to 2, (corresponding input ranges of ±20 V to ±1.25 V) in the sinc3 filter mode. 图 8-2 shows noise data versus data rate as input-referred values (μV_{RMS}) in gains 4 to 128, (corresponding input ranges of ±625 mV to ±19.5 mV) in the sinc3 filter mode. The noise data represent typical ADC performance at T_A = 25°C and the 2.5-V reference voltage.

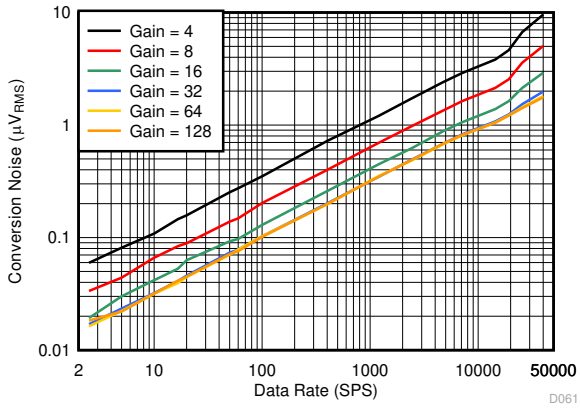
Peak-to-peak noise performance is typically 6.6 times the RMS value. Relative to the noise in the sinc3 filter mode, noise typically increases 30% in the finite-impulse response (FIR) and sinc1 filter mode because of the increased bandwidth of the sinc1 and FIR modes. Noise typically decreases 6% in the sinc4 filter mode because of the decreased bandwidth of the sinc4 filter mode.

The noise data are the standard deviation of the ADC data scaled in microvolts. The data are acquired with inputs shorted and based on consecutive ADC readings for a period of ten seconds or 8192 data points, whichever occurs first. Because of the statistical nature of noise, repeated measurements may yield higher or lower noise results.



Gain = 0.125 to 2, V_{REF} = 2.5 V, sinc3 filter
(sinc5 filter for $f_{DATA} \geqslant$ 14.4 kSPS)

图 8-1. Conversion Noise vs Data Rate



Gain = 4 to 128, V_{REF} = 2.5 V, sinc3 filter
(sinc5 filter for $f_{DATA} \geqslant$ 14.4 kSPS)

图 8-2. Conversion Noise vs Data Rate

ADC noise performance can also be expressed as *effective resolution* and *noise-free resolution* (bits). Effective resolution is based on the RMS value of the noise data and noise-free resolution is based on the peak-to-peak noise data; therefore, the noise-free resolution is the resolution with no code flicker. 方程式 1 is used to compute effective resolution based on the noise values plots of 图 8-1 and 图 8-2.

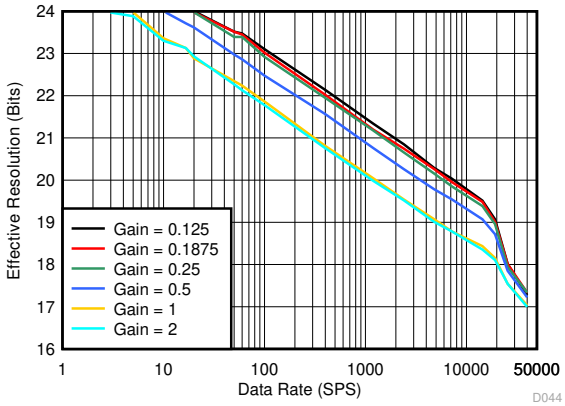
$$\text{Effective Resolution or Noise-Free Resolution (Bits)} = 3.32 \log (\text{FSR} / e_n) \quad (1)$$

where:

- FSR = Full-scale range = 2 V_{REF} / Gain
- e_n = Input-referred noise (RMS value for *effective resolution*, peak-to-peak value for *noise-free resolution*)

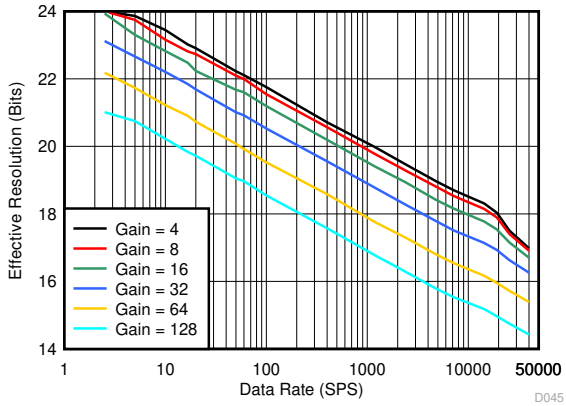
For example, using full-scale range = ±13.3 V, data rate = 20 SPS, and sinc3 filter mode, the RMS noise value (from 图 8-1) is 2.1 μV. The effective resolution is: 3.32 log (26.6 V / 2.1 μV) = 23.6 bits.

图 8-3 and 图 8-4 show effective resolution (bits) versus data rate. 图 8-5 and 图 8-6 show noise-free resolution (bits) versus data rate. When $f_{DATA} \leq$ 14.4 kSPS, effective resolution and noise-free resolution improve by 0.7 bits by increasing the reference voltage from 2.5 V to 4.096 V because of the increased input signal range.



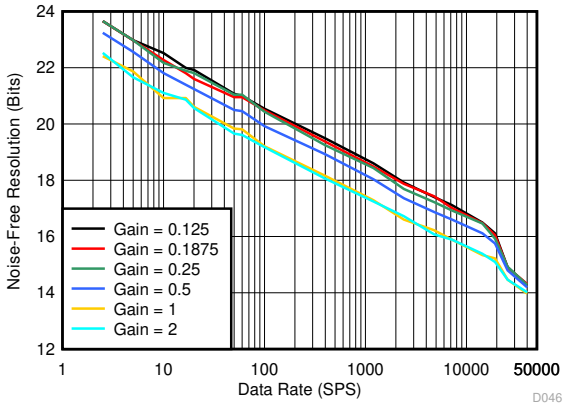
Gain = 0.125 to 2, V_{REF} = 2.5 V, sinc3 filter
(sinc5 filter for $f_{DATA} \geq$ 14.4 kSPS)

图 8-3. Effective Resolution vs Data Rate



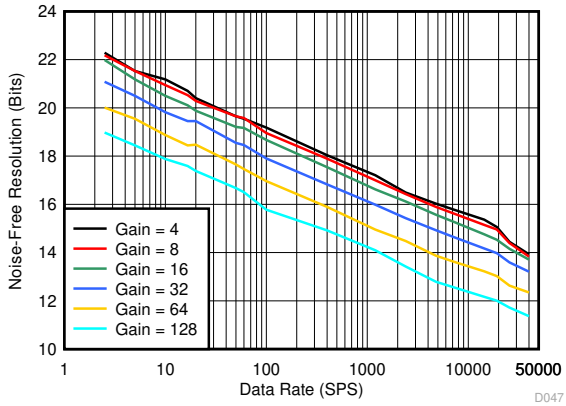
Gain = 4 to 128, V_{REF} = 2.5 V, sinc3 filter mode
(sinc5 filter for $f_{DATA} \geq$ 14.4 kSPS)

图 8-4. Effective Resolution vs Data Rate



Gain = 0.125 to 2, V_{REF} = 2.5 V, sinc3 filter
(sinc5 filter for $f_{DATA} \geq$ 14.4 kSPS)

图 8-5. Noise-Free Resolution vs Data Rate



Gain = 4 to 128, V_{REF} = 2.5 V, sinc3 filter
(sinc5 filter for $f_{DATA} \geq$ 14.4 kSPS)

图 8-6. Noise-Free Resolution vs Data Rate

9 Detailed Description

9.1 Overview

The ADS125H01 is a ±20-V signal input, 40-kSPS, 24-bit, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). The ADC provides a compact one-chip measurement solution for a wide range of input voltages, including typical current and voltage inputs of industrial programmable logic controllers (PLCs), such as ±10-V and 4-mA to 20-mA transmitters (using an external shunt resistor). The ADC provides the resolution necessary for direct interface to low-level sensors such as strain-gauge sensors and thermocouples.

The device features a programmable gain amplifier (PGA) with an attenuation range from 0.125 to 0.5 and a gain range from 1 to 128. The combination of attenuation and gain provide an overall input voltage range of ±20 V to ±20 mV (when V_{REF} = 2.5 V). The PGA is low-noise and low-drift with high input impedance, and includes internal monitors for detection of overload conditions.

In summary, the ADC features:

- 24-bit resolution
- Low-noise, 1-GΩ input impedance PGA
- Selectable attenuation and gain: overall full-scale range from ±20 mV to ±20 V
- Internal or external clock operation
- PGA and voltage reference monitors
- SPI-compatible serial interface with cyclic redundancy check (CRC) error check

Analog inputs (AINP and AINN) connect to the PGA via an input switch. The switch selects between the input signal and an internal test voltage (V_{CM}). Internal diodes protect the analog and reference inputs from ESD events.

The PGA is a high-impedance, differential-input and differential-output amplifier providing both gain and attenuation modes. In attenuation mode, the input voltage is reduced to the range of the ADC. In gain mode, the input voltage is amplified to the range of the ADC. The PGA output connects to the CAPP and CAPN pins. The ADC antialias filter is provided by the combination of the internal PGA output resistors and the external capacitor connected to these pins.

The PGA is monitored for signal overload conditions. Status bits in the STATUS1 register indicate possible PGA overload conditions.

The $\Delta\Sigma$ modulator measures the input voltage relative to the reference voltage to produce a 24-bit conversion result. The input range of the ADC is ±V_{REF} / Gain, where gain is programmable from 0.125 to 128.

The reference voltage is either external (pins REFP, REFN) or the AVDD power supply. The reference input includes a monitor to detect low voltage conditions. The status is reflected in the conversion data STATUS byte.

The digital filter averages and decimates the modulator data to provide the output conversion result. For data rates ≤ 7.2 kSPS, the digital filter provides programmable sinc orders allowing optimization of conversion latency, conversion noise, and line-cycle rejection. The finite-impulse response (FIR) filter mode provides no-latency conversion data with simultaneous rejection of 50-Hz and 60-Hz interference at data rates of 20 SPS or less.

User-programmable offset- and gain-calibration registers correct the conversion data to provide the final conversion result.

The SPI-compatible serial interface is used to read the conversion data and for device configuration. SPI I/O communication is validated by CRC error checking. The serial interface consists of the following signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, and DOUT/$\overline{DRDY}$ (see the *Chip-Select Pins ($\overline{CS1}$ and $\overline{CS2}$)* section for details). The dual-function DOUT/$\overline{DRDY}$ pin combines the functions of the serial data output and data-ready indication into one pin. $\overline{DRDY}$ is the data-ready output signal.

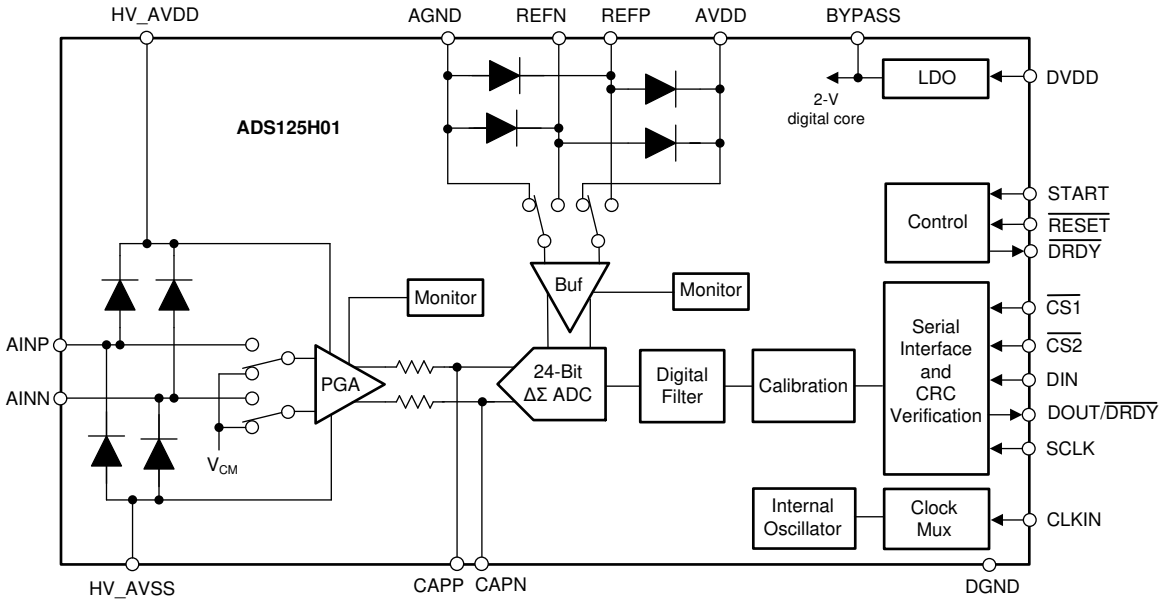
Clock operation is either by the internal oscillator or by an external clock source. The external clock is automatically detected by the ADC. The nominal clock frequency is 7.3728 MHz (10.24 MHz for f_{DATA} = 40 kSPS).

Conversions are controlled by the START pin or by the START command. Conversions are programmable for either continuous or one-shot (pulse) mode of operation.

The ADC is reset at power-on, or manually reset by the $\overline{\text{RESET}}$ input or by the RESET command.

The HV_AVDD and HV_AVSS power supplies allow either bipolar or unipolar configuration (bipolar: ±5 V to ±18 V, unipolar: 10 V to 36 V). The 5-V analog supply (AVDD) powers the ADC. The digital I/Os are powered by DVDD (3-V to 5-V range). An internal 2-V subregulator powers the ADC digital core from the DVDD supply. An external bypass capacitor is required at the subregulator output (BYPASS pin).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Voltage Range

方程式 2 defines the full-scale input voltage range of the ADC. 表 9-1 lists the input voltage range corresponding to the attenuation and gain setting when operating with a 2.5-V reference voltage. The input voltage range is limited under certain operating conditions due to the required headroom of the PGA and the ADC. See the *PGA Operating Range* section for details.

$$\text{Input Voltage Range} = \pm V_{REF} / \text{Gain} \quad (2)$$

表 9-1. Input Voltage Range

GAIN[2:0] BITS(1)	GAIN	INPUT VOLTAGE RANGE	
		DIFFERENTIAL	SINGLE-ENDED
0000	0.125	±20 V	0 V to ±15.5 V
0001	0.1875	±13.3 V	0 V to ±13.3 V
0010	0.25	±10 V	0 V to ±10 V
0011	0.5	±5 V	0 V to ±5 V
0100	1	±2.5 V	0 V to ±2.5 V
0101	2	±1.25 V	0 V to ±1.25 V
0110	4	±0.625 V	0 V to ±0.625 V
0111	8	±0.312 V	0 V to ±0.312 V
1000	16	±0.156 V	0 V to ±0.156 V
1001	32	±0.0781 V	0 V to ±0.0781 V
1010	64	±0.0391 V	0 V to ±0.0391 V
1011	128	±0.0195 V	0 V to ±0.0195 V

(1) Reference voltage = 2.5 V and HV power supply = ±18 V.

9.3.2 Analog Inputs (AINP, AINN)

9.3.2.1 ESD Diodes

ESD diodes are used to protect the ADC inputs from possible ESD events occurring during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. For system-level ESD protection, consider the use of external ESD protection devices for pins that are exposed to possible ESD, including the analog inputs.

If an analog input is driven below HV_AVSS – 0.3 V, or above HV_AVDD + 0.3 V, the internal ESD protection diodes can conduct. If this condition is possible, current can flow through the inputs and flow out from the HV_AVDD or HV_AVSS pins. Use external clamp diodes, series resistors, or both to limit the input current to the specified value.

9.3.2.2 Input Switch

The input switch selects between an internal test voltage and the external input signal. The internal test voltage (V_{CM}) is the mid-point of the HV_AVDD and HV_AVSS power-supply voltage. The internal voltage is used to verify the offset and noise of the ADC measurement path. The input switch is programmed by the MUX[2:0] bits of the MODE4 register (address = 10h). 表 9-2 lists the input switch settings.

表 9-2. Input Switch Settings

MUX[2:0] BITS OF REGISTER MODE4 (10h)	INPUT SELECTION
000	AINP to AINN
101	V_{CM}: (HV_AVDD + HV_AVSS) / 2 (default)

9.3.3 Programmable Gain Amplifier (PGA)

The PGA is a low-noise, programmable gain (attenuation), CMOS differential-input, differential-output amplifier. The PGA operates in gain or attenuation mode depending on the selected gain. Typically, the PGA is programmed for gain when the expected input signal voltage is $\leqslant V_{REF}$ and is programmed for attenuation when the expected input signal voltage is $\geqslant V_{REF}$.

图 9-1 shows the block diagram of the PGA.

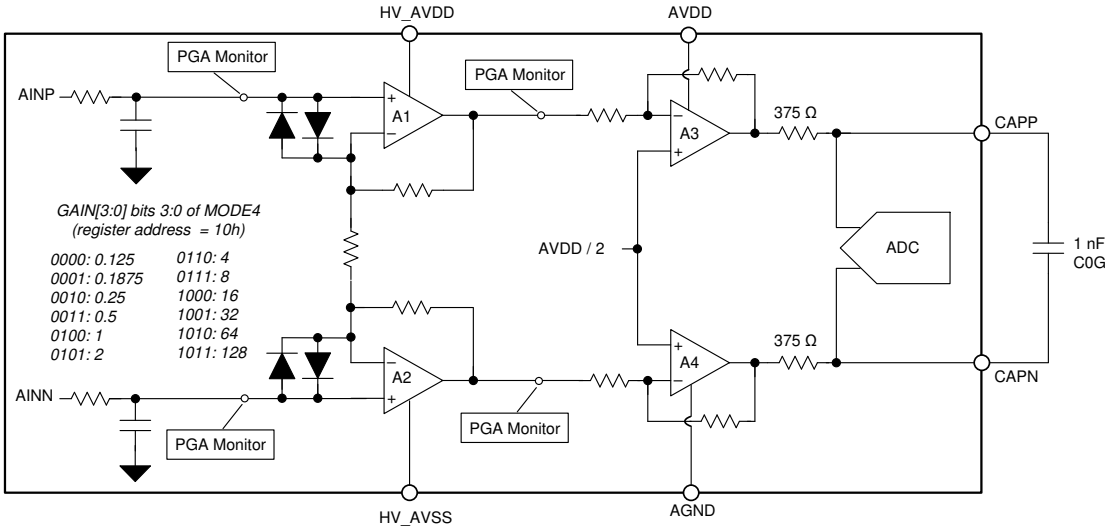


图 9-1. PGA Block Diagram

The signal inputs are RC filtered to reduce sensitivity to radio frequency interference (RFI) and electromagnetic interference (EMI). The first PGA stage is a high input-impedance, noninverting differential amplifier (amplifiers A1 and A2) and provides gain. Inverse-parallel connected diodes across the inputs of A1 and A2 clamp the amplifier input voltage if they are driven out-of-range. If the amplifier is out-of-range, the diodes can conduct, resulting in current flow through the analog input pins. High dV/dt input signals, such as those generated from the switching of a multiplexer, can lead to transient turn-on of the clamp diodes. In some cases, an RC filter at the PGA inputs may be necessary to limit the dV/dt of the signal to prevent the clamp diodes from turning on.

The second stage (amplifiers A3 and A4) is an inverting, differential amplifier. This stage provides attenuation of high-amplitude signal levels. The common-mode voltage of this stage is AVDD / 2. The second stage drives the modulator input of the ADC and is also connected to the CAPP and CAPN pins. An external 1-nF capacitor filters the modulator input sample pulses and also provides the antialias filter for the ADC. Place the capacitor close to the pins using short, direct traces. Avoid running clock traces or other digital traces underneath or in the vicinity of these pins. Gain is programmed by the GAIN[3:0] bits of the MODE 4 register.

Monitors verify the voltage headroom of the PGA input and output nodes. See the *PGA Monitors* section for details.

9.3.3.1 PGA Operating Range

The *absolute input voltage* range of the PGA must not be exceeded in order to maintain linear operation. The maximum and minimum absolute input voltage is determined by the PGA gain setting, the maximum differential input voltage (V_{IN}), and the minimum value of the high-voltage power supply. The absolute voltage is the combined differential and common-mode voltages. Maintain the absolute input voltage (V_{AINx}) within the range as shown in 方程式 3, otherwise incorrect conversion data can result.

$$HV\_AVSS + 2.5\ V + V_{IN} \times (Gain - 1) / 2 < V_{(AINx)} < HV\_AVDD - 2.5\ V - V_{IN} \times (Gain - 1) / 2 \quad (3)$$

where:

- Gain = PGA gain. For gain < 1, use value = 1
- $V_{(AINx)}$ = Absolute input voltage
- $V_{IN} = V_{AINP} - V_{AINN}$ = Maximum expected differential input voltage

Additionally, the *differential input signal* is limited in two conditions. The first condition is when the reference voltage exceeds AVDD – 1 V (nominally V_{REF} > 4 V). In this case, the differential input signal is limited to: V_{IN} = ±(AVDD – 1 V) / Gain, instead of the ideal $V_{IN} = \pm V_{REF}$ / Gain. The second condition applies to gains of 0.125 and 0.1875. In this case, the differential input signal range is limited to: V_{IN} = ±20 V, regardless of the reference voltage value.

图 9-2 and 图 9-3 show the relationship between the PGA input voltage and the PGA output voltage. In attenuation mode, the first PGA stage is configured as a unity-gain follower. The second PGA stage attenuates the differential input voltage and shifts the signal common-mode voltage to AVDD / 2 to drive the ADC input.

In gain mode, the first PGA stage amplifies the differential signal. The second PGA stage is configured as a unity-gain follower with level-shift. 图 9-2 and 图 9-3 show the corresponding output voltage of the PGA stages that must have operating voltage headroom.

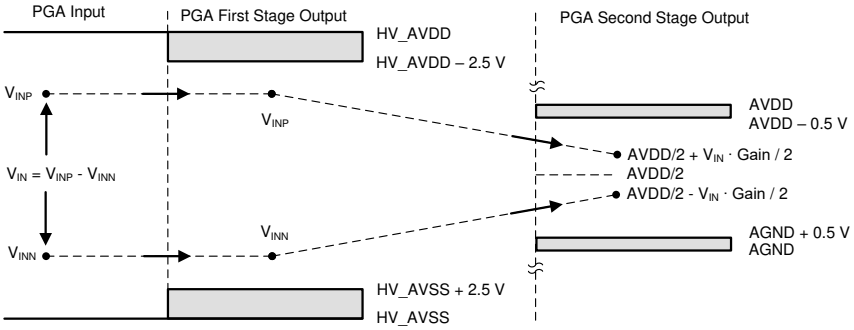


图 9-2. PGA Attenuation Mode

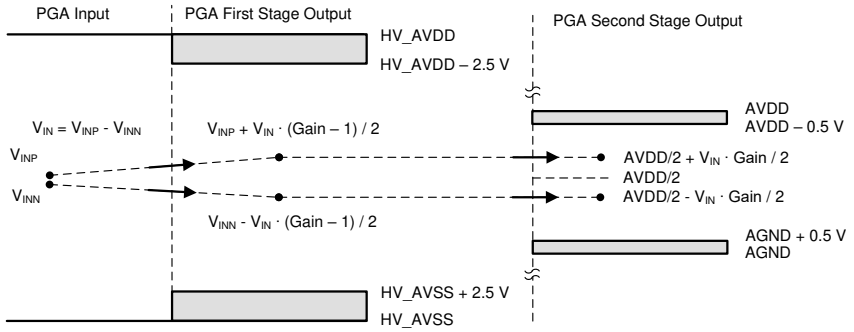


图 9-3. PGA Gain Mode

9.3.3.2 PGA Monitors

The PGA requires operating voltage headroom at the input and output nodes. The operating headroom must be maintained; otherwise the conversion data may not be valid. Use the internal PGA monitors to detect PGA out-of-range conditions. The PGA has four monitors (two monitors for the input and two monitors for the output) with high and low thresholds for each, for a total of eight possible alarms. The status of each PGA monitor is read in the STATUS1 register. The PGA monitoring points are illustrated in 图 9-1. 图 9-4 shows the operation of the high and low thresholds of each of the four PGA monitors.

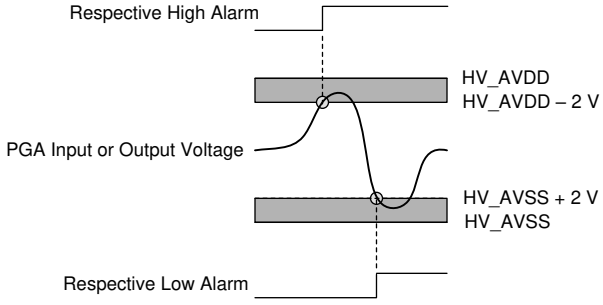


图 9-4. PGA Monitor Thresholds

Detect PGA out-of-range operating conditions by polling the STAT12 bit (bit 4 of the STATUS conversion byte or STATUS0 register). The STAT12 bit is the logical OR of all PGA error flags with the CRC2 error flag. When the STAT12 bit asserts, poll the STATUS1 and STATUS2 registers (address 11h and 12h) to determine the source of the STAT12 error. The PGA out-of-range flags latch in the STATUS1 register and remain latched after the overload condition is removed. Read the STATUS1 register to clear the PGA out-of-range bits (clear-on-read operation). The PGA overload flags *and* the CRC2 flag must be reset in order for the STAT12 bit to clear. See the STATUS1 register for a description of the PGA overload bits.

The PGA monitors are analog comparators that respond to transient out-of-range conditions.

9.3.4 Reference Voltage

A reference voltage is required for operation. An internal reference voltage switch selects between the external reference and the AVDD power supply voltage (default). Program the reference switch using the RMUX[3:0] bits to select the reference (see the REF register for details).

Apply the reference voltage to the REFP and REFN pins. The reference inputs are differential defined by: $V_{REF} = (V_{(REFP)} - V_{(REFN)})$, where $V_{(REFP)}$ and $V_{(REFN)}$ are the positive and negative absolute reference voltages. Follow the specified absolute and differential operating conditions. Use a 10-nF or larger bypass capacitor across the reference input pins to filter noise. The reference input current can lead to a voltage error if large reference impedances are present. If a reference impedance is present, the reference voltage may have an error.

9.3.4.1 Reference Monitor

The reference monitor detects a low or missing reference voltage. As illustrated in 图 9-5, when the differential reference voltage is ≤ 0.4 V (typical), the REFALM bit is set in the STATUS0 register. The alarm is read-only and resets at the next conversion after the fault condition is cleared. To implement the reference monitor, place a 100-kΩ resistor across the reference inputs. If either positive or negative reference inputs become disconnected, the reference inputs are differentially biased to 0 V, thereby triggering the low reference alarm. Poll bit 3 (REFALM) of the STATUS0 register to determine if the reference alarm has triggered.

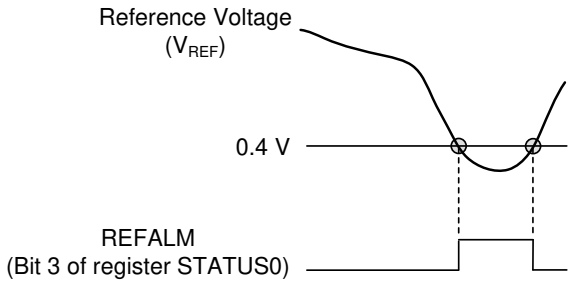


图 9-5. Reference Monitor Operation

9.3.5 ADC Modulator

The modulator is an inherently stable, fourth-order, 2 + 2 pipelined $\Delta\Sigma$ modulator. The modulator samples the analog input voltage at a high sample rate (f_{MOD} = f_{CLK} / 8) and converts the analog input to a 1's-density bit stream that is processed by the digital filter.

9.3.6 Digital Filter

The digital filter has two operating modes, as shown in 图 9-6: sin(x) / x (sinc) mode and finite impulse response (FIR) mode. The sinc mode provides data rates of 2.5 SPS to 40 kSPS, and selectable sinc1, sinc3, and sinc4 filter orders for $f_{DATA} \leqslant$ 7.2 kSPS. The FIR filter provides single-cycle settled conversions and simultaneous rejection of 50-Hz and 60-Hz signal interference frequencies with data rates of 2.5 SPS to 20 SPS.

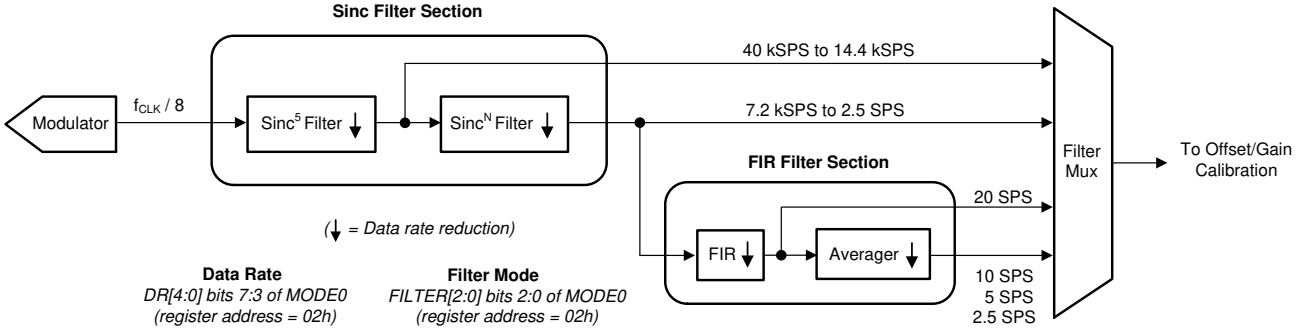


图 9-6. Digital Filter Block Diagram

9.3.6.1 Sinc Filter Mode

The sinc filter consists of a variable-decimation sinc5 filter followed by a variable-decimation, variable-order sinc filter. The sinc5 filter averages and down-samples the modulator data (f_{CLK} / 8) to provide 40 kSPS, 25.6 kSPS, 19.2 kSPS, and 14.4 kSPS data rates by using decimation ratios of 32, 36, 48, and 64. These data rates bypass the second filter stage and as a result are sinc5 output only. The second stage receives data at 14.4 kSPS and performs additional filtering and decimation to provide data rates of 7.2 kSPS to 2.5 SPS. The second stage has programmable sinc order. The data rate is programmed by the DR[4:0] bits and the filter mode is programmed by the FILTER[2:0] bits of the MODE0 register.

9.3.6.1.1 Sinc Filter Frequency Response

As shown in 图 9-7 and 图 9-8, the first-stage sinc5 filter has frequency response nulls occurring at N × f_{DATA} (where N = 1, 2, 3, and so on). At the null frequencies, the filter has zero gain.

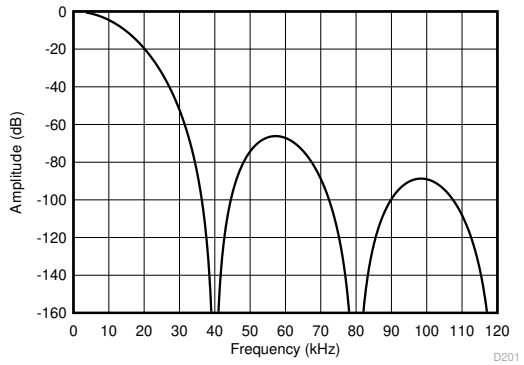


图 9-7. Sinc5 Filter Frequency Response (40 kSPS)

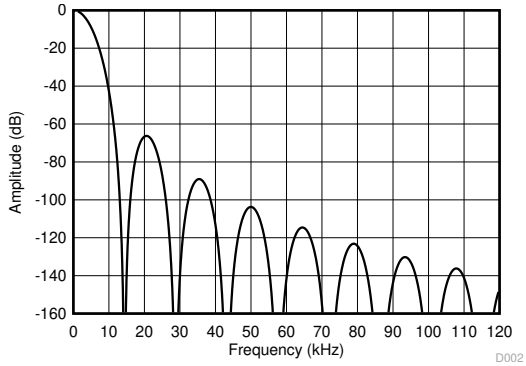


图 9-8. Sinc5 Filter Frequency Response (14.4 kSPS)

The second stage filter superimposes additional nulls to the nulls produced by the first stage. The first of the nulls occurs at the output data rate with additional nulls occurring at data rate multiples.

图 9-9 shows the frequency response at 2.4 kSPS. This data rate has five equally spaced nulls between the first stage 14.4-kHz nulls [(14.4 kHz / 2.4 kHz) – 1 = 5]. This frequency response is similar to that of data rates 2.5 SPS to 7.2 kSPS. 图 9-10 shows the frequency response nulls at 10 SPS.

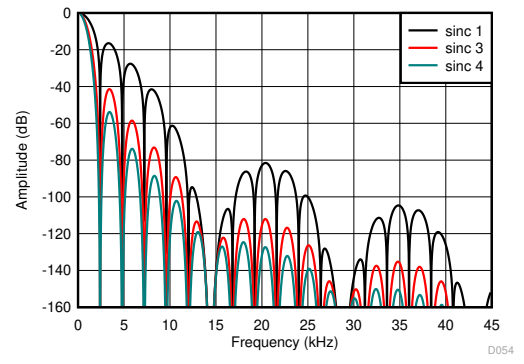


图 9-9. Sinc Filter Frequency Response (2400 SPS)

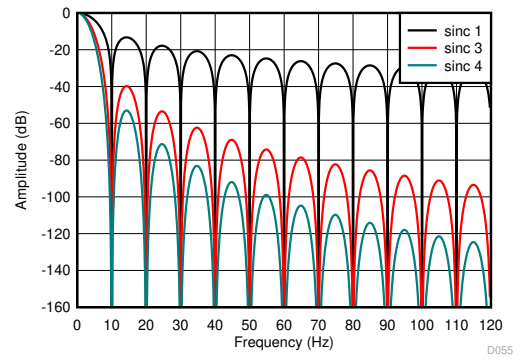


图 9-10. Sinc Filter Frequency Response (10 SPS)

图 9-11 and 图 9-12 show the frequency response of data rates 50 SPS and 60 SPS. 50-Hz or 60-Hz rejection is increased by increasing the order of the sinc filter.

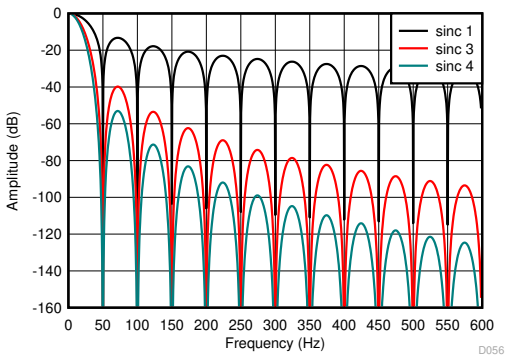


图 9-11. Sinc Filter Frequency Response (50 SPS)

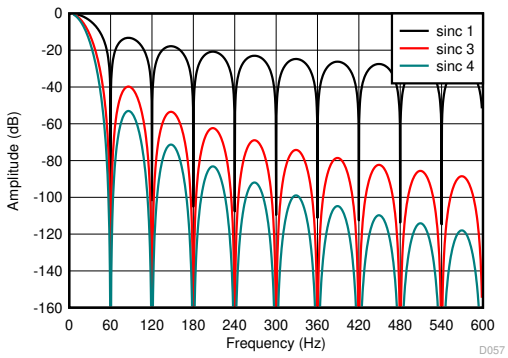


图 9-12. Sinc Filter Frequency Response (60 SPS)

图 9-13 and 图 9-14 show the detailed frequency response of the 50-SPS and 60-SPS data rates.

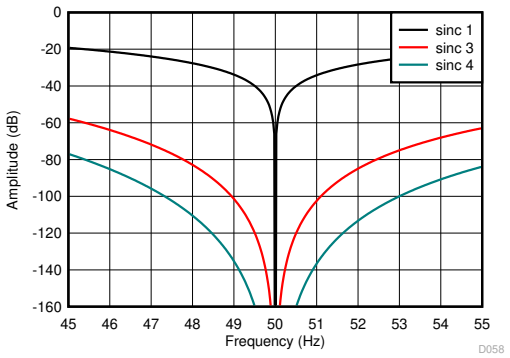


图 9-13. Sinc Filter Frequency Response (50 SPS)

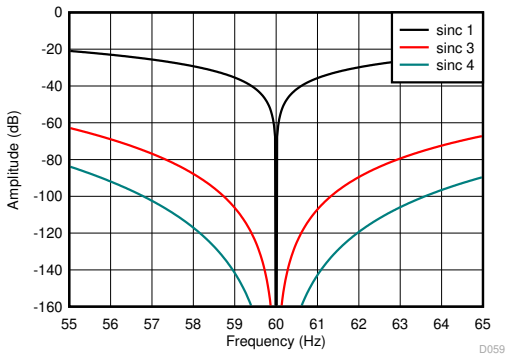


图 9-14. Sinc Filter Frequency Response (60 SPS)

The sinc filter has an overall low-pass response that rolls off high-frequency components of the signal. The filter bandwidth depends on the output data rate and the filter order. The *system* bandwidth is the combined bandwidths of the digital filter, the PGA antialias filter, and external signal filters. 表 9-3 lists the –3-dB bandwidth of the sinc filter.

表 9-3. Sinc Filter Bandwidth

–3-dB BANDWIDTH (Hz)				
DATA RATE (SPS)	SINC1	SINC3	SINC4	SINC5
2.5	1.10	0.65	0.58	—
5	2.23	1.33	1.15	—
10	4.43	2.62	2.28	—
16.6	7.38	4.37	3.80	—
20	8.85	5.25	4.63	—
50	22.1	13.1	11.4	—
60	26.6	15.7	13.7	—
100	44.3	26.2	22.8	—
400	177	105	91.0	—
1200	525	314	273	—
2400	1015	623	544	—
4800	1798	1214	1077	—
7200	2310	1750	1590	—
14400	—	—	—	2940
19200	—	—	—	3920
25600	—	—	—	5227
40000	—	—	—	8167

9.3.6.2 FIR Filter

The finite impulse response (FIR) filter provides simultaneous rejection of 50-Hz and 60-Hz line cycle frequencies and related harmonics at data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS. The conversion latency of the FIR filter is a single cycle; see 表 9-6 for detailed latency values. As illustrated in 图 9-6, the FIR filter section receives data from the second-stage sinc filter. The FIR filter section decimates the data to yield the output data rate of 20 SPS. A variable averaging filter (sinc1) yields 10 SPS, 5 SPS, and 2.5 SPS.

As shown in 图 9-15 and 图 9-16, the frequency response has nulls that are positioned near 50 Hz and 60 Hz.

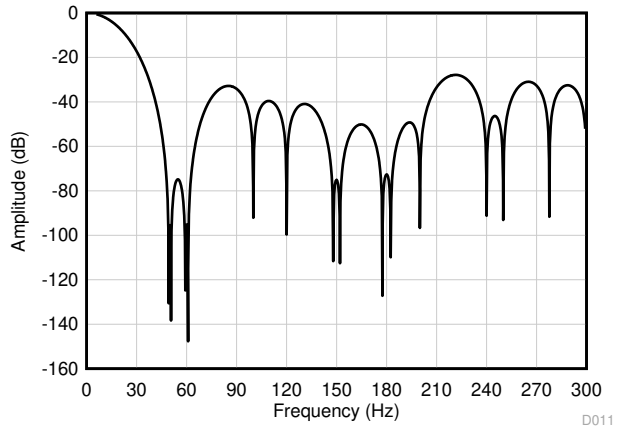


图 9-15. FIR Filter Frequency Response (20 SPS)

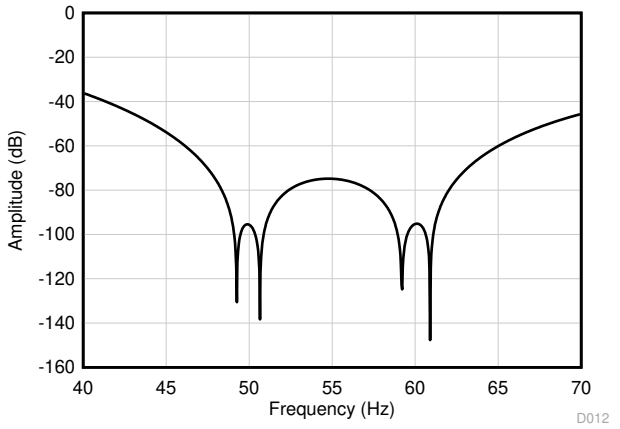


图 9-16. FIR Filter Frequency Response Detail (20 SPS)

Similar to the response of the sinc filter, the overall FIR filter frequency has a low-pass response that rolls off high frequencies. The signal bandwidth depends on the output data rate. 表 9-4 lists the –3-dB filter bandwidth of the FIR filter. The total system bandwidth is the combined response of the digital filter, the PGA antialias filter, and external filters.

表 9-4. FIR Filter Bandwidth

DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)
2.5	1.2
5	2.4
10	4.7
20	13

9.3.6.3 50-Hz and 60-Hz Normal-Mode Rejection

To reduce the effects of 50-Hz and 60-Hz interference, optimize the filter mode and data rate selection, and the accuracy of the ADC clock to provide the required 50-Hz and 60-Hz rejection. 表 9-5 summarizes the 50-Hz and 60-Hz noise rejection versus filter mode and data rate. The table values are based on a 2% and 6% tolerance of the 50-Hz and 60-Hz input frequencies relative to the ADC clock frequency. Common-mode noise is also rejected at 50 Hz and 60 Hz.

表 9-5. 50-Hz and 60-Hz Normal-Mode Rejection

DIGITAL FILTER AMPLITUDE (dB)					
DATA RATE (SPS)	FILTER TYPE	50 Hz (±2%)	50 Hz (±6%)	60 Hz (±2%)	60 Hz (±6%)
2.5	FIR	– 113	– 88	– 99	– 80
2.5	Sinc1	– 36	– 40	– 37	– 37
2.5	Sinc3	– 108	– 120	– 111	– 111
2.5	Sinc4	– 144	– 160	– 148	– 148
5	FIR	– 111	– 77	– 95	– 76
5	Sinc1	– 34	– 30	– 34	– 30
5	Sinc3	– 102	– 90	– 102	– 90
5	Sinc4	– 136	– 120	– 136	– 120
10	FIR	– 111	– 73	– 94	– 68
10	Sinc1	– 34	– 25	– 34	– 25
10	Sinc3	– 102	– 75	– 102	– 75
10	Sinc4	– 136	– 100	– 136	– 100
16.6	Sinc1	– 34	– 24	– 21	– 21
16.6	Sinc3	– 102	– 72	– 63	– 63
16.6	Sinc4	– 136	– 96	– 84	– 84
20	FIR	– 95	– 66	– 94	– 66
20	Sinc1	– 18	– 18	– 34	– 24
20	Sinc3	– 54	– 54	– 102	– 72
20	Sinc4	– 72	– 72	– 136	– 96
50	Sinc1	– 34	– 24	– 15	– 15
50	Sinc3	– 102	– 72	– 45	– 45
50	Sinc4	– 136	– 96	– 60	– 60
60	Sinc1	– 13	– 12	– 34	– 24
60	Sinc3	– 40	– 36	– 102	– 72
60	Sinc4	– 53	– 48	– 136	– 96

9.4 Device Functional Modes

9.4.1 Conversion Control

The START pin or the START command controls the conversions. If using commands to control conversions, keep the START pin low to avoid contention between pin control and command control. Commands take effect on the 32nd falling SCLK edge. See the *Switching Characteristics* table for details on conversion-control timing.

The ADC has two conversion-control operating modes: continuous-conversion mode and pulse-conversion mode. The continuous-conversion mode performs conversions indefinitely until conversions are stopped. Pulse-conversion mode performs one conversion and then stops. The CONVRT (bit 4 of the MODE1 register) programs the conversion mode.

9.4.1.1 Continuous-Conversion Mode

This conversion mode performs continuous conversions until the conversion process is stopped. To start conversions, take the START pin high or send the START command. $\overline{\text{DRDY}}$ is driven high when the conversion is started. $\overline{\text{DRDY}}$ is driven low when the conversion data are ready. Conversion data are available to read at that time. Take the START pin low or send a STOP command to stop conversions. When conversions are stopped, any conversion in progress runs to completion. To restart a conversion that is in progress, toggle the START pin low-then-high or send a new START command.

9.4.1.2 Pulse-Conversion Mode

In pulse-conversion mode, the ADC performs one conversion when the START pin is taken high or when the START command is sent. When the conversion completes, further conversions stop automatically. The $\overline{\text{DRDY}}$ output is driven high to indicate the conversion is actively in progress and is driven low when the conversion data are ready. Conversion data are available to read at that time. To restart a conversion in progress, toggle the START pin low-then-high or send a new START command. Driving START low or sending the STOP command does not interrupt the current conversion.

9.4.1.3 Conversion Latency

The digital filter averages data from the modulator to produce the conversion result. The internal stages of the digital filter must be settled to provide fully settled output data. The order and the decimation ratio of the digital filter determine the amount of data averaged that, in turn, affects the latency of the conversion result. The FIR and sinc1 filter modes are zero latency because the ADC provides the conversion result in one conversion cycle. Latency time is an important consideration for overall data throughput in multiplexed applications.

表 9-6 lists the conversion latency values of the ADC. Conversion latency is defined as the time from the start of the first conversion by taking the START pin high or sending the START command to the time of the first conversion data. The ADC is designed to provide fully settled data under this condition. The conversion latency values listed in 表 9-6 include the programmable start-conversion delay that delays the digital filter start. After the first conversion in continuous-conversion mode, the periods of the following conversions are equal to 1 / f_{DATA}.

表 9-6. Conversion Latency Time

DATA RATE (SPS)	CONVERSION LATENCY TIME ($t_{(STDR)}$ (1), ms)				
	SINC1	SINC3	SINC4	SINC5	FIR
2.5	400.4	1,200	1,600	—	402.2
5	200.4	600.4	800.4	—	202.2
10	100.4	300.4	400.4	—	102.2
16.6	60.43	180.4	240.4	—	—
20	50.43	150.4	200.4	—	52.22
50	20.43	60.43	80.43	—	—
60	17.09	50.43	67.09	—	—
100	10.43	30.43	40.43	—	—
400	2.925	7.925	10.43	—	—
1200	1.258	2.925	3.758	—	—
2400	0.841	1.675	2.091	—	—
4800	0.633	1.050	1.258	—	—
7200	0.564	0.841	0.980	—	—
14400	—	—	—	0.423	—
19200	—	—	—	0.336	—
25600	—	—	—	0.271	—
40000	—	—	—	0.179	—

(1) Conversion-start time delay = 50 µs (36 µs at f_{CLK} = 10.24 MHz) using DELAY[3:0] = 0001). Conversion latency scales with f_{CLK}.

As shown in 图 9-17, if the input-step change occurs during an active conversion, the conversion data are a mix of old and new data. After an input-step change, the number of conversion periods required to provide fully settled output data are determined dividing the conversion latency time by the conversion period plus one additional conversion period.

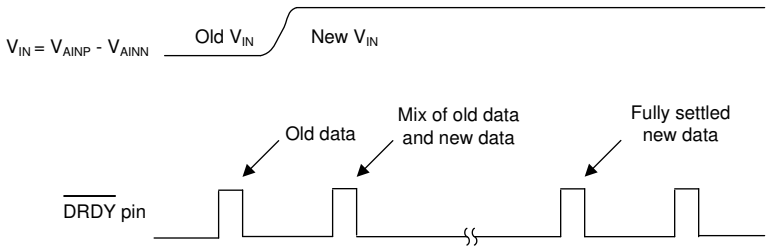


图 9-17. Input Change During Conversions

9.4.1.4 Start-Conversion Delay

At the start of a conversion, the ADC provides a programmable delay time to allow for PGA settling and to provide a delay time for the possible effects of settling of external components (such as multiplexers and R-C filters). The default value is 50 µs (f_{CLK} = 7.3728 MHz) to provide settling time for the PGA antialiasing filter after an input step change. Use additional delay time as needed to provide settling time for the settling effects of external components. As an alternative to this parameter, delay the start of conversion manually after an input change. See 表 9-27 for start-conversion delay values.

9.4.2 Clock Mode

The ADC is operated with an external clock or with the internal oscillator. For external clock operation, apply the clock signal to the CLKIN pin. The ADC detects the presence of the external clock and selects the clock automatically. Read the CLOCK bit in the STATUS0 register to verify the clock mode. As described in 表 9-7, the clock frequency depends on the data rate used. Be sure the external clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot.

To operate the ADC by the internal oscillator, connect CLKIN to DGND. Be aware of the accuracy of the internal oscillator as described in the *Electrical Characteristics*. The internal oscillator begins operating immediately at device power-on.

表 9-7. External Clock Frequency

CLOCK FREQUENCY	DATA RATE
7.3728 MHz	2.5 SPS – 25.6 kSPS
10.24 MHz	40 kSPS

9.4.3 Reset

The ADC is reset in three ways: automatic at power-on, manually via the $\overline{\text{RESET}}$ pin, or manually by the RESET command.

At reset, the serial interface, conversion-control logic, digital filter, and register map values are reset. The RESET bit of the STATUS0 register is set after a reset occurs. Clear the bit to detect the next device reset. If the START pin is high after reset, the ADC immediately begins conversions after reset.

9.4.3.1 Power-On Reset

After the supply voltages cross the respective reset thresholds at power-up, the ADC is reset and after 2^{16} f_{CLK} cycles the ADC is ready for communication. Until this time, $\overline{\text{DRDY}}$ is held low. $\overline{\text{DRDY}}$ is then driven high to indicate when ADC communication can begin. The conversion cycle starts 512 f_{CLK} cycles after $\overline{\text{DRDY}}$ asserts high if START is high. See 图 7-4 for power-on reset behavior.

9.4.3.2 Reset by $\overline{\text{RESET}}$ Pin

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low for a minimum of four f_{CLK} cycles, and then return the pin high. After reset, the conversion starts 512 f_{CLK} cycles later if START is high. See 图 7-5 for $\overline{\text{RESET}}$ pin timing requirements.

9.4.3.3 Reset by Command

Reset the ADC through the serial interface by the RESET command. Bring $\overline{\text{CS1}}$ high-then-low to first reset the serial interface, ensuring the ADC is ready for the RESET command. After reset, the conversion starts 512 f_{CLK} cycles later if START is high. See 图 7-5 for RESET command timing.

9.4.4 Calibration

The ADC incorporates calibration registers to calibrate offset and full-scale errors. Calibrate the ADC by using calibration commands, or calibrate by writing to the calibration registers directly (user calibration). To calibrate by command, send the offset or full-scale calibration commands. To user calibrate, write to the calibration registers with values based on the acquired conversion data. Perform the offset calibration operation before the full-scale calibration operation.

9.4.4.1 Offset and Full-Scale Calibration

Use the offset and full-scale (gain) registers to correct offset or full-scale errors, respectively. As illustrated in 图 9-18, the offset calibration register is subtracted from the output data before multiplication by the full-scale register, which is divided by 400000h. After the calibration operation, the final value of the output data is clipped to 24 bits.

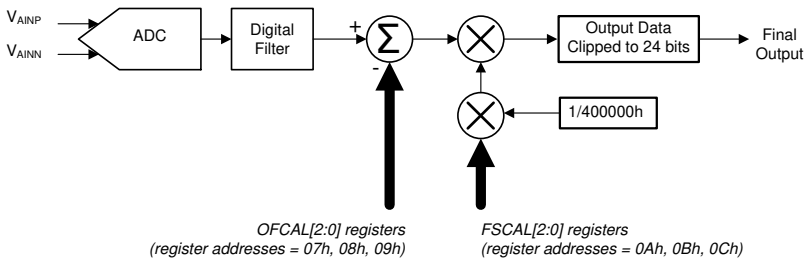


图 9-18. Calibration Block Diagram

方程式 4 shows the internal calibration.

$$\text{Final Output Data} = (\text{Pre Data} - \text{OFCAL[2:0]}) \times \text{FSCAL[2:0]} / 400000h \quad (4)$$

9.4.4.1.1 Offset Calibration Registers

The offset calibration word is 24 bits consisting of three 8-bit registers. The offset value is subtracted from the conversion result. The offset value is two's-complement format with a maximum positive value equal to 7FFFFFh and a maximum negative value equal to 800000h. A register value equal to 000000h has no offset correction. Although the calibration registers provide a wide offset value range, the input signal cannot exceed ±106% of the precalibrated range; otherwise the ADC is overranged. 表 9-8 lists example values of the offset register.

表 9-8. Offset Calibration Register Values

OFCAL[2:0] REGISTER VALUE	CALIBRATED OUTPUT VALUE(1)
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h

(1) V_{IN} = 0 V, ideal ADC with no offset error or noise.

9.4.4.1.2 Full-Scale Calibration Registers

The full-scale calibration word is 24 bits consisting of three 8-bit registers. The full-scale calibration value is straight binary and normalized to unity-gain at value = 400000h. 表 9-9 lists register values for selected gain factors. Gain errors greater than unity are corrected by full-scale values less than 400000h. Although the calibration registers provide a wide range of possible values, the input signal must not exceed ±106% of the precalibrated input range; otherwise the ADC is overranged.

表 9-9. Full-Scale Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
433333h	1.05
400000h	1
3CCCCCh	0.95

9.4.4.2 Offset Calibration Command (OFSCAL)

The offset calibration command corrects offset errors. To calibrate offset errors, short the inputs to the ADC or to calibrate the system, short the signal inputs to the system. When the command is sent, the ADC averages 16 conversion results to reduce conversion noise for improved calibration accuracy. When calibration is complete, the ADC performs one conversion using the new calibration value. The new calibration value is written to the offset calibration register.

9.4.4.3 Full-Scale Calibration Command (GANCAL)

The full-scale calibration command corrects gain errors. To calibrate, apply a positive calibration voltage to the ADC, or apply the voltage to the signal inputs of the system, wait for the signal to settle, and then send the command. The ADC averages 16 conversion results to reduce conversion noise to improve calibration accuracy. The ADC computes the full-scale calibration value so that the applied calibration voltage is scaled to an equal

positive full-scale output code. The computed result is written to the calibration register. The ADC then performs one new conversion using the new calibration value.

9.4.4.4 Calibration Command Procedure

Use the following calibration procedure using the calibration commands. When calibrating at power-on, make sure the reference voltage has stabilized. Perform an offset calibration operation prior to full-scale calibration.

1. Set the ADC configurations as required.
2. Apply the appropriate calibration signal (zero or full-scale) to the ADC or to the system inputs.
3. Take the START pin high or send the START command to start conversions. $\overline{\text{DRDY}}$ is driven high.
4. Before the first conversion completes, send the appropriate calibration command. Keep $\overline{\text{CS}}$ low until $\overline{\text{DRDY}}$ is driven low (calibration complete); otherwise the command is cancelled. Do not send other commands during the calibration period.
5. $\overline{\text{DRDY}}$ is driven low when calibration is complete. The calibration time, as described in 表 9-10, depends on the data rate and digital filter mode. The calibration registers are updated with new values. New conversion data are available immediately using the new calibration value.

表 9-10. Calibration Time (ms)

DATA RATE (SPS)(1)	FILTER MODE				
	SINC1	SINC3	SINC4	SINC5	FIR
2.5	6801	8401	9201	—	6805
5	3401	4201	4601	—	3405
10	1701	2101	2300	—	1705
16.6	1021	1261	1381	—	—
20	850.9	1051	1151	—	854.5
50	340.9	421	460.9	—	—
60	284.2	350.9	384.2	—	—
100	170.9	210.9	230.9	—	—
400	43.36	53.36	58.36	—	—
1200	15.02	18.36	20.02	—	—
2400	7.938	9.605	10.44	—	—
4800	4.397	5.230	5.647	—	—
7200	3.216	3.772	4.050	—	—
14400	—	—	—	1.892	—
19200	—	—	—	1.458	—
25600	—	—	—	1.133	—
40000	—	—	—	0.738	—

(1) Actual calibration time can vary depending on the accuracy of f_{CLK}.

9.4.4.5 User Calibration Procedure

To user calibrate, apply the calibration voltage, acquire conversion data, and compute the calibration value. Write the computed value to the corresponding calibration registers. Before starting calibration, preset the offset and full-scale registers to 000000h and 400000h, respectively.

To offset calibrate, short the inputs to the system and average *n* number of the conversion data. Averaging conversion data reduces noise to increase calibration accuracy. Write the average value of the conversion data to the offset registers.

To gain calibrate using a full-scale calibration signal, temporarily reduce the full-scale register by 95% to avoid any output clipped codes (set FSCAL[2:0] to 3CCCCCh). Acquire *n* number of conversions and average the conversions to increase calibration accuracy. 方程式 5 describes how to compute the full-scale calibration value:

$$\text{Full-Scale Calibration Value} = (\text{Expected Code} / \text{Actual Code}) \times 400000\text{h} \quad (5)$$

where:

- Expected code = 799998h using full-scale calibration signal and 95% precalibration scale factor

9.5 Programming

9.5.1 Serial Interface

The SPI-compatible serial interface is used to read conversion data, configure the device registers, and control ADC operation. The CRC is used to validate error-free transmission of the input and output data flow. The serial interface consists of the following control signals: $\overline{CS}$ $\overline{1}$, $\overline{CS2}$, SCLK, DIN, and DOUT/ $\overline{DRDY}$. Most microcontroller SPI peripherals can operate with the ADC. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated or changed on the SCLK rising edges; data are latched or read on the SCLK falling edges. Timing details of the SPI protocol are provided in 图 7-1 and 图 7-2.

9.5.1.1 Chip-Select Pins ($\overline{CS1}$ and $\overline{CS2}$)

The ADC consists of discrete PGA and ADC sections with each section selected for communication by separate chip-select inputs ($\overline{CS1}$ and $\overline{CS2}$). Most commands require the use of $\overline{CS1}$ to control the ADC section. However, for control of the PGA section, use $\overline{CS2}$ for register access commands at address 10h and above. Communicate to the device by taking either $\overline{CS1}$ or $\overline{CS2}$ low corresponding to the type of command and whether addressing the ADC or PGA registers.

$\overline{CS1}$ and $\overline{CS2}$ are active low inputs. In normal operation, take one chip-select input low at a time and keep that input low for the duration of the command operation. Take the chip-select input high after the command operation completes. When the chip-select input is taken high, the serial interface resets and SCLK activity is ignored (thus blocking commands). When both chip-select inputs are high, DOUT/$\overline{DRDY}$ enters a high-impedance state. $\overline{CS1}$ must be low in order to poll the data-ready function provided by DOUT/$\overline{DRDY}$. The $\overline{DRDY}$ pin remains active regardless of the state of the chip-select inputs.

9.5.1.2 Serial Clock (SCLK)

SCLK is the serial interface shift clock input that clocks data into and out of the device. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge of SCLK. Return SCLK low after the data operation completes. SCLK is a Schmidt-triggered input designed to provide noise immunity. Even though SCLK is noise resistant, keep SCLK noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. Use a series termination resistor at the SCLK drive pin to reduce ringing.

9.5.1.3 Data Input (DIN)

DIN is the serial interface data input. DIN inputs commands and register data to the device. Input data are latched on the falling edge of SCLK.

9.5.1.4 Data Output/Data Ready (DOUT/$\overline{DRDY}$)

The DOUT/$\overline{DRDY}$ pin is the serial interface data output. This pin also provides the conversion-data ready output. The function of the pin changes whether a read data (or read register) operation is in progress. With $\overline{CS1}$ low and when not reading register or conversion data, the pin indicates when data are ready by asserting low. For conversion data and register read operations, the pin function changes to data output. When the read operation is completed, the function changes back to the data-ready signal. In the data output mode, data are updated on the SCLK rising edge and the data is therefore latched by the host on the SCLK falling edge. $\overline{CS1}$ must be low for DOUT/$\overline{DRDY}$ to provide the data-ready function. When both chip-select pins are high, DOUT/$\overline{DRDY}$ is in high-impedance mode (tri-state).

9.5.2 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ asserts low to indicate that new conversion data are ready for readback. The operation of $\overline{DRDY}$ depends on the conversion mode (continuous or pulse) and whether or not the conversion data are retrieved. The $\overline{DRDY}$ output remains functional regardless of the state of the chip-select inputs.

9.5.2.1 $\overline{DRDY}$ in Continuous-Conversion Mode

In continuous-conversion mode, $\overline{DRDY}$ is driven high when a conversion is started and is driven low when conversion data are ready. During data readback, $\overline{DRDY}$ is driven high, which indicates completion of the read

operation. If the conversion data are not read, $\overline{DRDY}$ remains low then pulses high 16 f_{CLK} cycles prior to the next falling edge.

To read back the current conversion data before the next conversion completes, send the read data command at least 16 f_{CLK} cycles prior to the $\overline{DRDY}$ falling edge. If the readback command is sent *less than* 16 f_{CLK} cycles prior to the $\overline{DRDY}$ falling edge, *either* the previous or new conversion data are provided. The timing of the command determines whether previous or new data are provided. In the event that previous data are provided, $\overline{DRDY}$ transitioning to low is temporarily suspended until after the read data operation completes. In this case, the DRDY bit of the STATUS0 byte is low to indicate that the previous data have already been read. In the event that new conversion data are provided, $\overline{DRDY}$ transitions low as normal. The DRDY bit of the STATUS0 byte is high to indicate the conversion data are new. To ensure readback of new conversion data, wait until $\overline{DRDY}$ asserts low before starting the data read operation.

9.5.2.2 $\overline{DRDY}$ in Pulse-Conversion Mode

$\overline{DRDY}$ is driven high at conversion start and is driven low when the conversion data are ready. $\overline{DRDY}$ remains low until a new conversion is started.

图 9-19 shows the $\overline{DRDY}$ operation with and without data retrieval in pulse- and continuous-conversion modes.

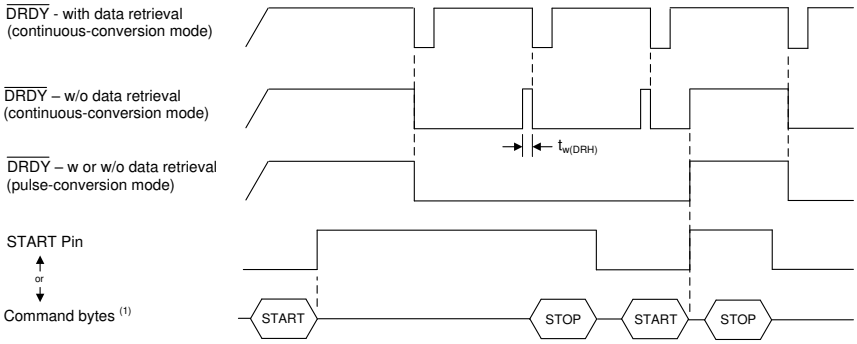


图 9-19. $\overline{DRDY}$ Operation

9.5.2.3 Data Ready by Software Polling

As an option to polling the $\overline{DRDY}$ pin or the DOUT/$\overline{DRDY}$ pin, poll the DRDY bit in the STATUS byte (sent with the conversion data) or the STATUS0 register byte. If the bit is high, the conversion data are new from the last data read operation. If the bit is low, conversion data are not new from the last data read operation. If DRDY = 0, the previous (old) conversion data are returned. In order to avoid missing conversion data in continuous-conversion mode, poll the bit at least as often as the period of the data rate.

9.5.3 Conversion Data

Conversion data are read by the RDATA command. To read conversion data, take $\overline{CS1}$ low and issue the read data command. The conversion data field consists of an optional STATUS0 byte, three data bytes, and the CRC byte. The CRC byte is computed over the combined STATUS0 byte (if enabled) and three conversion data bytes. See the *RDATA Command* section for details on reading conversion data.

9.5.3.1 Status Byte (STATUS0)

The status byte contains information on the operating status of the ADC. During the conversion data read operation, the contents of the STATUS0 register is transmitted together with the conversion data by setting the STATENB bit of the MODE3 register. Alternatively, read the STATUS0 register directly by the register read command without having to read conversion data.

9.5.3.2 Conversion Data Format

The conversion data are 24 bits, in two's-complement format to represent positive and negative values. The data begin with the most significant bit (sign bit) first. The data are scaled so that V_{IN} = 0 V results in an ideal code value of 000000h, the positive full-scale input is equal to an ideal value of 7FFFFFh, and the negative full-scale input is equal to an ideal code value of 800000h. 表 9-11 lists the code values. The data are clipped to 7FFFFFh and 800000h during positive and negative signal overdrive, respectively.

表 9-11. ADC Conversion Data Codes

DESCRIPTION	INPUT SIGNAL (V)	24-BIT CONVERSION DATA(1)
Positive full scale	≥ V_{REF} / Gain × (2^{23} – 1) / 2^{23}	7FFFFFh
1 LSB	V_{REF} / (Gain × 2^{23})	000001h
Zero scale	0	000000h
– 1 LSB	– V_{REF} / (Gain × 2^{23})	FFFFFFh
Negative full scale	≤ – V_{REF} / Gain	800000h

(1) Ideal output code excluding noise, offset, gain, and linearity errors.

9.5.4 Cyclic Redundancy Check (CRC)

Cyclic redundancy check (CRC) is an error detection byte that detects communication errors to and from the host and ADC. CRC is the division remainder of the payload data by the prescribed CRC polynomial. The payload data are 1, 2, 3, or 4 bytes depending on the data transfer operation.

The host computes the CRC over the two command bytes and appends the CRC to the command string (third byte). A fourth, zero-value byte completes the command field to the ADC. The ADC performs the CRC calculation and compares the result to the CRC transmitted by the host. If the host and ADC CRC values match, the command executes and the ADC responds by transmitting the valid CRC during the fourth byte of the command. If the CRC is error free and the operation is a data read, the ADC responds with a second CRC that is computed for the requested data byte payload. The response data payload is 1, 3, or 4 bytes depending on the type of operation.

If the host and ADC CRC values *do not* match, the command does not execute and the ADC responds with an *inverted* CRC value, calculated over the received command bytes. The inverted CRC is intended to signal the host of the failed operation. The host terminates transmission of further bytes to stop the command operation. The CRC1 bit is set in the STATUS0 register when an error pertaining to ADC commands occurs. The STAT12 and CRC2 flags are set when an error pertaining to PGA register access occurs.

The ADC is ready to accept the next command after all required bytes are transmitted when no CRC error occurs, or after a CRC error occurs when terminated at the end of the fourth command byte.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X + 1$. The nine binary polynomial coefficients are 100000111b. The following sections detail the input and output data of each command.

See the example C code for the CRC calculation in the *ADS125H02 Example C Code* software. Also see the *ADS125H02 Design Calculator* software to calculate specific CRC code values.

In the command descriptions from the *Commands* section, these CRC mnemonics apply:

- **CRC-2**: Input CRC of command byte 1 and command byte 2
- **Out CRC-1**: Output CRC of one register data byte
- **Out CRC-2:** Output CRC of two command bytes, inverted value if an input CRC error is detected
- **Out CRC-3:** Output CRC of three conversion data bytes
- **Out CRC-4:** Output CRC of three conversion data bytes plus the STATUS0 byte
- **Echo Byte 1:** Echo out of input byte 1
- **Echo Byte 2:** Echo out of input byte 2

9.5.5 Commands

Commands are used to read conversion data, control the device, and read and write register data. 表 9-12 provides a list of commands and the corresponding command byte sequence. Only send commands listed in 表 9-12.

The column labeled $\overline{CSx}$ shows the use of $\overline{CS1}$ or $\overline{CS2}$ for the particular command type. Most commands use $\overline{CS1}$. Only activate $\overline{CS2}$ to access register data at addresses 10h, 11h, and 12h. See the *Chip-Select Pins ($\overline{CS1}$ and $\overline{CS2}$)* section for details of the chip-select operation.

表 9-12. Command Byte Summary

MNEMONIC	$\overline{CSx}$	DESCRIPTION	BYTE 1	BYTE 2(2)	BYTE 3	BYTE 4
CONTROL COMMANDS						
NOP	$\overline{CS1}$ or $\overline{CS2}$	No operation	00h	Arbitrary	CRC-2	00h
RESET	$\overline{CS1}$	Reset	06h	Arbitrary	CRC-2	00h
START	$\overline{CS1}$	Start conversion	08h	Arbitrary	CRC-2	00h
STOP	$\overline{CS1}$	Stop conversion	0Ah	Arbitrary	CRC-2	00h
READ DATA COMMAND						
RDATA	$\overline{CS1}$	Read conversion data	12h	Arbitrary	CRC-2	00h
CALIBRATION COMMANDS						
OFSCAL	$\overline{CS1}$	Offset calibration	16h	Arbitrary	CRC-2	00h
GANCAL	$\overline{CS1}$	Gain calibration	17h	Arbitrary	CRC-2	00h
REGISTER COMMANDS						
RREG	$\overline{CS1}$ or $\overline{CS2}$	Read register data	20h + rrh(1)	Arbitrary	CRC-2	00h
WREG	$\overline{CS1}$ or $\overline{CS2}$	Write register data	40h + rrh(1)	Register data	CRC-2	00h

(1) rrh = 5-bit register address.
(2) Excluding the write-register command, the value of the second byte is arbitrary (any value) but *is* included in the CRC calculation.

9.5.5.1 General Command Format

图 9-20 shows an example register write operation to register address 02h (command = 42h). For this register address (02h), take $\overline{CS1}$ low. The first byte output from the ADC is always FFh. The host calculates the CRC of the two input command bytes. The Out CRC-2 byte is the ADC-calculated, output CRC based on the received command bytes. If the CRC values match, the command is executed beginning at the last SCLK of the fourth byte in the sequence. Forcing the chip select high before the command completes results in command termination. Toggle the chip select low-to-high between command operations.

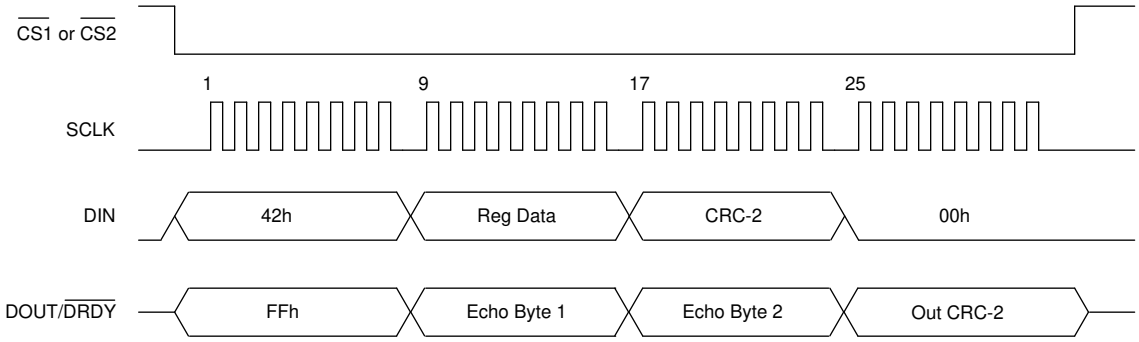


图 9-20. Register Write Command Sequence (Address = 02h)

The following sections detail the input and output byte sequence corresponding to each command. See the *Cyclic Redundancy Check (CRC)* section for the notation used for the CRC.

9.5.5.2 NOP Command

This command has no operation. Use the NOP command to validate the CRC response byte and error detection without affecting normal operation. 表 9-13 shows the NOP command byte sequence.

表 9-13. NOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	00h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.3 RESET Command

The RESET command resets the ADC operation and resets all registers to default. See the *Reset by Command* section for details. 表 9-14 lists the RESET command byte sequence.

表 9-14. RESET Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	06h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.4 START Command

This command starts conversions. See the *Conversion Control* section for details. 表 9-15 lists the START command byte sequence.

表 9-15. START Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	08h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.5 STOP Command

This command is used to stop conversions. See the *Conversion Control* section for details. 表 9-16 lists the STOP command byte sequence.

表 9-16. STOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	0Ah	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.6 RDATA Command

This command reads conversion data. Because the data are buffered, the data can be read at any time during the conversion sequence. If data are read *near* the completion of the conversion phase, old or new conversion data are returned. See the *Data Ready (DRDY)* section for details.

The response data of the ADC varies in length depending if the optional STATUS0 byte is included. See the *Conversion Data Format* section for details of the format of the conversion data. 表 9-17 and 图 9-21 describe the RDATA command byte sequence that includes the STATUS0 byte.

表 9-17. RDATA Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
DIN	12h	Arbitrary	CRC-2	00h	00h	00h	00h	00h	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2	STATUS0(1)	MSB data	MID data	LSB data	Out CRC-3 or Out CRC-4(2)

(1) Optional STATUS0 byte shown.
(2) Out CRC-4 (4-byte CRC = STATUS0 + data) if the STATUS0 byte is included in the data packet.

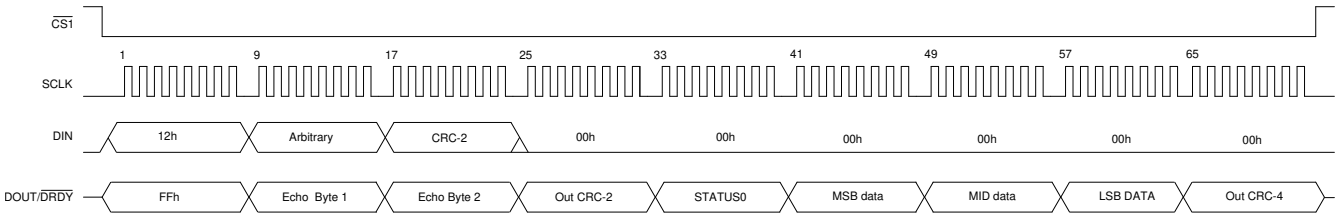


图 9-21. Conversion Data Read Operation

9.5.5.7 OFSCAL Command

This command is used for offset calibration. See the *Calibration* section for details. 表 9-18 lists the OFSCAL command byte sequence.

表 9-18. OFSCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	16h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.8 GANCAL Command

This command is used for gain calibration. See the *Calibration* section for details. 表 9-19 lists the GANCAL command byte sequence.

表 9-19. GANCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	17h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.5.5.9 RREG Command

Use the RREG command to read register data. Take $\overline{CS1}$ low to access registers within the ADC register block. Take $\overline{CS2}$ low to access registers within the PGA register block (see the *Register Map* section for the register block map). Register data are read one byte at a time using the RREG command for each operation. Add the register address (rrh) to the base value (20h) to complete the command byte (20h + rrh). 表 9-20 lists the RREG command byte sequence. The ADC responds with the register data byte, most significant bit first. Data for registers addressed outside the range is 00h. Out CRC-2 is the output CRC corresponding to the received command bytes. Out CRC-1 is the output CRC corresponding to the single register data byte.

表 9-20. RREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
DIN	20h + rrh	Arbitrary	CRC-2	00h	00h	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2	Register data	Out CRC-1

9.5.5.10 WREG Command

Use the WREG command to write register data. Take $\overline{CS1}$ low to access registers within the ADC register block. Take $\overline{CS2}$ low to access registers within the PGA register block (see the *Register Map* section for the register block map). The WREG command writes the register data one byte at a time using the WREG command for each operation. Add the register address (rrh) to the base value (40h) to complete the command byte (40h + rrh). 表 9-21 lists the WREG command byte sequence. Writing to certain registers results in conversion restart. 表 9-22 lists the affected registers. Do not write to registers outside the address range.

表 9-21. WREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	40h + rrh	Register data	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

9.6 Register Map

表 9-22 shows the device register map consisting of a series of byte-wide registers. Collectively, the registers are used to configure the device. Access the registers by using the RREG and WREG commands (register-read and register-write, respectively). Data are accessed one register byte at a time for each command operation. The address of the register corresponds to using either $\overline{CS1}$ or $\overline{CS2}$ for the register command operation. The *$\overline{CSx}$* column shows the correlation of $\overline{CS1}$ or $\overline{CS2}$ to the register address. Changing the data of certain registers will result in restart of conversions. The *Restart* column lists these registers.

表 9-22. Register Map Summary

ADDRESS	REGISTER	DEFAULT	RESTART	$\overline{CSx}$	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	4xh		$\overline{CS1}$	DEV_ID[3:0]				REV_ID1[3:0]			
01h	STATUS0	01h		$\overline{CS1}$	0	CRC1	0	STAT12	REFALM	DRDY	CLOCK	RESET
02h	MODE0	24h	Yes	$\overline{CS1}$	DR[4:0]				FILTER[2:0]			
03h	MODE1	01h	Yes	$\overline{CS1}$	0	0	0	CONVRT	DELAY[3:0]			
04h	RESERVED	00h		$\overline{CS1}$	00h							
05h	MODE3	00h		$\overline{CS1}$	0	STATENB	0	0	0	0	0	0
06h	REF	05h	Yes	$\overline{CS1}$	0	0	0	0	RMUX[3:0]			
07h	OFCAL0	00h		$\overline{CS1}$	OFC[7:0]							
08h	OFCAL1	00h		$\overline{CS1}$	OFC[15:8]							
09h	OFCAL2	00h		$\overline{CS1}$	OFC[23:16]							
0Ah	FSCAL0	00h		$\overline{CS1}$	FSC[7:0]							
0Bh	FSCAL1	00h		$\overline{CS1}$	FSC[15:8]							
0Ch	FSCAL2	40h		$\overline{CS1}$	FSC[23:16]							
0Dh	RESERVED	FFh		$\overline{CS1}$	FFh							
0Eh	RESERVED	00h		$\overline{CS1}$	00h							
0Fh	RESERVED	00h		$\overline{CS1}$	00h							
10h	MODE4	50h		$\overline{CS2}$	0	MUX[2:0]			GAIN[3:0]			
11h	STATUS1	xxh		$\overline{CS2}$	PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
12h	STATUS2	0xh		$\overline{CS2}$	0	0	0	CRC2	REV_ID2[3:0]			

表 9-23 lists the access codes for the ADS125H01 registers.

表 9-23. ADS125H01 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R/W	R-W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.6.1 Device Identification (ID) Register (address = 00h) [reset = 4xh]

ID is shown in 图 9-22 and described in 表 9-24.

Return to Register Map Summary.

图 9-22. ID Register

(1)7	6	5	4	3	2	1	0
DEV_ID[3:0]				REV_ID1[3:0]			
R-4h				R-xh			

(1) Reset values are device dependent.

表 9-24. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DEV_ID[3:0]	R	4h	**Device ID** 0100 = ADS125H01
3:0	REV_ID1[3:0]	R	xh	**Revision ID1** There are two revision ID fields: REV_ID1 and REV_ID2. The revision IDs can change without notification.

9.6.2 Main Status (STATUS0) Register (address = 01h) [reset = 01h]

STATUS0 is shown in 图 9-23 and described in 表 9-25.

Return to Register Map Summary.

图 9-23. STATUS0 Register

7	6	5	4	3	2	1	0
RESERVED	CRC1	RESERVED	STAT12	REFALM	DRDY	CLOCK	RESET
R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-xh	R/W-1h

表 9-25. STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	**Reserved** Always write 0.
6	CRC1	R/W	0h	**CRC1 Error** Indicates if a CRC error occurred during commands when $\overline{CS1}$ is active. Write 0 to clear the CRC error. 0: No CRC error during commands using $\overline{CS1}$ 1: CRC error occurred during commands using $\overline{CS1}$ See the STATUS2 register for the CRC error status for commands using $\overline{CS2}$.
5	RESERVED	R/W	0h	**Reserved** Always write 0.
4	STAT12	R	0h	**STAT12 Error Flag** Indicates one or more error events have been logged in the STATUS1 or STATUS2 registers. Read the STATUS1 and STATUS2 registers to determine the error. This bit clears automatically after all errors are cleared. 0: No error 1: Error logged in the STATUS1 or STATUS2 registers
3	REFALM	R	0h	**Reference Voltage Alarm** This bit sets when the reference voltage falls below < 0.4 V (typical). The alarm updates at each new conversion cycle (auto-reset). 0: No reference low alarm 1: Reference low alarm
2	DRDY	R	0h	**Data Ready** Indicates new conversion data. 0: Conversion data are not new from the last data read 1: Conversion data are new from the last data read
1	CLOCK	R	xh	**Clock** Indicates internal or external clock mode. The ADC automatically selects the clock mode. 0: ADC clock is internal 1: ADC clock is external
0	RESET	R/W	1h	**Reset** Indicates an ADC reset has occurred. Clear the bit to detect the next device reset. 0: No reset 1: Reset (default)

9.6.3 Mode 0 (MODE0) Register (address = 02h) [reset = 24h]

MODE0 is shown in 图 9-24 and described in 表 9-26.

Return to Register Map Summary.

图 9-24. MODE0 Register

7	6	5	4	3	2	1	0
DR[4:0]					FILTER[2:0]		
R/W-4h					R/W-4h		

表 9-26. MODE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	DR[4:0]	R/W	4h	**Data Rate** These bits select the data rate. 00000: 2.5 SPS 00001: 5 SPS 00010: 10 SPS 00011: 16. $\overline{6}$ SPS 00100: 20 SPS (default) 00101: 50 SPS 00110: 60 SPS 00111: 100 SPS 01000: 400 SPS 01001: 1.2 kSPS 01010: 2.4 kSPS 01011: 4.8 kSPS 01100: 7.2 kSPS 01101: 14.4 kSPS 01110: 19.2 kSPS 01111: 25.6 kSPS 10000 - 11111: 40 kSPS
2:0	FILTER[2:0]	R/W	4h	**Digital Filter** See the *Digital Filter* section for details. (1) These bits select the digital filter mode. 000: Sinc1 001: Reserved 010: Sinc3 011: Sinc4 100: FIR (default) 101-111: Reserved

(1) For $f_{DATA} \geqslant$ 14.4 kSPS, the filter mode is sinc5 only. In this case, the filter bits are don't care.
The FIR filter option is available for f_{DATA} = 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS only.

9.6.4 Mode 1 (MODE1) Register (address = 03h) [reset = 01h]

MODE1 is shown in 图 9-25 and described in 表 9-27.

Return to Register Map Summary.

图 9-25. MODE1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CONVRT	DELAY[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h			

表 9-27. MODE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0h	**Reserved** Always write 0
4	CONVRT	R/W	0h	**Conversion Mode** Select the ADC conversion mode. See the *Conversion Control* section. 0: Continuous-conversion mode (default) 1: Pulse-conversion (one shot) mode
3:0	DELAY[3:0]	R/W	1h	**Conversion Start Delay** Program the time delay at the start of conversion. See the *Start-Conversion Delay* section for details. Values listed are with f_{CLK} = 7.3718 MHz. Values shown in parenthesis are at f_{CLK} = 10.24 MHz. 0000: 0 µs (not for 25.6-kSPS or 40-kSPS operation) 0001: 50 µs (36 µs) (default) 0010: 59 µs (42µs) 0011: 67 µs (48 µs) 0100: 85 µs (61 µs) 0101: 119 µs (85 µs) 0110: 189 µs (136 µs) 0111: 328 µs (236 µs) 1000: 605 µs (435 µs) 1001: 1.16 ms (835 µs) 1010: 2.27 ms (1.63 ms) 1011: 4.49 ms (3.23 ms) 1100: 8.93 ms (6.43 ms) 1101: 17.8 ms (12.8 ms) 1110-1111: Reserved

9.6.5 Reserved (RESERVED) Register (address = 04h) [reset = 00h]

RESERVED is shown in 图 9-26 and described in 表 9-28.

Return to Register Map Summary.

图 9-26. RESERVED Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-00h							

表 9-28. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	00h	**Reserved bits** Always write 00h.

9.6.6 Mode 3 (MODE3) Register (address = 05h) [reset = 00h]

MODE3 is shown in 图 9-27 and described in 表 9-29.

Return to Register Map Summary.

图 9-27. MODE3 Register

7	6	5	4	3	2	1	0
RESERVED	STATENB	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 9-29. MODE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	**Reserved** Always write 0h.
6	STATENB	R/W	0h	**STATUS0 Byte Enable** Enable the STATUS0 byte contents for inclusion during conversion data read operation. 0: Exclude STATUS0 byte during conversion data read (default) 1: Include STATUS0 byte during conversion data read
5:0	RESERVED	R/W	0h	**Reserved** Always write 0h.

9.6.7 Reference Configuration (REF) Register (address = 06h) [reset = 05h]

REF is shown in 图 9-28 and described in 表 9-30.

Return to Register Map Summary.

图 9-28. REF Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RMUX[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-5h			

表 9-30. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0h	**Reserved** Always write 0h.
3:0	RMUX[3:0]	R/W	5h	**Reference Input Multiplexer** (see the *Reference Voltage* section) Select the ADC reference input. 0101: AVDD (default) 1010: External reference (REFP – REFN) All other code values are reserved.

9.6.8 Offset Calibration (OFCALx) Registers (address = 07h, 08h, 09h) [reset = 00h, 00h, 00h]

OFCALx is shown in 图 9-29 and described in 表 9-31.

Return to Register Map Summary.

图 9-29. OFCAL0, OFCAL1, OFCAL2 Registers

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

表 9-31. OFCAL0, OFCAL1, OFCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration** These three registers are the 24-bit offset calibration word. The offset calibration value is in two's-complement data format. The offset value is subtracted from the conversion result before the full-scale operation.

9.6.9 Full-Scale Calibration (FSCALx) Registers (address = 0Ah, 0Bh, 0Ch) [reset = 00h, 00h, 40h]

FSCALx is shown in 图 9-30 and described in 表 9-32.

Return to Register Map Summary.

图 9-30. FSCAL0, FSCAL1, FSCAL2 Registers

7	6	5	4	3	2	1	0
FSCAL[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSCAL[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSCAL[23:16]							
R/W-40h							

表 9-32. FSCAL0, FSCAL1, FSCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	FSCAL[23:0]	R/W	400000h	**Full-Scale Calibration** These three registers are the 24-bit full-scale calibration word. The full-scale calibration value is in straight binary data format. The full-scale value is divided by 400000h and multiplied with the conversion data. The scaling operation occurs after the offset calibration operation.

9.6.10 Reserved (RESERVED) Register (address = 0Dh) [reset = FFh]

RESERVED is shown in 图 9-31 and described in 表 9-33.

Return to Register Map Summary.

图 9-31. RESERVED Register

7	6	5	4	3	2	1	0
RESERVED							
R-FFh							

表 9-33. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	FFh	**Reserved Bits** Always write FFh.

9.6.11 Reserved (RESERVED) Register (address = 0Eh) [reset = 00h]

RESERVED is shown in 图 9-32 and described in 表 9-34.

Return to Register Map Summary.

图 9-32. RESERVED Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

表 9-34. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	00h	**Reserved Bits** Always write 00h.

9.6.12 Reserved (RESERVED) Register (address = 0Fh) [reset = 00h]

RESERVED is shown in 图 9-33 and described in 表 9-35.

Return to Register Map Summary.

图 9-33. RESERVED Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

表 9-35. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESERVED	R	00h	**Reserved Bits** Always write 00h.

9.6.13 MODE4 (MODE4) Register (address = 10h) [reset = 50h]

MODE4 is shown in 图 9-34 and described in 表 9-36.

Return to Register Map Summary.

图 9-34. MODE4 Register

7	6	5	4	3	2	1	0
RESERVED	MUX[2:0]			GAIN[3:0]			
R/W-0h	R/W-5h			R/W-0h			

表 9-36. MODE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	**Reserved** Always write 0h.
6:4	MUX[2:0]	R/W	5h	**Input Switch** These bits set the input switch. 000: External (AINP – AINN) 101: Internal V_{CM}: (HV_AVDD + HV_AVSS) / 2 (default) All other code values are reserved.
3:0	GAIN[3:0]	R/W	0h	**PGA Gain** These bits set the PGA gain. 0000: 0.125 (default) 0001: 0.1875 0010: 0.25 0011: 0.5 0100: 1 0101: 2 0110: 4 0111: 8 1000: 16 1001: 32 1010: 64 1011: 128 1100-1111: Reserved

9.6.14 PGA Alarm (STATUS1) Register (address = 11h) [reset = xxh]

STATUS1 is shown in 图 9-35 and described in 表 9-37.

Return to Register Map Summary.

图 9-35. STATUS1 Register

7	6	5	4	3	2	1	0
PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
R-xxh	R-xxh	R-xxh	R-xxh	R-xxh	R-xxh	R-xxh	R-xxh

表 9-37. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGA_ONL	R	xh	**PGA Output Negative Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
6	PGA_ONH	R	xh	**PGA Output Negative High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
5	PGA_OPL	R	xh	**PGA Output Positive Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
4	PGA_OPH	R	xh	**PGA Output Positive High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
3	PGA_INL	R	xh	**PGA Input Negative Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
2	PGA_INH	R	xh	**PGA Input Negative High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
1	PGA_IPL	R	xh	**PGA Input Positive Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
0	PGA_IPH	R	xh	**PGA Input Positive High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active

9.6.15 Status 2 (STATUS2) Register (address = 12h) [reset = 0xh]

STATUS2 is shown in 图 9-36 and described in 表 9-38.

Return to Register Map Summary.

图 9-36. STATUS2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CRC2	REV_ID2[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-xh			

表 9-38. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0h	**Reserved** Always write 0h.
4	CRC2	R/W	0h	**CRC2 Error** Indicates if a CRC error occurred during commands with use of $\overline{CS2}$. The CRC error is latched until cleared by the user. Write 0 to clear the error. 0: No CRC error during commands with use of $\overline{CS2}$ 1: CRC error occurred during commands with use of $\overline{CS2}$
3:0	REV_ID2[3:0]	R	x	**Revision ID2** Revision ID 2 field. The revision ID1 and ID2 can change without notification.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Example to Determine the PGA Linear Operating Range

Linear operation of the PGA requires that the absolute input voltage does not exceed the specified range. The following example shows how to verify the absolute input voltage is within the valid range. In this example, the input signal is ±10 V using a chosen 15% overrange capability. The negative input lead of the sensor is connected to AGND and AINN. The ADC gain is chosen at 0.1875 using a 2.5-V reference voltage and ±15-V power supplies with a 5% voltage tolerance. The summary of conditions to verify PGA operating conformance are:

- $V_{(AINP\_MAX)}$ = 10 V × 115% = 11.5 V
- $V_{(AINP\_MIN)}$ = – 10 V × 115% = – 11.5 V
- $V_{(AINN)}$ = AGND
- HV_AVDD_{MIN} = 15 V × 95% = 14.25 V
- HV_AVSS_{MAX} = – 15 V × 95% = – 14.25 V
- Gain = 0.1875
- V_{REF} = 2.5 V

The evaluation of 方程式 3 (for gain < 1) results in:

– 11.75 V < – 11.5 V and 11.5 V < 11.75 V

The inequality is satisfied, and as a result, the absolute input voltage is within the PGA input range.

10.1.2 Input Signal Rate of Change (dV/dt)

A high dV/dt signal at the ADC input can lead to transient turn-on of the PGA inverse-parallel protection diodes (see 图 9-1 for details). Turn-on of the PGA diodes can result in current flow in the analog inputs that can cause a disturbance in the measurement channel. For example, a high dV/dt voltage can be generated at the output of a signal multiplexer after a channel selection, leading to a possible flow of transient currents through the ADC inputs. Filter the ADC input voltage to limit the rate of voltage change (dV/dt).

10.1.3 Unused Inputs and Outputs

- **Digital I/O**

  ADC operation is possible using a subset of the digital I/Os. However, tie any unused digital input high or low (DVDD or DGND, as appropriate). Do not float (tri-state) the digital inputs or unpredictable operation can result. The following is a summary of an optional digital I/O:

  - **CLKIN:** Tie CLKIN to DGND to operate the ADC using the internal oscillator. The internal oscillator stops operation if CLKIN is connected to DVDD, resulting in loss of ADC functionality. Connect CLKIN to an external clock source to operate with an external clock.
  - **START:** Tie START low in order to control conversions entirely by command. Tie START high to free-run conversions (only when programmed to continuous-conversion mode). Connect START to the host controller to control conversions directly by the pin.
  - **$\overline{\text{RESET}}$:** Tie $\overline{\text{RESET}}$ high if desired. An external RC delayed-reset or a reset device connected to the $\overline{\text{RESET}}$ pin is not necessary because the ADC automatically resets at power on. The ADC can be reset by the RESET command. Connect the $\overline{\text{RESET}}$ pin to the host controller to reset the ADC by hardware.

- **$\overline{\text{DRDY}}$:** The data-ready indicator is also provided by the DOUT/$\overline{\text{DRDY}}$ pin. $\overline{\text{CS}}$ must be low to use DOUT/$\overline{\text{DRDY}}$ to provide the data-ready function. Data-ready is also determined by polling the DRDY bit of the STATUS0 byte. Using these alternate methods, the connection of $\overline{\text{DRDY}}$ to the host controller is not necessary and the pin can be left unconnected.

10.2 Typical Application

图 10-1 illustrates an example of the ADS125H01 used in a ±10-V analog input programmable logic controller (PLC) module. The ADC inputs are protected by external ESD diodes to provide system-level protection. The external 100-MΩ resistor is used to pull the positive analog input to 15 V if the field-wiring connection is open or the transmitter connected the ADC inputs has a failed open circuit. A failed input results in a full-scale code value.

The signal from the transmitter is filtered to remove EMI and RFI interference to enhance noise immunity. The resistor also serves to limit input current in the event of a DC overvoltage, including if the module loses power while the input signal is present. The negative input is connected to AINN, which is also connected to AGND. Connection to AGND is necessary if the sensor power supply is not referenced to the ADC ground.

The input configuration is single-ended with the input voltage driven to 0 V and –10 V relative to AINN (AGND).

The reference voltage is applied to the REFP and REFN pins. A 100-kΩ resistor biases the differential reference voltage to 0 V when either reference input is open circuit. With the resistor, a failed or missing reference voltage is detected by the internal monitor.

The internal oscillator is selected by grounding the CLKIN pin. The serial interface and digital control lines of the ADC connect to the host.

The Zener diode clamps the high-voltage supply (HV_AVDD – HV_AVSS) to 40 V to provide overvoltage protection if an input signal is applied with module power off.

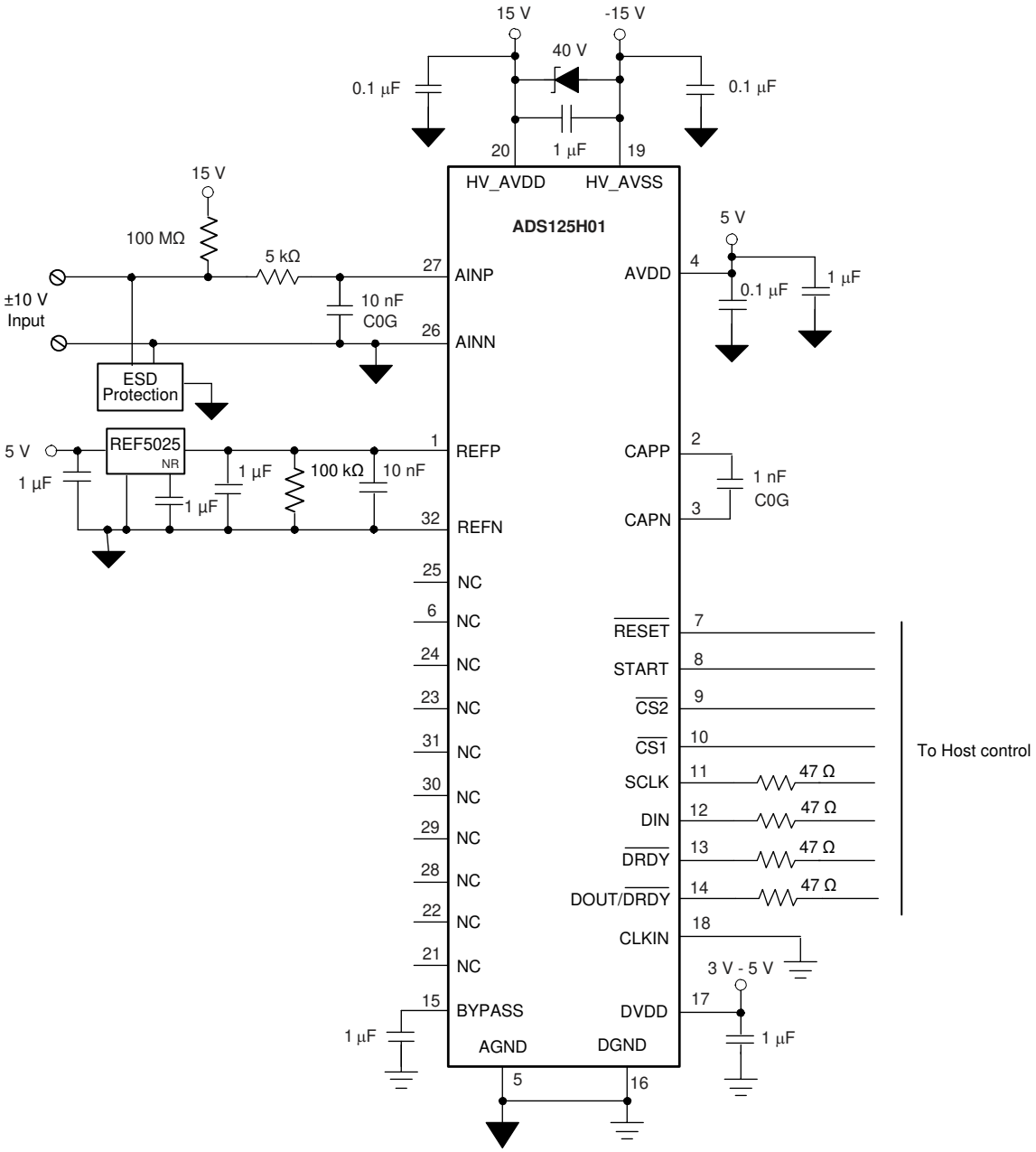


图 10-1. ±10-V Analog Input PLC Module

10.2.1 Design Requirements

表 10-1 shows the design goals of the analog input PLC module. The ADC programmability allows various tradeoffs of sample rate, conversion noise, and conversion latency. 表 10-2 shows the design parameters of the analog input PLC module.

表 10-1. Design Goals

DESIGN GOAL	VALUE
Accuracy	±0.1%
Temperature range (internal module)	0°C to +105°C
Update rate	50 µs
Effective resolution	18 bits

表 10-2. Design Parameters

DESIGN PARAMETER	VALUE
Nominal signal range	±10 V
Extended range	±12 V
Input impedance	100 MΩ
Overvoltage rating	±35 V

10.2.2 Detailed Design Procedure

A key consideration in the design of an analog input module is the error over the ambient temperature range resulting from the drift of gain, offset, reference voltage, and linearity error. This example assumes the initial offset and gain (including reference voltage error) are user calibrated at T_A = 25°C. 表 10-3 shows the maximum drift error of the ADC over the 0°C to +105°C temperature range.

表 10-3. Error Over Temperature

PARAMETER	ERROR (0°C to +105°C)
Offset drift error	0.00125%
Gain drift error	0.032%
Nonlinearity error (over temperature)	0.001%
Reference drift error (REF5025IDGK external reference)	0.024%
Total drift error	0.05825%

As shown in 表 10-3, the total drift error is 0.058% when using the REF5025IDGK reference, which satisfies the 0.1% total error design goal.

The ADC gain is programmed to 0.1875. With a 2.5-V reference voltage, the ADC input range is ±2.5 V / 0.1875 = ±13.3 V. However, using ±15-V power supplies, the required headroom of the PGA limits the range to ±12.5 V (which excludes the tolerance of the ±15-V power supplies). The input range satisfies the extended range design target of ±12 V.

The 1-GΩ minimum input impedance of the ADC and the 100-MΩ external pullup resistor meets the input impedance goal of 100 MΩ. The input fault overvoltage requirement (35 V) is met by limiting the input current to the 10-mA maximum specification. The external 5-kΩ series input resistor limits the input current to 7 mA.

The data rate that meets the continuous-conversion, 50-µs acquisition period is 25600 SPS (39 µs actual). If a precise 50-µs conversion period is desired, reduce the clock frequency to the ADC with an external clock source. The clock frequency that produces a precise 50-µs conversion period is 5.76 MHz.

Referring to the data illustrated in 图 8-3, the effective resolution is 18 bits at data rate = 25600 SPS and gain = 0.1875.

10.2.3 Application Curve

图 10-2 shows 100,000 consecutive conversions over a four-second interval with the ADC inputs shorted using the ADC configuration given in this example. 100,000 conversions demonstrate the consistency of the ADC conversion results over time. The conversion noise in this example is 107 μV_{RMS}. Based on this measurement data, the equivalent effective resolution is 18 bits, which meets the design requirement.

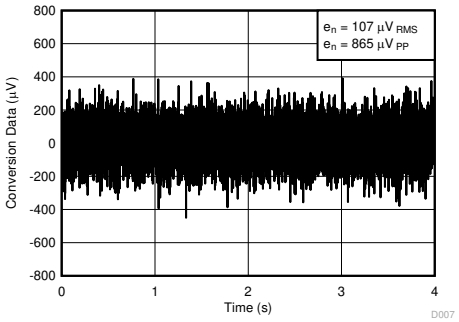


图 10-2. Conversion Noise

11 Power Supply Recommendations

The ADC requires three analog power supplies (high-voltage supplies HV_AVDD and HV_AVSS, and a low-voltage supply AVDD) and a digital power supply (DVDD). The high-voltage analog power-supply configuration is either bipolar (±5 V to ±18 V) or unipolar (10 V to 36 V). The AVDD power supply is 5 V. The digital supply range is 2.7 V to 5.25 V. AVDD and DVDD can be tied together as long as the 5-V power supply is free from noise and glitches that can affect conversion results. An internal low-dropout regulator (LDO) powers the digital core from the DVDD power supply. DVDD sets the digital I/O voltage.

Voltage ripple produced by switch-mode power supplies can interfere with the ADC conversion accuracy. Use LDOs at the switching regulator output to reduce power-supply ripple.

11.1 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve optimum performance. Power supplies must be decoupled close to the device supply pins. For the high-voltage analog supply (HV_AVDD and HV_AVSS), place a 1-µF capacitor between the pins and place 0.1-µF capacitors from each supply to the ground plane. Connect 0.1-µF and 1-µF capacitors in parallel at AVDD to the ground plane. Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from the BYPASS pin to the ground plane. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and equivalent series inductance (ESL) characteristics for power-supply decoupling purposes.

11.2 Analog Power-Supply Clamp

Circumstances must be evaluated when an input signal is present while the ADC is unpowered. When the input signal exceeds the forward voltage of the internal ESD diodes, the diodes conduct resulting in backdrive of the analog power-supply voltage through the internal ESD diodes. Backdriving the ADC power supply can also occur when the power supply is on. If the power supply is not able to sink current during a backdrive condition, the power-supply voltage can rise and can ultimately exceed the breakdown rating of the ADC. The maximum supply voltage rating of the ADC must not be exceeded under any condition. One solution is to clamp the analog supply using a Zener diode placed across HV_AVSS and HV_AVDD.

11.3 Power-Supply Sequencing

The power supplies can be sequenced in any order, but do not allow analog or digital voltage inputs to exceed the respective analog or digital power supplies without limiting the input current.

12 Layout

12.1 Layout Guidelines

Good layout practices are crucial to realize the full performance of the ADC. Poor grounding can quickly degrade the ADC noise performance. This section discusses layout recommendations that help provide the best results.

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on layout restrictions, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a single, direct connection to the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital signals away from the CAPP and CAPN pins and away from all analog inputs and associated components to prevent crosstalk.

Because large capacitance on DOUT/$\overline{\text{DRDY}}$ can lead to increased ADC noise levels, minimize the length of the PCB trace. Use a series resistor or a buffer if long traces are used.

Use C0G capacitors for the analog input filter and for the CAPP to CAPN capacitor. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections with multiple vias on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noisy conversion data.

12.2 Layout Example

图 12-1 illustrates an example layout of the ADS125H01, requiring a minimum of three PCB layers. The example circuit is shown with bipolar supply operation (±15 V). In this example, the inner layer is dedicated to the ground plane and the outer layers are used for signal and power traces. If a four-layer PCB is used, dedicate an additional inner layer for the power planes. In this example, the ADC is oriented in such a way to minimize crossover of the analog and digital signal traces.

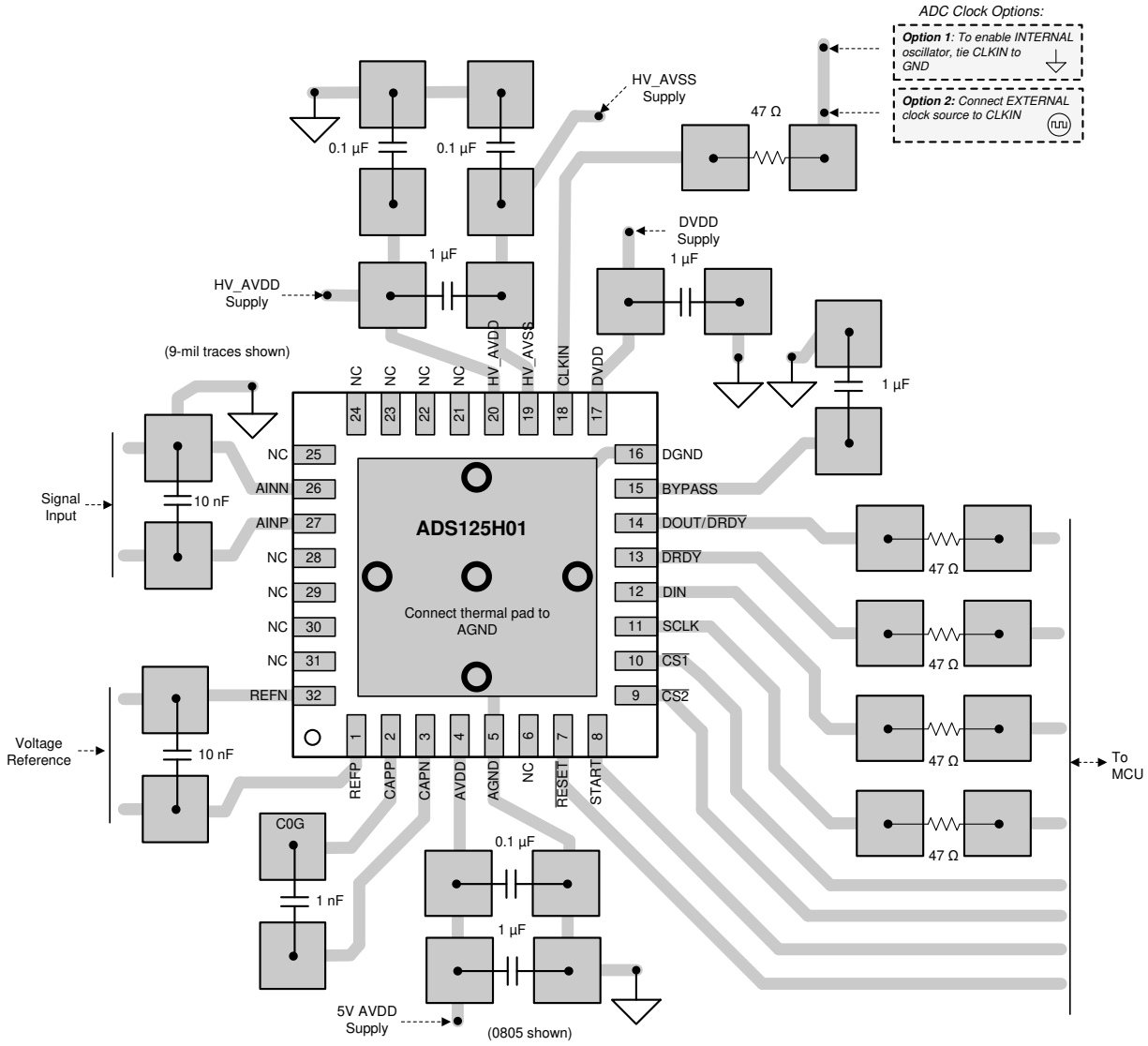


图 12-1. Example Top-Layer PCB Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *ADS125H02 ±20-V Input, 40-kSPS, 24-Bit, Delta-Sigma ADC with Voltage Reference* data sheet
- Texas Instruments, *ADS125H02 Example C Code* software
- Texas Instruments, *ADS125H02 Design Calculator* software
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.4 Trademarks

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13.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS125H01IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 125H01	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

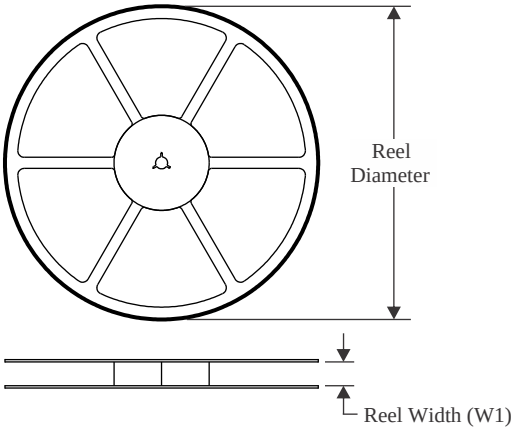
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

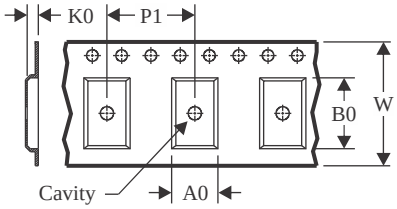
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

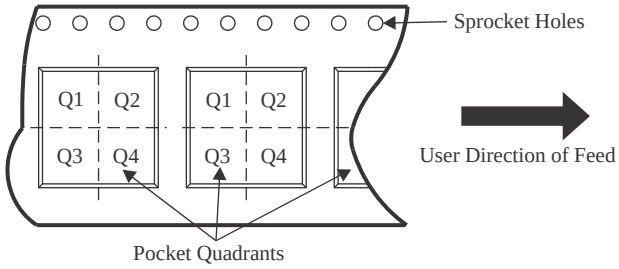


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

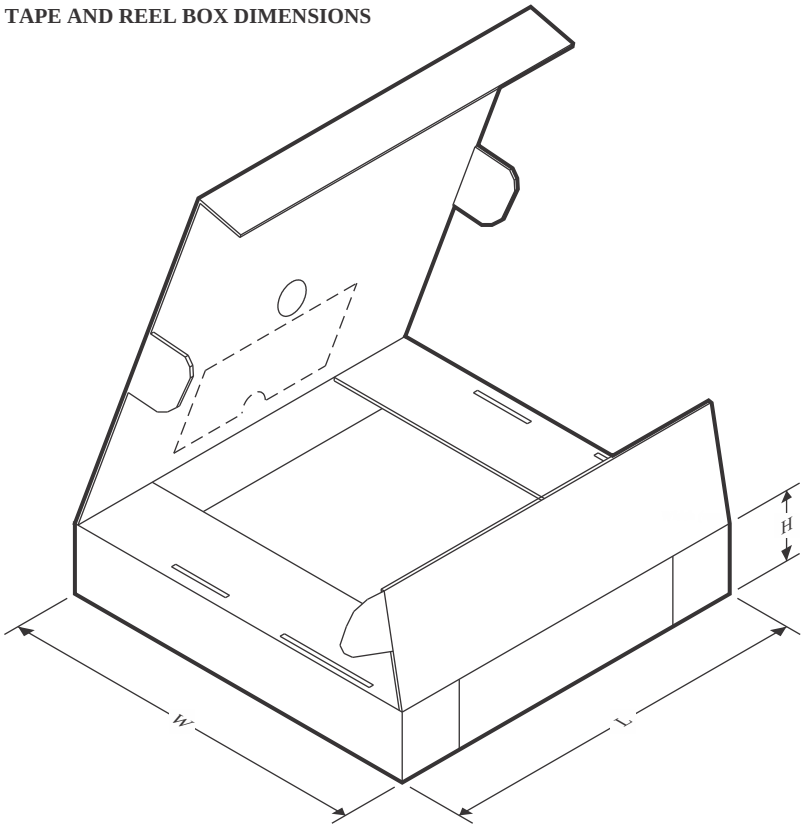
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS125H01IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS125H01IRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0

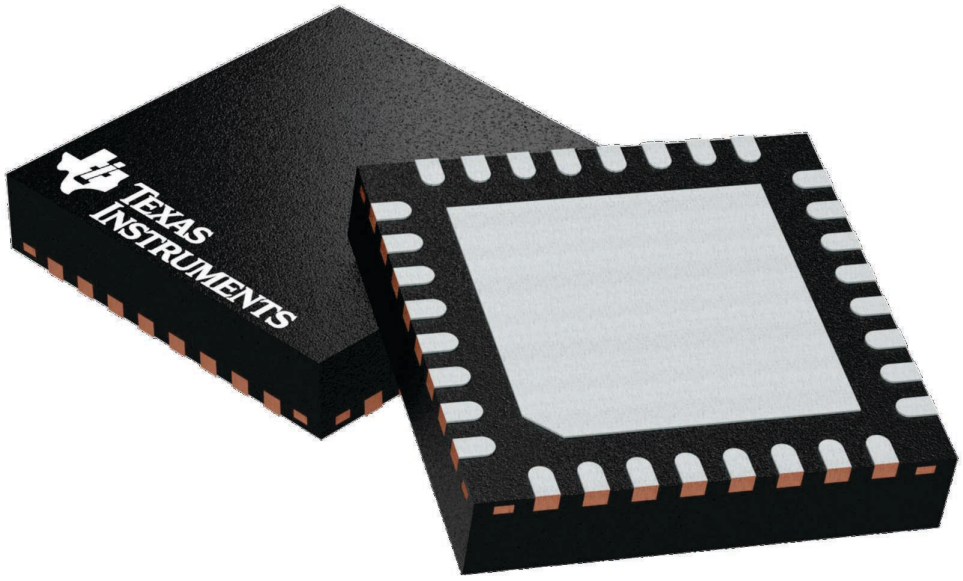
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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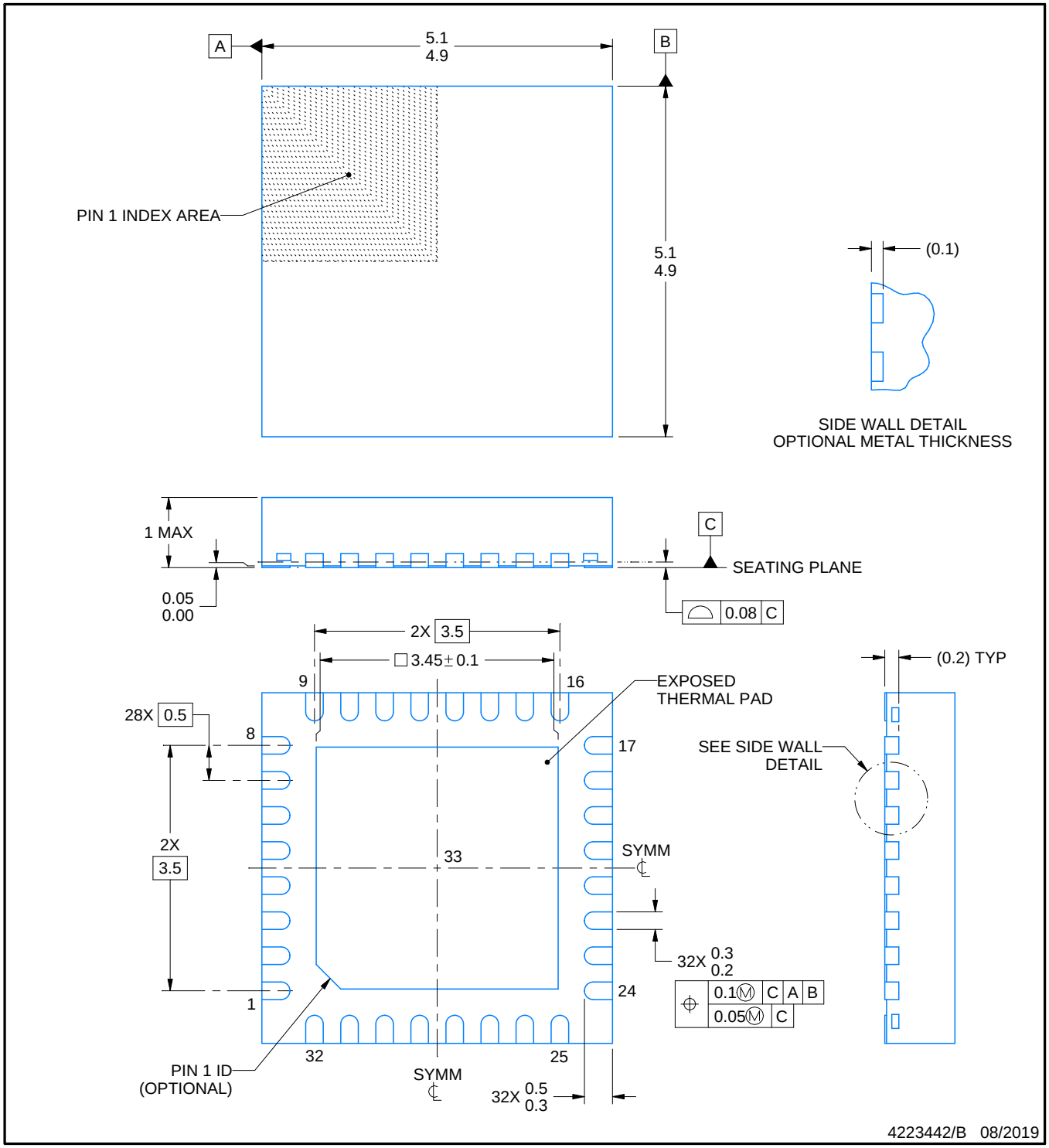
RHB0032E

PACKAGE OUTLINE

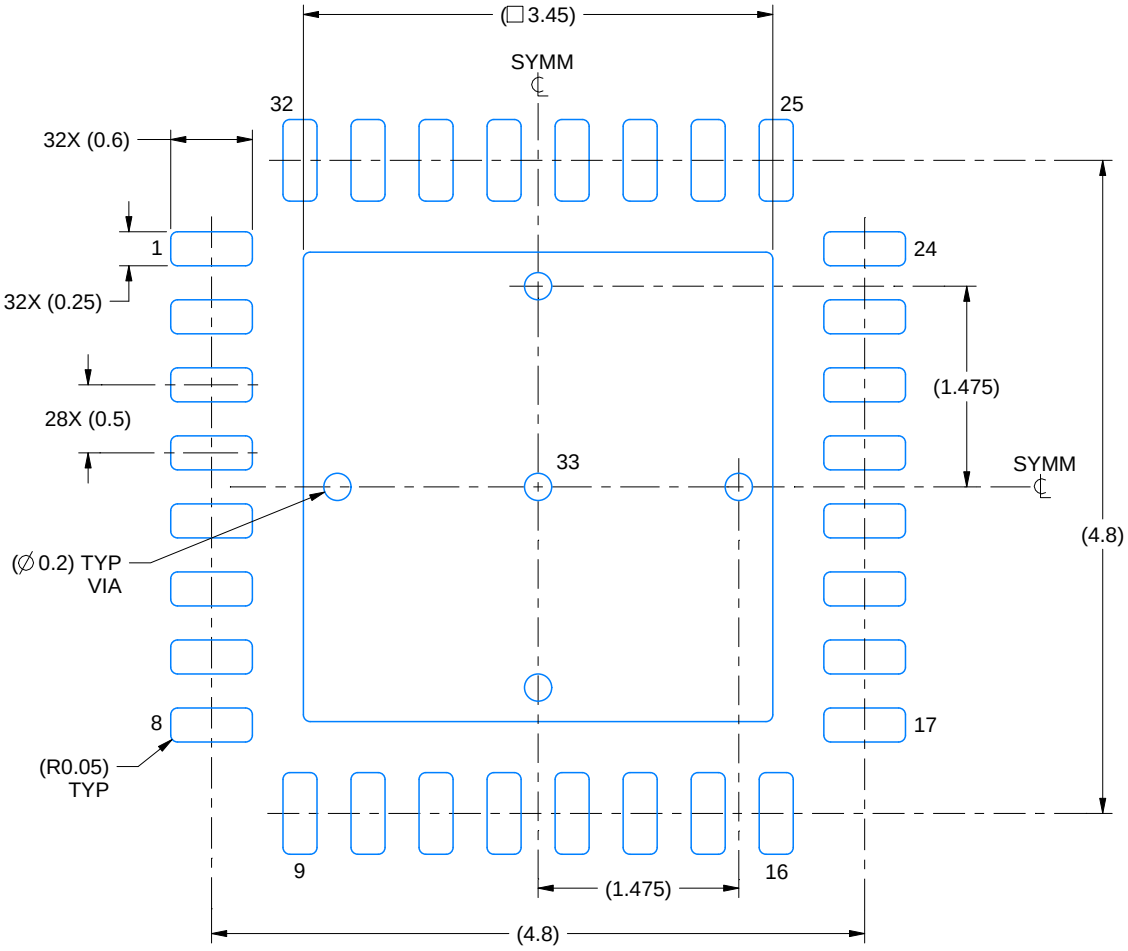
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

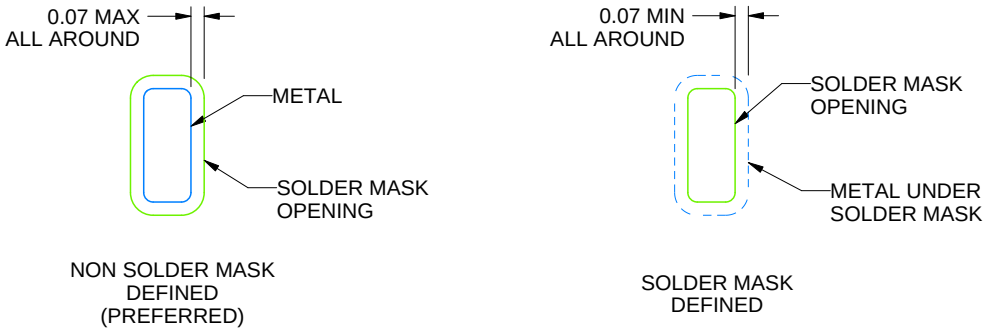


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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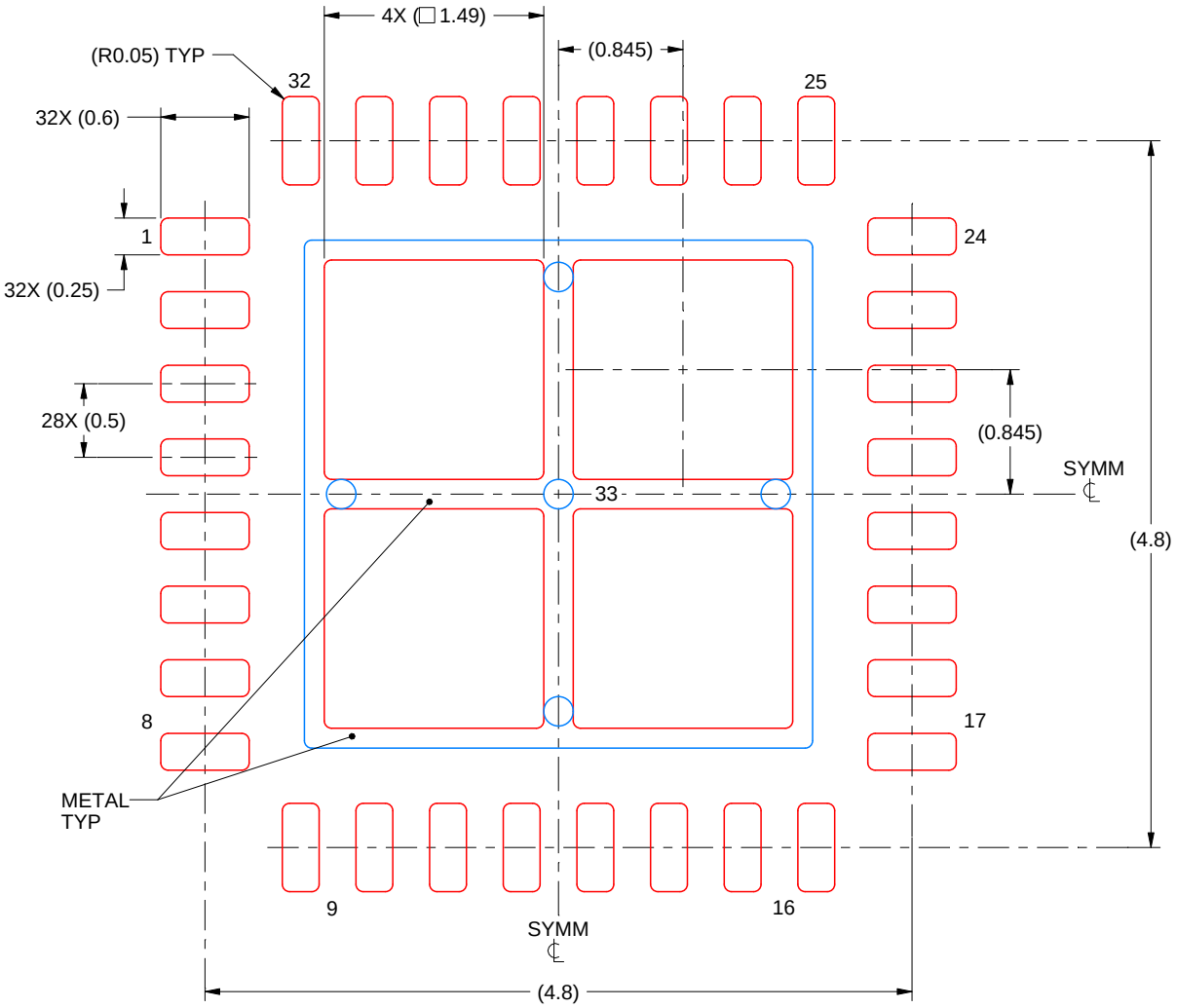
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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