ADS58J89 四通道 14 位 250/500MSPS 接收器和反馈 IC

1 特性

- 4 通道、14 位 500MSPS，具有数字信号处理功能
- 功率放大器线性化（反馈）模式
  - 14 位 250MSPS 间隔采样
  - 可编程分辨率与占空比
    - 占空比 3:2（60% 11 位，40% 9 位）
    - 占空比 2:3（40% 12 位，60% 9 位）
    - 占空比 1:3（25% 14 位，75% 9 位）
- 流量接收器模式
  - 14 位 250MSPS：2 倍抽取率滤波器，高通/低通
  - 9 位滤波器信噪比 (SNR) 提升模式（最大带宽为 150MHz）
  - 9 至 14 位时分双工 (TDD) 突发模式（最大带宽为 200MHz）
- 灵活的输入时钟缓冲器，支持 1/2/4 分频
- JESD204B 数字接口（速率高达 5.0Gbps）
  - 每个通道有 1 或 2 个信道，支持子类 1
- 64 引脚超薄型四方扁平无引线 (VQFN) 封装 (9mm × 9mm)

2 应用

- 多载波、多模式、多频带蜂窝接收器
  - TDD-LTE
  - FDD-LTE
  - CDMA、WCMDA、CMDA2k
  - GSM
- 射频 (RF) 和微波回程
  - 点对点回程
  - 点对多点回程
- 无线中继器
- 分布式天线系统 (DAS)
- 无线宽带

3 说明

ADS58J89 是一款高线性度、四通道、14 位 250/500MSPS IF（中频）接收器。 四个通道上均有 14 位 500MSPS 模数转换器 (ADC)，用于处理无线基础设施系统的信号。 各通道可根据带宽、分辨率和采样时间要求配置为不同模式。 信号处理模块包含可选模式：抽取滤波器模式、滤波器 SNR 提升模式、分辨率与时间模式以及时分双工 (TDD) 突发模式。 这 4 个通道针对多天线系统进行设计，为采用小型封装的多通道接收器提供了较高的带宽与线性度。 在 TDD 系统中，此器件可同时用作流量接收器和功率放大器线性化反馈路径。

主要技术规格：
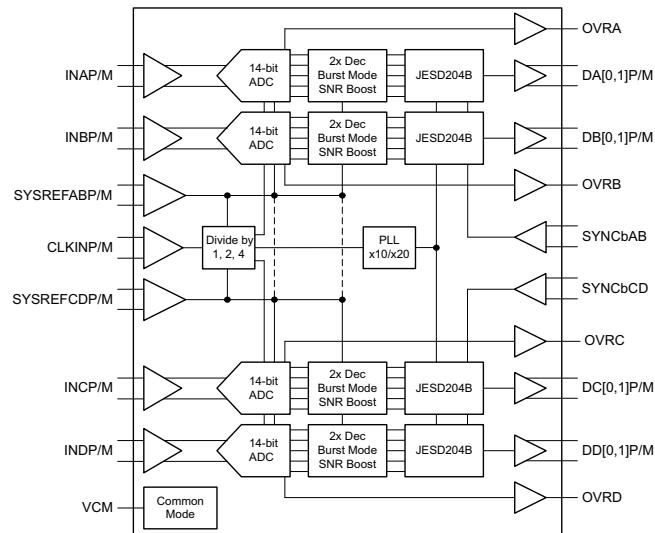
- 功耗：每通道 875mW
- 输入带宽 (3dB)：900MHz
- 孔径抖动：98fs rms
- 通道隔离：85dB
- f_{in} = 170MHz（−1dBFS，−1dBFS）条件下的性能
  - SNR：65.8dBFS
  - 无杂散动态范围 (SFDR)：85dBc（HD2，HD3）；95dBFS（非 HD2，HD3）

器件信息[1]

| 部件号	封装	最大输出速率
ADS58J89	VQFN (64)	500MSPS

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图

目录

4   修订历史记录

日期	修订版本	注释
2014 年 11 月	*	最初发布。

5 Pin Configuration and Functions

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INPUT OR REFERENCE			
INAP, INAM	63, 62	I	Differential analog input for channel A
INBP, INBM	58, 59	I	Differential analog input for channel B
INCP, INCM	18, 19	I	Differential analog input for channel C
INDP, INDM	23, 22	I	Differential analog input for channel D
VCM	16	O	Common mode output voltage to bias analog inputs, Vcm = 2.0 V
VREF	15	O	Voltage reference output. A 0.1-µF bypass capacitor to ground close to the pin is recommended
CLOCK/SYNC			
CLKINP, CLKINM	9, 8	I	Differential clock input for channel
SYSREFABP, SYSREFABM	6, 5	I	LVDS input with internal 100-Ω termination. External SYSREF input for channels A, B, C, and D

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
SYSREFCDP, SYSREFCDM	11, 12	I	LVDS input with internal 100-Ω termination. External SYSREF input for channels C and D if output rate of channel A/B is different from channel C/D. Can be configured to trigger input for burst modes with SPI register write. Can be used as differential input or two single-ended inputs (SYSREFCDP becomes TRIGGERAB and SYSREFCDM becomes TRIGGERCD) for channel A/B and channel C/D.
CONTROL OR SERIAL			
ENABLE	14	I	Chip enable. Active high. Power down functionality can be configured through SPI register setting and exercised using the ENABLE pin. Internal 51-kΩ pulldown resistor.
SCLK	3	I	Serial interface clock input
SDATA	2	I/O	Bidirectional serial data in 3-pin mode. In 4-pin interface, the SDATA pin is an input only.
SDENb	4	I	Serial interface enable
SDOUT	1	O	Serial interface data output
SRESETb	13	I	Hardware reset. Active low. Initializes internal registers during high to low transition. This pin has an internal 51-kΩ pullup resistor.
DATA OUTPUT INTERFACE			
DA[0,1]P, DA[0,1]M	55, 54, 52, 51	O	JESD204B output interface for channel A
DB[0,1]P, DB[0,1]M	46, 45, 43, 42	O	JESD204B output interface for channel B
DC[0,1]P, DC[0,1]M	26, 27, 29, 30	O	JESD204B output interface for channel C
DD[0,1]P, DD[0,1]M	35, 36, 38, 39	O	JESD204B output interface for channel D
OVRA	50	I/O	Fast over-range indicator channel A. In burst mode can be configured to TRIGGERAB input.
OVRB	49	O	Fast over-range indicator channel B. In burst mode can be configured to TRDY output.
OVRC	31	I/O	Fast over-range indicator channel C. In burst mode can be configured to TRIGGERCD input.
OVRD	32	O	Fast over-range indicator channel D. In burst mode can be configured to TRDY output.
SYNCbABP, SYNCbABM	47, 48	I	SYNCb input for JESD204B interface for channel A/B, internal 100-Ω termination
SYNCbCDP, SYNCbCDM	34, 33	I	SYNCb input for JESD204B interface for channel C/D, internal 100-Ω termination
POWER SUPPLY			
AVDDC	7, 10	I	Clock 1.8-V power supply
AVDD18	21, 24, 57, 60	I	Analog 1.9-V power supply
AVDD33	17, 20, 61, 64	I	Analog 3.3-V power supply
DVDD	25, 56	I	Digital 1.8-V power supply
GND	PowerPAD™	I	Ground
IOVDD	28, 37, 44, 53	I	JESD204B output interface 1.8-V power supply
PLLVDD	40, 41	I	PLL 1.8-V power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	AVDD33	−0.3	3.6	V
	AVDD18	−0.3	2.1	
	AVDDC	−0.3	2.1	
	DVDD	−0.3	2.1	
	IOVDD	−0.3	2.1	
	PLLVDD	−0.3	2.1	
Voltage between AGND and DGND		−0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INCP, INDP, INAM, INBM, INCM, INDM	−0.3	3	V
	CLKINP, CLKINM	−0.3	AVDD18 + 0.3 V	
	SYNCbABP, SYNCbABM, SYNCbCDP, SYNCbCDM	−0.3	AVDD18 + 0.3 V	
	SYSREFABP, SYSREFABM, SYSREFCDP, SYSREFCDM	−0.3	AVDD18 + 0.3 V	
	SCLK, SDENb, SDATA, SRESETb, ENABLE	−0.3	DVDD + 0.5 V	
T_A	Operating free-air temperature	−40	85	ºC
T_J	Operating junction temperature[2]		125	ºC

(1) Stresses beyond those listed as *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature		−65	150	°C
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	−2	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	ADC clock frequency	250		500	MSPS
	Resolution	14		14	bits
Supply	AVDD33	3.15	3.3	3.45	V
	AVDD18	1.8	1.9	2.0	
	AVDDC	1.7	1.8	1.9	
	DVDD	1.7	1.8	1.9	
	IOVDD	1.7	1.8	1.9	
	PLLVDD	1.7	1.8	1.9	
T_A	Operating free-air temperature	−40		85	°C
T_J	Operating junction temperature			125	°C

6.4 Thermal Information

Thermal Metric[1]		RGC (64 PINS)	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	23.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case, top	7.0	
$R_{\Theta JB}$	Junction-to-board thermal resistance	2.6	
φ_{JT}	Junction-to-top of package	0.1	
φ_{JB}	Junction-to-board characterization parameter	2.6	
$R_{\Theta JC(bot)}$	Junction-to-case, bottom	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values at T_A = 25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, AVDD33 = 3.3 V; AVDD18 = 1.9 V; AVDDC, DVDD, IOVDD, PLLVDD = 1.8 V, −1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{AVDD33}	3.3-V analog supply current				500		mA
I_{AVDD18}	1.9-V analog supply current				320		mA
I_{AVDDC}	1.8-V clock supply current				18		mA
I_{DVDD}	1.8-V digital supply current	4-channel SNR boost			472		mA
		4-channel decimation filter			323		
		4-channel burst mode			324		
		2-channel burst mode, 2-channel SNR boost			398		
		2-channel decimation filter, 2-channel burst mode			324		
		2-channel decimation filter, 2-channel, discard every other sample			289		
I_{IOVDD}	I/O voltage supply current	2 lanes per ADC			373		mA
		1 lane per ADC			185		
I_{PLLVDD}	PLL voltage supply current				42		mA
Pdis	Total power dissipation	4-channel SNR boost			3.94		W
		4-channel Burst mode			3.67		
		4-channel decimation filter			3.34		
		4-channel decimation filter, 1 lane per ADC			3.27	3.5	
		2-channel SNR Boost, 2-channel burst mode			3.81		
		2-channel decimation filter, 2-channel burst mode			3.51		
		2-channel decimation filter, 2-channel, discard every other sample			3.28		
Deep sleep mode power					791		mW
Wake-up time from deep sleep mode		SNR > 60 dB			1.4		ms
Light sleep mode power					1.68		W
Wake-up time from light sleep mode		SNR > 60 dB			8		µs
ANALOG INPUTS							
Differential input full-scale				1.0	1.25	1.5	Vpp
Input common mode voltage					Vcm ± 50 mV		V
Input resistance	Differential at DC				1		kΩ
Input capacitance	Each input to GND				2.75		pF
VCM	Common mode voltage output				2.18		V
Analog input bandwidth (−3 dB)					900		MHz
CHANNEL-TO-CHANNEL ISOLATION							
Crosstalk[1]		Near channel	f_{IN} = 170 MHz		85		dB
		Far channel	f_{IN} = 170 MHz		95		
CLOCK INPUT							
Input clock frequency				250		2000[2]	MHz
Input clock amplitude				0.4		1.5	Vpp
Input clock duty cycle				45%	50%	55%	
Internal clock biasing					0.9		V

(1) Crosstalk is measured with a −1-dBFS input signal on aggressor channel and no input on victim channel.
(2) CLK / 4 mode

6.6 Electrical Characteristics: 250 MSPS Output, 2x Decimation Filter

Typical values at T_A = 25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, AVDD33 = 3.3 V; AVDD18 = 1.9 V; AVDDC, DVDD, IOVDD, PLLVDD = 1.8 V, −1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		68.3		dBFS
		f_{IN} = 100 MHz		68.2		
		f_{IN} = 170 MHz	65	68.2		
		f_{IN} = 310 MHz		67.6		
		f_{IN} = 450 MHz		66.8		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		85		dBc
		f_{IN} = 100 MHz		85		
		f_{IN} = 170 MHz	75	85		
		f_{IN} = 310 MHz		85		
		f_{IN} = 450 MHz		75		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		85		dBc
		f_{IN} = 100 MHz		85		
		f_{IN} = 170 MHz	75	85		
		f_{IN} = 310 MHz		85		
		f_{IN} = 450 MHz		85		
SFDR (Non-HD2, Non-HD3)	Spur free dynamic range (excluding HD2 and HD3)	f_{IN} = 10 MHz		95		dBc
		f_{IN} = 100 MHz		95		
		f_{IN} = 170 MHz	75	95		
		f_{IN} = 310 MHz		90		
		f_{IN} = 450 MHz		85		
IMD3	2F1-F2, 2F2-F1, Ain = −7 dBFS	F_{IN} = 169 and 171 MHz		93		dBFS

6.7 Electrical Characteristics: 500 MSPS Output

Typical values at T$_A$ = 25°C, full temperature range is T$_{MIN}$ = −40°C to T$_{MAX}$ = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, AVDD33 = 3.3 V; AVDD18 = 1.9 V; AVDDC, DVDD, IOVDD, PLLVDD = 1.8 V, −1-dBFS differential input, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-Noise Ratio	SNR Boost (150-MHz bandwidth)	f_{IN} = 100 MHz		65.7		dBFS
			f_{IN} = 170 MHz		65.7		
			f_{IN} = 350 MHz		65		
		Burst Mode (14 bit)	f_{IN} = 10 MHz		65.3		dBFS
			f_{IN} = 100 MHz		65.2		
			f_{IN} = 170 MHz		65.1		
			f_{IN} = 370 MHz		64.7		
			f_{IN} = 450 MHz		64.6		
HD2	Second Harmonic Distortion		f_{IN} = 10 MHz		85		dBc
			f_{IN} = 100 MHz		85		
			f_{IN} = 170 MHz		85		
			f_{IN} = 370 MHz		75		
			f_{IN} = 450 MHz		75		
HD3	Third Harmonic Distortion		f_{IN} = 10 MHz		85		dBc
			f_{IN} = 100 MHz		85		
			f_{IN} = 170 MHz		85		
			f_{IN} = 370 MHz		78.3		
			f_{IN} = 450 MHz		85		
SFDR (Non-HD2, Non-HD3)	Spur Free Dynamic Range (excluding HD2 and HD3)		f_{IN} = 10 MHz		85		dBFS
			f_{IN} = 100 MHz		85		
			f_{IN} = 170 MHz		85		
			f_{IN} = 370 MHz		83		
			f_{IN} = 450 MHz		83		
IMD3	2F1-F2, 2F2-F1, Ain = −7 dBFS		F$_{IN}$ = 169 and 171 MHz		87		dBFS

6.8 Electrical Characteristics: Sample Clock Timing Characteristics

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500 MSPS, 50% clock duty cycle, AVDD33 = 3.3 V; AVDD18 = 1.9 V; AVDDC, DVDD, IOVDD, PLLVDD = 1.8 V, –1 dBFS differential input, unless otherwise noted.

	PARAMETER	MIN	TYP	MAX	UNIT
	Aperture jitter, RMS		98		fs rms
	Data latency		38		Sample clock cycles
	Fast over-range (OVR) latency		6		
t_{PDI}	Clock aperture delay		1.1		ns

6.9 Electrical Characteristics: Digital Outputs

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3 V; AVDD18 = 1.9 V; AVDDC, DVDD, IOVDD, PLLVDD = 1.8 V.

PARAMETER		MIN	TYP	MAX	UNIT
DIGITAL OUTPUTS: JESD204B INTERFACE **(DA[0,1], DB[0,1], DC[0,1], DD[0,1])**					
Output differential voltage, |VOD|		450	577	750	mV
Transmitter short circuit current	Transmitter terminals shorted to any voltage between –0.25 and 1.45 V		45		mA
Single ended output impedance			50		Ω
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF
Unit interval, UI	5.0 Gbps		200		ps
Rise and fall times			110		ps
Output jitter			57		ps
Serial output data rate			5.0		Gbps

6.10 Timing Requirements

		MIN	TYP	MAX	UNIT
DIGITAL INPUTS: **SRESETb, SCLK, SDENb, SDATA, ENABLE, OVRA, OVRC, SYSREFCDP, SYSREFCDM**					
High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels	1.2			V
Low-level input voltage				0.4	V
High-level input current			50		µA
Low-level input current			−50		µA
Input capacitance			4		pF
DIGITAL OUTPUTS: **SDOUT, OVRA, OVRB, OVRC, OVRD**					
High-level output voltage	$I_{Load} = -100$ µA	DVDD – 0.2	DVDD		V
Low-level output voltage				0.2	V
DIGITAL INPUTS: **SYNCbABP/M, SYNCbCDP/M, SYSREFABP/M, SYSREFCDP/M**					
Input voltage VID		250	350	450	mV
Input common mode voltage VCM		0.4	0.9	1.4	V
$t_{S\_SYSREFxx}$	Referenced to rising edge of input clock		100		ps
$t_{H\_SYSREFxx}$	Referenced to rising edge of input clock		100		ps

6.11 Reset Timing

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up to active-low RESET pulse	3			ms
t_2	Reset pulse duration	Active-low RESET pulse duration	20			ns
t_3	Register write delay	Delay from RESET disable to SDENb active	100			ns
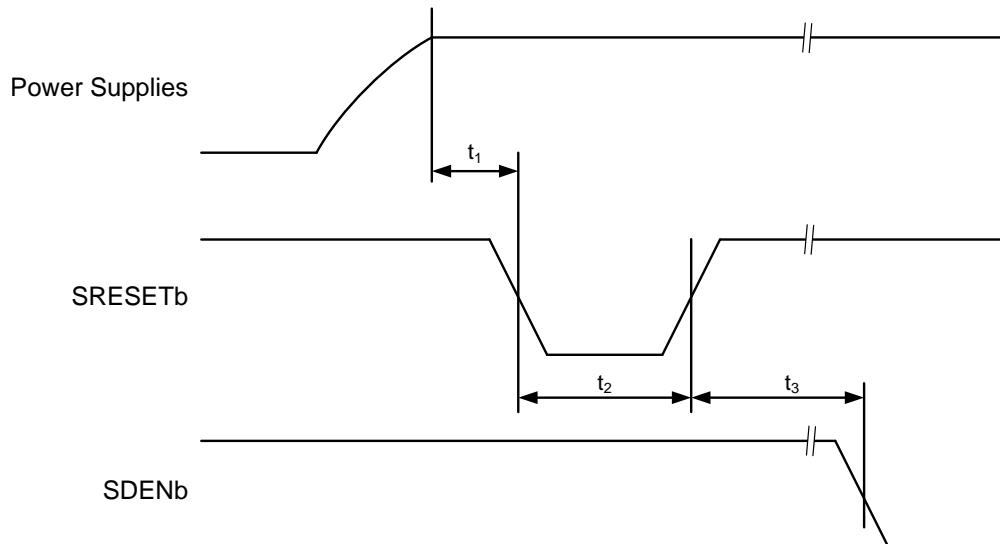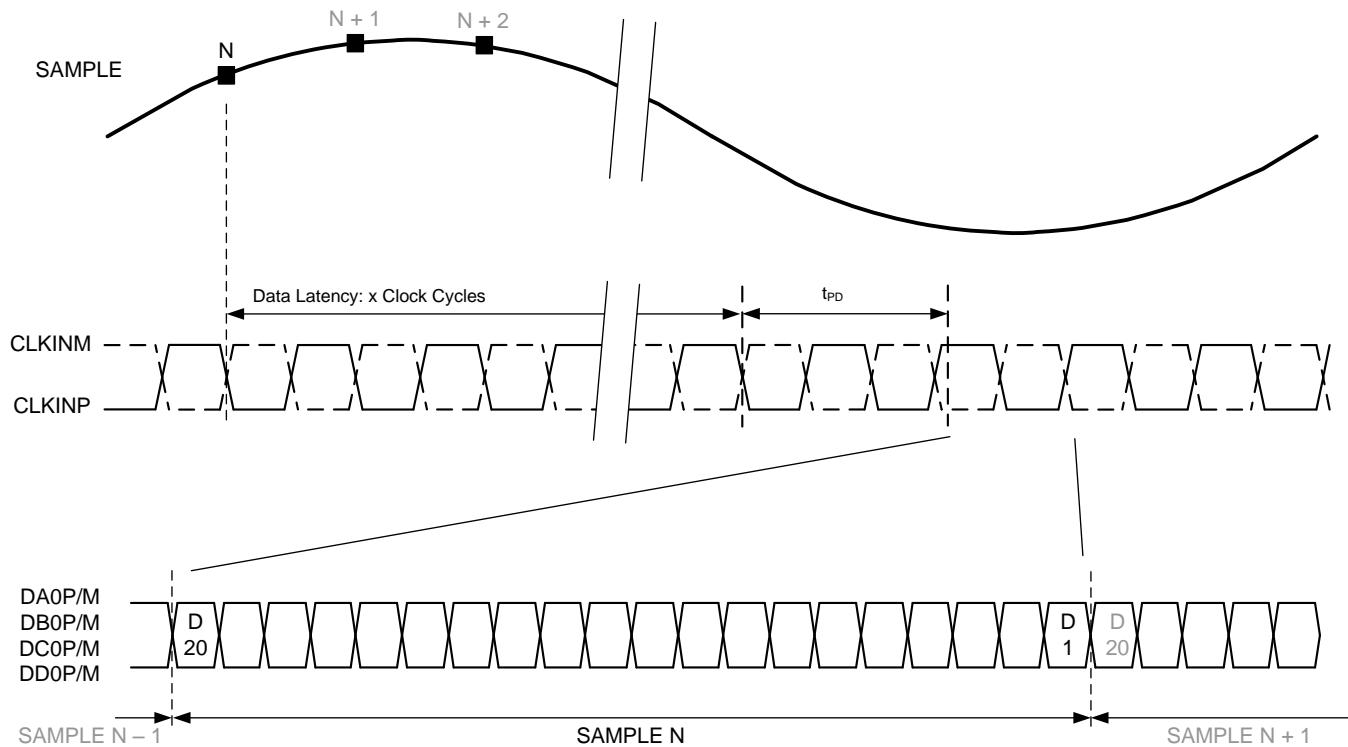
图 1. **Reset Timing Diagram**

A. t_{PD} is the propagation delay from sample clock input edge to serial data output transition

图 2. **Timing Diagram: 250 MSPS Output Data Rate**

B. t_{PD} is the propagation delay from sample clock input edge to serial data output transition
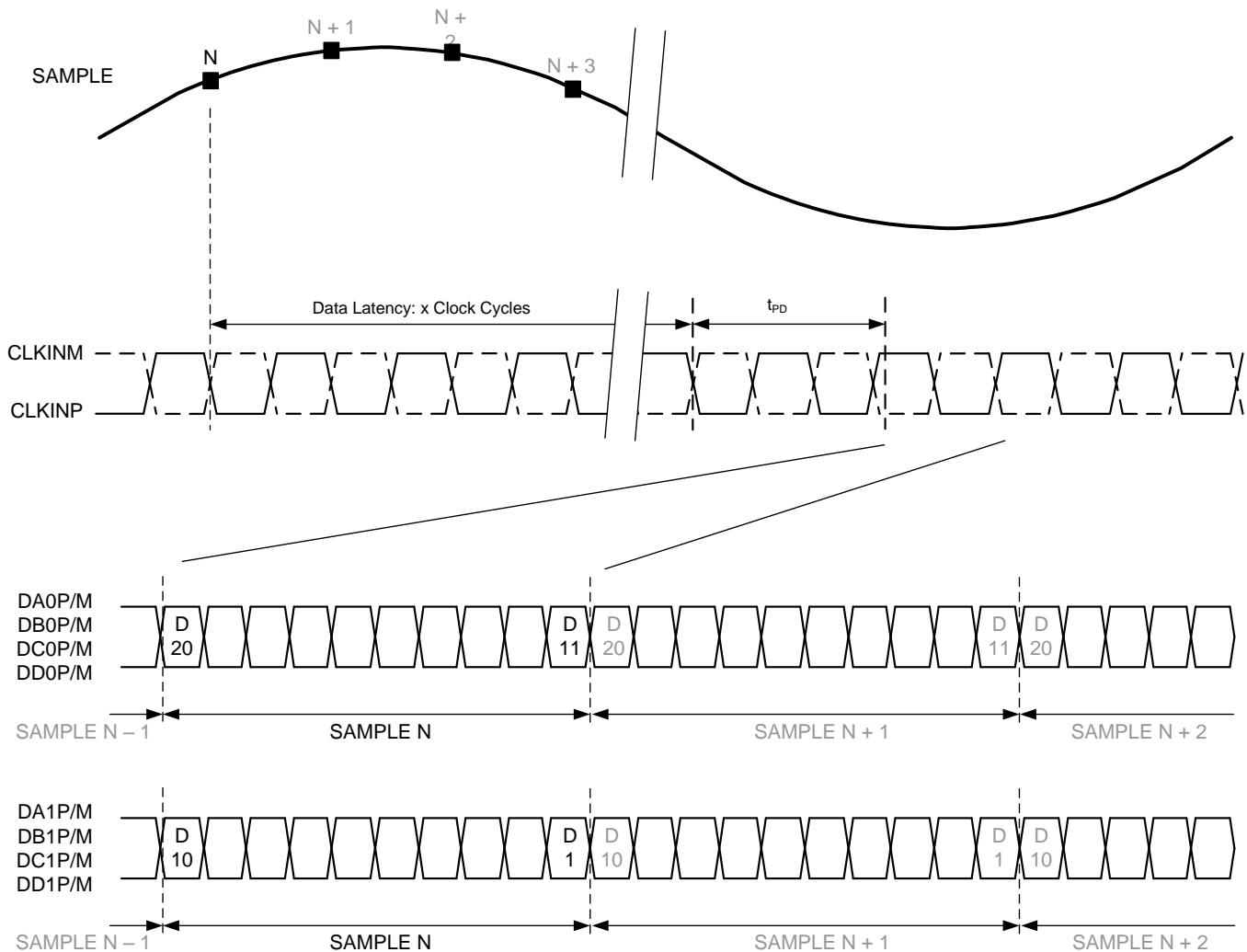
图 3. Timing Diagram: 500 MSPS Output Data Rate
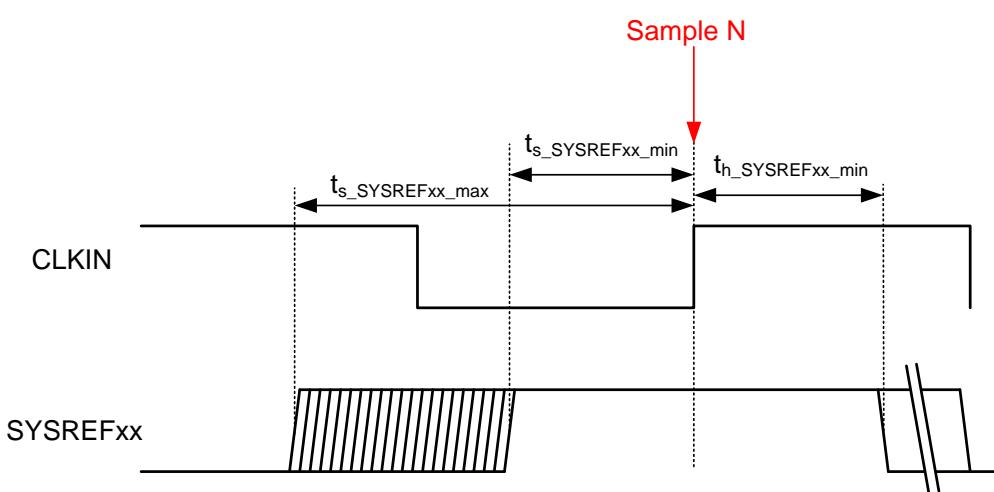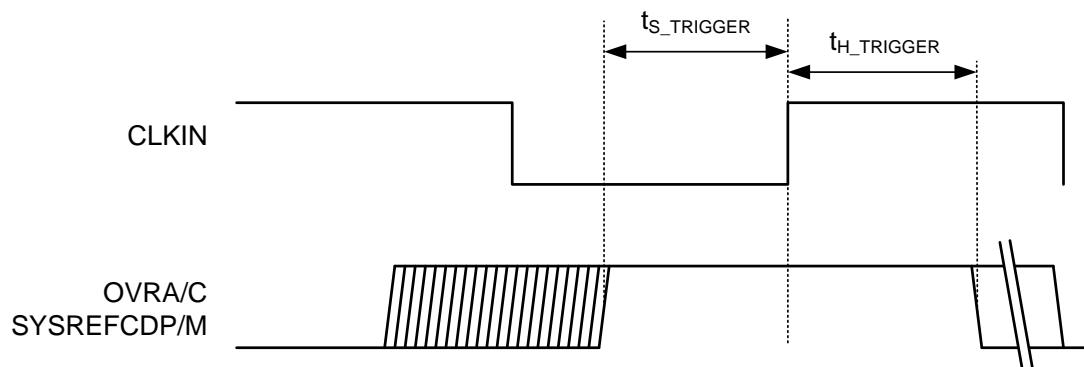
图 4. Timing Using SYSREF (Subclass 1)

C. Trigger is allowed to be asynchronous to the sample clock. If the trigger input does not meet setup and hold timing around one clock cycle, then the trigger will be caught on the next cycle.

图 5. **Timing for External Manual Trigger Input**

6.12   Typical Characteristics

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, Device clock frequency = 500 MHz,
Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD
= 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, –1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.

| Fin = 10 MHz | 1-lane 2x decimation | Ain = –1 dBFS |
| SNR = 65.29 dBFS | | SFDR = 84.72 dBc |

图 6. FFT 10 MHz

| Fin = 100 MHz | 1-lane 2x decimation | Ain = –1 dBFS |
| SNR = 65.40 dBFS | | SFDR = 82.50 dBc |

图 7. FFT 100 MHz

| Fin = 170 MHz | 1-lane 2x decimation | Ain = –1 dBFS |
| SNR = 65.34 dBFS | | SFDR = 91.62 dBc |

图 8. FFT 170 MHz

| Fin = 230 MHz | 1-lane 2x decimation | Ain = –1 dBFS |
| SNR = 65.16 dBFS | | SFDR = 76.83 dBc |

图 9. FFT 230 MHz

1-lane 2x decimation   Ain = –1 dBFS

图 10. SFDR vs Frequency

1-lane 2x decimation   Ain = –1 dBFS

图 11. SNR vs. Frequency

Typical Characteristics (接下页)

Typical values at T$_A$ = 25°C, full temperature range is T$_{MIN}$ = −40°C to T$_{MAX}$ = 85°C, Device clock frequency = 500 MHz, Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD = 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, −1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.

1-lane 2x decimation   Fin = −170 MHz

图 12. SFDR vs. Amplitude

1-lane 2x decimation   Fin = −170 MHz

图 13. SNR vs. Amplitude

1-lane 2x decimation   Fin = −170 MHz

图 14. SFDR vs. VCM

1-lane 2x decimation   Fin = −170 MHz

图 15. SNR vs VCM

1-lane 2x decimation   Ain = −1 dBFS

图 16. SFDR vs. VREF

1-lane 2x decimation   Ain = −1 dBFS

图 17. SNR vs. VREF

Typical Characteristics (接下页)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = 85°C, Device clock frequency = 500 MHz, Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD = 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, −1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 18. SFDR vs. AVDD18

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 19. SNR vs. AVDD18

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 20. SFDR vs. AVDD33

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 21. SNR vs. AVDD33

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 22. SFDR vs. PLLVDD

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 23. SNR vs PLLVDD

Typical Characteristics (接下页)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = 85°C, Device clock frequency = 500 MHz, Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD = 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, −1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz
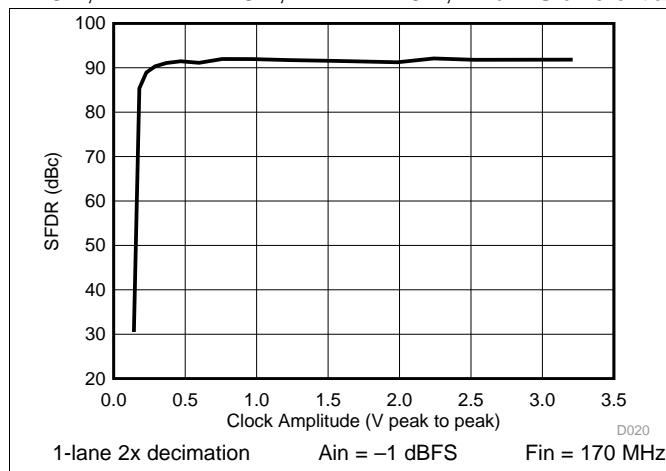
图 24. SFDR vs. Clock Amplitude

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 25. SNR vs. Clock Amplitude

Fin = 170 MHz   1-MHz spacing   1-lane 2x decimation
Ain = −7 dBFS   60 to 100 MHz shown

图 26. 2-Tone FFT

AVDD18 = 1.9 V   AVDD33 = 3.3 V   Other supplies = 1.8 V
Ain = −1 dBFS   Fin = 170 MHz
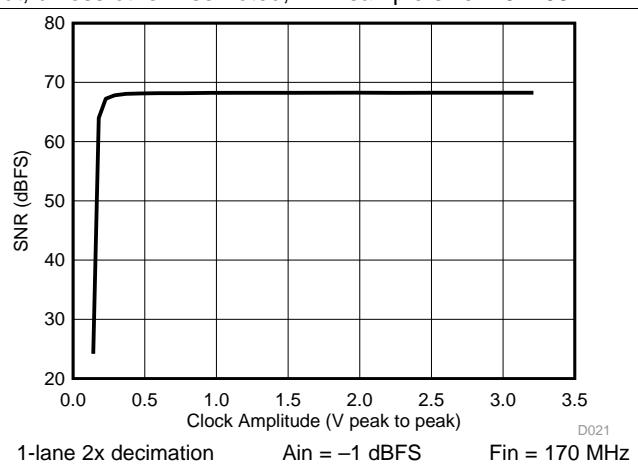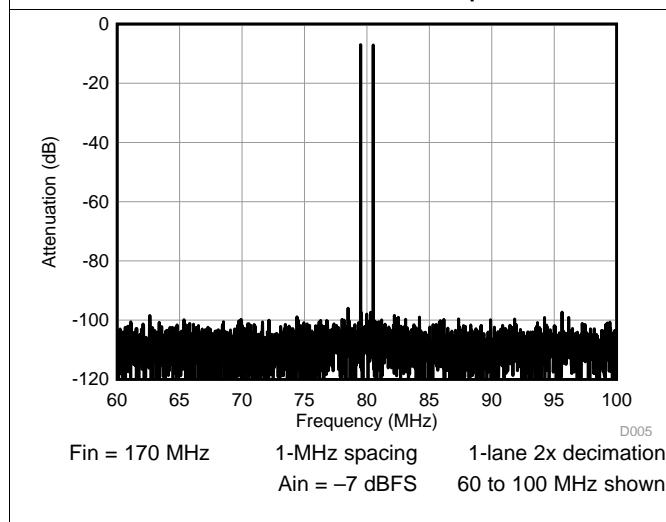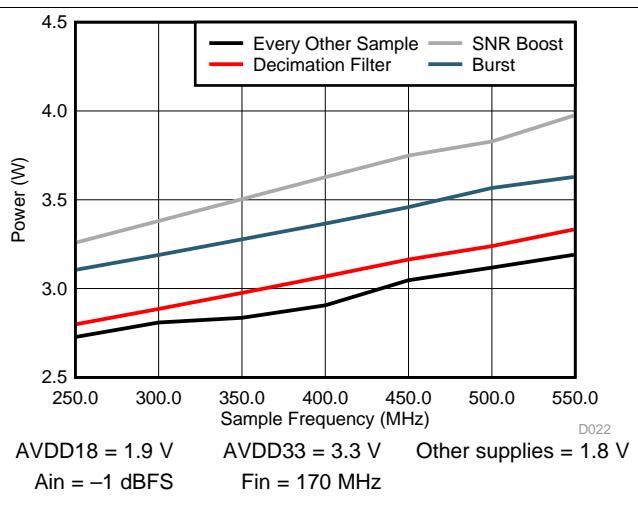
图 27. Power vs. Sample Frequency

1-lane 2x decimation   Ain = −1 dBFS   Fin = 170 MHz

图 28. Crosstalk by Channel

2-lane burst mode   Ain = −1 dBFS   Fin = 170 MHz
SNR = 65.26 dBFS   SFDR = 90.42 dBc
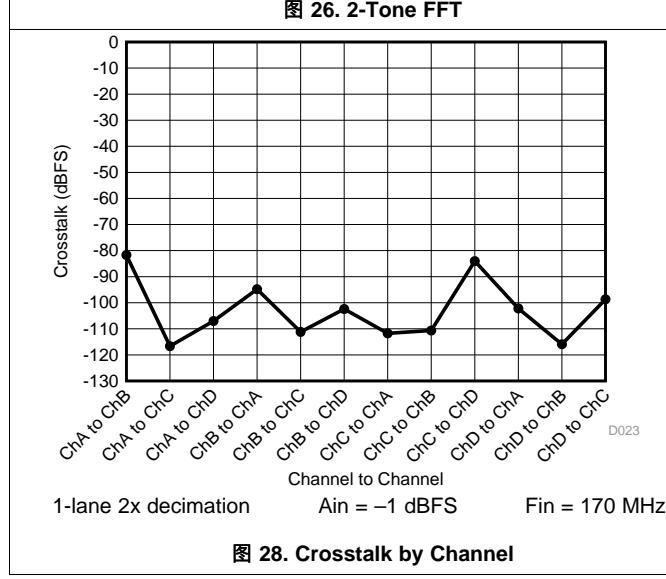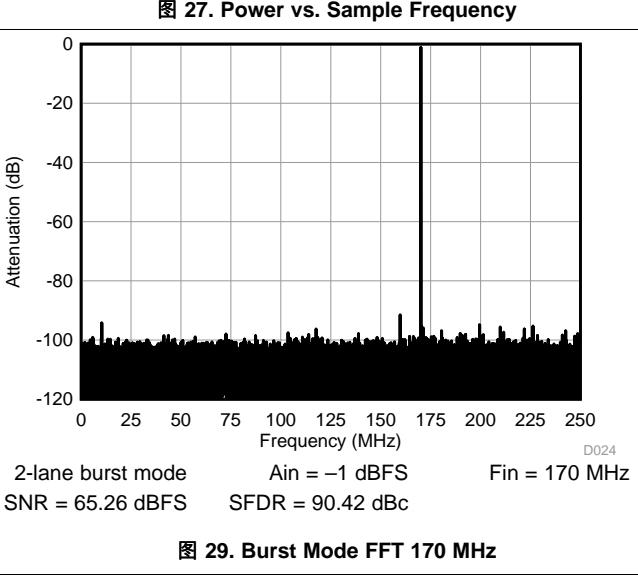
图 29. Burst Mode FFT 170 MHz

Typical Characteristics (接下页)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, Device clock frequency = 500 MHz, Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD = 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, –1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.

2-lane burst mode   Ain = –1 dBFS
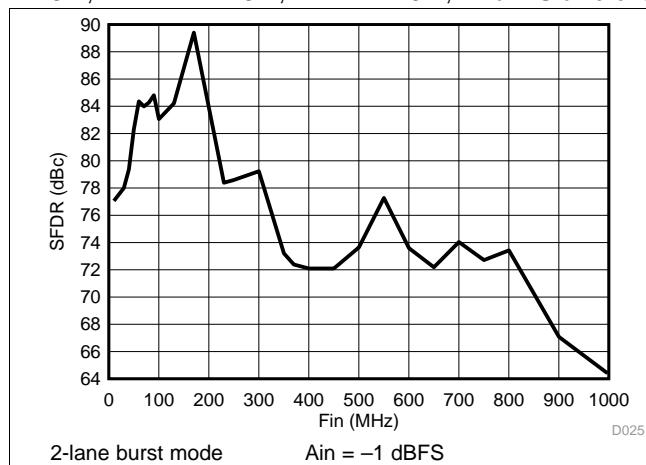
图 30. Burst Mode SFDR vs. Frequency

2-lane burst mode   Ain = –1 dBFS
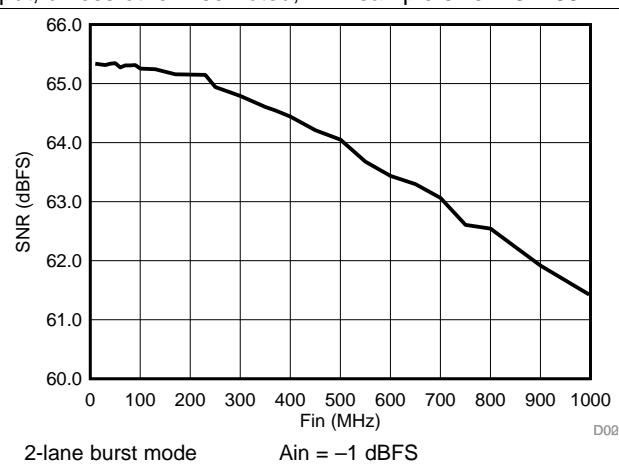
图 31. Burst Mode SNR vs Frequency

2-lane burst mode   Ain = –1 dBFS   Fin = 170 MHz
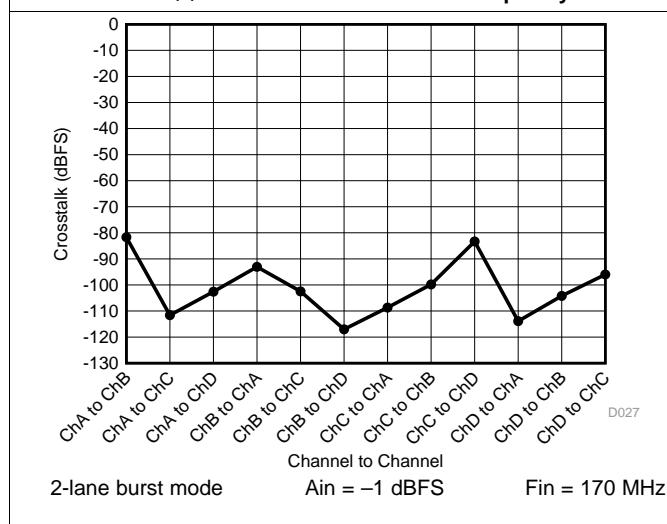
图 32. Burst Mode Crosstalk by Channel

2-lane SNR boost mode   Ain = –1 dBFS   Fin = 170 MHz
Blackman-Harris filter

图 33. SNRBoost FFT 170MHz

2-lane SNR boost mode   Ain = –1 dBFS
Blackman-Harris filter
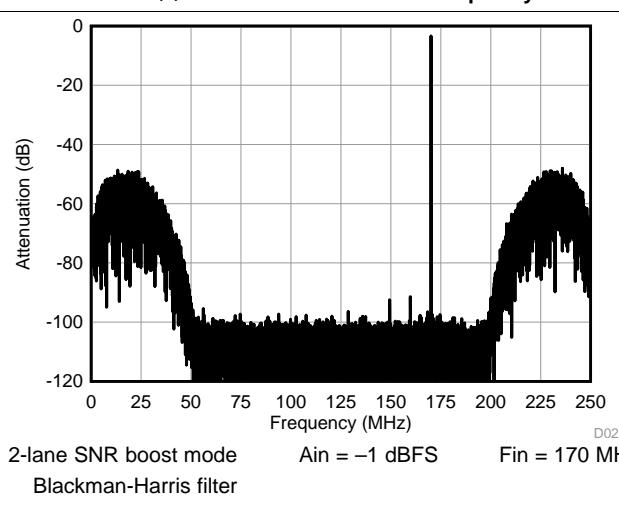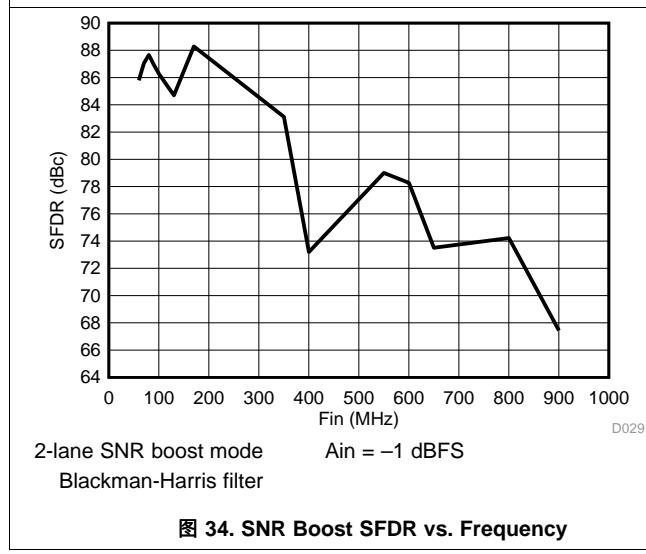
图 34. SNR Boost SFDR vs. Frequency

2-lane SNR boost mode   Ain = –1 dBFS
Blackman-Harris filter
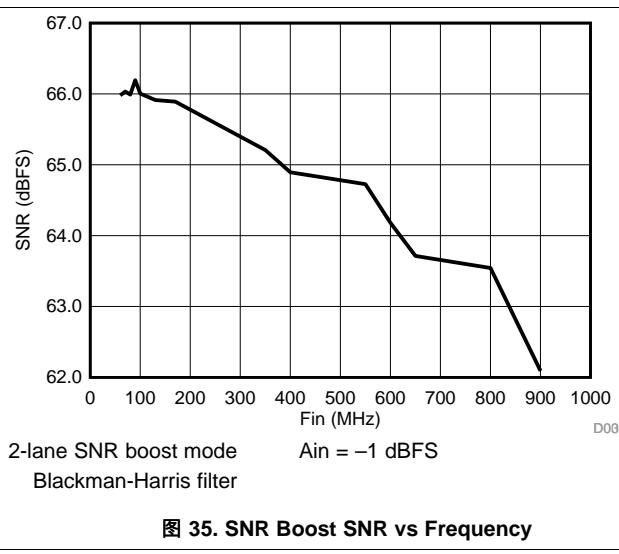
图 35. SNR Boost SNR vs Frequency

Typical Characteristics (接下页)

Typical values at T$_{A}$ = 25°C, full temperature range is T$_{MIN}$ = −40°C to T$_{MAX}$ = 85°C, Device clock frequency = 500 MHz, Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD = 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, −1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.

2-lane SNR boost mode   Ain = −1 dBFS   Fin = 170 MHz
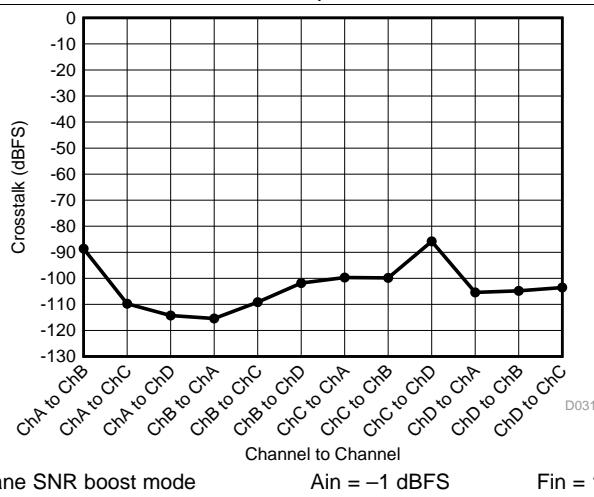
图 36. SNR Boost Crosstalk by Channel

Typical Characteristics (接下页)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = 85°C, Device clock frequency = 500 MHz, Output sample data rate = 5Gbps, 50% Device clock duty cycle, AVDD33 = 3.3 V, AVDD18 = 1.9 V, AVDDC = 1.8 V, IOVDD = 1.8 V, PLLVDD = 1.8 V, DVDD = 1.8 V, −1 dBFS differential input, unless otherwise noted, FFT sample size = 32768.
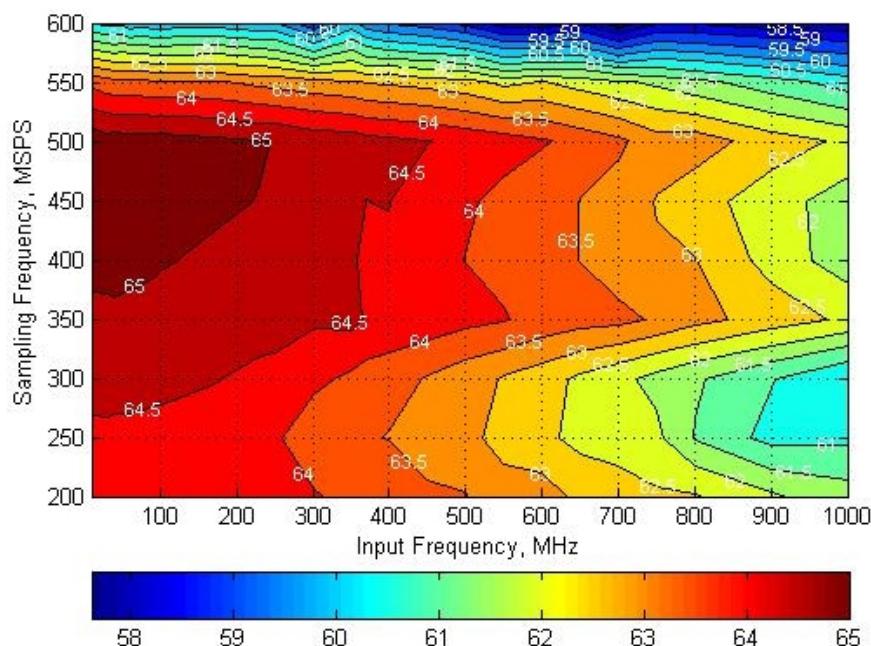

图 37. SNR Contour Plot
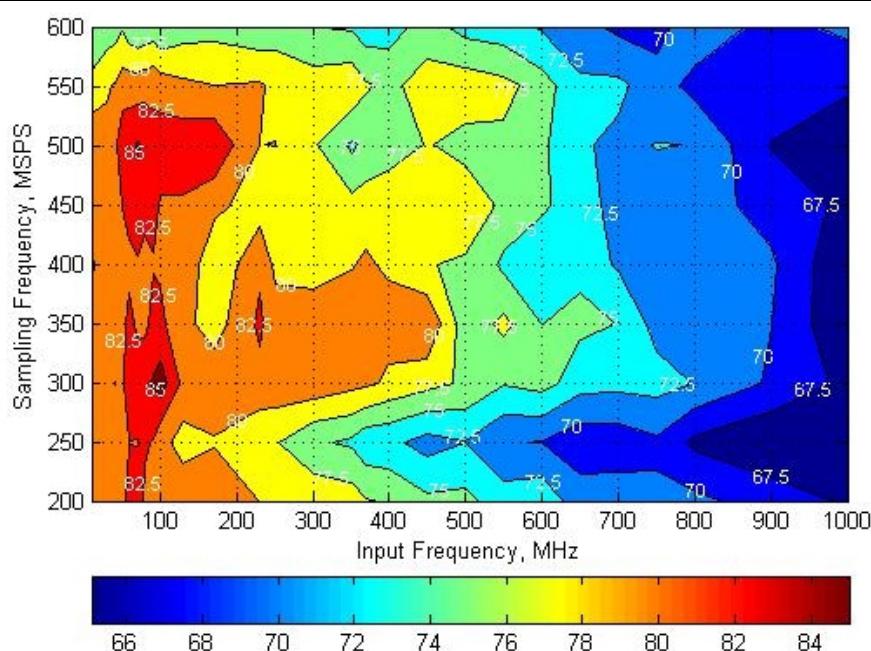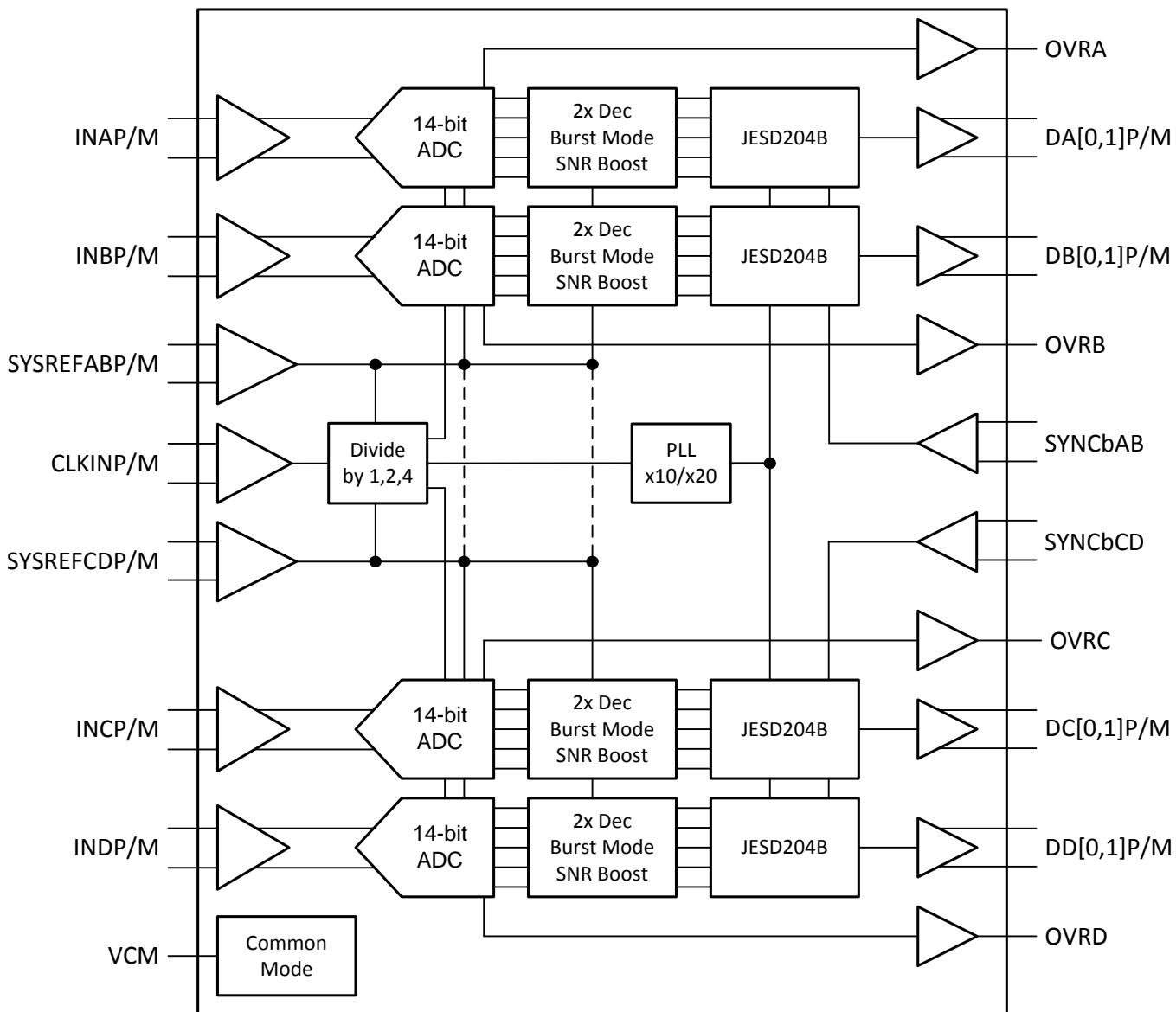
图 38. SFDR Contour Plot

7 Detailed Description

7.1 Overview

The ADS58J89 is a pin-to-pin compatible, very-low power, wide bandwidth 14-bit 250 or 500 MSPS quad channel receiver and feedback IC. It supports the JESD204B serial interface with data rates up to 5.0 Gbps supporting 1 or 2 lanes per channel. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A sampling clock divider allows more flexibility for system clock architecture design. The ADS58J89 provides excellent SFDR over a large input frequency range with very-low power consumption.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Decimation by 2 (250 MSPS Output)

Each channel has a digital filter in the data path as shown in 图 39. The filter can be programmed as a low-pass or high-pass filter and the normalized frequency response of both filters is shown in 图 40.
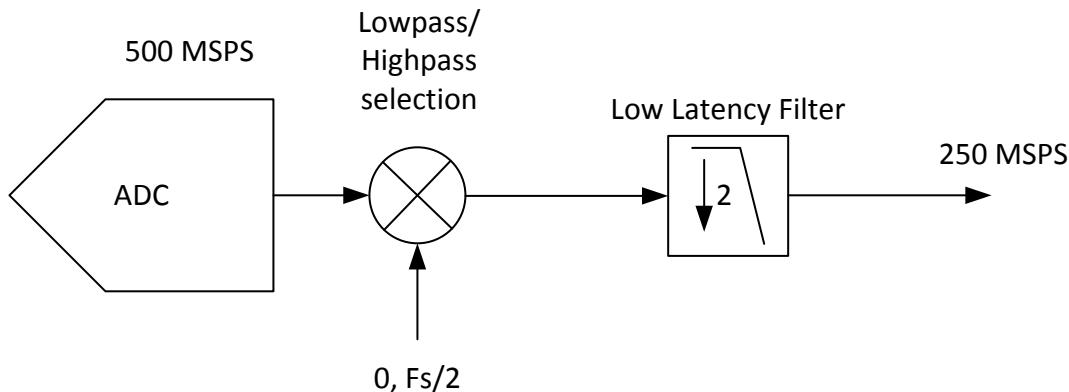
图 39. 2x Decimation Filter

The decimation filter response has a 0.1-dB pass band ripple with approximately 41% pass-band bandwidth. The stop-band attenuation is approximately 40 dB.
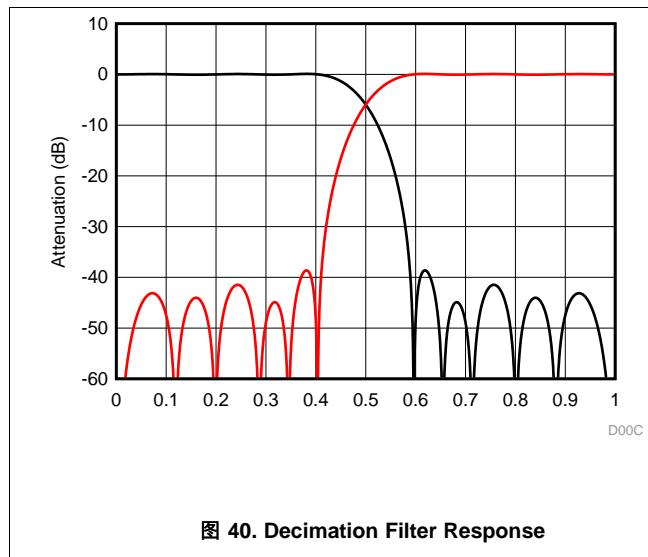
图 40. Decimation Filter Response
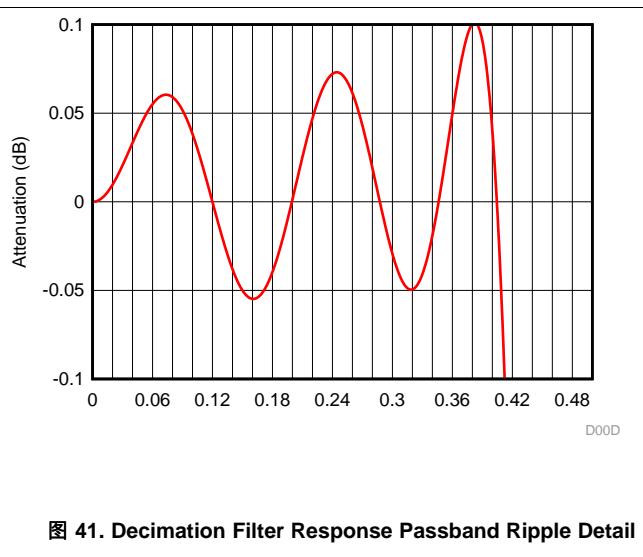
图 41. Decimation Filter Response Passband Ripple Detail

7.3.2 Over-Range Indication

The ADS58J89 provides a fast over-range indication on the OVRA, OVRB, OVRC, and OVRD pins. The fast OVR is triggered if the input voltage exceeds the programmable over-range threshold and is output after just 6 clock cycles, enabling a quicker reaction to an over-range event. The OVR threshold can be configured using SPI register writes.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the over-range threshold bits.

The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] / 8). After reset, the default value of the over-range threshold is set to 7 (decimal), which corresponds to a threshold of 1.12 dB below full scale (20 × log(7/8)).

表 **1. Fast Over Range Threshold Settings**

OVR Setting (decimal)	OVR Threshold (dBFS)
1	–18.1
2	–12.0
3	–8.5
4	–6.0
5	–4.1
6	–2.5
7 (default)	–1.1

Because the fast over-range indicator is single-ended LVCMOS logic, the ADS58J89 device can be configured through the SPI register write to keep the over-range indicator asserted high for an extra one, two, or four clock cycles. This longer assertion of the signal ensures the processor can capture the over-range event.
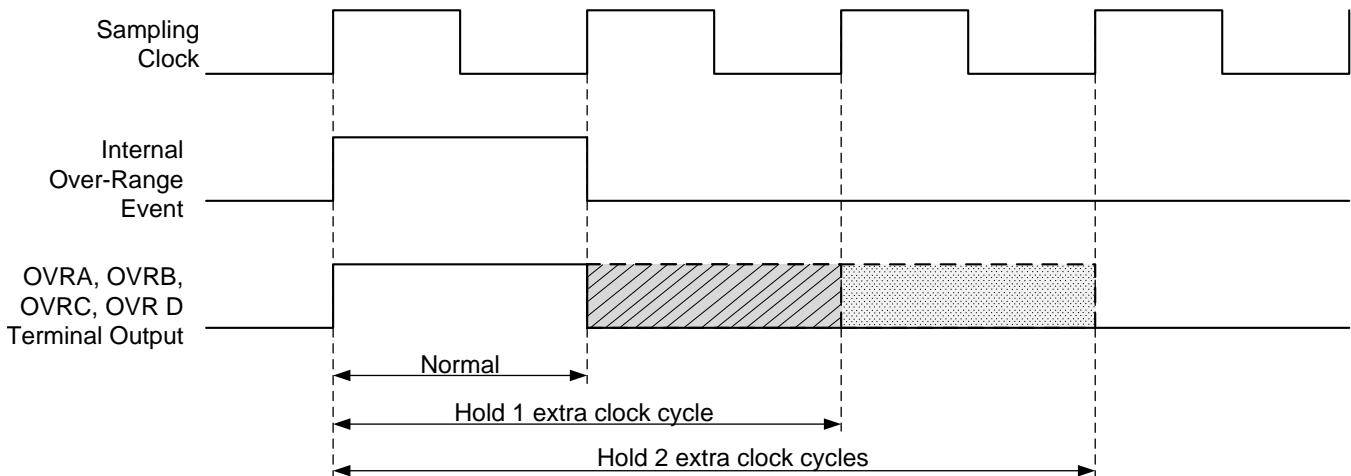
图 **42. Fast Over Range Output Timing**

The ADS58J89 device also provides the fast over-range indication bit in the JESD204B output data stream.
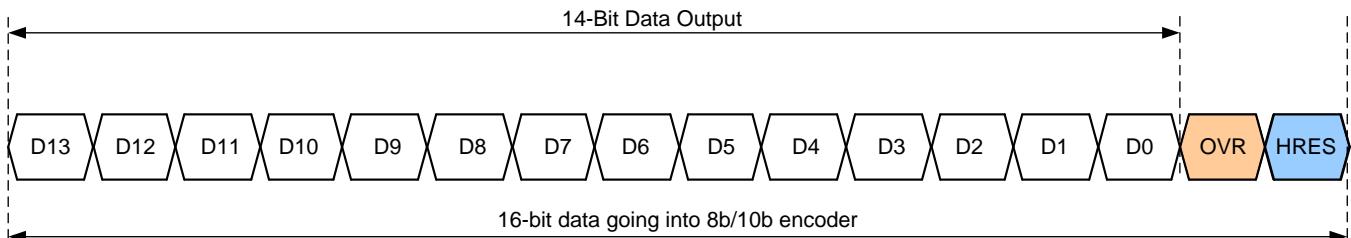
图 **43. Sample Data and Status Bit Format**

7.3.3 JESD204B Interface

The ADS58J89 supports device subclass 1 with a maximum output data rate of 5.0 Gbps for each serial transmitter. It allows independent JESD204B format configuration for channel A and B and channel C and D.

An external SYSREF signal is used to align all internal clock phases and the local multi-frame clock to a specific sampling clock edge. This allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. SYNCbAB input is used to control all the JESD204B SerDes blocks for channel A and B while SYNCbCD is used to control channel C and D. If the same LMFS configuration is used for all four channels, the SYNCbAB and SYNCbCD signals can be tied together externally and driven from the same source.

Depending on the channel output data rate, the JESD204B output interface can be operated with either 1 or 2 lanes per single channel. The JESD204B setup and configuration of the frame assembly parameters are controlled via SPI interface.

The JESD204B transmitter block consists of the transport layer, the data scrambler and the link layer. The transport layer maps the channel output data into the selected JESD204B frame data format and manages if the channel output data or test patterns are being transmitted. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNCb input signal. Optionally, data from the transport layer can be scrambled.
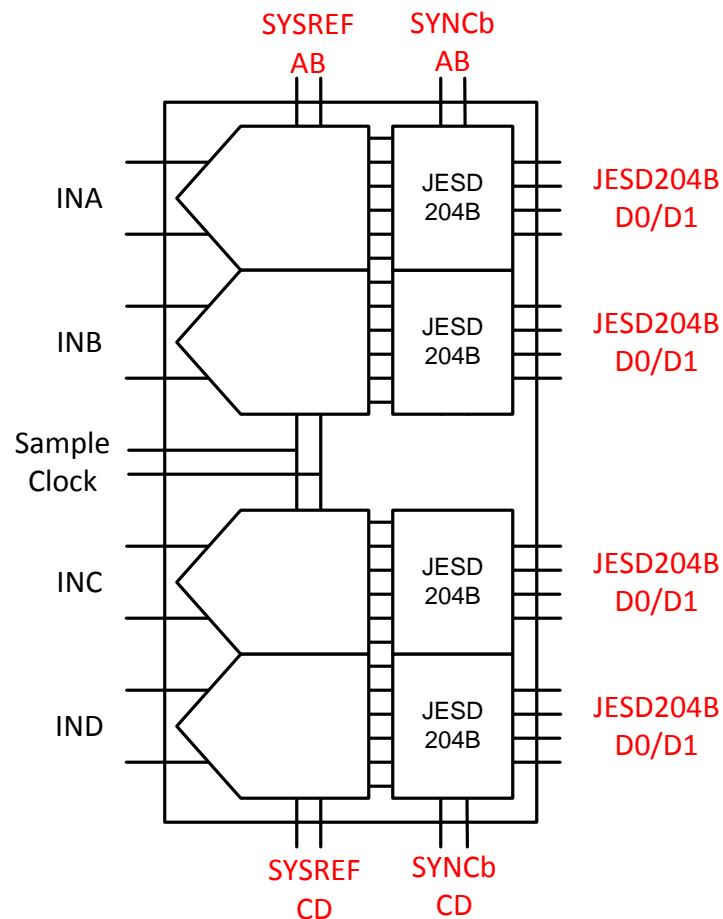
图 44. **JESD204B Lane Assignment**
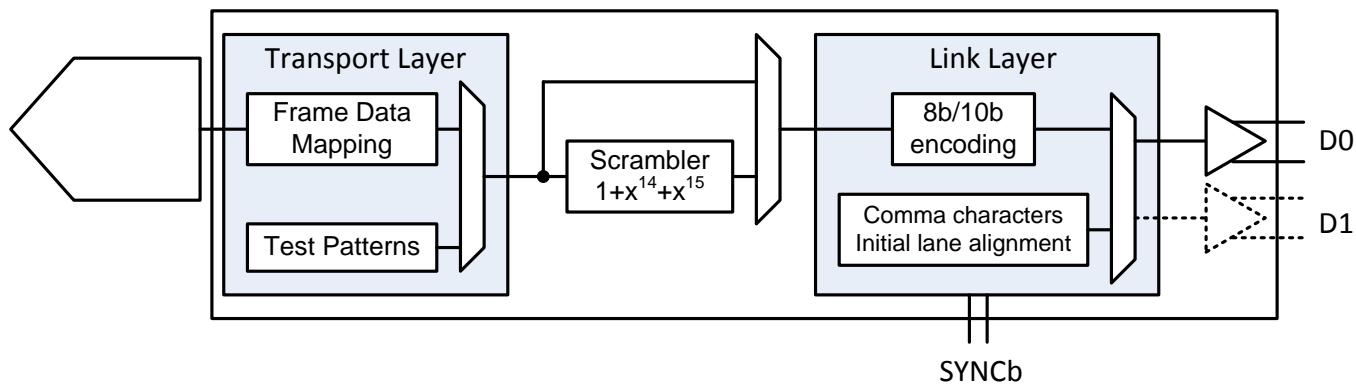
图 45. **JESD204B Block**

7.3.3.1 JESD204B Initial Lane Alignment (ILA)

The ILA process is started by the receiving device by deasserting the SYNCb signal. Upon detecting a logic low on the SYNCbAB input pins, the ADS58J89 device starts transmitting comma (K28.5) characters on channels A and B to establish code group synchronization. Upon detecting a logic high on the SYNCbCD input pins, the ADS58J89 device starts transmitting comma (K28.5) characters on channels C and D to establish code group synchronization.

After synchronization is completed, the receiving device asserts the SYNCb signal and the ADS58J89 starts the ILA sequence with the next local multi-frame clock boundary. The ADS58J89 device transmits 4 multi-frames each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the second multi-frame also contains the JESD204 link configuration data.
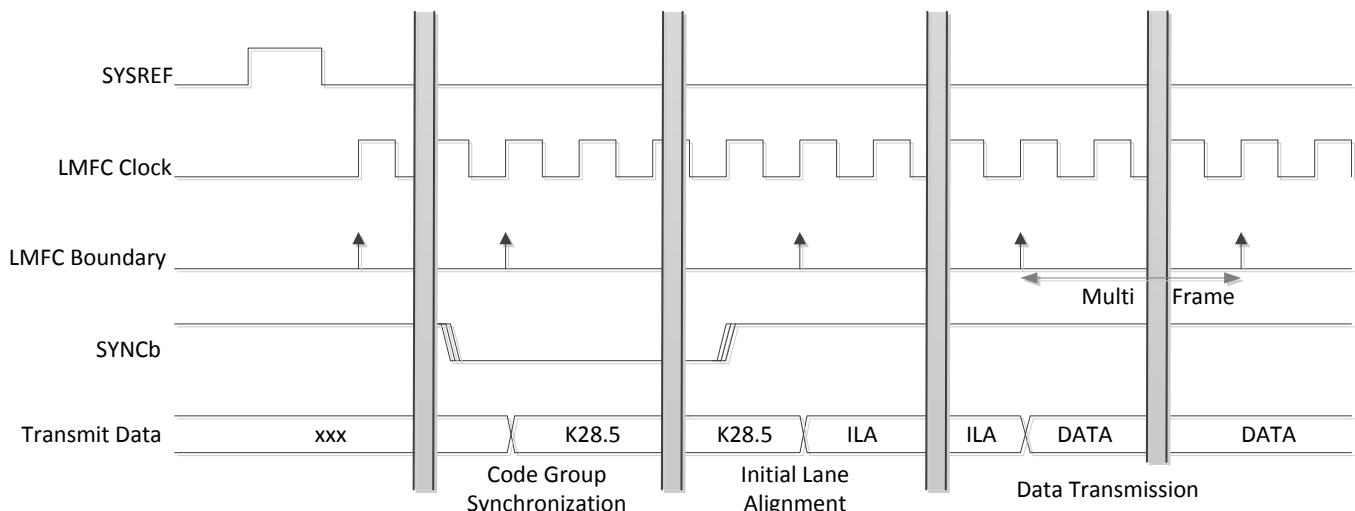
图 46. Initial Lane Assignment Format

7.3.3.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADS58J89 supports a RAMP, 1555/2AAA and different PRBS patterns. They can be enabled through SPI register write and are located in address 0x1D and 0x32/33.

7.3.3.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:
- L = number of lanes per link
- M = number of converters for device
- F = number of octets per frame clock period
- S = number of samples per frame
- HD = high density mode

The ADS58J89 supports independent configuration of the JESD204B format for channel A and B and channel C and D. 表 2 lists the available JESD204B formats and valid ranges for the ADS58J89. The ranges are limited by the SerDes line rate and the maximum channel sample frequency.

表 2. Permissible LMFS Settings

L	M	F	S	HD	Max Channel Output Rate (MSPS)	Max f_{SerDes} (Gsps)
8	4	1	1	1	500	5.0
4	4	2	1	0	250	5.0

The detailed frame assembly is shown in 表 3.

表 3. LMFS Data Formats

	LMFS = 8411				LMFS = 4421					
Lane DA0	A0[13:6]	A1[13:6]	A2[13:6]	A3[13:6]	A0[13:6]	A0[5:0], 00	A1[13:6]	A1[5:0], 00	A2[13:6]	A2[5:0], 00
Lane DA1	A0[5:0], 00	A1[5:0], 00	A2[5:0], 00	A3[5:0], 00						
Lane DB0	B0[13:6]	B1[13:6]	B2[13:6]	B3[13:6]	B0[13:6]	B0[5:0], 00	B1[13:6]	B1[5:0], 00	B2[13:6]	B2[5:0], 00
Lane DB1	B0[5:0], 00	B1[5:0], 00	B2[5:0], 00	B3[5:0], 00						
Lane DC0	C0[13:6]	C1[13:6]	C2[13:6]	C3[13:6]	C0[13:6]	C0[5:0], 00	C1[13:6]	C1[5:0], 00	C2[13:6]	C2[5:0], 00
Lane DC1	C0[5:0], 00	C1[5:0], 00	C2[5:0], 00	C3[5:0], 00						
Lane DD0	D0[13:6]	D1[13:6]	D2[13:6]	D3[13:6]	D0[13:6]	D0[5:0], 00	D1[13:6]	D1[5:0], 00	D2[13:6]	D2[5:0], 00
Lane DD1	D0[5:0], 00	D1[5:0], 00	D2[5:0], 00	D3[5:0], 00						

7.3.4 SYSREF Clocking Schemes

Periodic: The SYSREF signal is always on. This mode is supported, but not recommended as the continuous SYSREF signal appears like an additional clock input, which can cause clock mixing spurs in the channel output spectrum.

Gapped-Periodic (recommended): A periodic SYSREF signal is presented to the ADS58J89 SYSREF inputs for a very short period of time. This configuration requires a DC-coupled SYSREF connection for proper operation. Most of the time the SYSREF signal is in a logic-low state, and thus cannot cause any glitches and spurs in the channel output spectrum.

Pulse/One Shot (recommended): A single SYSREF reset pulse is used to synchronize the ADS58J89. The ADS58J89 device requires a minimum of 3 SYSREF pulses to complete the synchronization phase. The SYSREF signal is in a logic-low state most of the time, and thus cannot cause any glitches and spurs in the channel output spectrum. Special attention should be given to ensure the single pulse meets required the SYSREF input setup and hold time.

7.3.5 Split-Mode Operation

The ADS58J89 provides several different options to interface it to the digital processor or processors. If the ADS58J89 device is operated in split sampling rate (2 channels at 500-MSPS output rate and 2 channels at 250-MSPS output rate), then it requires dual SYSREF (SYSREFAB and SYSREFCD) and dual SYNC (SYNCbAB and SYNCbCD).

Subclass 1 – Deterministic Latency: The device clock and synchronous SYSREF signal are provided by the timing unit to the ADS58J89 and the processor. The processor controls the SYNCb input signals for the JESD204B state machine for all four channels. In case the ADS58J89 is connected to two different processors, the differential SYNCb inputs of the ADS58J89 can be configured to two single-ended inputs where each pin controls the JESD204B state machine of the two corresponding channels.
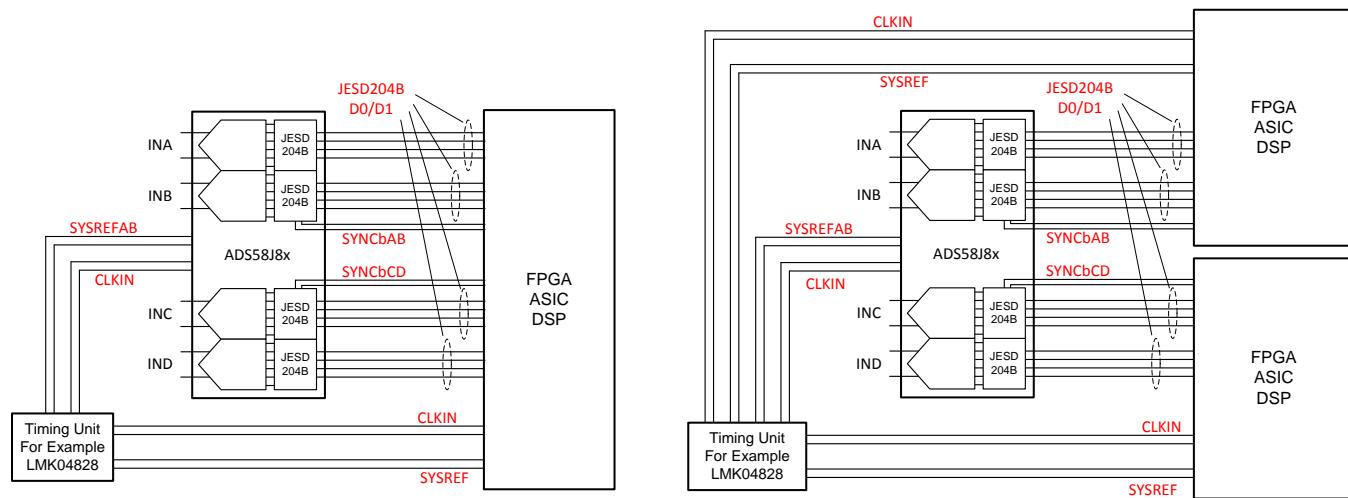
图 47. Four Channel and Dual Two Channel Usage

Split Mode Operation: If the ADS58J89 device is operated with 2-channel output at 500 MSPS and 2-channel output at 250 MSPS, then dual SYSREF (SYSREFAB for channel A and B, SYSREFCD for channel C and D) as well as dual SYNC (SYNCbAB for channel A and B, SYNCbCD for channel C and D) is required to ensure normal operation because the JESD204B link configuration is different for the two channel pairs.
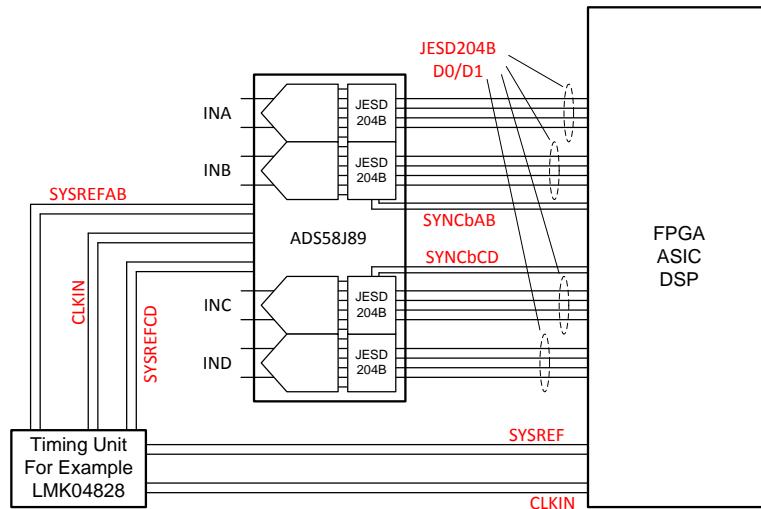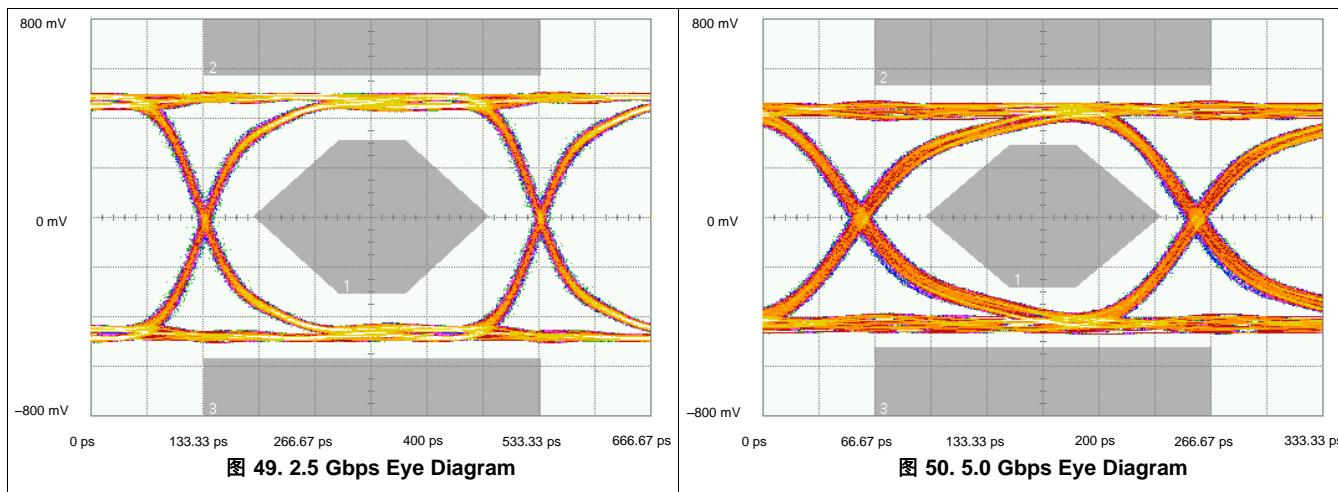
图 48. Dual SYSREF Usage

7.3.6 Eye Diagram Information

图 49 and 图 50 is the measured eye diagram at 2.5 and 5Gbps output data rate, respectively. These are overlaid with the JESD204B LV-OIF-6G-SR specification.

图 49. 2.5 Gbps Eye Diagram

图 50. 5.0 Gbps Eye Diagram

7.3.7 Analog Inputs

The ADS58J89 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high-impedance input across a very-wide frequency range to the external driving source, which enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, which results in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to 2 V using 500-Ω resistors, which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.3125 V) and (VCM − 0.3125 V), resulting in a 1.25-Vpp (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 900 MHz.
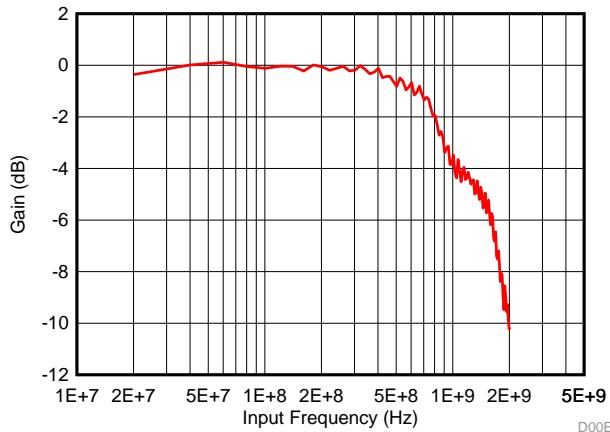
图 51. Normalized Input Bandwidth
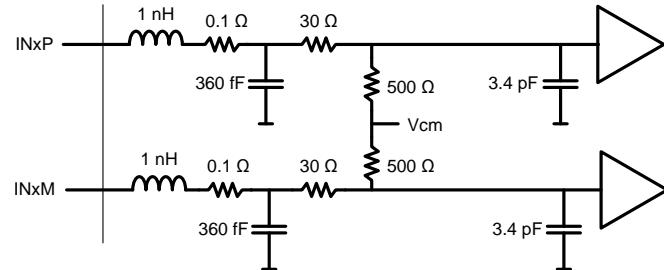
图 52. Equivalent Analog Input Circuit

7.3.8 Clock Inputs

The ADS58J89 clock input can be driven differentially with a sine wave or LVPECL source with little or no difference in performance. The common mode voltage of the clock input is set to 0.9 V using internal 2-kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close as possible to the clock inputs in order to minimize signal reflections and jitter degradation.
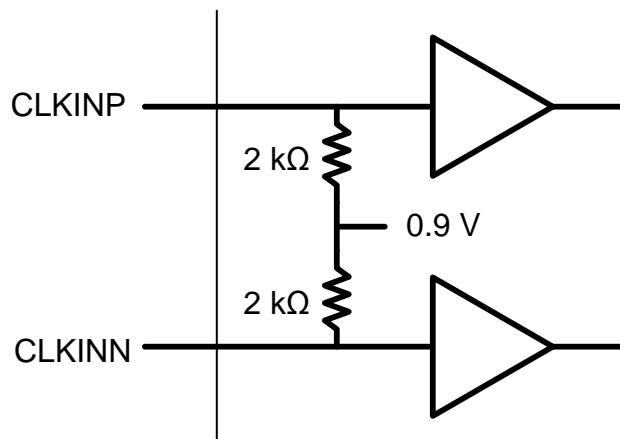
图 53. **Equivalent Clock Input Circuit**

7.3.9 Input Clock Divider

The ADS58J89 is equipped with two internal dividers on the clock input – one on channel AB and one on channel CD. The clock divider allows operation with a faster input clock simplifying the system clock distribution design. The clock dividers can be bypassed (/1) for operation with a 500-MHz clock while /2 option supports a maximum input clock of 1 GHz and the /4 option a maximum input clock frequency of 2 GHz. Different divider options can be selected for channel AB and channel CD clock output. By default the divider output of channel AB block is routed to all 4 channels but the configuration can be customized with different SPI register settings to use either the channel AB or CD divider blocks for any two channels.
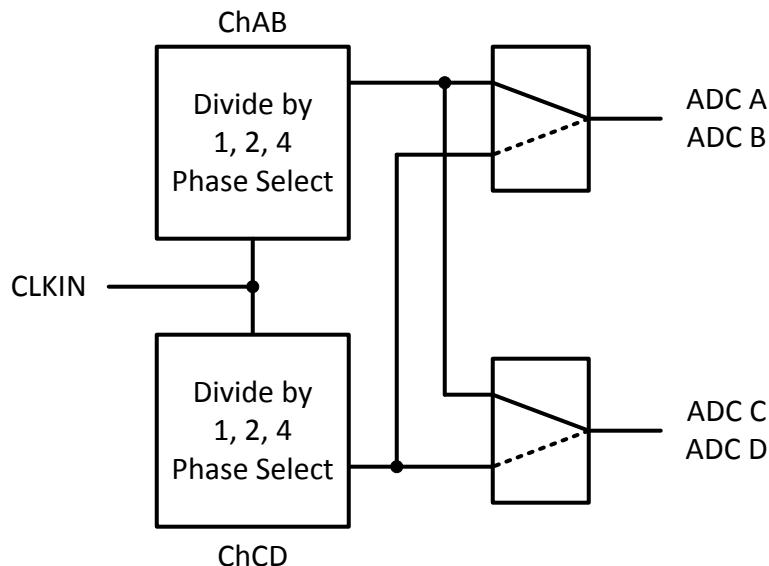
图 54. **Input Clock Divider**

7.3.10 Power-Down Control

The power down functions of the ADS58J89 can be controlled either through the parallel control pin (ENABLE) or through a SPI register setting. Power-down modes for the different channels as well as for the JESD204B interface are supported.

The ADS58J89 supports the following power-down modes. The analog sleep mode configurations are in register 0x05/06 and the JESD204b sleep mode configurations are in register 0x1E and 0x1F.

表 4. **Low-Power Mode Power Consumption and Wake-Up Times**

Configuration	Power Consumption	Wake-Up Time
Global power down	24 mW	Needs JESD resynch
Standby	31 mW	Needs JESD resynch
Deep sleep	791 mW	1.4 ms
Light sleep	1.68 W	8 µs

Control power-down function through ENABLE pin:

1. Configure power-down mode in register 0x05 and 0x1E
2. Normal operation: ENABLE pin high
3. Power-down mode: ENABLE pin low

Control power-down function through SPI (ENABLE pin always high):

1. Assign power-down mode in register 0x06 and 0x1F
2. Normal operation: 0x06 and 0x1F are 0xFFFF
3. Power-down mode: configure power down mode in register 0x06 and 0x1F

7.3.11 Device Configuration

The serial interface (SIF) included in the ADS58J89 is a simple 3- or 4-pin interface. In normal mode, 3 pins are used to communicate with the device. There is an enable (SDENb), a clock (SCLK), and a bidirectional IO port (SDATA). If the user would like to use the 4-pin interface, one write must be implemented in the 3-pin mode to enable 4-pin communications. In this mode, the SDOUT pin becomes the dedicated output. The serial interface has an 8-bit address word and a 16-bit data word. The first rising edge of SCLK after SDENb goes low will latch the read or write bit. If a high is registered, then a read is requested, if it is low, then a write is requested. SDENb must be brought high again before another transfer can be requested.

7.3.12 JESD204B Interface Initialization Sequence

After power-up, the internal JESD204B digital block must be initialized with the following sequence of steps:

1. Set JESD RESET AB/CD and JESD INIT AB/CD to 0 (address 0x0D, value 0x0000)
2. Set JESD INIT AB/CD to 1 (0x0D, 0x0202)
3. Set JESD RESET AB/CD to 1 (0x0D, 0x0303)
4. Configure all other JESD register and clock settings. If those settings change later on, this initialization sequence must be repeated.
5. Set JESD RESET AB/CD to 0 (0x0D, 0x0202)
6. Set JESD RESET AB/CD to 1 (0x0D, 0x0303)
7. Wait for two SYSREF pulses
8. Set JESD INIT AB/CD to 0 (0x0D, 0x0101)

7.3.13 Device and Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a low pulse on the SRESETb pin (of width greater than 10 ns), as shown in 图 1. If required later during operation, the serial interface registers can be cleared by applying:

- Another hardware reset using the SRESETb pin
- A software reset (bit D0 in register 0x00). This setting resets the internal registers to the default values and then self-resets the RESET bit (D0) back to 0. In this case, the RESET pin is kept high.

7.4 Device Functional Modes

7.4.1 Operating Modes

表 5 details the five different operating modes. A pair of channels (channel A and B and channel C and D) can be configured in the same operating mode.

Device Functional Modes (接下页)

表 5. Operating Modes Information

Channel Sampling Rate (MSPS)	Digital Feature	Output Data Rate (MSPS)	Output Resolution	Output SerDes Rate (GSPS)	Number of Lanes per Channel
500	Decimation by 2	250	14 bit	5.0	1
	Burst mode of every other sample	250	11 to 14 bit	5.0	1
500	SNR boost (150-MHz BW)	500	9 bit	5.0	2
	Burst mode	500	9 to 14 bit	5.0	2
	TDD-burst mode	500	9 to 14 bit	5.0	2

7.4.2 Mode Configuration

表 6 shows examples for different mode configurations for channel A/B and channel C/D regarding input options for SYSREF as well as the trigger for the different burst mode options. Each channel pair (A/B and C/D) can support each mode for 250-MSPS and 500-MSPS output.

表 6. SYSREF and Trigger Options by Operating Mode

Channel	Output Rate	Mode	SYSREF Input	Trigger Input
2	500 MSPS	SNR boost	SYSREFAB	–
2	500 MSPS	SNR boost		–
2	500 MSPS	TDD burst mode	SYSREFAB	SYSREFP/M
2	500 MSPS	TDD burst mode		OVRA/C
2	500 MSPS	TDD burst mode	SYSREFAB	SYSREFCDP/M
2	500 MSPS	Burst mode		OVRA/C
2	500 MSPS	SNR boost	SYSREFAB	SYSREFCDP/M
2	500 MSPS	Burst mode		OVRA/C
2	500 MSPS	SNR boost	SYSREFAB	OVRA/C
2	250 MSPS	Burst mode of every other sample	SYSREFCD	
2	500 MSPS	Burst mode	SYSREFAB	OVRA/C
2	250 MSPS	Decimation by 2	SYSREFCD	
2	250 MSPS	Decimation by 2	SYSREFAB	SYSREFCDP/M
2	250 MSPS	Burst mode of every other sample		OVRA/C
2	250 MSPS	Decimation by 2	SYSREFAB	–
2	250 MSPS	Decimation by 2		–

7.4.3 Output Format

表 7 provides detailed information on how the MSB or LSB get aligned for the different output data rates and resolution in the different operating modes.

表 7. Output Data Formats

Function	Output Rate	Mode	Resolution	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX	250 MSPS	Decimate by 2	14 bit	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	OVR	0
FB	250 MSPS	Burst Mode	14 bit	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	OVR	HRES
RX	500 MSPS	SNR Boost	9 bit	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	OVR	0
FB	500 MSPS	Burst Mode	11 bit	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	OVR	HRES
			12 bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	OVR	HRES
			14 bit	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	OVR	HRES

7.4.4 Burst Mode of Every Other Sample (250 MSPS Output)

In this mode, the channel is sampling at full sampling rate but the output only transmits every other sample with burst mode. During burst mode operation the output is alternated between low resolution 11-bit and high resolution 12- or 14-bit output. The burst mode operation can be configured to auto or manual trigger (see *Burst Mode*).
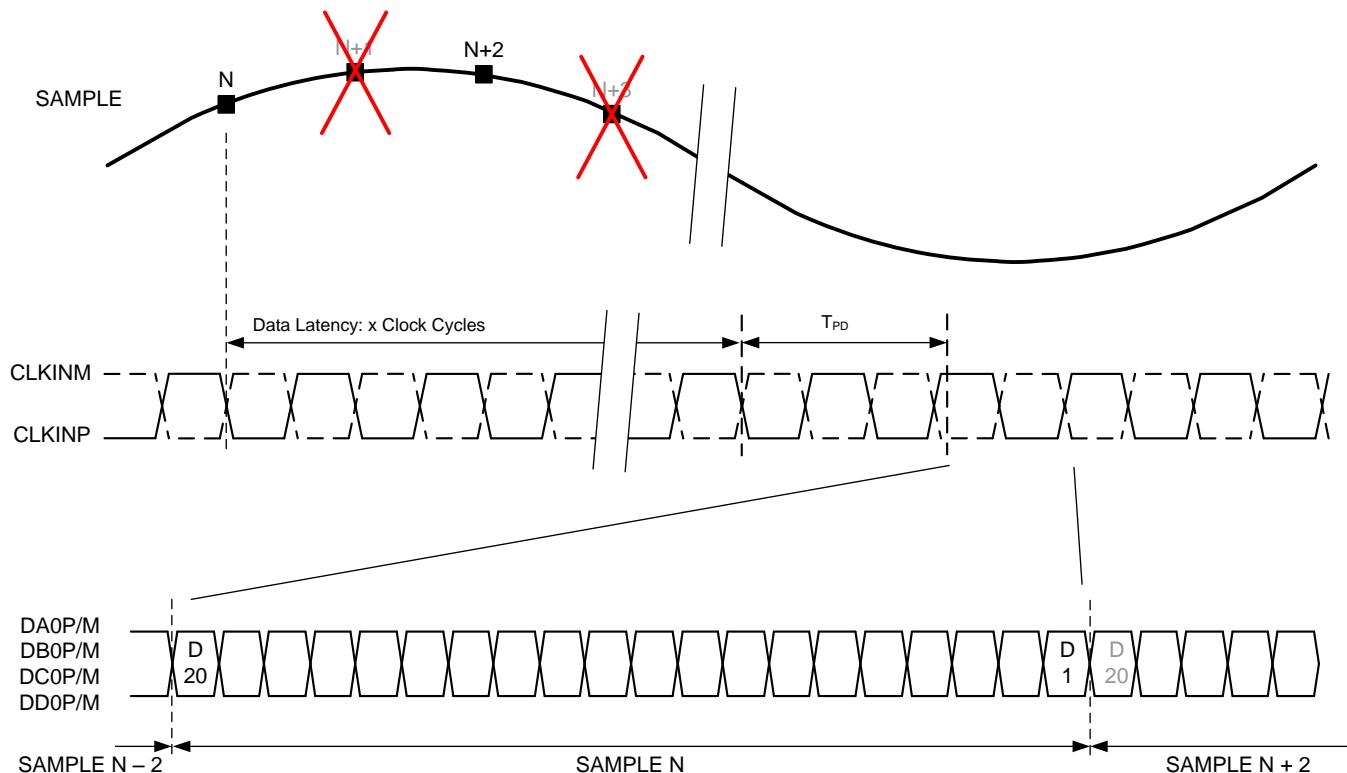

图 55. Timing Diagram Burst Mode of Every Other Sample

7.4.5 SNR Boost (500 MSPS Output)

In this mode, the channel output data is truncated to 9-bit resolution and the quantization noise is shaped using TI SNR Boost 3G technology. The SNR Boost passband bandwidth maximum is 150 MHz at 500 MSPS centered at the mid-point of the Nyquist zone.
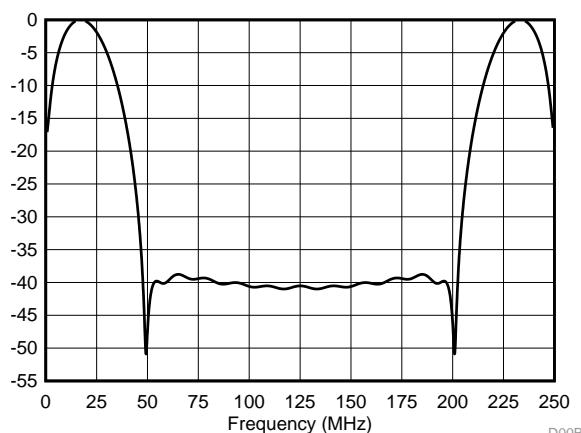
图 56. SNR Boost Noise Shape Response

7.4.6 Burst Mode

The ADS58J89 supports TI's next generation burst mode technology which can be used for the DPD feedback path as well for the receive path (TDD burst mode) in TDD applications. In receive mode, the TDD burst mode is used to support very wide band and high resolution or duty cycle operation. Both modes can also be used simultaneously where two channels operate in burst mode and two channels in TDD burst mode.

In burst mode operation, the ADS58J89 alternatively transmits low resolution (11 bit for 250 MSPS operation and 9 bit for 500 MSPS operation, LSBs are set to 0) and high resolution (11-, 12-, or 14-bit) output data and can be configured via SPI register writes. The number of low and high resolution samples is configured through programmable counters.

7.4.6.1 Burst Mode Counters

The ADS58J89 provides eight independent counters each for channel A and B and channel C and D for burst mode operation. The TDD burst mode employs all eight counters (four for the low resolution samples and four for the high resolution samples) while the normal burst mode uses only H_1 and L_1. Each count corresponds to four samples and each counter can be programmed through a 22-bit register entry (1 to 4194303).

The counter values can be updated at any time, but the update does not go into effect until the start of the next burst mode cycle with low resolution output data (L_1). After programming the counters, the ADS58J89 calculates the corresponding duty cycle for the selected high resolution output. If the duty cycle violates the limits, the digital outputs are limited to low resolution output.

$$\text{Duty Cycle} = \frac{H_1(+H_2 + H_3 + H_4)}{L_1(+L_2 + L_3 + L_4)}$$

(1)

The duty cycle limits per selected high resolution output is shown in 表 8.

表 8. Burst Mode Maximum Allowed Duty Cycle

Maximum Allowed Duty Cycle (High : Low Resolution Output)	500 MSPS	250 MSPS
14 bit	1/3	1/1
12 bit	2/3	4/1
11 bit	3/2	–

7.4.6.2 Burst Mode

The number of high and low resolution samples is $H_1 \times 2^2$ and $L_1 \times 2^2$. The maximum number of low resolution samples is $2^2 \times 2^{22} = 2^{24}$ while the maximum number of high resolution samples depends on the duty cycle.

7.4.6.3 TDD Burst Mode

The number of high and low resolution samples per cycle is $(H_1 + H_2 + H_3 + H_4) \times 2^2$ and $(L_1 + L_2 + L_3 + L_4) \times 2^2$.

In TDD burst mode, the output data gets transmitted in the following order: $L_1, H_1, L_2, H_2, L_3, H_3, L_4, H_4, L_1, H_1$, and so forth

7.4.6.4 Trigger Input

The burst mode can be operated in auto trigger or manual trigger mode while the TDD burst mode supports only the manual trigger mode.

In manual trigger mode, the trigger input releases the first high resolution data (H_1) burst after the low resolution data counter L_1 has timed out. The OVRB outputs can be configured via SPI (address 0x6F) as output flags TRDY for channel A and B. The OVRD outputs can be configured via SPI (address 0x6F) as output flags TRDY for channel C and D. Both these configurations indicate that counter L_1 timed out and the high resolution output data burst can be triggered.

The ADS58J89 provides a lot of flexibility for the configuration of the trigger input. In default operation, the single-ended input pin TRIGGERAB controls all four channels. Alternatively, the trigger input can be changed to the OVRA pin as single-ended input or as a differential input with TRIGGERAB as positive and TRIGGERCD as negative input (differential input requires external 100-Ω termination).

For simultaneous receive and DPD feedback applications, it may be more useful to split the control where the TRIGGERAB or OVRA pin controls channel A and B and the TRIGGERCD or OVRC pin controls channel C and D. In addition, the OVRB and OVRD pins can be configured to output the TRDY flag for channel A and B and channel C and D, respectively.

The trigger input for channel A/B and channel C/D can each be selected with 2 register bits (address 0x2C and 0x3A) as shown in 表 9.

表 9. Burst Mode Trigger Sources

Register Setting	Trigger Source
00	TRIGGERAB (= pin SYSREFCDP)
01	TRIGGERCD (= pin SYSREFCDM)
10	OVRA (for channel A/B) OVRC (for channel C/D)
11	TRIGGERAB/CD (as differential LVDS input, single trigger input for all 4 channels)

7.4.6.5 Manual Trigger Mode

Upon enabling manual trigger mode, the ADS58J89 starts transmission of low resolution data. As soon as the L_1 counter is finished, the manual trigger is unlocked and the high resolution output H_1 or burst mode sequence of H_1, L_2, H_2, L_3, H_3, L_4, H_4, L_1 can be triggered. After the low resolution counter L_1 is finished, the next high resolution output or burst mode sequence can be triggered again. The HRES flag is embedded in the JESD204B output data stream. The counter values can be updated until a new burst mode cycles starts with transmission of low resolution samples.

See 图 57 for an example of normal burst mode with manual trigger.
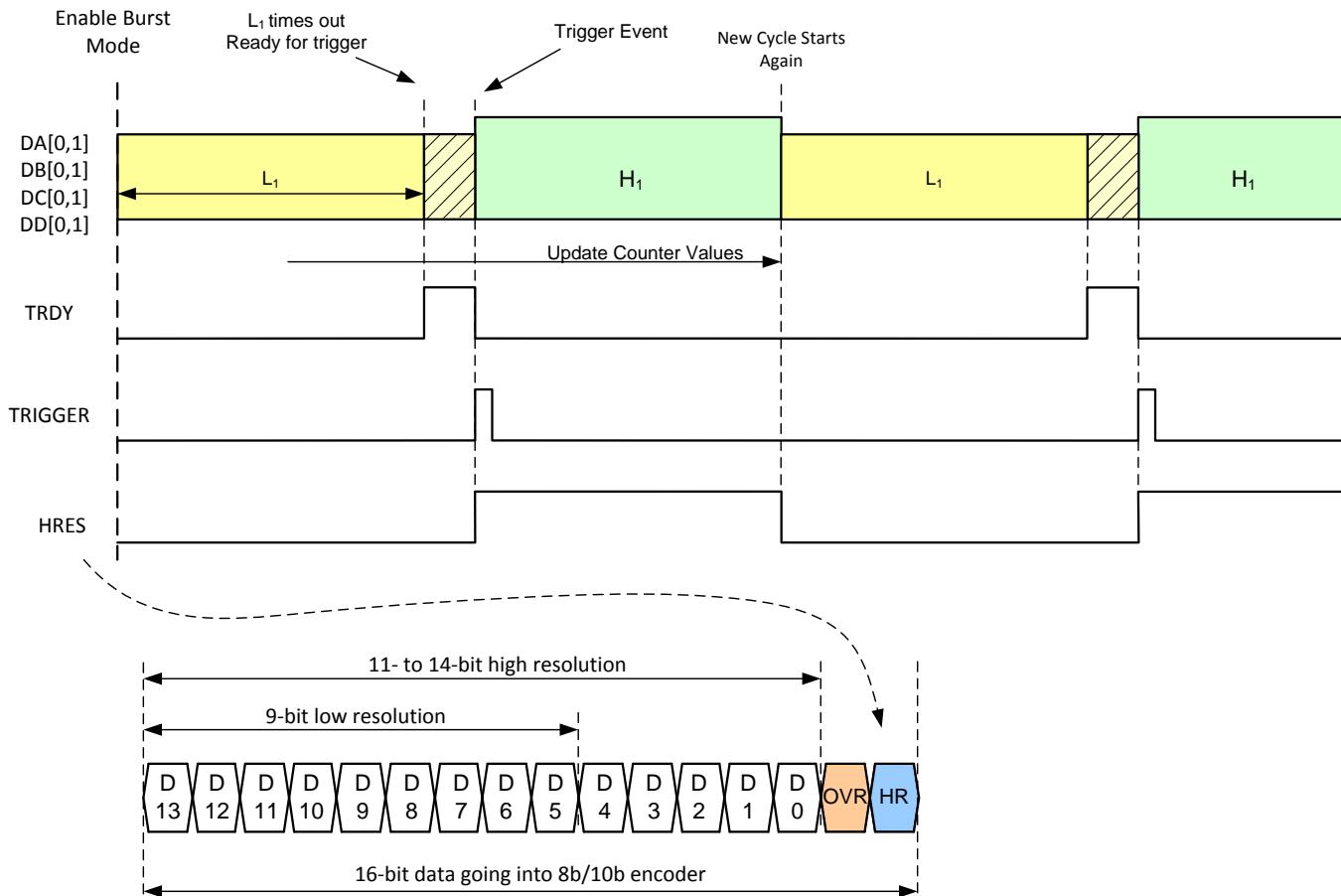
图 57. Burst Mode Duty Cycle Timing

See 图 58 for an example of TDD burst mode with manual trigger:
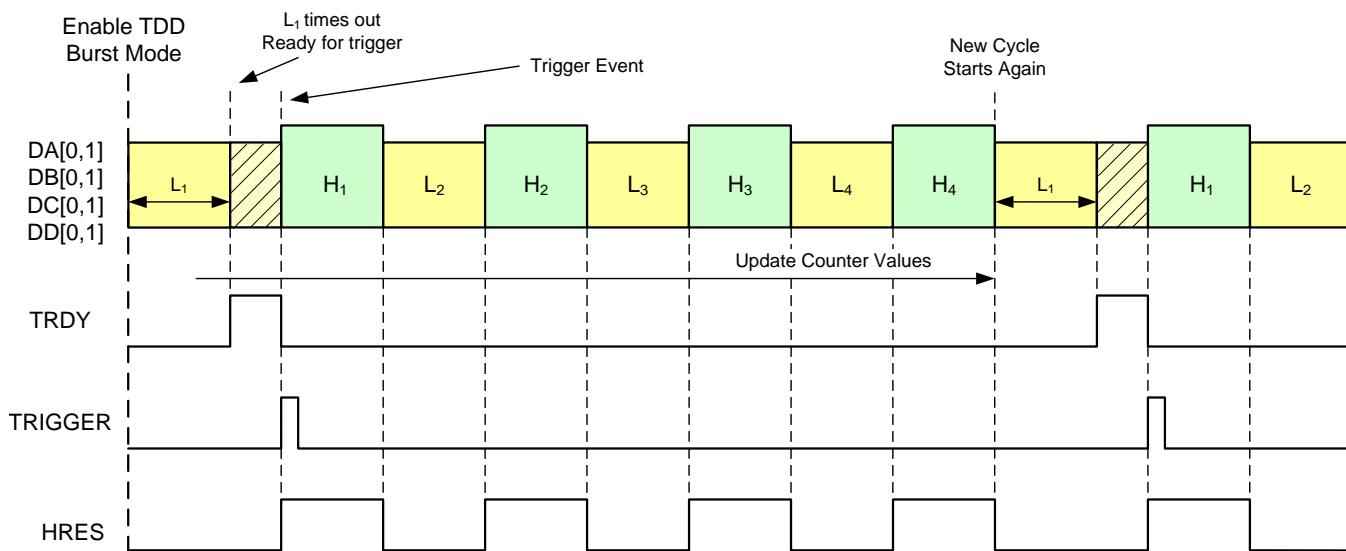
图 58. TDD Burst Mode Duty Cycle Timing

7.4.6.6 Auto Trigger Mode

This mode is primarily intended for the DPD observation path. Upon enabling auto trigger mode, the ADS58J89 starts transmission of low resolution data. As soon as the L_1 counter is finished, the ADS58J89 immediately begins transmitting the high resolution output H_1. The HRES flag can also be embedded in the JESD204B output data stream. The counter values can be updated until a new burst mode cycles starts with transmission of low resolution samples. Any input on the trigger input pins is ignored.

See 图 59 for an example of normal burst mode with automatic trigger:
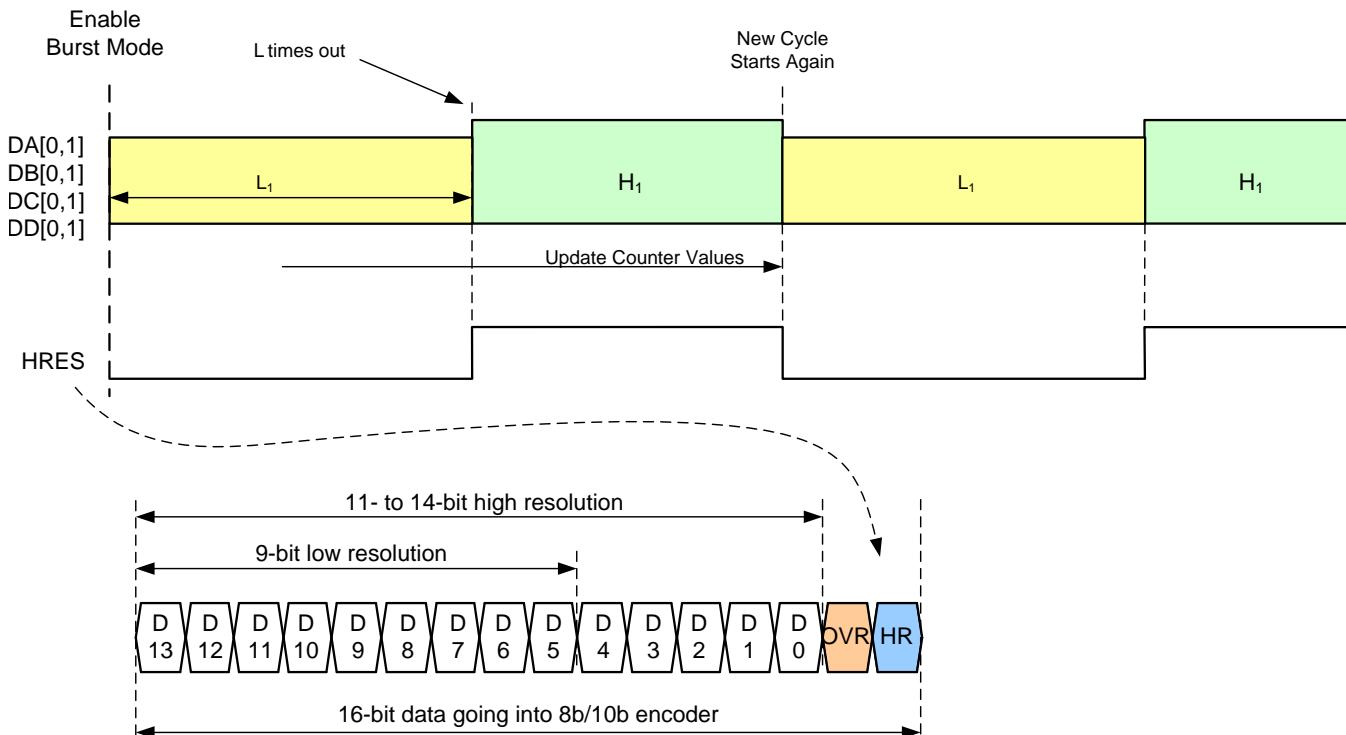
图 59. Auto-Trigger Mode Duty Cycle Timing

7.4.6.7 *TDD-Burst Mode*

This mode is intended for the receive path in TDD LTE receivers. The individual counters for high and low resolution output data can be programmed so that the high resolution samples line up with receive (uplink) frames and the low resolution samples line up with transmit (downlink) and setup frames where no data is present in the receive path.

表 10. TDD Burst Mode Duty Cycle

Option	Number of Setup Frames	Number of Downlink Frames	Number of Uplink Frames	Duty Cycle	High Resolution Output (500 MSPS)
1		8	1	1:9 (0.11)	14 bit
2		7	2	2:8 (0.25)	14 bit
3	1	6	3	3:7 (0.43)	12 bit
4		5	4	4:6 (0.67)	11/12 bit
5		1 to 4	5 to 8	(1+)	11 bit
6		6	2	2:8 (0.25)	14 bit
7	2	5	3	3:7 (0.43)	12 bit
8		4	4	4:6 (0.67)	11/12 bit
9		1 to 3	5 to 7	>1	11 bit

7.4.6.7.1 TDD Burst Mode Examples

Following are two examples to illustrate the intention for the TDD burst mode. The TDD frame has 10 equal size sub frames. For the downlink-uplink (DL-UL) configuration number 2 for example, the high and low resolution counters can be set for a given channel sampling rate to match the downlink-uplink profile as shown in 图 60. The manual trigger is used to initiate the high resolution output data, which maintains synchronization. The counter L_1 covers the low resolution data across two consecutive TDD frames and most of setup frame.

For configuration number 2, a duty cycle of approximately 2 / 8 can be achieved; with a sampling rate of 500 MSPS, the high resolution output of 14 bit can be used.

DL-UL Config	Subframe Number									
	0	1	2	3	4	5	6	7	8	9
2	D	S	U	D	D	D	S	U	D	D
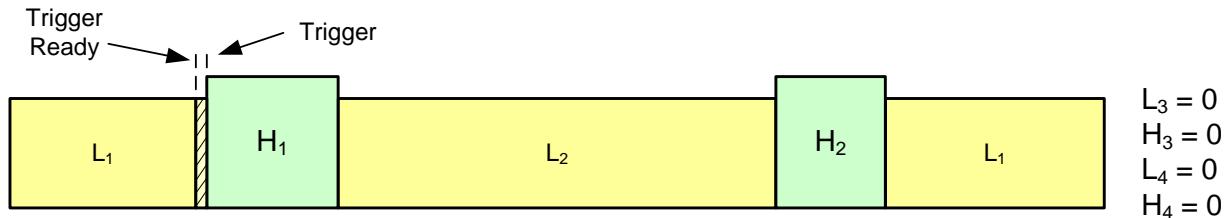
图 60. TDD Burst Mode Example 1

For configuration number 3, a duty cycle of approximately 3 / 7 can be achieved and only two counters have to be programmed. With a sampling rate of 500 MSPS, a high resolution output of 12 bit can be used.

DL-UL Config	Subframe Number									
	0	1	2	3	4	5	6	7	8	9
3	D	S	U	U	U	D	D	D	D	D

$L_2 = 0$
$H_2 = 0$
$L_3 = 0$
$H_3 = 0$
$L_4 = 0$
$H_4 = 0$
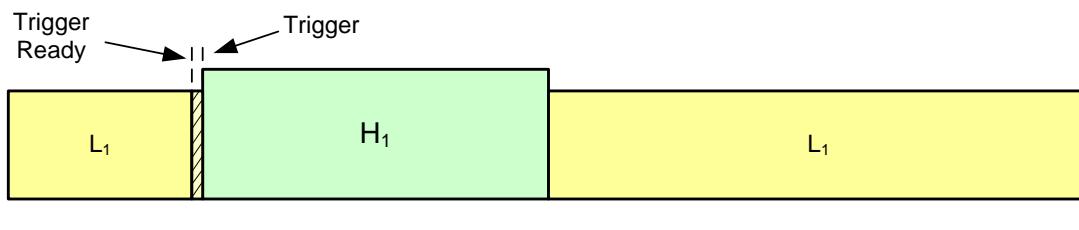
图 61. TDD Burst Mode Example 2

7.5 Programming

7.5.1 Serial Register Write

The internal register of the ADS58J89 can be programmed following these steps:

1. Drive SDENb pin low.
2. Set the R/W bit to '0' (bit A7 of the 8 bit address).
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be written.
4. Write 16-bit data which is latched on the rising edge of SCLK.

表 11. Serial Register Read or Write Timing[1]

	PARAMETER	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	>DC		10	MHz
t_{SLOADS}	SDENb to SCLK setup time	50			ns
t_{SLOADH}	SCLK to SDENb hold time	50			ns
t_{DSU}	SDATA setup time	50			ns
t_{DH}	SDATA hold time	50			ns

(1) Typical values at 25°C; minimum and maximum values across the full temperature range: $T_{MIN} = -40°C$ to $T_{MAX} = 85°C$, AVDD33 = 3.3 V; AVDD18, AVDDC, DVDD, IOVDD, PLLVDD = 1.8 V, unless otherwise noted.
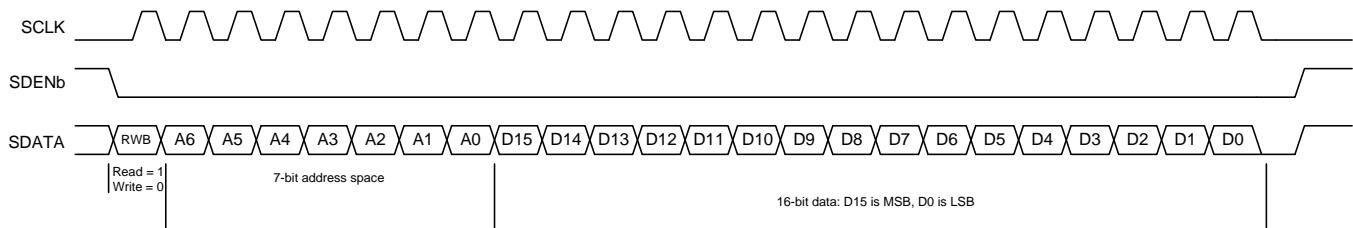
图 62. Serial Register Write Timing Diagram

7.5.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT and SDATA pins. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the channel.

1. Drive SDENb pin low.

2. Set the RW bit (A7) to 1. This setting disables any further writes to the registers.

3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be read.

4. The device outputs the contents (D15 to D0) of the selected register on the SDOUT/SDATA pin.

5. The external controller can latch the contents at the SCLK rising edge.

6. To enable register writes, reset the RW register bit to 0.
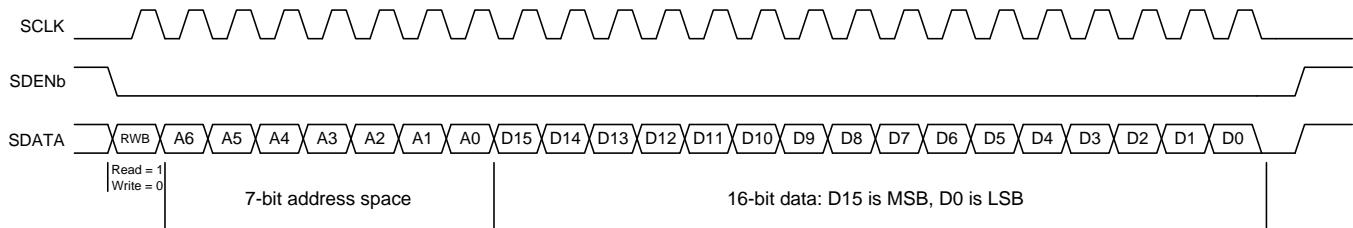
图 63. Serial Register Read Timing Diagram

7.6 Register Maps

Register Address A7 to A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						Register Data										
0	3/4 WIRE	FORMAT	DEC EN AB	HP/LP AB	0	DEC EN CD	HP/LP CD	0	SNRB EN AB	SNRB EN CD	0	0	0	0	0	RESET
1	MODE 1	0	1	0	FOVR THRESH AB		FOVR LENGTH AB		FOVR THRESH CD		FOVR LENGTH CD				1	0
2	0	1	BM RES		DISCARD AB	DISCARD CD	0	0	0	0	0	0	0	0	0	0
3	0	CLK SEL CD	CLK DIV CD		0	CLK PHASE SELECT CD			SYSREF SEL CD	CLK SEL AB	CLK DIV AB		0	CLK PHASE SELECT AB		
4	OVRA OUT EN	OVRB OUT EN	OVRC OUT EN	OVRD OUT EN	SYSREF AB DELAY		SYSREF CD DELAY		0	0	0	0	SYNCb AB EN	SYNCb CD EN	1	1
5	ANALOG SLEEP MODES – ENABLE PIN															
6	ANALOG SLEEP MODES – SPI															SYSREF CD EN
7	0	0	0	0	0	0	CLK SW AB	1	0	1	0	0	0	1	0	0
8	0	0	0	0	0	0	CLK SW CD	1	0	1	0	0	0	1	0	0
C	0	0	1	1	0	0	0	1	1	1	SYSREF JESD MODE CD			SYSREF JESD MODE AB		
D	0	0	0	0	0	0	JESD INIT CD	JESD RESET CD	0	0	0	0	0	0	JESD INIT AB	JESD RESET AB
E	0	0	0	0	0	0	0	0	TX LANE EN CD				TX LANE EN AB			
F	0	0	0	0	0	0	CTRL F AB		0	0	0	0	0	0	CTRL M AB	
10	0	0	0	0	0	0	CTRL K AB					0	0	0	CTRL L AB	
13	0	0	0	0	0	0	0	0	0	INV SYNCb AB	HD AB	SCR EN AB	0	0	0	0
16	0	0	0	0	0	0	CTRL F CD		0	0	0	0	0	0	CTRL M CD	
17	0	0	0	0	0	0	CTRL K CD					0	0	0	CTRL L CD	
1A	0	0	0	0	0	0	0	0	0	INV SYNCb CD	HD CD	SCR EN CD	0	0	0	0
1D	0	0	0	0	0	0	0	0	0	TEST PATTERN EN CD	TEST PATTERN EN AB	0	TEST PATTERN	0	0	0
1E	0	0	0	0	0	0	JESD SLEEP MODES – ENABLE PIN									
1F	1	1	1	1	1	1	JESD SLEEP MODES – SPI									

Register Maps (接下页)

Register Address	Register Data															
A7 to A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
20	JESD LANE POLARITY INVERT								PRBS EN							
21	0	PRBS SEL		0	0	0	0	0	0	0	0	0	0	VREF SEL		

表 12.

Register Address A7 to A0 in hex	Register Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24	TDD BURST MODE COUNTER L1 [15:0] AB															
25	TDD BURST MODE COUNTER L2 [15:0] AB															
26	TDD BURST MODE COUNTER L3 [15:0] AB															
27	TDD BURST MODE COUNTER L4 [15:0] AB															
28	TDD BURST MODE COUNTER H1 [15:0] AB															
29	TDD BURST MODE COUNTER H2 [15:0] AB															
2A	TDD BURST MODE COUNTER H3 [15:0] AB															
2B	TDD BURST MODE COUNTER H4 [15:0] AB															
2C	BM TRIG AB		TDD BURST MODE COUNTER L2 [21:16] AB						0	0	TDD BURST MODE COUNTER L1 [21:16] AB					
2D	0	0	TDD BURST MODE COUNTER L4 [21:16] AB						0	0	TDD BURST MODE COUNTER L3 [21:16] AB					
2E	0	0	TDD BURST MODE COUNTER H2 [21:16] AB						0	0	TDD BURST MODE COUNTER H1 [21:16] AB					
2F	AUTO TRIG AB	TDD EN AB	TDD BURST MODE COUNTER H4 [21:16] AB						0	0	TDD BURST MODE COUNTER H3 [21:16] AB					
32	TDD BURST MODE COUNTER L1 [15:0] CD															
33	TDD BURST MODE COUNTER L2 [15:0] CD															
34	TDD BURST MODE COUNTER L3 [15:0] CD															
35	TDD BURST MODE COUNTER L4 [15:0] CD															
36	TDD BURST MODE COUNTER H1 [15:0] CD															
37	TDD BURST MODE COUNTER H2 [15:0] CD															
38	TDD BURST MODE COUNTER H3 [15:0] CD															
39	TDD BURST MODE COUNTER H4 [15:0] CD															
3A	BM TRIG CD		TDD BURST MODE COUNTER L2 [21:16] CD						0	0	TDD BURST MODE COUNTER L1 [21:16] CD					
3B	0	0	TDD BURST MODE COUNTER L4 [21:16] CD						0	0	TDD BURST MODE COUNTER L3 [21:16] CD					
3C	0	0	TDD BURST MODE COUNTER H2 [21:16] CD						0	0	TDD BURST MODE COUNTER H1 [21:16] CD					
3D	AUTO TRIG CD	TDD EN CD	TDD BURST MODE COUNTER H4 [21:16] CD						0	0	TDD BURST MODE COUNTER H3 [21:16] CD					
63	0	0	0	0	0	0	0	TEMP SENSOR								
64	PRE EMP SEL AB			PRE EMP EN AB			DCC EN AB			0	0	0	0			
67	OUTPUT CURRENT CONTROL AB															
68	PRE EMP SEL CD			PRE EMP EN CD			DCC EN CD			0	0	0	0			
6B	OUTPUT CURRENT CONTROL CD															

表 12. (接下页)

Register Address	Register Data															
A7 to A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
6C	0	0	0	0	0	0	0	0	0	0	TDD RATIO CD	TDD RATIO AB	BM RATIO CD	BM RATIO AB	JESD PLL CD	JESD PLL AB
6F	0	0	0	0	0	0	0	0	0	TRDY EN AB	0	0	0	0	0	TRDY EN CD

7.6.1 Register Descriptions

7.6.1.1 Register Address 0

图 64. Register Address 0, Default 0x0000, Hex = 0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3/4 WIRE	FORMAT	DEC EN AB	HP/LP AB	0	DEC EN CD	HP/LP CD	0	SNRB EN AB	SNRB EN CD	0	0	0	0	0	RESET

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. Register Address 0 Field Descriptions

Bit	Field	Type	Reset	Description
D15	3/4 WIRE			Enables 4-bit serial interface when set 0 = 3-wire SPI (SDATA is bidirectional) 1 = 4-wire SPI (SDOUT is data output)
D14	FORMAT			Selects digital output format 0 = Output is 2s complement 1 = Offset binary
D13	DEC EN AB			Enables decimation filter for channel AB 0 = Normal operation 1 = Decimation filter enabled
D12	HP/LP AB			Determines high-pass or low-pass configuration of decimation filter for channel AB 0 = Low pass 1 = High pass
D10	DEC EN CD			Enables decimation filter for channel CD 0 = Normal operation 1 = Decimation filter enabled
D9	HP/LP CD			Determines high-pass or low-pass configuration of decimation filter for channel CD 0 = Low pass 1 = High pass
D7	SNRB EN AB			Enables SNR boost for channel AB 0 = Normal operation 1 = SNR boost enabled
D6	SNRB EN CD			Enables SNR boost for channel CD 0 = Normal operation 1 = SNR boost enabled
D0	RESET			Software reset, self clears to 0 0 = Normal operation 1 = Execute software reset

7.6.1.2 Register Address 1

图 65. Register Address 1, Default 0xAF7A, Hex = 1
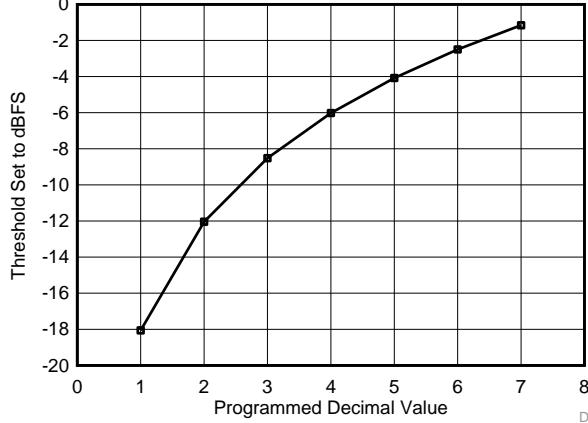
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MODE 1	0	1	0	FOVR THRESH AB			FOVR LENGTH AB		FOVR THRESH CD			FOVR LENGTH CD		1	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 14. Register Address 1 Field Descriptions

Bit	Field	Type	Reset	Description
D15	MODE 1			Set bit D15 to 0 for optimum performance
D13				Reads back 1

表 14. Register Address 1 Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
D11:D9	FOVR THRESH AB			Sets fast OVR thresholds for channel A and B The fast over-range detection is triggered 6 output clock cycles after the overload condition occurs. The threshold at which the OVR is triggered is: Input full scale × [decimal value of <over-range threshold>] / 8. After power-up or reset, the default value is 7 (decimal), which corresponds to an OVR threshold of 1.16-dB below full scale (20 × log(7/8)). 图 66. OVR Detection Threshold
D8:D7	FOVR LENGTH AB			Determines minimum pulse length for FOVR output 00 = 1 clock cycle 01 = 2 clock cycles 10 = 4 clock cycles 11 = 8 clock cycles
D6:D4	FOVR THRESH CD			Sets fast OVR thresholds for channel C and D See description for channel A and B
D3:D2	FOVR LENGTH CD			Determines minimum pulse length for FOVR output 00 = 1 clock cycle 01 = 2 clock cycles 10 = 4 clock cycles 11 = 8 clock cycles
D1				Reads back 1

7.6.1.3 Register Address 2

图 67. Register Address 2, Default: 0x4000, Hex = 2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BM RES		DISCARD AB	DISCARD CD	0	0	0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 15. Register Address 2 Field Descriptions

Bit	Field	Type	Reset	Description
D14				Reads back 1
D13:D12	BM RES			Sets high resolution output for burst mode and TDD burst mode 00 = 14-bit high resolution output 01 = 12-bit high resolution output 10 = 11-bit high resolution output 11 = 9-bit high resolution output (in 500-MSPS operation, burst mode is disabled)

表 15. Register Address 2 Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
D11	DISCARD AB			Outputs every other sample with 11-bit resolution for channel A and B. Burst mode is used if output resolution is set to 12 or 14 bit (bit D13 to D12). 0 = Normal operation 1 = Discard mode enabled
D10	DISCARD CD			Outputs every other sample with 11-bit resolution for channel C and D. Burst mode is used if output resolution is set to 12 or 14 bit (bit D13 to D12). 0 = Normal operation 1 = Discard mode enabled

7.6.1.4 Register Address 3

图 68. Register Address 3, Default: 0x4040, Hex = 3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	CLK SEL CD	CLK DIV CD		0	CLK PHASE SELECT CD			SYSREF SEL CD	CLK SEL AB	CLK DIV AB		0	CLK PHASE SELECT AB		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 16. Register Address 3 Field Descriptions

Bit	Field	Type	Reset	Description
D14	CLK SEL CD			Clock source selection for channel C and D 0 = Channel CD clock output divider 1 = Channel AB clock output divider (default)
D13:D12	CLK DIV CD			Channel CD clock divider setting 00 = Clock input is up to 500 MHz. Input clock is not divided (default) 01 = /2 10 = /4 11 = Not used
D10:D8	CLK PHASE SELECT CD			Selects phase of channel divided clock, but depends on clock divider setting. When clock CD divider is set to: /1 = 2 phases are available (0º or 180º) /2 = 4 phases are available (0º, 90º, 180º or 270º) /4 = 8 phases are available (0º, 45º, 90º, 135º, 180º, 225º, 270º or 315º) When switching clock phases, register 0x08, D9 must be enabled first and then disabled after the switch to ensure glitch-free operation.
D7	SYSREF SEL CD			SYSREF Input selection for channel C and D 0 = Use SYSREFAB inputs (default) 1 = Use SYSREFCD inputs
D6	CLK SEL AB			Clock source selection for channel A and B 0 = Channel CD clock output divider 1 = Channel AB clock output divider (default)
D5:D4	CLK DIV AB			Channel AB clock divider setting 00 = Clock input is up to 500 MHz. Input clock is not divided (default) 01 = /2 10 = /4 11 = Not used
D2:D0	CLK PHASE SELECT AB			Selects phase of channel AB divided clock, but depends on clock divider setting. When clock divider is set to: /1 = 2 phases are available (0º or 180º) /2 = 4 phases are available (0º, 90º, 180º or 270º) /4 = 8 phases are available (0º, 45º, 90º, 135º, 180º, 225º, 270º or 315º) When switching clock phases, register 0x07, D9 must be enabled first and then disabled after the switch to ensure glitch-free operation.

7.6.1.5 Register Address 4

图 69. Register Address 4, Default: 0x000F, Hex = 4

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OVRA OUT EN	OVRB OUT EN	OVRC OUT EN	OVRD OUT EN	SYSREF AB DELAY		SYSREF CD DELAY		0	0	0	0	SYNCb AB EN	SYNCb CD EN	1	1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. Register Address 4 Field Descriptions

Bit	Field	Type	Reset	Description
D15	OVRA OUT EN			OVRA pin output enable 0 = OVRA is an input for burst mode trigger (see register 0x2C) 1 = OVRA is an output
D14	OVRB OUT EN			OVRB pin output enable 0 = Not used (default) 1 = OVRB is an output
D13	OVRC OUT EN			OVRC pin output enable 0 = OVRC is an input for burst mode trigger (see register 0x3A) 1 = OVRC is an output
D12	OVRD OUT EN			OVRD pin output enable 0 = Not used (default) 1 = OVRD is an output
D11:D10	SYSREF AB DELAY			Programmable input delay on SYSREFAB input 00 = 0-ps delay (default) 01 = 200-ps delay 10 = 100-ps delay 11 = 300-ps delay
D9:D8	SYSREF CD DELAY			Programmable input delay on SYSREFCD input 00 = 0-ps delay (default) 01 = 200-ps delay 10 = 100-ps delay 11 = 300-ps delay
D3	SYNCb AB EN			SYNCbAB input buffer enable 0 = Input buffer disabled 1 = Input buffer enabled (default)
D2	SYNCb CD EN			SYNCbCD input buffer enable 0 = Input buffer disabled 1 = Input buffer enabled (default)
D1				Reads back 1
D0				Reads back 1

7.6.1.6 Register Address 5

图 70. Register Address 5, Default: 0x0000, Hex = 5

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ANALOG SLEEP MODES – ENABLE pin															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 18. Register Address 5 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D0	ANALOG SLEEP MODES – ENABLE pin			Power-down function assigned to ENABLE pin. When any bit is set, the corresponding function is always enabled regardless of status of the ENABLE pin. This assumes address 0x06 is in default configuration.
D13				Light sleep channel A
D11				Light sleep channel B
D9				Light sleep channel C
D7				Light sleep channel D

表 18. Register Address 5 Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
D6				Temperature sensor
D4				Clock buffer
D3				Clock divider channel AB
D2				Clock divider channel CD
D1				Buffer SYSREFAB
D0				Buffer SYSREFCD

表 19. Configurations When ENABLE Pin is Low

	Description
0000 0000 0000 0000	Global power down
1000 0000 0000 0000	Standby
1000 0000 0001 1111	Deep sleep
1010 1010 1001 1111	Light sleep (if unused, clock divider CD and SYSREFCD can be set to 0 also)

7.6.1.7 Register Address 6

图 71. Register Address 6, Default: 0xFFFF, Hex = 6

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ANALOG SLEEP MODES – SPI															SYSREFCD EN

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 20. Register Address 6 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D1	ANALOG SLEEP MODES – SPI			Power-down function controlled via SPI. When a bit is set to 0, the function is powered down when ENABLE pin is high. However, register 0x05 has higher priority. For example, if D13 (deep sleep channel A) in 0x05 is enabled, it cannot be powered down with the SPI.
D13				Light sleep channel A
D11				Light sleep channel B
D9				Light sleep channel C
D7				Light sleep channel D
D6				Temperature sensor
D4				Clock buffer
D3				Clock divider channel AB
D2				Clock divider channel CD
D1				Buffer SYSREFAB
D0	SYSREFCD EN			Enables SYSREFCD input for dual SYSREF operation 0 = TRIGGER input for burst mode (differential or single ended, see address 0x2C/3A) 1 = SYSREF input for channel C/D (default)

表 21. Configurations When ENABLE Pin is High

	Description
0000 0000 0000 000	Global power down
1000 0000 0000 000	Standby
1000 0000 0001 111	Deep sleep

表 21. Configurations When ENABLE Pin is High (接下页)

	Description
1010 1010 1001 111	Light sleep
1111 1111 1111 111	Normal operation

Control power down function through ENABLE pin:

1. Configure power-down mode in register 0x05
2. Normal operation: ENABLE pin high
3. Power-down mode: ENABLE pin low

Control power down function through SPI (ENABLE pin always high):

1. Assign power-down mode in register 0x06
2. Normal operation 0x06 is 0xFFFF
3. Power-down mode: configure power down mode in register 0x06

7.6.1.8 Register Address 7

图 72. Register Address 7, Default: 0x0124, Hex = 7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CLK SW AB	1	0	1	0	0	0	1	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 22. Register Address 7 Field Descriptions

Bit	Field	Type	Reset	Description
D9	CLK SW AB			User should set this bit to 1 when changing the clock phase of the clock divider AB. After the change is complete user needs to write this bit back to 0.
D8				Reads back 1
D6				Reads back 1
D2				Reads back 1

7.6.1.9 Register Address 8

图 73. Register Address 8, Default: 0x0124, Hex = 8

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CLK SW CD	1	0	1	0	0	0	1	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. Register Address 8 Field Descriptions

Bit	Field	Type	Reset	Description
D9	CLK SW CD			User should set this bit to 1 when changing the clock phase of the clock divider CD. After the change is complete user needs to write this bit back to 0.
D8				Reads back 1
D6				Reads back 1
D2				Reads back 1

7.6.1.10 Register Address 12

图 74. Register Address 12, Default: 0x31E4, Hex = C

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	1	1	1	SYSREF JESD MODE CD			SYSREF JESD MODE AB		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 24. Register Address 12 Field Descriptions

Bit	Field	Type	Reset	Description
D13				Reads back 1
D12				Reads back 1
D8				Reads back 1
D7				Reads back 1
D6				Reads back 1
D5:D3	SYSREF JESD MODE CD			Determines how SYSREF is used in the JESD block for channel CD 000 = Ignore SYSREF input 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses (default) 101 = Skip two SYSREF pulses and then use one 111 = Skip two SYSREF pulses and then use all
D2:D0	SYSREF JESD MODE AB			Determines how SYSREF is used in the JESD block for channel AB. Same functionality as SYSREF JESD MODE CD

7.6.1.11 Register Address 13

图 75. Register Address 13, Default: 0x0202, Hex = D

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	JESD INIT CD	JESD RESET CD	0	0	0	0	0	0	JESD INIT AB	JESD RESET AB

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 25. Register Address 13 Field Descriptions

Bit	Field	Type	Reset	Description
D9	JESD INIT CD			Puts the JESD block in INITIALIZATION state when set high. In this state the JESD parameters can be programmed and the outputs will stay at 0. See also JESD start-up sequence.
D8	JESD RESET CD			Resets the JESD block when low
D1	JESD INIT AB			Puts the JESD block in initialization state when set high. In this state the JESD parameters can be programmed and the outputs will stay at 0.
D0	JESD RESET AB			Resets the JESD block when low

7.6.1.12 Register Address 14

图 76. Register Address 14, Default: 0x00FF, Hex = E

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	TX LANE EN CD				TX LANE EN AB			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 26. Register Address 14 Field Descriptions

Bit	Field	Type	Reset	Description
D7:D4	TX LANE EN CD			Enables JESD204B transmitter for channel C and D. Set to 1 to enable. D7 = Lane DD1 D6 = Lane DD0 D5 = Lane DC1 D4 = Lane DC0
D3:D0	TX LANE EN AB			Enables JESD204B transmitter for channel A and B. Set to 1 to enable. D3 = Lane DB1 D2 = Lane DB0 D1 = Lane DA1 D0 = Lane DA0

7.6.1.13 Register Address 15

图 77. Register Address 15, Default: 0x0001, Hex = F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CTRL F AB		0	0	0	0	0	0	CTRL M AB	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 27. Register Address 15 Field Descriptions

Bit	Field	Type	Reset	Description
D9:D8	CTRL F AB			Controls number of octets per frame for channel AB. 00 = F = 1 (default) 01 = F = 2
D1:D0	CTRL M AB			Controls number of converters per link for channel AB. 01 = M = 2. This is the only valid option (default)

7.6.1.14 Register Address 16

图 78. Register Address 16, Default: 0x03E3, Hex = 10

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CTRL K AB					0	0	0	CTRL L AB	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 28. Register Address 16 Field Descriptions

Bit	Field	Type	Reset	Description
D9:D5	CTRL K AB			Controls number of frames per multi-frame for channel AB. 0: K = 1 30 K = 31 1: K = 2 31 K = 32 (default) And so forth
D1:D0	CTRL L AB			Controls number of lanes for channel AB. 01: L = 2 11: L = 4 (default)

7.6.1.15 Register Address 19

图 79. Register Address 19, Default: 0x0020, Hex = 13

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	INV SYNCb AB	HD AB	SCR EN AB	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 29. Register Address 19 Field Descriptions

Bit	Field	Type	Reset	Description
D6	INV SYNCb AB			Inverts polarity of SYNCbAB input 0 = Normal operation 1 = Polarity inverted
D5	HD AB			Enables high density mode for channel AB. This mode is needed for LMFS = 4221. 0 = High-density mode disabled for mode LMFS = 2221 1 = High-density mode enabled for mode LMFS = 4221 (default)
D4	SCR EN AB			Enables scramble mode for channel AB 0 = Scramble mode disabled (default) 1 = Scramble mode enabled

7.6.1.16 Register Address 22

图 80. Register Address 22, Default: 0x0001, Hex = 16

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CTRL F CD		0	0	0	0	0	0	CTRL M CD	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 30. Register Address 22 Field Descriptions

Bit	Field	Type	Reset	Description
D9:D8	CTRL F CD			Controls number of octets per frame for channel CD. 00: F = 1 (default) 01: F = 2
D1:D0	CTRL M CD			Controls number of converters per link for channel CD. 01: M = 2. This is the only valid option (default)

7.6.1.17 Register Address 23

图 81. Register Address 23, Default: 0x03E3, Hex = 17

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CTRL K CD					0	0	0	CTRL L CD	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 31. Register Address 23 Field Descriptions

Bit	Field	Type	Reset	Description
D9:D5	CTRL K CD			Controls number of frames per multi-frame for channel CD 0: K = 1 30 K = 31 1: K = 2 31 K = 32 (default) And so forth
D1:D0	CTRL L CD			Controls number of lanes for channel CD 01: L = 2 11: L = 4 (default)

7.6.1.18 Register Address 26

图 82. Register Address 26, Default: 0x0020, Hex = 1A

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	INV SYNCb CD	HD CD	SCR EN CD	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 32. Register Address 26 Field Descriptions

Bit	Field	Type	Reset	Description
D6	INV SYNCb CD			Inverts polarity of SYNCbCD input 0 = Normal operation 1 = Polarity inverted
D5	HD CD			Enables high density mode for channel CD. This mode is needed for LMFS = 4221. 0 = High density mode disabled for mode LMFS = 2221 1 = High density mode enabled for mode LMFS = 4221 (default)
D4	SCR EN CD			Enables scramble mode for channel CD 0 = Scramble mode disabled (default) 1 = Scramble mode enabled

7.6.1.19 Register Address 29

图 83. Register Address 29, Default: 0x0000, Hex = 1D

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	TEST PATTERN EN CD	TEST PATTERN EN AB	0	TEST PATTERN	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 33. Register Address 29 Field Descriptions

Bit	Field	Type	Reset	Description
D6	TEST PATTERN EN CD			Enables test pattern output for channel C and D 0 = Normal operation 1 = Test pattern output enabled
D5	TEST PATTERN EN AB			Enables test pattern output for channel A and B 0 = Normal operation 1 = Test pattern output enabled
D4	TEST PATTERN			Selects test pattern 0 = RAMP pattern 1 = Output alternates between 0x1555 and 0x2AAA

7.6.1.20 Register Address 30

图 84. Register Address 30, Default: 0x0000, Hex = 1E

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	JESD SLEEP MODES – ENABLE pin									

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 34. Register Address 30 Field Descriptions

Bit	Field	Type	Reset	Description
D9:D0	JESD SLEEP MODES – ENABLE pin			Power-down function assigned to ENABLE pin. When any bit is set, the corresponding function is always enabled regardless of status of the ENABLE pin. D9 = JESD PLL channel CD D8 = JESD PLL channel AB D7 = Lane DD1 D6 = Lane DD0 D5 = Lane DC1 D4 = Lane DC0 D3 = Lane DB1 D2 = Lane DB0 D1 = Lane DA1 D0 = Lane DA0

表 35. Configurations

	Description
00 0000 0000	Global power down (default)
00 0000 0000	Standby
11 0000 0000	Deep sleep
11 0000 0000	Light sleep

7.6.1.21 Register Address 31

图 85. Register Address 31, Default: 0xFFFF, Hex = 1F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	JESD SLEEP MODES – SPI									

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 36. Register Address 31 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D0	JESD SLEEP MODES – SPI			Power-down function controlled via SPI. When a bit is set to 0, the function is powered down when ENABLE pin is high. However register 0x1E has higher priority. For example, if D9 (JESD PLL channel CD) in 0x1E is enabled, it cannot be powered down with the ENABLE pin. D9 = JESD PLL channel CD D8 = JESD PLL channel AB D7 = Lane DD1 D6 = Lane DD0 D5 = Lane DC1 D4 = Lane DC0 D3 = Lane DB1 D2 = Lane DB0 D1 = Lane DA1 D0 = Lane DA0

表 37. Configurations

	Description
00 0000 0000	Global power down
00 0000 0000	Standby
11 0000 0000	Deep sleep
11 0000 0000	Light sleep
11 1111 1111	Normal operation (default)

Control power down function through ENABLE pin:
1. Configure power down mode in register 0x1E
2. Normal operation: ENABLE pin high
3. Power down mode: ENABLE pin low

Control power down function through SPI (ENABLE pin always high):
1. Assign power down mode in register 0x1F
2. Normal operation 0x1F is 0xFFFF
3. Power-down mode: configure power down mode in register 0x1F

7.6.1.22 Register Address 32

图 86. Register Address 32, Default: 0x0000, Hex = 20

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			JESD LANE POLARITY INVERT								PRBS EN				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 38. Register Address 32 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D8	JESD LANE POLARITY INVERT			Set to 1 for polarity inversion D15 = Lane DD1 D14 = Lane DD0 D13 = Lane DC1 D12 = Lane DC0 D11 = Lane DB1 D10 = Lane DB0 D9 = Lane DA1 D8 = Lane DA0
D7:D0	PRBS EN			Outputs PRBS pattern selected in address 0x21 on the selected serial output lanes D7 = Lane DD1 D6 = Lane DD0 D5 = Lane DC1 D4 = Lane DC0 D3 = Lane DB1 D2 = Lane DB0 D1 = Lane DA1 D0 = Lane DA0

7.6.1.23 Register Address 33

图 87. Register Address 33, Default: 0x0000, Hex = 21

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PRBS SEL		0	0	0	0	0	0	0	0	0	0		VREF SEL	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 39. Register Address 33 Field Descriptions

Bit	Field	Type	Reset	Description
D14:D13	PRBS SEL			Selects different PRBS output pattern (these are not 8b/10b encoded) $000 = 2^{31} - 1$ $001 = 2^7 - 1$ $010 = 2^{15} - 1$ $011 = 2^{23} - 1$
D2:D0	VREF SEL			Selects different input full-scale amplitude by adjusting voltage reference setting 000 = Full scale is 1.25 Vpp (default) 001 = Full scale is 1.35 Vpp 010 = Full scale is 1.5 Vpp 011 = External 100 = Full scale is 1.15 Vpp 101 = Full scale is 1.0 Vpp

7.6.1.24 Address: 0x24, 0x25, 0x26, 0x27

图 88. Address: 0x24, 0x25, 0x26, 0x27; Default: 0x0000, Hex = 24, 25, 26, 27

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					TDD BURST MODE COUNTER L_1 [15:0] AB										
					TDD BURST MODE COUNTER L_2 [15:0] AB										
					TDD BURST MODE COUNTER L_3 [15:0] AB										
					TDD BURST MODE COUNTER L_4 [15:0] AB										

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 40. Address: 0x24, 0x25, 0x26, 0x27 Field Descriptions

Bit	Field	Type	Reset	Description
	TDD BURST MODE COUNTER L_1, L_2, L_3, L_4 [15:0] AB			Low-resolution counters L_1, L_2, L_3, L_4 for channel A and B. L_1 is also used for regular bust mode. Each count equals 4 samples. Upper 6 MSB [21:16] for each counter are located in address 0x2C and 0x2D

7.6.1.25 Address: 0x28, 0x29, 0x2A, 0x2B

图 89. Address: 0x28, 0x29, 0x2A, 0x2B; Default: 0x0000, Hex = 28, 29, 2A, 2B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDD BURST MODE COUNTER H_1 [15:0] AB															
TDD BURST MODE COUNTER H_2 [15:0] AB															
TDD BURST MODE COUNTER H_3 [15:0] AB															
TDD BURST MODE COUNTER H_4 [15:0] AB															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 41. Address: 0x28, 0x29, 0x2A, 0x2B Field Descriptions

Bit	Field	Type	Reset	Description
	TDD BURST MODE COUNTER H_1, H_2, H_3, H_4 [15:0] AB			High-resolution counters H_1, H_2, H_3, H_4 for channel A and B. H_1 is also used for regular bust mode. Each count equals 4 samples. Upper 6 MSB [21:16] for each counter are located in address 0x2E and 0x2F

7.6.1.26 Register Address 44

图 90. Register Address 44, Default: 0x0000, Hex = 2C

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BM TRIG AB		TDD BURST MODE COUNTER L_2 [21:16] AB						0	0	TDD BURST MODE COUNTER L_1 [21:16] AB					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 42. Register Address 44 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D14	BM TRIG AB			Burst mode trigger source selection for channel A and B 00 = TRIGGERAB input (SYSREFCDP pin) 01 = TRIGGERCD input (SYSREFCDM pin) 10 = OVRA input 11 = TRIGGERAB and TRIGGERCD as differential input
D13:D8	TDD BURST MODE COUNTER L_2 [21:16] AB			Low-resolution counter L_2 upper 6 MSB, channel AB
D5:D0	TDD BURST MODE COUNTER L_1 [21:16] AB			Low-resolution counter L_1 upper 6 MSB, channel AB

7.6.1.27 Register Address 45

图 91. Register Address 45, Default: 0x0000, Hex = 2D

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	TDD BURST MODE COUNTER L_4 [21:16] AB						0	0	TDD BURST MODE COUNTER L_3 [21:16] AB					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 43. Register Address 45 Field Descriptions

Bit	Field	Type	Reset	Description
D13:D8	TDD BURST MODE COUNTER L_4 [21:16] AB			Low-resolution counter L_4 upper 6 MSB, channel AB
D5:D0	TDD BURST MODE COUNTER L_3 [21:16] AB			Low-resolution counter L_3 upper 6 MSB, channel AB

7.6.1.28 Register Address 46

图 92. Register Address 46, Default: 0x0000, Hex = 2E

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	TDD BURST MODE COUNTER H_2 [21:16] AB						0	0	TDD BURST MODE COUNTER H_1 [21:16] AB					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 44. Register Address 46 Field Descriptions

Bit	Field	Type	Reset	Description
D13:D8	TDD BURST MODE COUNTER H_2 [21:16] AB			High-resolution counter H_2 upper 6 MSB, channel AB
D5:D0	TDD BURST MODE COUNTER H_1 [21:16] AB			High-resolution counter H_1 upper 6 MSB, channel AB

7.6.1.29 Register Address 47

图 93. Register Address 47, Default: 0x0000, Hex = 2F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AUTO TRIG AB	TDD EN AB	TDD BURST MODE COUNTER H_4 [21:16] AB						0	0	TDD BURST MODE COUNTER H_3 [21:16] AB					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 45. Register Address 47 Field Descriptions

Bit	Field	Type	Reset	Description
D15	AUTO TRIG AB			Enables auto trigger mode for regular burst mode for channel A and B 0 = Auto trigger disabled 1 = Auto trigger enabled
D14	TDD EN AB			Enables TDD burst mode 0 = TDD burst mode disabled 1 = TDD burst mode enabled
D13:D8	TDD BURST MODE COUNTER H_4 [21:16] AB			High-resolution counter H_4 upper 6 MSB, channel AB
D5:D0	D5 to D0 TDD BURST MODE COUNTER H_3 [21:16] AB			High-resolution counter H_3 upper 6 MSB, channel AB

7.6.1.30 Address: 0x32, 0x33, 0x34, 0x35

图 94. Address: 0x32, 0x33, 0x34, 0x35; Default: 0x0000, Hex = 32, 33, 34, 35

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDD BURST MODE COUNTER L_1 [15:0] CD															
TDD BURST MODE COUNTER L_2 [15:0] CD															
TDD BURST MODE COUNTER L_3 [15:0] CD															
TDD BURST MODE COUNTER L_4 [15:0] CD															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 46. Address: 0x32, 0x33, 0x34, 0x35 Field Descriptions

Bit	Field	Type	Reset	Description
	TDD BURST MODE COUNTER L$_1$, L$_2$, L$_3$, L$_4$ [15:0] CD			Low-resolution counters L$_1$, L$_2$, L$_3$, L$_4$ for channel C and D. L$_1$ is also used for regular bust mode Each count equals 4 samples. Upper 6 MSB [21:16] for each counter are located in address 0x3A and 0x3B

7.6.1.31 Address: 0x36, 0x37, 0x38, 0x39

图 95. Address: 0x36, 0x37, 0x38, 0x39; Default: 0x0000, Hex = 36, 37, 38, 39

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						TDD BURST MODE COUNTER H$_1$ [15:0] CD									
						TDD BURST MODE COUNTER H$_2$ [15:0] CD									
						TDD BURST MODE COUNTER H$_3$ [15:0] CD									
						TDD BURST MODE COUNTER H$_4$ [15:0] CD									

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 47. Address: 0x36, 0x37, 0x38, 0x39 Field Descriptions

Bit	Field	Type	Reset	Description
	TDD BURST MODE COUNTER H$_1$, H$_2$, H$_3$, H$_4$ [15:0] CD			High-resolution counters H$_1$, H$_2$, H$_3$, H$_4$ for channel C and D. H1 is also used for regular bust mode Each count equals 4 samples. Upper 6 MSB [21:16] for each counter are located in address 0x3C and 0x3D

7.6.1.32 Register Address 58

图 96. Register Address 58, Default: 0x0000, Hex = 3A

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BM TRIG CD		TDD BURST MODE COUNTER L$_2$ [21:16] CD						0	0	TDD BURST MODE COUNTER L$_1$ [21:16] CD					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 48. Register Address 58 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D14	BM TRIG CD			Burst mode trigger source selection for channel C and D 00 = TRIGGERAB input (SYSREFCDP pin) 01 = TRIGGERCD input (SYSREFCDM pin) 10 = OVRC input 11 = TRIGGERAB and TRIGGERCD as differential input
D13:D8	TDD BURST MODE COUNTER L$_2$ [21:16] CD			Low-resolution counter L$_2$ upper 6 MSB, channel AB
D5:D0	TDD BURST MODE COUNTER L$_1$ [21:16] CD			Low-resolution counter L$_1$ upper 6 MSB, channel AB

7.6.1.33 Register Address 59

图 97. Register Address 59, Default: 0x0000, Hex = 3B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	TDD BURST MODE COUNTER L$_4$ [21:16] CD						0	0	TDD BURST MODE COUNTER L$_3$ [21:16] CD					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 49. Register Address 59 Field Descriptions

Bit	Field	Type	Reset	Description
D13:D8	TDD BURST MODE COUNTER L_4 [21:16] CD			Low-resolution counter L_4 upper 6 MSB, channel CD
D5:D0	TDD BURST MODE COUNTER L_3 [21:16] CD			Low-resolution counter L_3 upper 6 MSB, channel CD

7.6.1.34 Register Address 60

图 98. Register Address 60, Default: 0x0000, Hex = 3C

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	TDD BURST MODE COUNTER H_2 [21:16] CD						0	0	TDD BURST MODE COUNTER H_1 [21:16] CD					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 50. Register Address 60 Field Descriptions

Bit	Field	Type	Reset	Description
D13:D8	TDD BURST MODE COUNTER H_2 [21:16] CD			High-resolution counter H_2 upper 6 MSB, channel CD
D5:D0	TDD BURST MODE COUNTER H_1 [21:16] CD			High-resolution counter H_1 upper 6 MSB, channel

7.6.1.35 Register Address 61

图 99. Register Address 61, Default: 0x0000, Hex = 3D

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AUTO TRIG CD	TDD EN CD	TDD BURST MODE COUNTER H_4 [21:16] CD						0	0	TDD BURST MODE COUNTER H_3 [21:16] CD					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 51. Register Address 61 Field Descriptions

Bit	Field	Type	Reset	Description
D15	AUTO TRIG CD			Enables auto trigger mode for regular burst mode for channel C and D 0 = Auto trigger disabled 1 = Auto trigger enabled
D14	TDD EN CD			Enables TDD burst mode for channel C and D 0 = TDD burst mode disabled 1 = TDD burst mode enabled
D13:D8	TDD BURST MODE COUNTER H_4 [21:16] CD			High-resolution counter H_4 upper 6 MSB, channel CD
D5:D0	TDD BURST MODE COUNTER H_3 [21:16] CD			High-resolution counter H_3 upper 6 MSB, channel CD

7.6.1.36 Register Address 99

图 100. Register Address 99, Default: 0x0000, Hex = 63

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	TEMP SENSOR								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 52. Register Address 99 Field Descriptions

Bit	Field	Type	Reset	Description
D8:D0	TEMP SENSOR			Value of on chip temperature sensor (read only). Value is 2s complement of die temperature sensor in °C For example: 0x0032 equals 50°C

7.6.1.37 Register Address 100

图 101. Register Address 100, Default: 0x0000, Hex = 64

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PRE EMP SEL AB				PRE EMP EN AB				DCC EN AB				0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 53. Register Address 100 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D12	PRE EMP SEL AB			Selects pre-emphasis of serializers for channel A and B 0 = Pre-emphasis 1 = De-emphasis
D11:D8	PRE EMP EN AB			Enables pre-emphasis, 0 = disabled, 1 = enabled D11 = Lane DB1 D10 = Lane DB0 D9 = Lane DA1 D8 = Lane DA0
D7:D4	DCC EN AB			Enables the duty cycle correction circuit for each of the serializers D7 = Lane DB1 D6 = Lane DB0 D5 = Lane DA1 D4 = Lane DA0

7.6.1.38 Register Address 103

图 102. Register Address 103, Default: 0x0000, Hex = 67

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT CURRENT CONTROL AB															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 54. Register Address 103 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D0	OUTPUT CURRENT CONTROL AB			Selects pre-emphasis current for the serializers. There are 4 bit per serializer of channel A and B. D15:D12 = Lane DB1 D11:D8 = Lane DB0 D7:D4 = Lane DA1 D3:D0 = Lane DA0

表 55. Pre-Emphasis Level is: Decimal Value / 30

	Description
0000	Normal operation
0001	1 / 30
0010	2 / 30
and so forth	

7.6.1.39 Register Address 104

图 103. Register Address 104, Default: 0x0000, Hex = 68

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PRE EMP SEL CD				PRE EMP EN CD				DCC EN CD				0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 56. Register Address 104 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D12	PRE EMP SEL CD			Selects pre-emphasis of serializers for channel C and D 0 = Pre-emphasis 1 = De-emphasis
D11:D8	PRE EMP EN CD			Enables pre-emphasis, 0 = disabled, 1 = enabled D11 = Lane DD1 D10 = Lane DD0 D9 = Land DC1 D8 = Lane DC0
D7:D4	DCC EN CD			Enables the duty cycle correction circuit for each of the serializers D7 = Lane DD1 D6 = Lane DD0 D5 = Land DC1 D4 = Lane DC0

7.6.1.40 Register Address 107

图 104. Register Address 107, Default: 0x0000, Hex = 6B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT CURRENT CONTROL CD															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 57. Register Address 107 Field Descriptions

Bit	Field	Type	Reset	Description
D15:D0	OUTPUT CURRENT CONTROL CD			Selects pre-emphasis current for the serializers. There are 4 bit per serializer of channel C and D. D15:D12 = Lane DD1 D11:D8 = Lane DD0 D7:D4 = Land DC1 D3:D0 = Lane DC0

表 58. Pre-Emphasis Level is: Decimal Value / 30

	Description
0000	Normal operation
0001	1 / 30
0010	2 / 30
And so forth	

7.6.1.41 Register Address 108

图 105. Register Address 108, Hex = 6C

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	TDD RATIO CD	TDD RATIO AB	BM RATIO CD	BM RATIO AB	JESD PLL CD	JESD PLL AB

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 59. **Register Address 108 Field Descriptions**[1]

Bit	Field	Type	Reset	Description
D5	TDD RATIO CD			TDD burst mode high-to-low resolution duty cycle for channel CD is invalid when flag is set
D4	TDD RATIO AB			TDD burst mode high-to-low resolution duty cycle for channel AB is invalid when flag is set
D3	BM RATIO CD			Burst mode high-to-low resolution duty cycle for channel CD is invalid when flag is set
D2	BM RATIO CD			Burst mode high-to-low resolution duty cycle for channel AB is invalid when flag is set
D1	JESD PLL CD			JESD PLL for channel CD lost lock when flag is set high
D0	JESD PLL CD			JESD PLL for channel AB lost lock when flag is set high

(1)   Register values in address 0x6C are read only alarms

7.6.1.42   Register Address 111

图 106. **Register Address 111, Default: 0x0000, Hex = 6F**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	TRDY EN AB	0	0	0	0	0	TRDY EN CD

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 60. **Register Address 111 Field Descriptions**

Bit	Field	Type	Reset	Description
D6	TRDY EN AB			Selects to output TRDY flag in burst mode operation on OVRB pin for channel A/B 0 = Fast overrange indicator for channel B is output on OVRB pin 1 = Trigger ready flag output on OVRB pin
D0	TRDY EN CD			Selects to output TRDY flag in burst mode operation on OVRD pin for channel C/D 0 = Fast overrange indicator for channel D is output on OVRD pin 1 = Trigger ready flag output on OVRD pin

8 Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In the design of any application involving a high-speed data converter, particular attention should be paid the design of the analog input, the clocking solution, and careful layout of the clock and analog signals. In addition, the JESD204B interface means there now are high-speed serial lines that should be handled to preserve adequate signal integrity at the device that receives the sample data. The ADS58J89 evaluation module (EVM) is one practical example of the design of the analog input circuit and clocking solution, as well as a practical example of good circuit board layout practices around the ADC.

8.1.1 SNR and Clock Jitter

The signal-to-noise ratio of the channel is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit channel. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2}$$

(2)

Calculate the SNR limitation due to sample clock jitter using the following:

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter})$$

(3)

The total clock jitter (t_{Jitter}) has two components – the internal aperture jitter (85 fs for ADS58J89), which is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. Calculate total clock jitter using the following:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2}$$

(4)

External clock jitter can be minimized by using high quality clock sources and jitter cleaners, as well as bandpass filters at the clock input while a faster clock slew rate improves the channel aperture jitter.

The ADS58J89 has a thermal noise of 66 dBFS and internal aperture jitter of 98 fs. The SNR depending on amount of external jitter for different input frequencies is shown in 图 107.
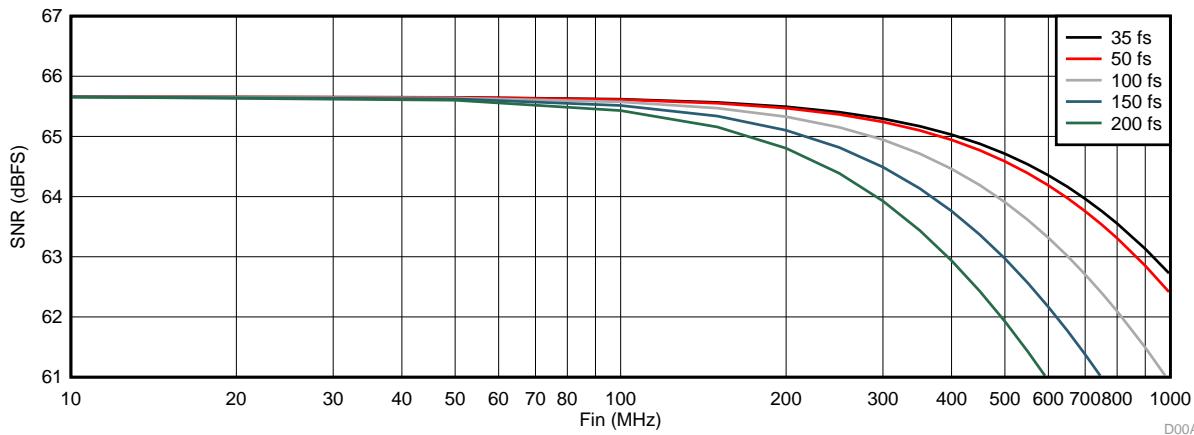

图 107. SNR vs Input Frequency and External Clock Jitter

8.2 Typical Application

The analog inputs of the ADS58J89 must be fully differential and biased to a desired common mode voltage, VCM. Therefore, there will be a signal conditioning circuit for each of the analog inputs. If the amplitude of the input circuit is such that no gain is needed to make full use of the full-scale range of the ADC, then a transformer coupled circuit as in 图 108 may be used with good results. The transformer coupling is inherently low-noise, and inherently AC-coupled so that the signal may be biased to VCM after the transformer coupling. If signal gain is required, or the input bandwidth is to include the spectrum all the way down to DC such that AC coupling is not possible, then an amplifier-based signal conditioning circuit would be required.

By using the simple drive circuit of 图 108, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.
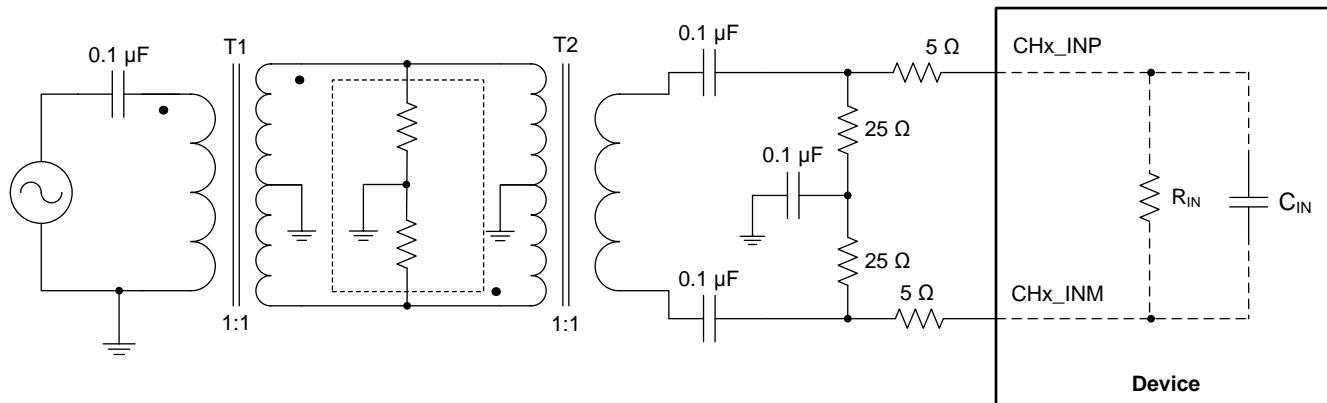
图 108. Input Drive Circuit
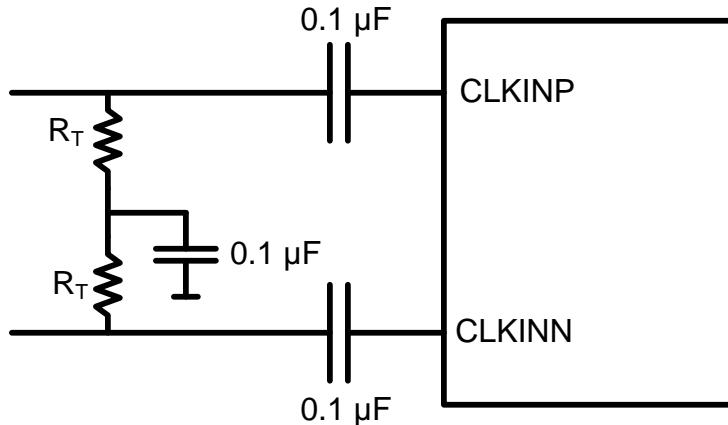
图 109. Recommended Differential Clock Driving Circuit

8.2.1 Design Requirements

The ADS58J89 requires a fully differential analog input with a full-scale range not to exceed 1.25 V peak to peak, biased to a common mode voltage of 2.0 V. In addition the input circuit must provide proper transmission line termination (or proper load resistors in an amplifier-based solution) so the input of the impedance of the ADC analog inputs should be considered as well.

The clocking solution will have a direct impact on performance in terms of SNR, as shown in 图 107. The ADS58J89 is capable of a typical SNR of 66 dBFS for input frequencies of about 100 MHz (in 14-bit burst mode), so we will want to have a clocking solution that can preserve this level of performance.

Typical Application (接下页)
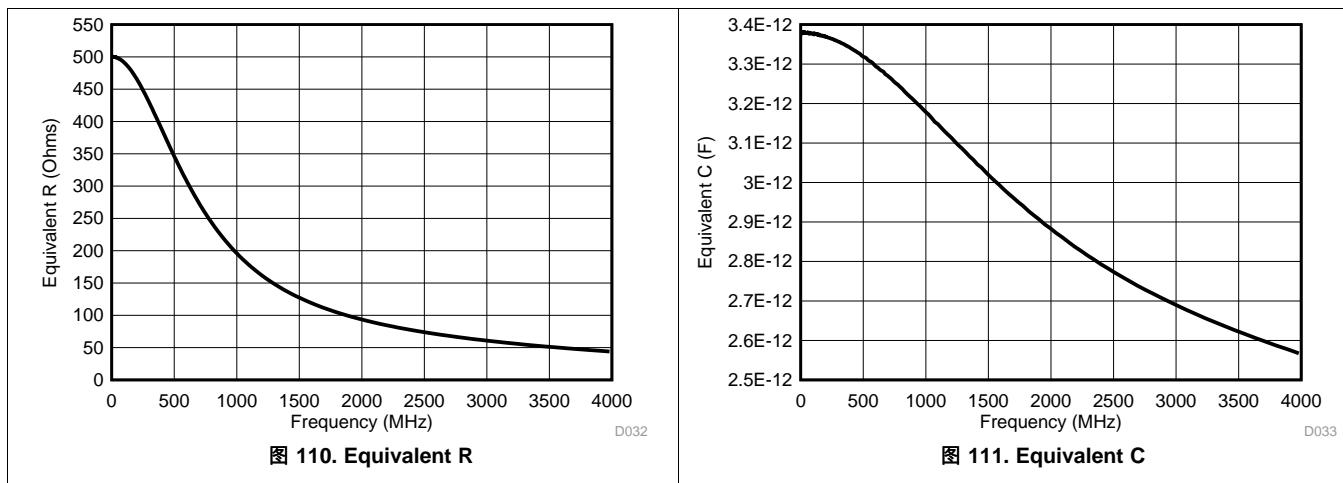
8.2.2 Detailed Design Procedure

The ADS58J89 has an input bandwidth of approximately 900 MHz, but we will consider an application involving the first or second Nyquist zones, so we will limit the frequency bandwidth here to be under 250 MHz. We will also consider a 50-ohm signal source, so the proper termination would be 50-Ω differential. As seen in 图 110 and 图 111, the input impedance of the analog input at 250 MHz is large compared to 50 Ω, so the proper termination can be 50-Ω differential as shown in 图 108. Splitting the termination into two 25-Ω resistors with an AC capacitor to ground provides a path to filter out any ripple on the common mode that may result from any amplitude or phase imbalance of the differential input, improving SFDR performance. The ADS58J89 provides a VCM output that may be used to bias the input to the desired level, but as seen in 图 52 the signal is internally biased inside the ADC so an external biasing to VCM is not required. If an external biasing to VCM were to be employed, the VCM voltage may be applied to the mid-point of the two 25-Ω termination resistors in 图 108.

For the clock input, 图 107 shows the SNR of the device above 100 MHz begins to degrade with external clock jitter of greater than 100 fs rms, so we will recommend the clock source be limited to approximately 100 fS of rms jitter. For the ADS58J89 EVM, the LMK04828 clock device is capable of providing a low-jitter sample clock as well as providing the SYSREF signal required as shown in 图 47 and 图 48, so that clocking device is one good choice for the clocking solution for the ADS58J89.

8.2.3 Application Curves

图 110 and 图 111 show the differential impedance between the channel INP and INM pins. The impedance is modeled as a parallel combination of RIN and CIN (RIN || 1 / jwCIN).

图 110. Equivalent R	图 111. Equivalent C

9 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDDC, IOVDD, PLLVDD, and DVDD. The device also requires a 1.9-V supply for AVDD18 and a 3.3-V supply for AVDD33. There are no specific sequence power-supply requirements during device power-up. AVDD, DVDD, IOVDD, PLLVDD, and AVDD33 can power up in any order.

10 Layout

10.1 Layout Guidelines

The Device EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in . Some important points to remember during laying out the board are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk on-board, the analog inputs should exit the pinout in opposite directions, as shown in the reference layout of as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of as much as possible.
- Digital outputs should be kept away from the analog inputs. When these digital outputs exit the pinout, the digital output traces should not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. The digital sample data rate can be as high as 5.0 Gsps, so care must be taken to maintain the signal integrity of these signals. A low-loss dielectric circuit board is recommended or else these traces should be kept as short as possible. These traces should be kept away from the analog inputs ad n clock input to the device as well.
- At each power-supply pin (AVDD, DRVDD, or AVDDD3V), a 0.1-µF decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

10.1.1 CML SerDes Transmitter Interface

Each of the 5 Gbps SerDes CML transmitter outputs requires AC coupling between transmitter and receiver. The differential pair should be terminated with a 100-Ω resistor as close to the receiving device as possible to avoid unwanted reflections and signal degradation.

10.2 Layout Example
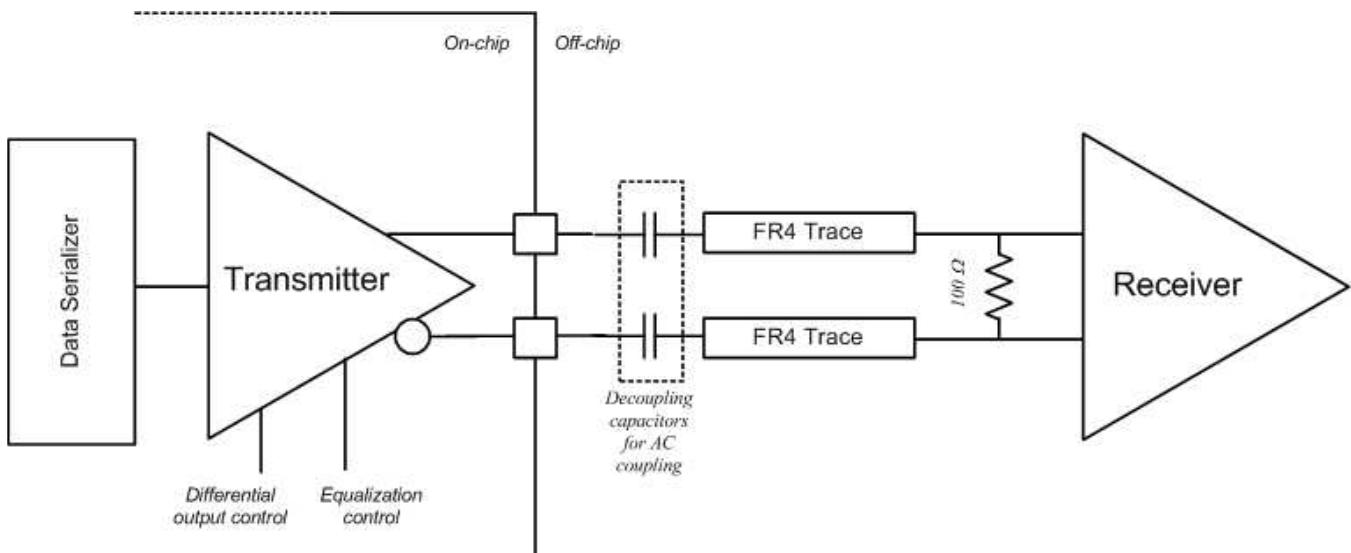
图 112. Layout Example Schematic

Layout Example (接下页)
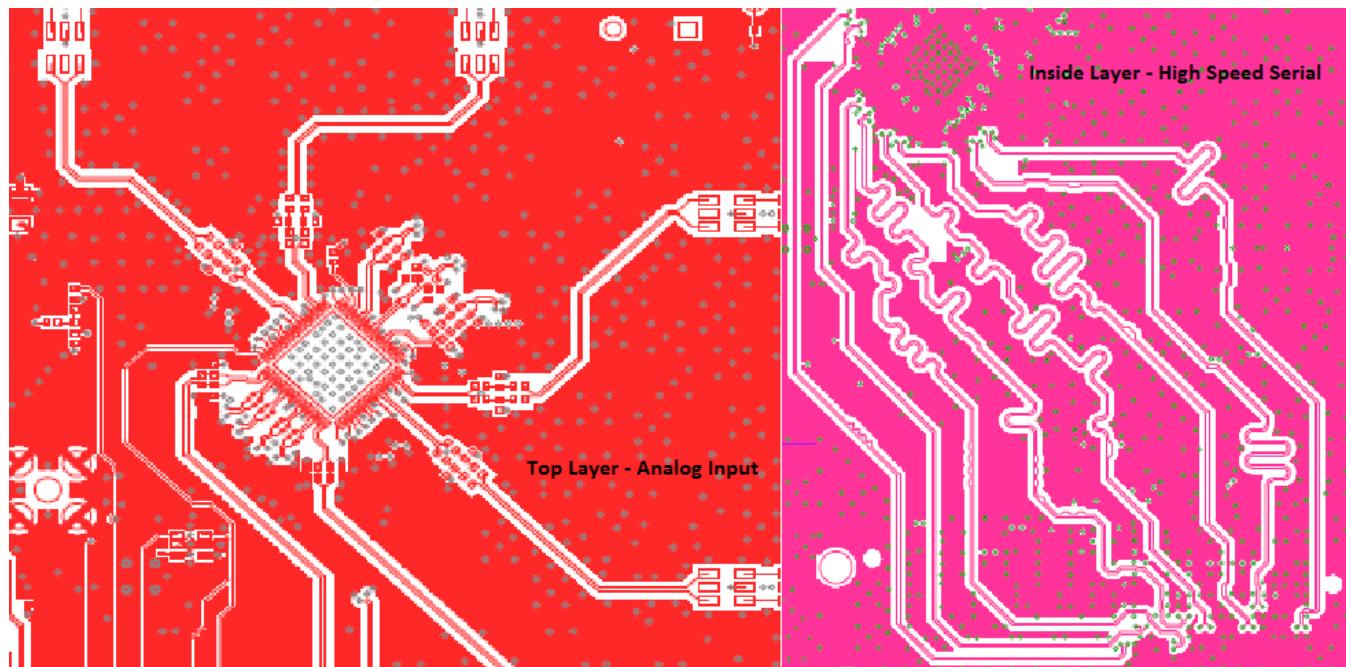
图 113. Top and Bottom Layers

11 器件和文档支持

11.1 商标

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS58J89IRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58J89	Samples
ADS58J89IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58J89	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGC 64

9 x 9, 0.5 mm pitch

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

B ◄── 9.15 / 8.85 ──► A

PIN 1 INDEX AREA

9.15
8.85

1.0
0.8

0.05
0.00

C

SEATING PLANE

⌒ 0.08 C

2X 7.5

EXPOSED
THERMAL PAD

SYMM
₵

17   32

16   33

SYMM
₵

65   □ 7.4 ± 0.1

2X 7.5

(0.2) TYP

60X
0.5

1

64   49

PIN 1 ID

48

64X 0.30 / 0.18

64X 0.5 / 0.3

⊕ 0.1 Ⓜ C A B
  0.05 Ⓜ

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS
INSTRUMENTS
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RGC0064H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

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NOTES: (continued)
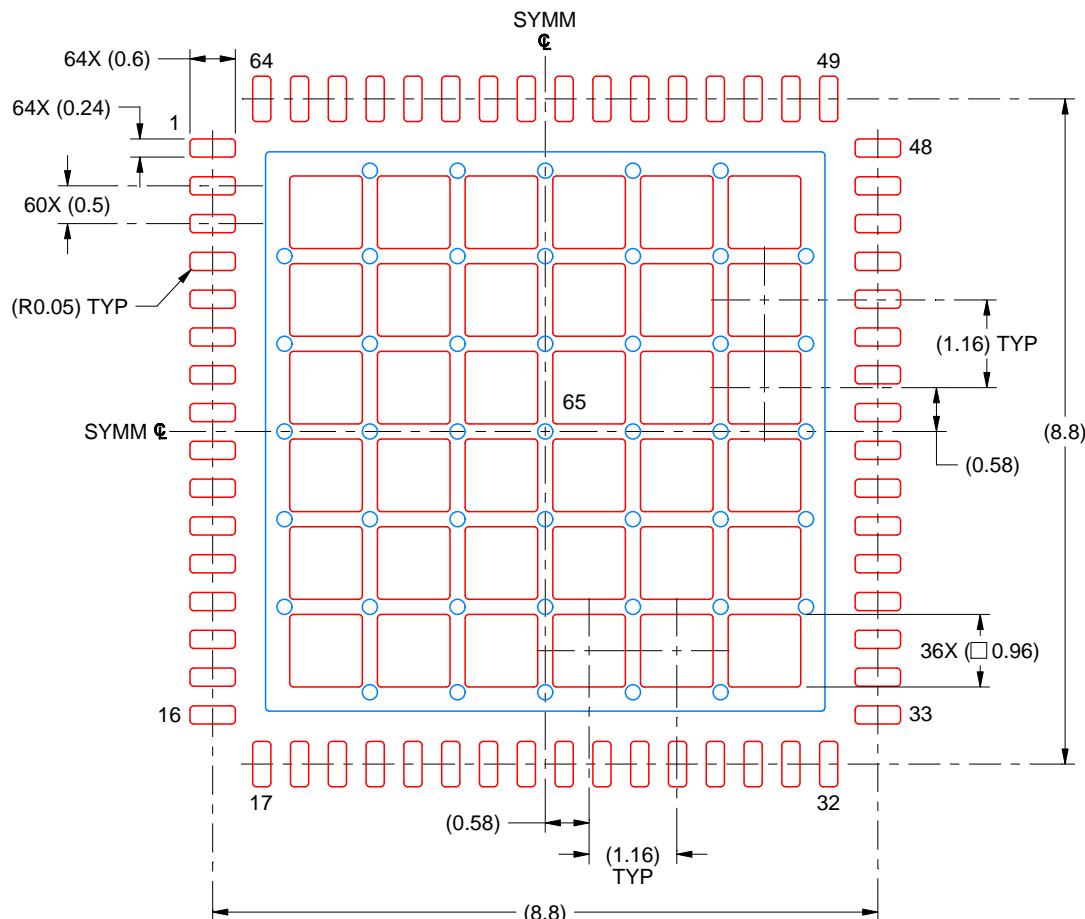
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SYMM

64X (0.6)
64X (0.24)
1
60X (0.5)
(R0.05) TYP
SYMM
64
49
48
65
16
33
17
32
(1.16) TYP
(8.8)
(0.58)
36X (□ 0.96)
(0.58)
(1.16) TYP
(8.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.