

触摸屏控制器

 查询样品: [ADS7843-Q1](#)

特性

- 符合汽车应用要求
- 按比例转换
- 单电源: **2.7V 至 5V**
- 转换率高达 **125kHz**
- 串行接口
- 可编程 **8 位或 12 位**分辨率
- **2 个**辅助模拟输入
- 完全断电控制

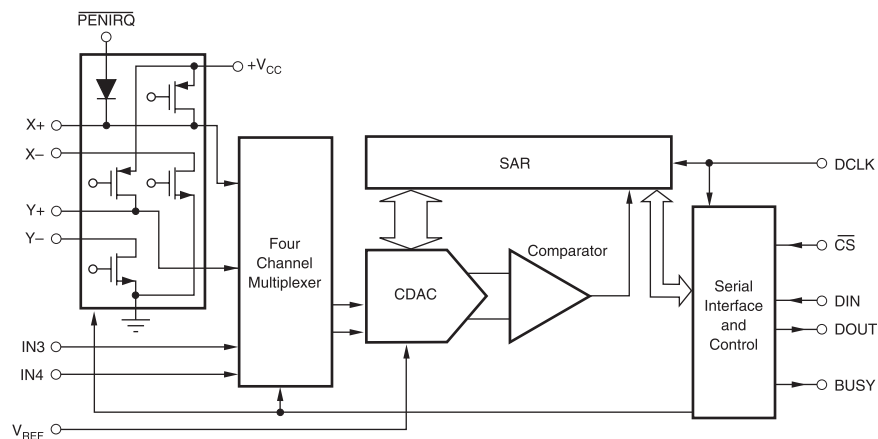
应用范围

- 个人数字助理
- 便携式仪表
- 销售点终端
- 寻呼机
- 触摸屏监视器

说明

ADS7843-Q1 是一款具有一个同步串行接口以及用于驱动触摸屏的低导通电阻开关的 12 位采样模数转换器 (ADC)。吞吐率为 125kHz 并且由一个 +2.7V 电源供电时, 典型功率耗散为 750 μ W。基准电压 (V_{REF}) 可以在 1V 至 + V_{CC} 之间变化, 相应地提供 0V 至 V_{REF} 的输入电压范围。该器件包括一个可将典型功率耗散减少至低于 0.5 μ W 的关断模式。ADS7843-Q1 可在低至 2.7V 的电压下工作。

ADS7843-Q1 所具有的低功耗、高速度以及板载开关使其成为电池供电类系统, 例如带有电阻式触摸屏的个人数字助理和其它便携式设备的理想选择。ADS7843-Q1 采用 SSOP-16 封装, 额定温度范围 -40 $^{\circ}$ C 至 +85 $^{\circ}$ C。



订购信息⁽¹⁾

| T_A | 封装 ⁽²⁾ | | 可订购部件号 | 正面标记 |
|------------------------------------|-------------------|----|----------------|--------|
| -40 $^{\circ}$ C 至 85 $^{\circ}$ C | SSOP-16-DBQ | 卷带 | ADS7843IDBQRQ1 | S7843Q |

(1) 要获得最新的封装和订货信息, 请参阅本文档末尾的封装选项附录, 或者浏览 TI 网站www.ti.com进行查询。

(2) 封装图样、热数据和符号可从网站www.ti.com/packaging中获取。



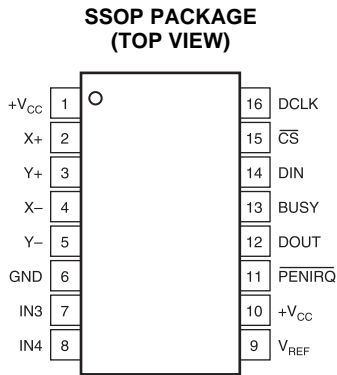
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN DESCRIPTIONS (continued)



PIN DESCRIPTIONS

| PIN | | DESCRIPTION |
|-----|------|---|
| NO. | NAME | |
| 1 | +VCC | Power Supply, 2.7V to 5V. |
| 2 | X+ | X+ Position Input. ADC input Channel 1. |
| 3 | Y+ | Y+ Position Input. ADC input Channel 2. |
| 4 | X- | X- Position Input |

| PIN | | DESCRIPTION |
|-----|----------------------------|---|
| NO. | NAME | |
| 5 | Y- | Y- Position Input |
| 6 | GND | Ground |
| 7 | IN3 | Auxiliary Input 1. ADC input Channel 3. |
| 8 | IN4 | Auxiliary Input 2. ADC input Channel 4. |
| 9 | VREF | Voltage Reference Input |
| 10 | +VCC | Power Supply, 2.7V to 5V. |
| 11 | $\overline{\text{PENIRQ}}$ | Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally). |
| 12 | DOUT | 1 Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH. |
| 13 | BUSY | Busy Output. This output is high impedance when CS is HIGH. |
| 14 | DIN | Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK. |
| 15 | CS | Chip Select Input. Controls conversion timing and enables the serial input/output register. |
| 16 | DCLK | External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | VALUE | UNIT |
|-----------------------------------|--------------------------------|------|
| +V _{CC} to GND | -0.3 V to 6.5 V | |
| +V _{CC} to GND | -0.3 to +6 | V |
| Analog inputs to GND | -0.3 to +V _{CC} + 0.3 | V |
| Digital inputs to GND | -0.3 to +V _{CC} + 0.3 | V |
| Power dissipation | 250 | mW |
| Maximum junction temperature | +150 | °C |
| Operating temperature range | -40°C to +85 | °C |
| Storage temperature range | -65°C to +150 | °C |
| Lead temperature (soldering, 10s) | +300 | °C |
| Electrostatic discharge (ESD) | Human-Body Model (HBM) | 400 |
| | Machine Model (MM) | 100 |
| | Charged-Device Model (CDM) | 750 |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $+V_{CC} = +2.7\text{V}$, $V_{REF} = +2.5\text{V}$, $f_{SAMPLE} = 125\text{kHz}$, $f_{CLK} = 16 \cdot f_{SAMPLE} = 2\text{MHz}$, 12-bit mode, and digital inputs = GND or $+V_{CC}$, unless otherwise noted.

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------|--|-------|---------------------|-----------------|--------------------|
| Analog Input | | | | | | |
| Full-Scale Input Span | | Positive Input – Negative Input | 0 | | VREF | V |
| Absolute Input Range | | Positive Input | -0.2 | | $+V_{CC} + 0.2$ | V |
| Negative Input | | -0.2 | +0.2 | | V | |
| Capacitance | | | | 25 | | pF |
| Leakage Current | | | | 0.1 | | μA |
| System Performance | | | | | | |
| Resolution | | | | 12 | | Bits |
| No Missing Codes | | | 11 | | | Bits |
| Integral Linearity Error | | | | | ± 2 | LSB ⁽¹⁾ |
| Offset Error | | | | | ± 6 | LSB |
| Offset Error Match | | | | 0.1 | 1 | LSB |
| Gain Error | | | | | ± 4 | LSB |
| Gain Error Match | | | | 0.1 | 1 | LSB |
| Noise | | | | 30 | | μVrms |
| Power-Supply Rejection | | | | 70 | | dB |
| Sampling Dynamics | | | | | | |
| Conversion Time | | | | | 12 | Clk Cycles |
| Acquisition Time | | | 3 | | | Clk Cycles |
| Throughput Rate | | | | | 125 | kHz |
| Multiplexer Settling Time | | | | 500 | | ns |
| Aperture Delay | | | | 30 | | ns |
| Aperture Jitter | | | | 100 | | ps |
| Channel-to-Channel Isolation | | $V_{IN} = 2.5\text{Vp-p}$ at 50kHz | | 100 | | dB |
| Switch Drivers | | | | | | |
| On-Resistance | Y+, X+ | | | 5 | | Ω |
| | Y-, X- | | | 6 | | Ω |
| Reference Input | | | | | | |
| Range | | | 1 | | $+V_{CC}$ | V |
| Resistance | | CS = GND or $+V_{CC}$ | | 5 | | G Ω |
| Input Current | | | | 13 | 40 | μA |
| $f_{SAMPLE} = 12.5\text{kHz}$ | | | | 2.5 | | μA |
| CS = $+V_{CC}$ | | | 0.001 | | 3 | μA |
| Digital Input/Output | | | | | | |
| Logic Family | | | | CMOS | | |
| Logic Levels, Except $\overline{\text{PENIRQ}}$ | V_{IH} | $ I_{IH} \leq +5\mu\text{A}$ | | $+V_{CC} \cdot 0.7$ | $+V_{CC} + 0.3$ | |
| | V_{IL} | $ I_{IL} \leq +5\mu\text{A}$ | | -0.3 | +0.8 | V |
| | V_{OH} | $I_{OH} = -250\mu\text{A}$ | | $+V_{CC} \cdot 0.8$ | | V |
| | V_{OL} | $I_{OL} = 250\mu\text{A}$ | | | 0.4 | V |
| $\overline{\text{PENIRQ}}$ | V_{OL} | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, 100k Ω Pull-Up | | | 0.8 | V |
| Data Format | | | | Straight Binary | | |

(1) LSB means Least Significant Bit. With V_{REF} equal to $+2.5\text{V}$, 1LSB is $610\mu\text{V}$.

ELECTRICAL CHARACTERISTICS (continued)

at $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{CC} = +2.7\text{V}$, $V_{REF} = +2.5\text{V}$, $f_{SAMPLE} = 125\text{kHz}$, $f_{CLK} = 16 \cdot f_{SAMPLE} = 2\text{MHz}$, 12-bit mode, and digital inputs = GND or $+V_{CC}$, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------|-----|-----|-----|--------------------|
| Power-Supply Requirements | | | | | |
| +VCC | Specified Performance | 2.7 | | 3.6 | V |
| Quiescent Current | | | 280 | 650 | μA |
| $f_{SAMPLE} = 12.5\text{kHz}$ | | | 220 | | μA |
| Shutdown Mode with $DCLK = DIN = +VCC$ | | | | 3 | μA |
| Power Dissipation | $+VCC = +2.7\text{V}$ | | | 1.8 | mW |
| Temperature Range | | | | | |
| Specified Performance | | -40 | | +85 | $^{\circ}\text{C}$ |

TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

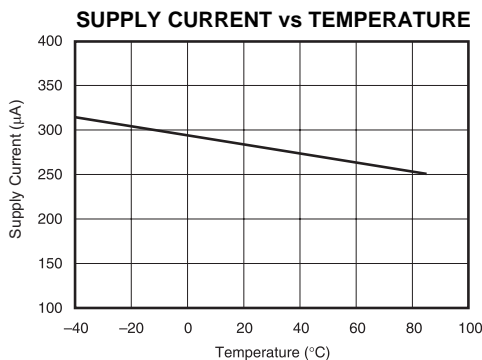


Figure 1.

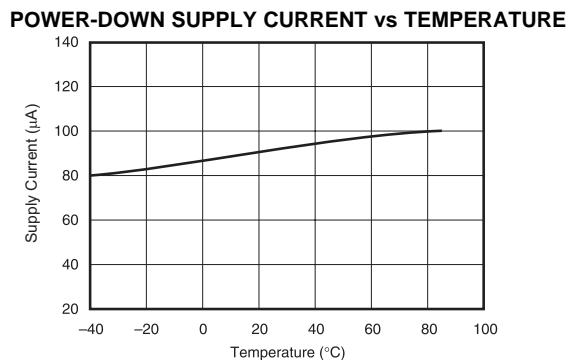


Figure 2.

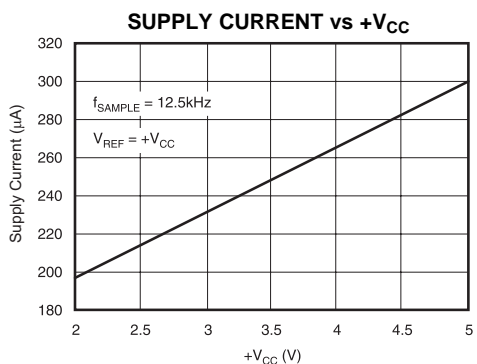


Figure 3.

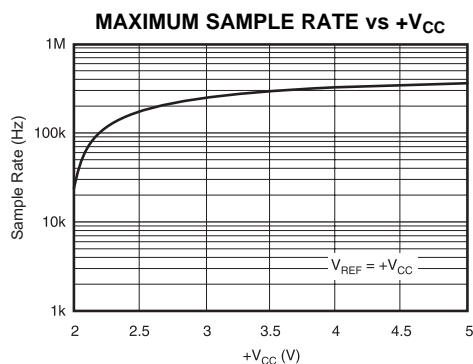


Figure 4.

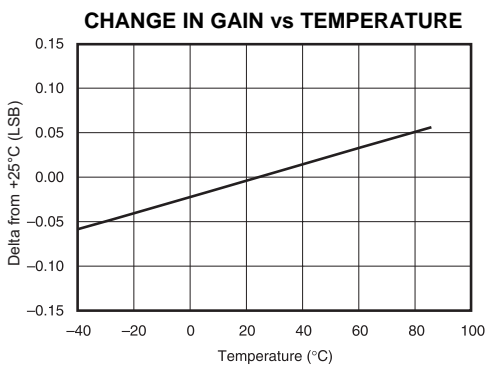


Figure 5.

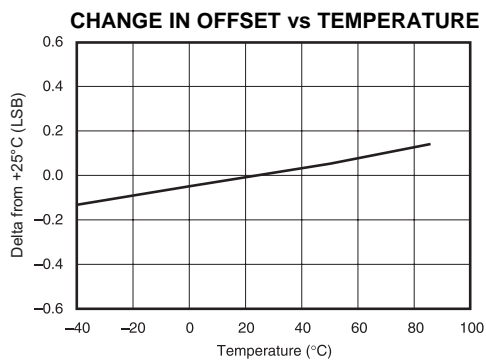


Figure 6.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

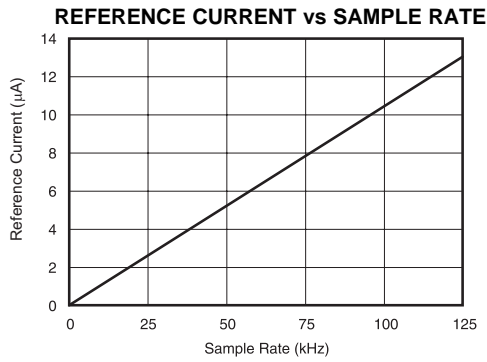


Figure 7.

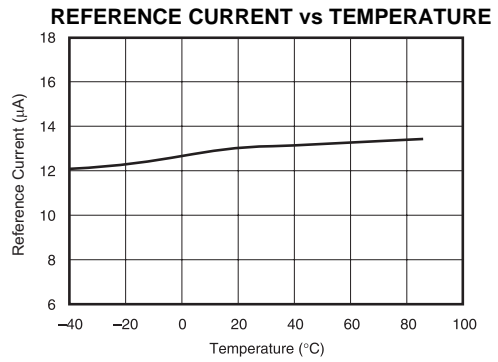


Figure 8.

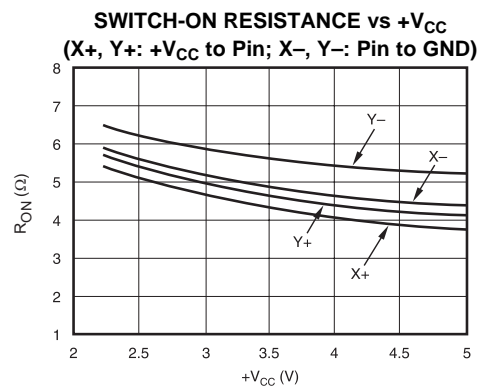


Figure 9.

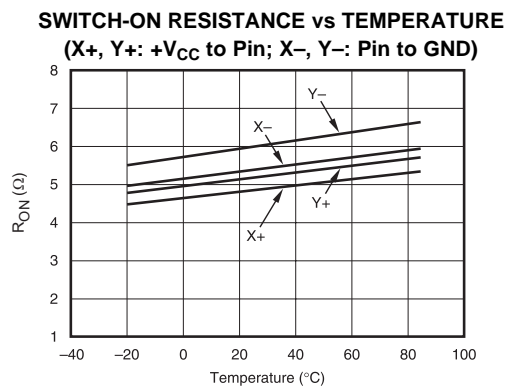


Figure 10.

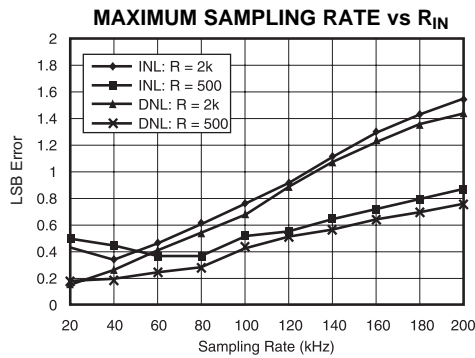


Figure 11.

THEORY OF OPERATION

The ADS7843-Q1 is a classic Successive Approximation Register (SAR) ADC. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µm CMOS process.

The basic operation of the ADS7843-Q1 is shown in Figure 12. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 1V and +VCC. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7843-Q1.

The analog input to the converter is provided via a four-channel multiplexer. A unique configuration of low on-resistance switches allows an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the switch's on-resistance error (should this be a source of error for the particular measurement).

ANALOG INPUT

See Figure 13 for a block diagram of the input multiplexer on the ADS7843-Q1, the differential input of the ADC, and the converter's differential reference. Table 1 and Table 2 show the relationship between the A2, A1, A0, and SER/DFR control bits and the configuration of the ADS7843-Q1. The control bits are provided serially via the DIN pin—see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 13) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

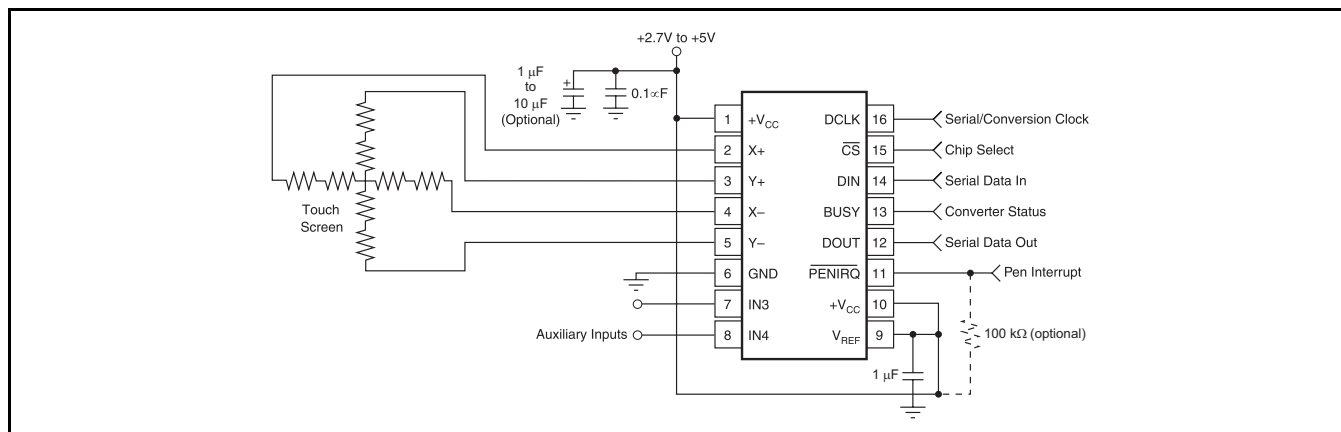


Figure 12. Basic Operation of the ADS7843-Q1

Table 1. Input Configuration, Single-Ended Reference Mode (SER/DFR HIGH)

| A2 | A1 | A0 | X+ | Y+ | IN3 | IN4 | –IN(1) | X SWITCHES | Y SWITCHES | +REF ⁽¹⁾ | –REF ⁽¹⁾ |
|----|----|----|-----|-----|-----|-----|--------|------------|------------|---------------------|---------------------|
| 0 | 0 | 1 | +IN | | | | GND | OFF | ON | +VREF | GND |
| 1 | 0 | 1 | | +IN | | | GND | ON | OFF | +VREF | GND |
| 0 | 1 | 0 | | | +IN | | GND | OFF | OFF | +VREF | GND |
| 1 | 1 | 0 | | | | +IN | GND | OFF | OFF | +VREF | GND |

(1) Internal node, for clarification only—not directly accessible by the user.

Table 2. Input Configuration, Differential Reference Mode (SER/DFR LOW).

| A2 | A1 | A0 | X+ | Y+ | IN3 | IN4 | -IN(1) | X SWITCHES | Y SWITCHES | +REF ⁽¹⁾ | -REF ⁽¹⁾ |
|----|----|----|-----|-----|-----|-----|--------|------------|------------|---------------------|---------------------|
| 0 | 0 | 1 | +IN | | | | -Y | OFF | ON | +Y | -Y |
| 1 | 0 | 1 | | +IN | | | -X | ON | OFF | +X | -X |
| 0 | 1 | 0 | | | +IN | | GND | OFF | OFF | +VREF | GND |
| 1 | 1 | 0 | | | | +IN | GND | OFF | OFF | +VREF | GND |

(1) Internal node, for clarification only—not directly accessible by the user.

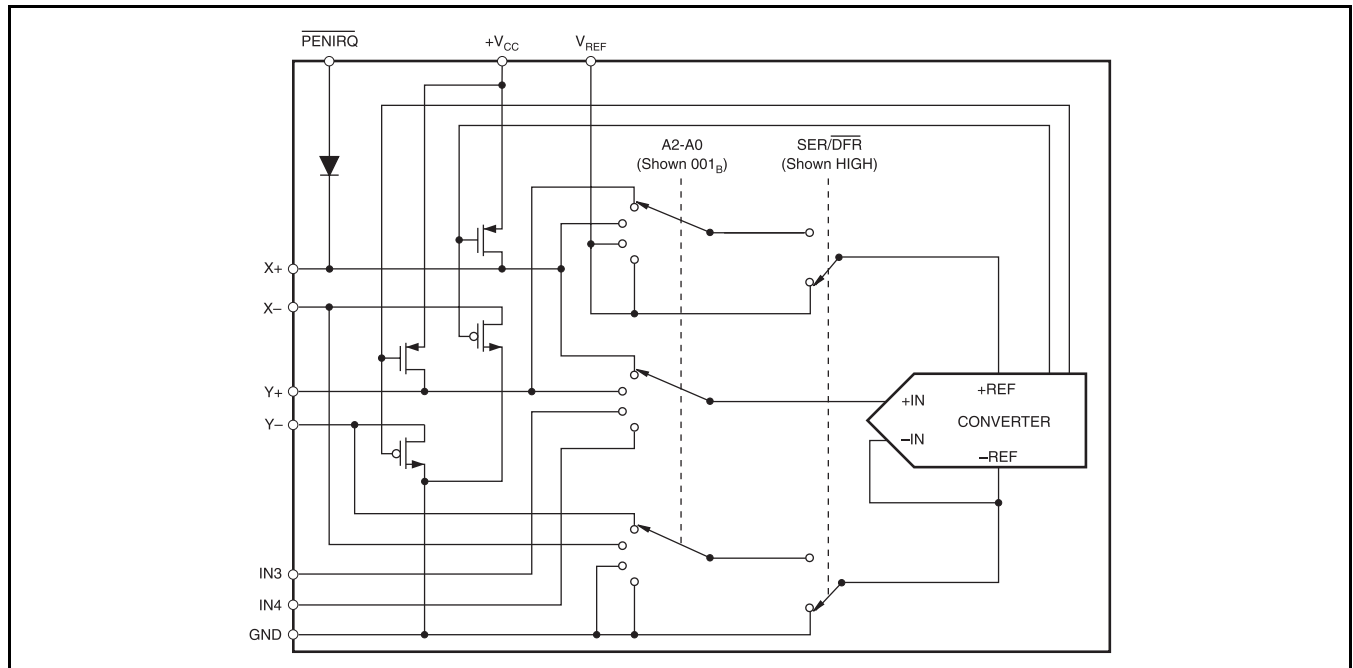


Figure 13. Simplified Diagram of Analog Input

REFERENCE INPUT

The voltage difference between +REF and -REF (shown in Figure 13) sets the analog input range. The ADS7843-Q1 will operate with a reference in the range of 1V to +VCC. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, it will typically be 5LSBs with a 1V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal.

The voltage into the VREF input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS7843-Q1. Typically, the input current is 13µA with VREF = 2.7V and fSAMPLE = 125kHz. This value will vary by a few microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

There is also a critical item regarding the reference when making measurements where the switch drivers are on. For this discussion, it's useful to consider the basic operation of the ADS7843-Q1 as shown in Figure 12. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y- drivers, and digitizing the voltage on X+ (shown in Figure 14). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern).

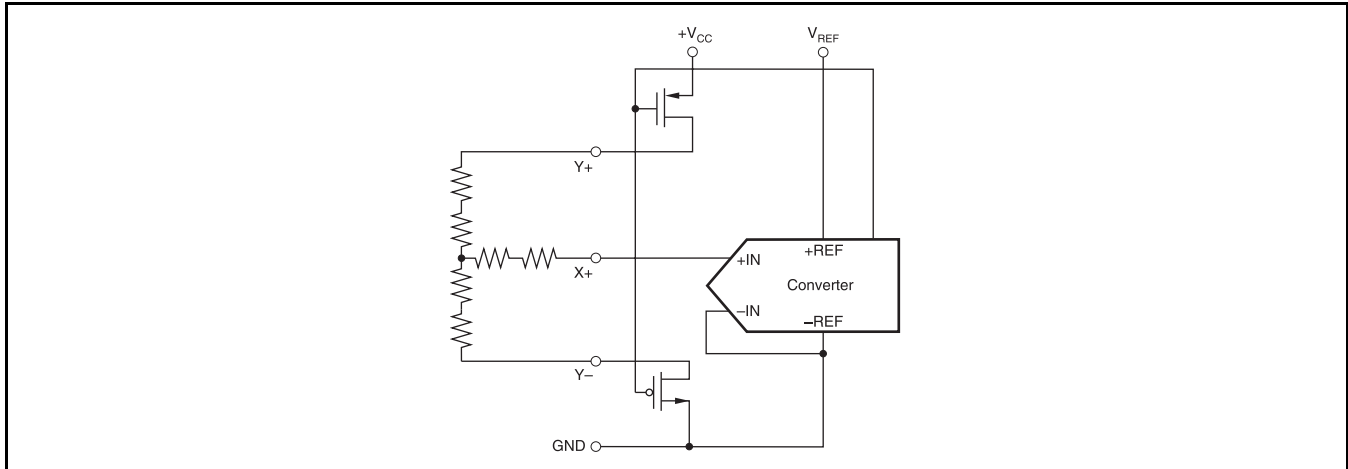


Figure 14. Simplified Diagram of Single-Ended Reference (SER/DFR HIGH, Y Switches Enabled, X+ is Analog Input)

However, since the resistance between Y+ and Y- is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error. This situation can be remedied as shown in Figure 15. By setting the SER/DFR bit LOW, the +REF and -REF inputs are connected directly to Y+ and Y-. This makes the A/D conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation, see the Power Dissipation section for more details. As a final note about the differential reference mode, it must be used with +VCC as the source of the +REF voltage and cannot be used with VREF. It is possible to use a high precision reference on VREF and single-ended reference mode for measurements which do not need to be ratiometric. Or, in some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the ADS7843-Q1, but they might not be able to supply enough current for the external load (such as a resistive touch screen).

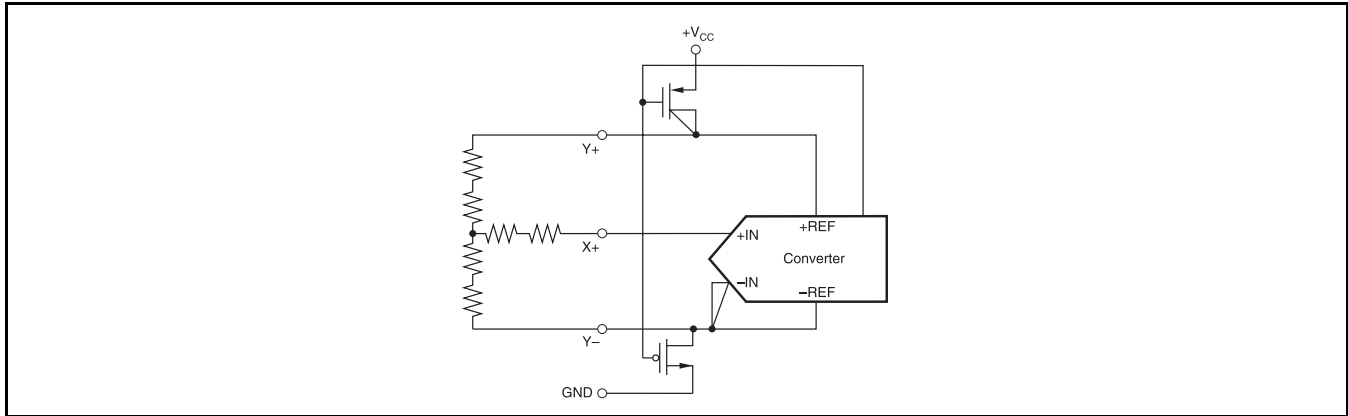


Figure 15. Simplified Diagram of Differential Reference (SER/DFR LOW, Y Switches Enabled, X+ is Analog Input).

DIGITAL INTERFACE

Figure 16 shows the typical operation of the ADS7843-Q1's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer, switches, and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the internal switches are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the internal switches may turn off. The next 12th clock cycles accomplish the actual A/D conversion. If the conversion is ratiometric (SER/DFR LOW), the internal switches are on during the conversion. A 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

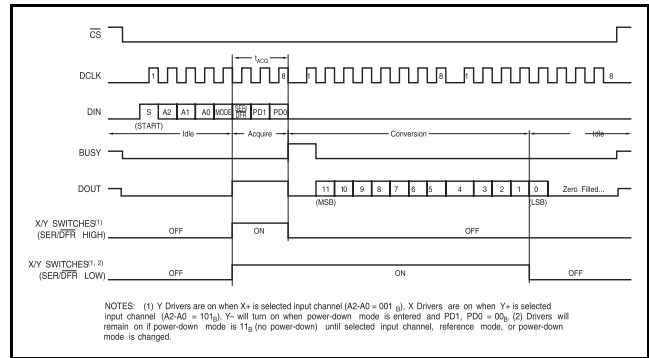


Figure 16. Conversion Timing, 24 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

Control Byte

See Figure 16 for the placement and order of the control bits within the control byte. Table 3 and Table 4 give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7843-Q1 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Table 1 and Table 2 and Figure 13). The MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SER/DFR bit controls the reference mode: either single-ended (HIGH) or differential (LOW). (The differential mode is also referred to as the ratiometric conversion mode.) In single-ended mode, the converter's reference voltage is always the difference between the VREF and GND pins. In differential mode, the reference voltage is the difference between the currently enabled switches. See Table 1 and Table 2 and Figure 13 through Figure 15 for more information. The last two bits (PD1-PD0) select the power-down mode as shown in Table 5. If both inputs

are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion

is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid. There are two power-down modes: one where PENIRQ is disabled and one where it is enabled.

Table 3. Order of the Control Bits in the Control Byte

| Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) |
|-------------|-------|-------|-------|-------|---------------------|-------|-------------|
| S | A2 | A1 | A0 | MODE | SER/D _{FR} | PD1 | PD0 |

16-Clocks per Conversion

The control bits for conversion $n + 1$ can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in [Figure 17](#). This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter.

Table 4. Descriptions of the Control Bits within the Control Byte

| BIT | NAME | DESCRIPTION |
|-----|---------|--|
| 7 | S | Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 16th clock cycle in 12-bit conversion mode or every 12th clock cycle in 8-bit conversion mode. |
| 6-4 | A2-A0 | Channel Select Bits. Along with the SER/DFR bit, these bits control the setting of the multiplexer input, switches, and reference inputs, see Tables I and II. |
| 3 | MODE | 12-Bit/8-Bit Conversion Select Bit. This bit controls the number of bits for the following conversion: 12 bits (LOW) or 8 bits (HIGH). |
| 2 | SER/DFR | Single-Ended/Differential Reference Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, switches, and reference inputs, see Tables I and II. |
| 1-0 | PD1-PD0 | Power-Down Mode Select Bits. See Table V for details. |

Table 5. Power-Down Selection

| PD1 | PD0 | PENIRQ | DESCRIPTION |
|-----|-----|----------|--|
| 0 | 0 | Enabled | Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. The Y– switch is on while in power-down. |
| 0 | 1 | Disabled | Same as mode 00, except PENIRQ is disabled. The Y– switch is off while in power-down mode. |
| 1 | 0 | Disabled | Reserved for future use. |
| 1 | 1 | Disabled | No power-down between conversions, device is always powered. |

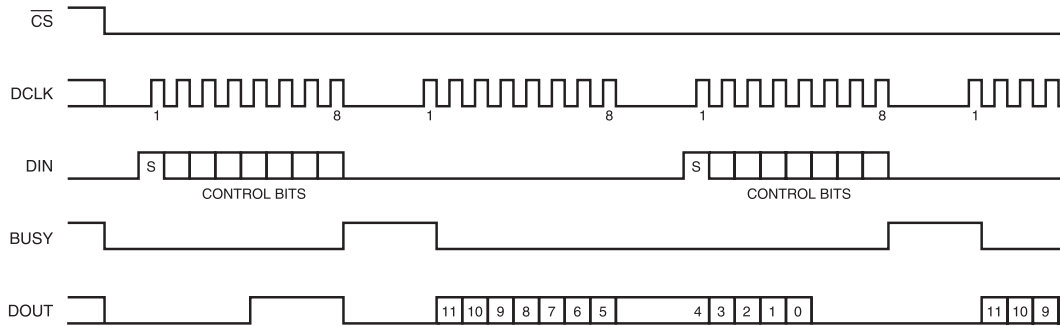


Figure 17. Conversion Timing, 16 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the ADS7843-Q1 is fully powered while other serial communications are taking place during a conversion.

Digital Timing

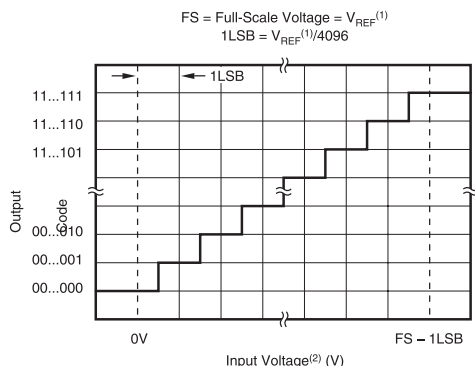
Figure 19 and Table 6 provide detailed timing for the digital interface of the ADS7843-Q1.

Table 6. Timing Specifications
 (+V_{CC} = +2.7V and Above, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

| SYMBOL | DESCRIPTION | MIN | MAX | UNITS |
|------------------|--|----------------------|-----|-------|
| t _{ACQ} | Acquisition Time | 1.5 | | μs |
| t _{DS} | DIN Valid Prior to DCLK Rising | 100 | | ns |
| t _{DH} | DIN Hold After DCLK HIGH | 10 | | ns |
| t _{DO} | DCLK Falling to DOUT Valid | | 200 | ns |
| t _{DV} | \overline{CS} Falling to DOUT Enabled | | 200 | ns |
| t _{TR} | \overline{CS} Rising to DOUT Disabled | | 200 | ns |
| t _{CSS} | \overline{CS} Falling to First DCLK Rising | 100 | | ns |
| t _{CSH} | \overline{CS} Rising to DCLK Ignored | 0 | | ns |
| t _{CH} | DCLK HIGH | 200 | | ns |
| t _{CL} | DCLK LOW | 200 | | ns |
| t _{BD} | DCLK Falling to BUSY Rising | | 200 | ns |
| t _{BDV} | \overline{CS} Falling to BUSY Enabled | | 200 | ns |
| t _{BTR} | \overline{CS} Rising to BUSY Disabled | 200 200 200 ns ns ns | 200 | ns |

Data Format

The ADS7843-Q1 output data is in Straight Binary format, as shown in Figure 18. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF – (–REF). See Figure 2.
(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 2

Figure 18. Ideal Input Voltages and Output Codes

8-Bit Conversion

The ADS7843-Q1 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide 12-bit transfers or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7843-Q1 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

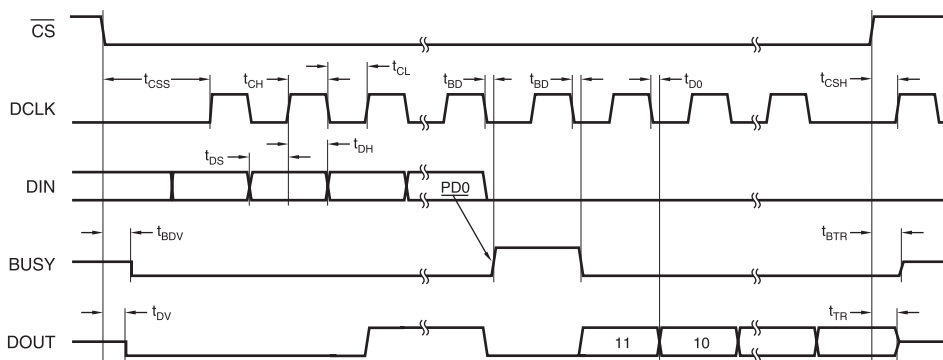


Figure 19. Detailed Timing Diagram

POWER DISSIPATION

There are two major power modes for the ADS7843-Q1: full power (PD1-PD0 = 11B) and auto power-down (PD1-PD0 = 00B). When operating at full speed and 16 clocks per conversion (see Figure 17), the ADS7843-Q1 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full power mode and auto power-

down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are simply done less often, the difference between the two modes is dramatic.

Figure 20 shows the difference between reducing the DCLK frequency (“scaling” DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the converter’s internal switches are on only when the analog input voltage is being acquired (see Figure 16). Thus, the external device, such as a resistive touch screen, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 16). If the conversion rate is high, this could substantially increase power dissipation.

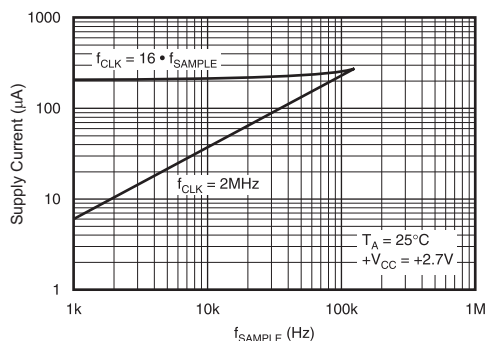


Figure 20. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency

LAYOUT

The following layout suggestions should provide the most optimum performance from the ADS7843-Q1. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly “clean” power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter’s power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the ADS7843-Q1 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just

prior to latching the output of the analog comparator. Thus, during any single conversion for an ‘n-bit’ SAR converter, there are n ‘windows’ in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7843-Q1 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between +VCC and the power supply is high. The reference should be similarly bypassed with a 0.1µF capacitor. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation. The ADS7843-Q1 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7843-Q1 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections will be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

REVISION HISTORY

| Changes from Original (March, 2011) to Revision A | Page |
|---|------|
| • 将正面标记从 ADS7843Q 改为 S7843Q。 | 1 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| ADS7843IDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | S7843Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

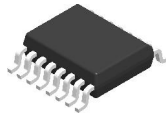
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS7843IDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS7843IDBQRQ1 | SSOP | DBQ | 16 | 2500 | 367.0 | 367.0 | 35.0 |

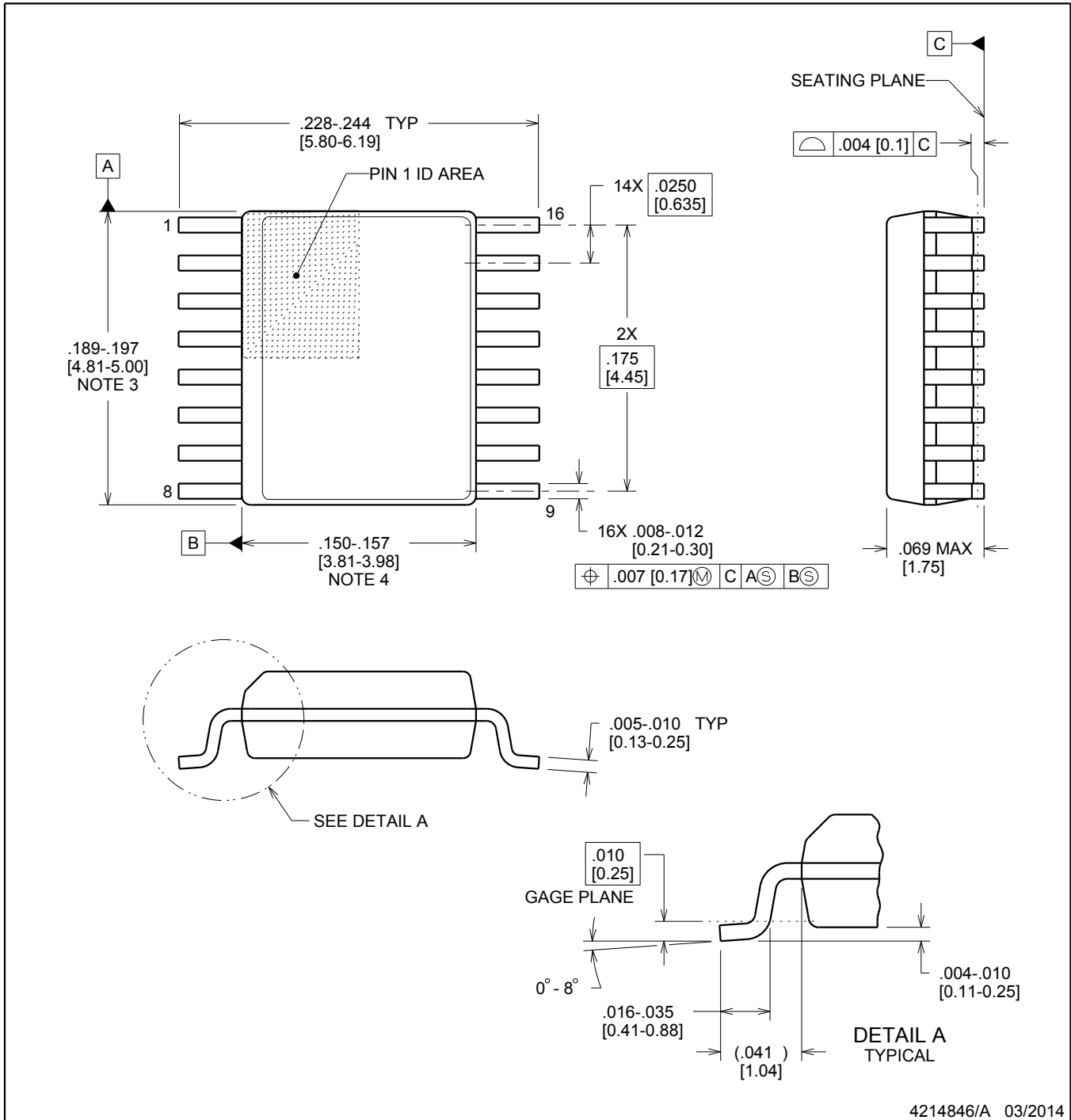


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

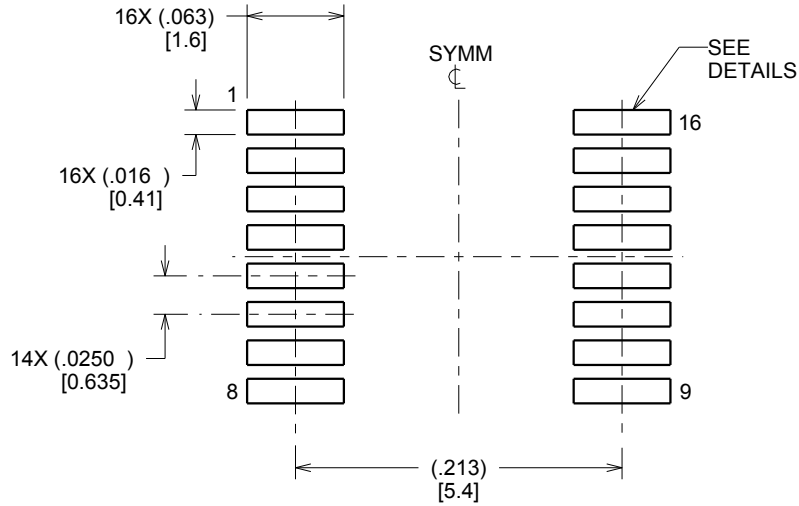
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

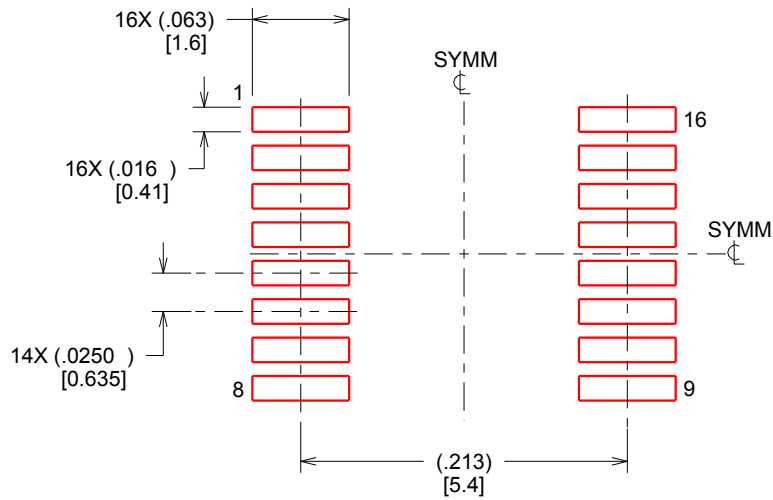
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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