

## AM26LV31E 具有 $\pm 15\text{kV}$ IEC ESD 保护功能的 低电压高速四路差分线路驱动器

### 1 特性

- 达到或超出 TIA/EIA-422-B 和 ITU 建议 V.11 的要求
- 由单个 3.3V 电源供电
- 为 RS422 总线引脚提供 ESD 保护
  - $\pm 15\text{kV}$  人体放电模型 (HBM)
  - $\pm 8\text{kV}$  IEC61000-4-2 接触放电
  - $\pm 15\text{kV}$  IEC61000-4-2 气隙放电
- 开关频率高达 32MHz
- 传播延迟时间: 8ns (典型值)
- 脉冲偏移时间: 500ps (典型值)
- 高输出驱动电流:  $\pm 30\text{mA}$
- 受控上升和下降时间: 5ns (典型值)
- 100  $\Omega$  负载时的差分输出电压: 2.6V (典型值)
- 支持 5V 逻辑输入及 3.3V 电源
- $I_{\text{off}}$  支持局部关断模式运行
- 驱动器输出短路保护电路
- 无干扰上电和断电保护
- 封装选项: SO、SOIC、TSSOP、VQFN

### 2 应用

- 电机驱动
- 航天、航空和国防
- 医疗、保健和健身
- 无线基础设施
- 工厂自动化和控制

### 3 说明

AAM26LV31E 是一款具有三态输出的四路差分线路驱动器。此驱动器具有  $\pm 15\text{kV}$  ESD (HBM 和 IEC61000-4-2, 空气间隙放电) 和  $\pm 8\text{kV}$  ESD (IEC61000-4-2, 接触放电) 保护。该器件能够以较小的电源电压满足 TIA/EIA-422-B 和 ITU 建议 V.11 驱动器的要求。

这款器件经过优化, 可在高达 32MHz 的开关速率下实现平衡总线传输。输出端可提供很高的电流, 从而驱动双绞线传输线路等平衡线路, 并在关断情况下提供高阻抗。

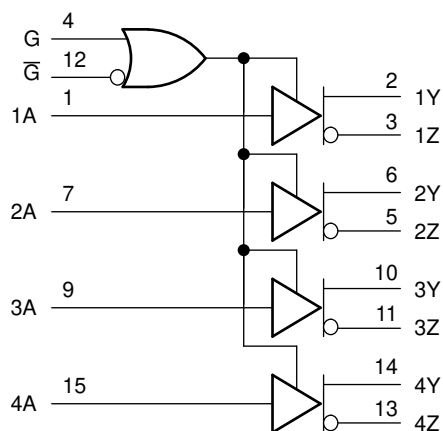
AM26LV31E 的工作温度范围是  $-40^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$ 。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
AM26LV31E	SOIC ( D , 16 )	9.9mm × 6mm
	SO ( NS , 16 )	10.2mm × 7.8mm
	TSSOP ( PW , 16 )	5mm × 6.4mm
	VQFN ( RGY , 16 )	4mm × 3.5mm

(1) 有关更多信息, 请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



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逻辑图



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## 4 Pin Configuration and Functions

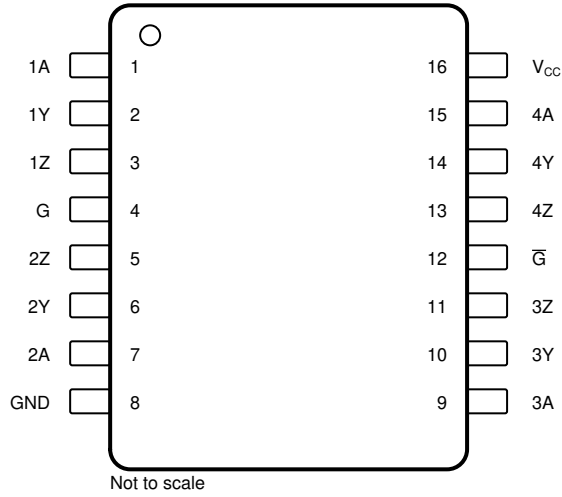


图 4-1. D, NS, or PW Package  
16-Pin SOIC, SO, TSSOP  
(Top View)

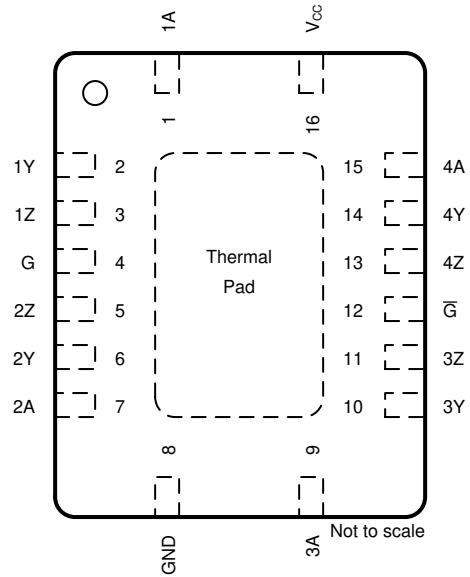


图 4-2. RGY Package  
16-Pin VQFN With Thermal Pad  
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	1	I	Logic data input to RS422 driver 1
1Y	2	O	RS-422 data line for driver 1
1Z	3	O	RS-422 data line for driver 1
2A	7	I	Logic data input to RS422 driver 2
2Y	6	O	RS-422 data line for driver 2
2Z	5	O	RS-422 data line for driver 2
3A	9	I	Logic data input to RS422 driver 3
3Y	10	O	RS-422 data line for driver 3
3Z	11	O	RS-422 data line for driver 3
4A	15	I	Logic data input to RS422 driver 4
4Y	14	O	RS-422 data line for driver 4
4Z	13	O	RS-422 data line for driver 4
G	4	I	Driver enable (active high)
Ḡ	12	I	Driver enable (active low)
GND	8	—	Device ground pin
V <sub>CC</sub>	16	—	Power input (5V)

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	- 0.5	6	V
V <sub>I</sub>	Input voltage	- 0.5	6	V
V <sub>O</sub>	Output voltage	- 0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	- 20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	- 20	mA
I <sub>O</sub>	Continuous output current		±150	mA
	Continuous current through V <sub>CC</sub> or GND		±200	mA
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>A</sub>	Operating free-air temperature	- 40	85	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential input voltage are with respect to the network GND.

### 5.2 ESD Ratings

		VALUE	UNIT		
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±15000	V
			All pins except 2, 3, 5, 6, 10, 11, 13, and 14	±2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±1000		
	IEC 61000-4-2 contact discharge	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±8000		
	IEC 61000-4-2 air-gap discharge	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±15000		

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
V <sub>I</sub>	Input voltage	0		5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current			- 30	mA
I <sub>OL</sub>	Low-level output current			30	mA
T <sub>A</sub>	Operating free-air temperature	- 40		85	°C

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	AM26LV31E				UNIT
	D (SOIC)	PW (TSSOP)	NS (SO)	RGY (VQFN)	
	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	84.6	107.5	88.5	48.4	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	43.5	38.4	46.2	46.8	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	43.2	53.7	50.7	24.6	°C/W
$\psi_{JT}$ Junction-to-top characterization parameter	10.4	3.2	13.5	2.3	°C/W
$\psi_{JB}$ Junction-to-board characterization parameter	42.8	53.1	50.3	24.5	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -20mA$	2.4	3		V
$V_{OL}$ Low-level output voltage	$V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA$		0.2	0.4	V
$ V_{OD1} $ Differential output voltage	$I_O = 0mA$	2		4	V
$ V_{OD2} $ Differential output voltage	$R_L = 100\Omega$ (see <a href="#">图 6-1</a> )	2	2.6		V
$\Delta V_{OD} $ Change in magnitude of differential output voltage	$R_L = 100\Omega$ (see <a href="#">图 6-1</a> )			±0.4	V
$V_{OC}$ Common-mode output voltage	$R_L = 100\Omega$ (see <a href="#">图 6-1</a> )		1.5	2	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage	$R_L = 100\Omega$ (see <a href="#">图 6-1</a> )			±0.4	V
$I_{O(OFF)}$ Output current with power off	$V_{CC} = 0, V_O = -0.25V$ or $5.5V$			±100	μA
$I_{OZ}$ High-impedance state output current	$V_O = -0.25V$ or $5.5V, G = 0.8V$ or $\bar{G} = 2V$			±100	μA
$I_I$ Input current	$V_{CC} = 0$ or $3.6V, V_I = 0$ or $5.5V$			±10	μA
$I_{OS}$ Short-circuit output current	$V_O = V_{CC}$ or GND <sup>(2)</sup>	-30		-150	mA
$I_{CC}$ Supply current (total package)	$V_I = V_{CC}$ or GND, No load, enable			100	μA
$C_{pd}$ Power dissipation capacitance	No load <sup>(3)</sup>		160		pF

- (1) All typical values are at  $V_{CC} = 3.3V, T_A = 25^\circ C$ .  
(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  
(3)  $C_{pd}$  determines the no-load dynamic current consumption.  $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

## 5.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output	See 图 6-2	4	8	12	ns
$t_{PLH}$	Propagation delay time, low- to high-level output		4	8	12	ns
$t_t$	Transition time ( $t_r$ or $t_f$ )	See 图 6-2		5	10	ns
$t_{PZH}$	Output-enable time to high level	See 图 6-3		10	20	ns
$t_{PZL}$	Output-enable time to low level	See #none#		10	20	ns
$t_{PHZ}$	Output-disable time from high level	See 图 6-3		10	20	ns
$t_{PLZ}$	Output-disable time from low level	See #none#		10	20	ns
$t_{sk(p)}$	Pulse skew	See 图 6-2 (2) (3)		0.5	1.5	ns
$t_{sk(o)}$	Skew limit (pin to pin)				1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)				3	ns
$f_{(max)}$	Maximum operating frequency	See 图 6-2		32		MHz

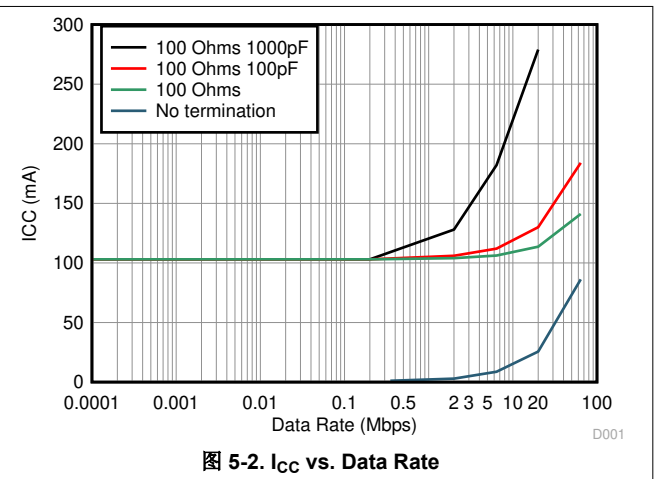
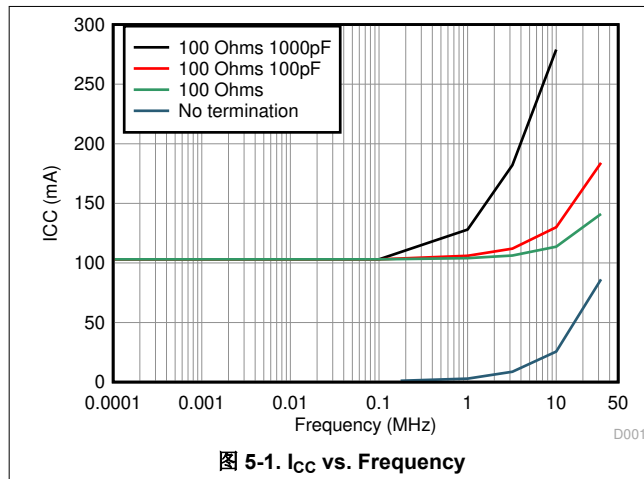
(1) All typical values are at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

(3) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.7 Typical Characteristics

图 5-1 and 图 5-2 show typical  $I_{CC}$  values at various frequencies/data rates for various termination conditions.



## 6 Parameter Measurement Information

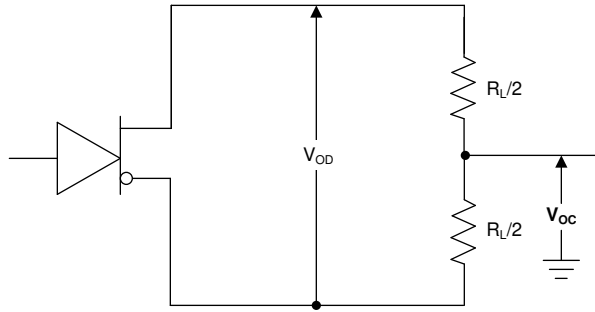
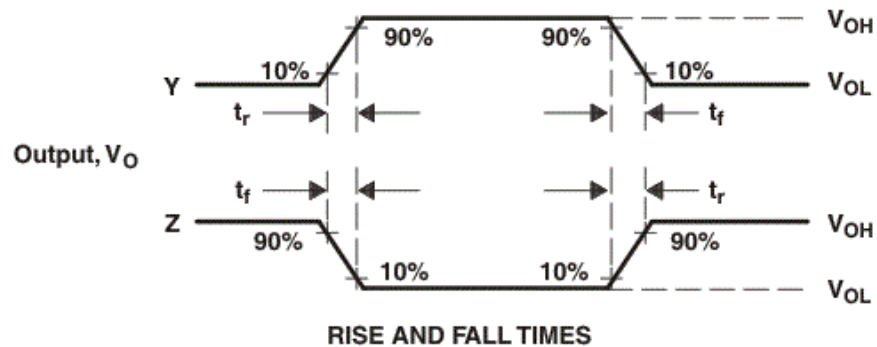
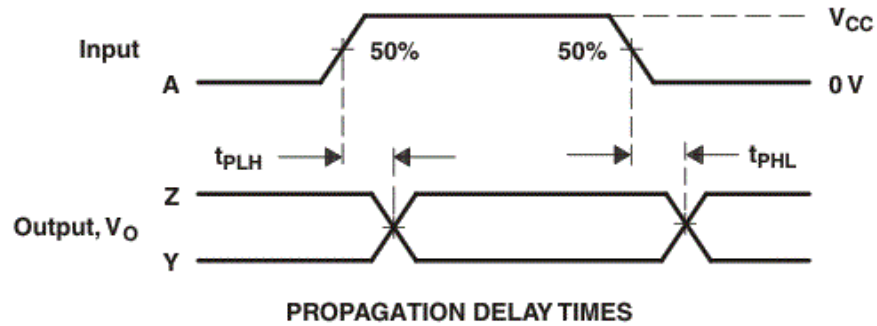
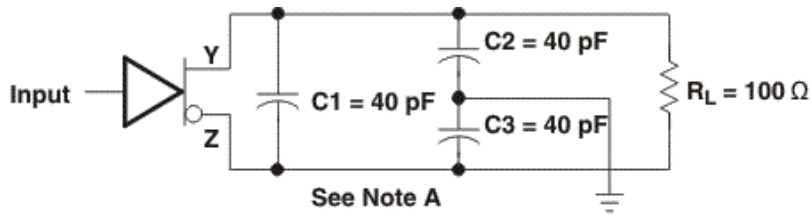
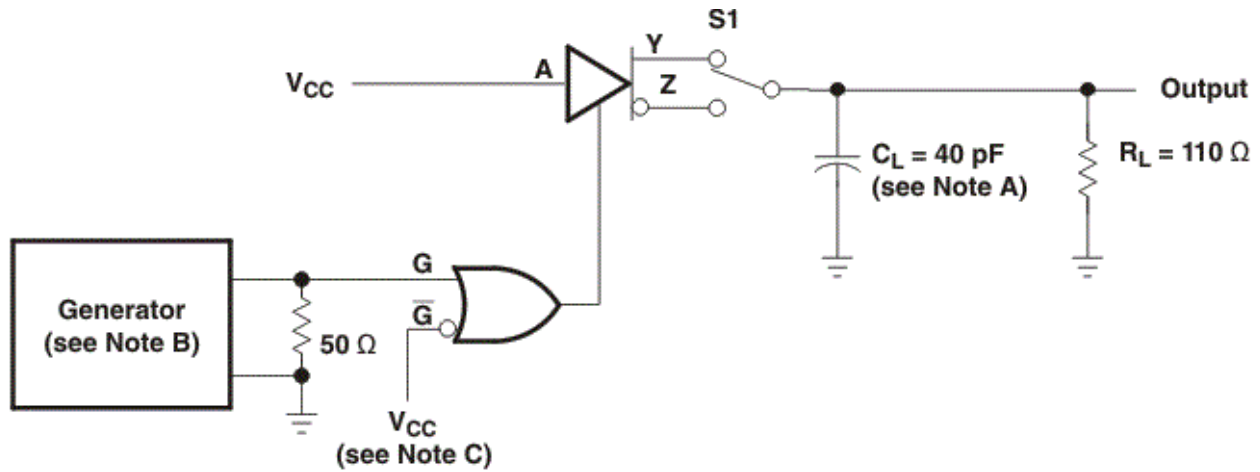


图 6-1. Test Circuit,  $V_{OD}$  and  $V_{OC}$

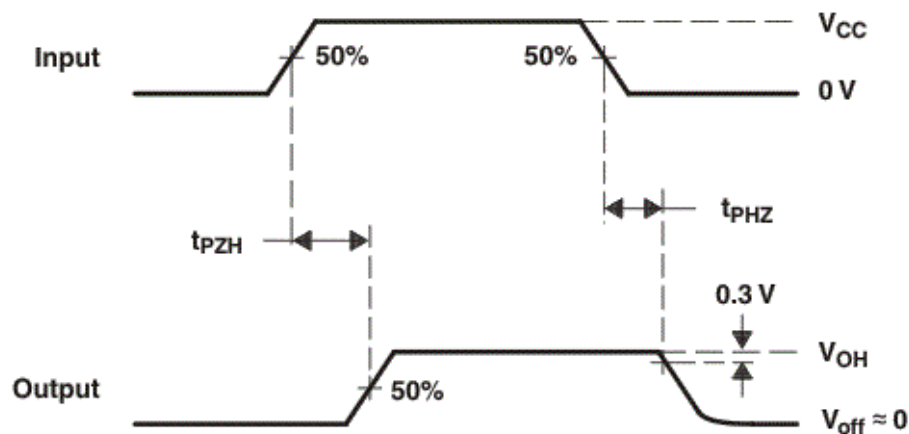


- A.  $C_L$  includes probe and stray capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10MHz, 50% duty cycle,  $t_r$  and  $t_f \leq 10$ ns.

图 6-2. Test Circuit and Voltage Waveforms,  $t_{PHL}$  and  $t_{PLH}$



TEST CIRCUIT

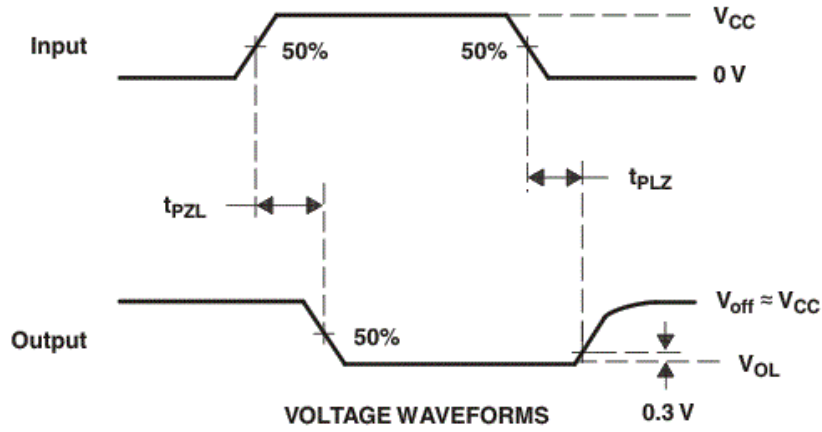
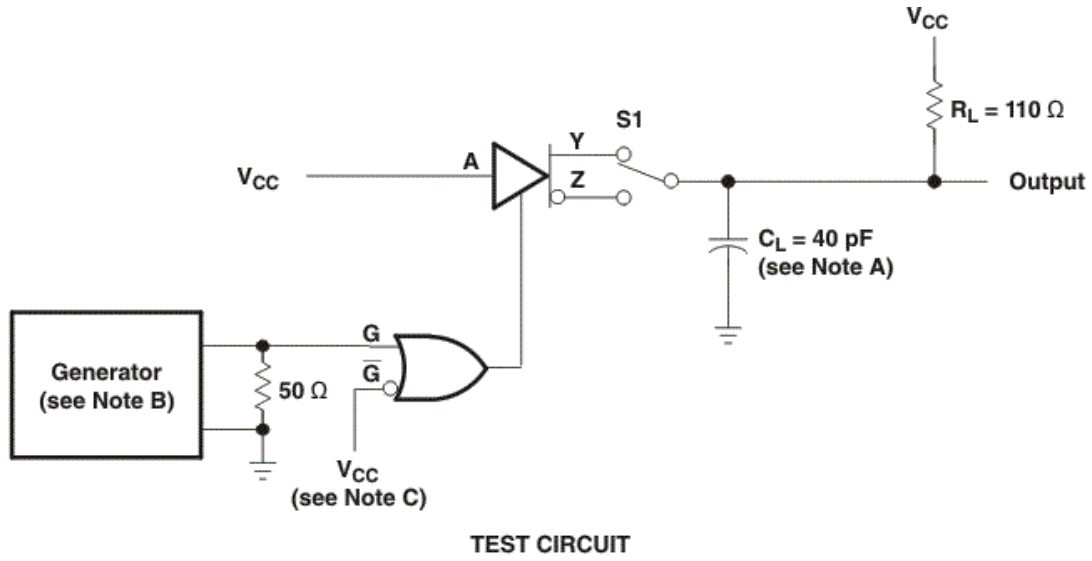


VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and stray capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r$  and  $t_f \leq 2$ ns.
- C. To test the active-low enable  $\bar{G}$  ground G and apply inverted waveform to  $\bar{G}$ .

图 6-3. Test Circuit and Voltage Waveforms,  $t_{PZH}$  and  $t_{PHZ}$





- A.  $C_L$  includes probe and stray capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle,  $t_r$  and  $t_f \leq 2\text{ns}$ .
- C. To test the active-low enable  $\overline{G}$  ground G and apply inverted waveform to  $\overline{G}$ .

## 7 Detailed Description

### 7.1 Overview

The AM26LV31E is a quadruple differential line driver with 3-state outputs. The device is designed to meet TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage. The high current capability of the outputs allow for driving balanced lines, such as twisted-pair transmission lines, and provide a high impedance in the power-off condition. The AM26LV31E is optimized for balanced-bus transmission line at switching rates up to 32MHz.

From a single 3.3V power supply, the device operates four 3-state differential line drivers with integrated active high and active low enables for precise control. The device is capable of accepting 5V logic inputs with a 3.3V supply. The driver is designed to handle loads of a minimum of  $\pm 30\text{mA}$  of sink or source current.

### 7.2 Functional Block Diagram

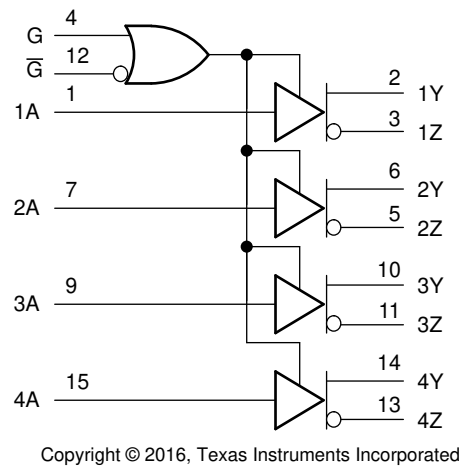


图 7-1. Logic Diagram

### 7.3 Feature Description

#### 7.3.1 Complementary Out-Enable Inputs

The AM26LV31E transmitter outputs can be configured using the G and  $\overline{G}$  logic inputs. The transmitter outputs are enabled when either G is set to logic HIGH or  $\overline{G}$  is set to logic LOW. The reverse disables the outputs (G = LOW,  $\overline{G}$  = HIGH). See 表 7-1 for the complete truth table.

#### 7.3.2 High Output Impedance for Specific Driver Enable Inputs

When the AM26LV31E transmitter outputs are disabled using G and  $\overline{G}$  logic inputs, the outputs are set to a high impedance state.

## 7.4 Device Functional Modes

表 7-1 lists the functional modes of the AM26LV31E.

表 7-1. Function Table

INPUT A <sup>(1)</sup>	ENABLES		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant,  
Z = high impedance (off)

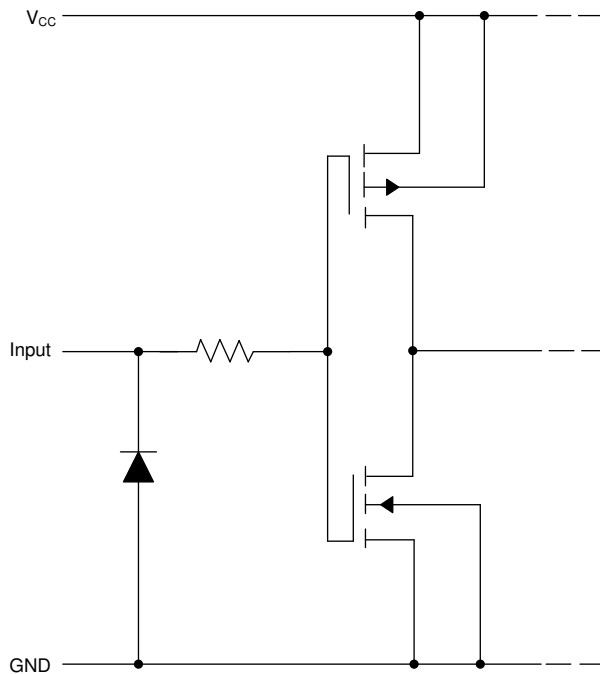


图 7-2. Equivalent of Each Input (A, G, or  $\bar{G}$ ) Schematic

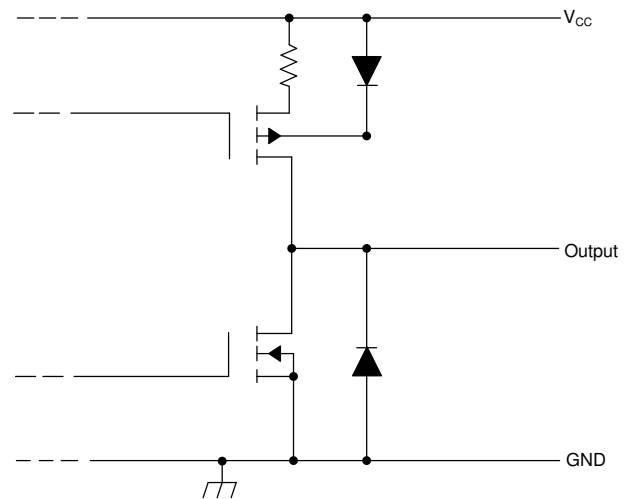


图 7-3. Typical of Each Driver Output Schematic

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100  $\Omega$ , 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31E and AM26LV32E, respectively, were tested at room temperature with a 3.3V supply voltage. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

### 8.2 Typical Application

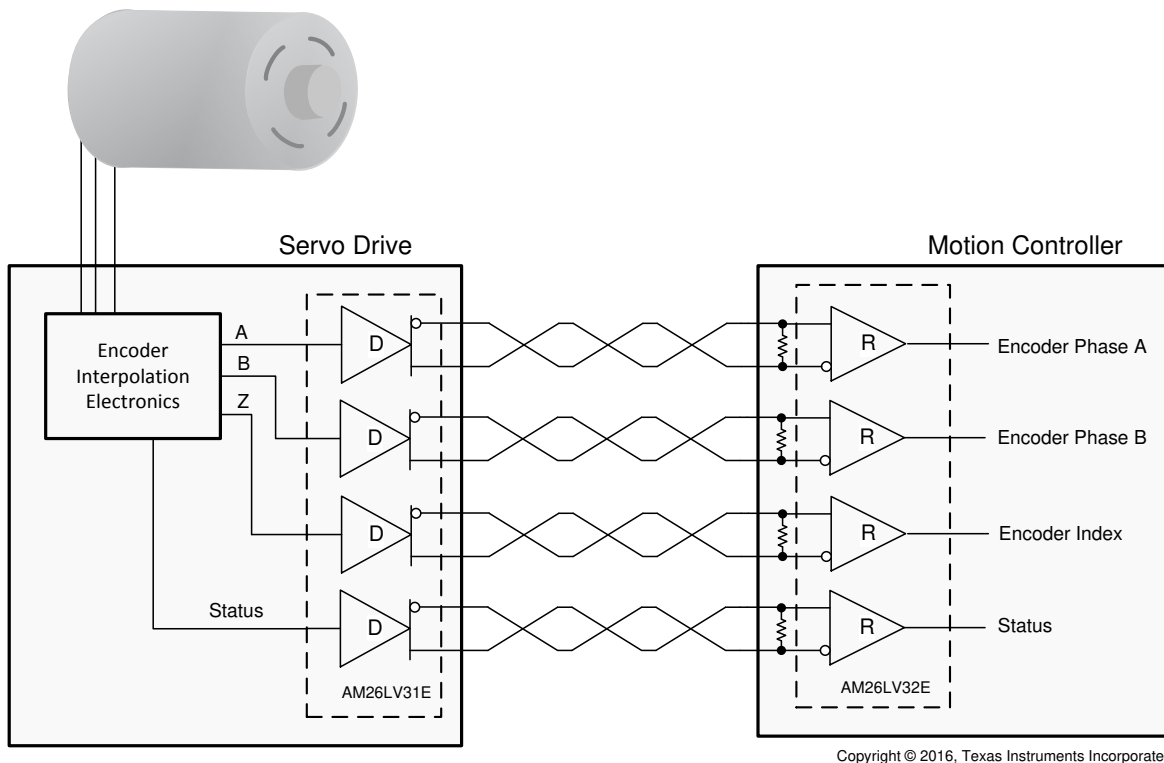


图 8-1. Encoder Application

### 8.2.1 Design Requirements

This example requires the following:

- 3.3V power source
- RS-485 bus operating at speed compatible with cable length
- Connector that ensures the correct polarity for port pins

### 8.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200mV on the A-B port, if the drive is in high impedance state (see [Fail-safe in RS-485 data buses](#), SLYT080).

### 8.2.3 Application Curve

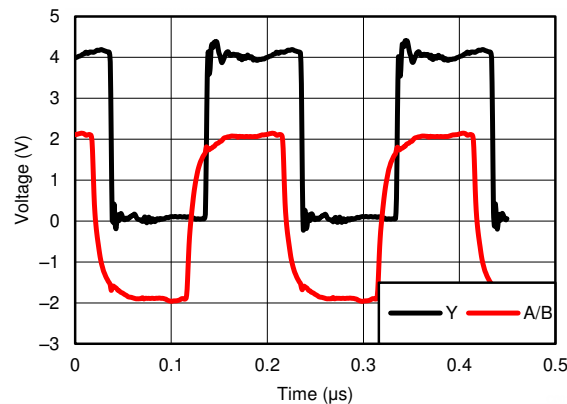


图 8-2. Differential 120  $\Omega$  Terminated Output Waveforms (Cat 5E Cable)

## 8.3 Power Supply Recommendations

Place 0.1 $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can often propagate into analog circuitry through the power supply of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1  $\mu$  F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

### 8.4.2 Layout Example

For all Y and Z outputs, make sure the traces are impedance matched to cable used.

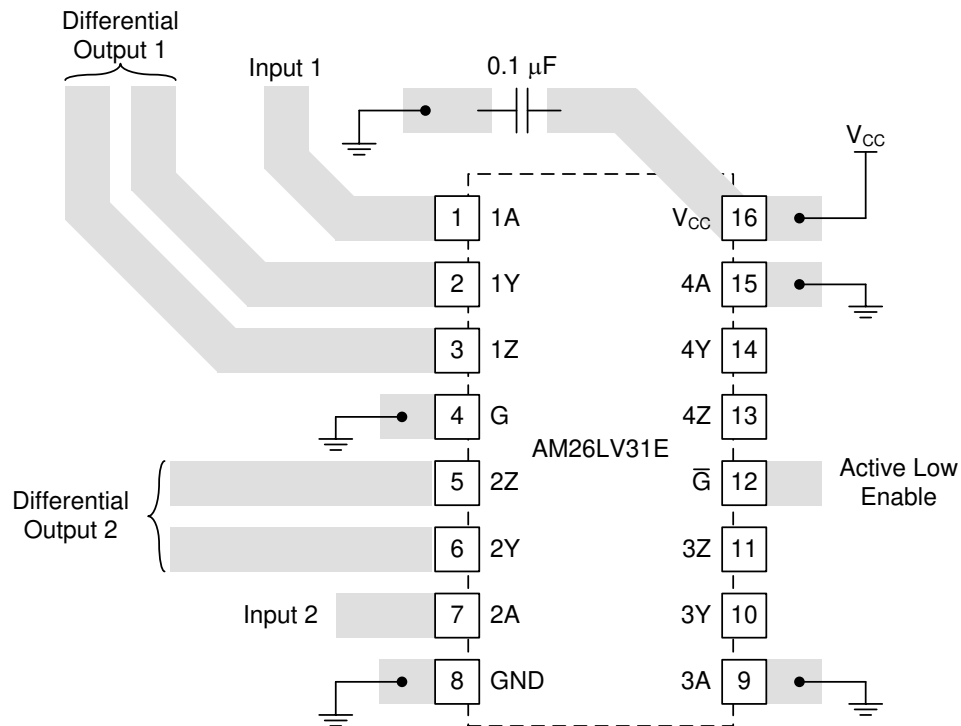


图 8-3. Layout Recommendation

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

[Failsafe in RS-485 data buses](#), SLYT080

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (September 2016) to Revision C (April 2024)	Page
• 将“器件信息”表更改为封装信息表.....	1
• Changed the <i>Thermal Information</i> table.....	5
• Changed the note in 图 6-3 .....	7

Changes from Revision A (May 2008) to Revision B (September 2016)	Page
• 添加了应用部分、热性能信息表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 删除了订购信息表，请参阅数据表末尾的机械、封装和可订购信息 .....	1
• Changed ESD PROTECTION to ESD Ratings table.....	4
• Changed R <sub>θ JA</sub> for PW package from 108°C/W: to 99.5°C/W.....	5
• Changed R <sub>θ JA</sub> for NS package from 64°C/W: to 74.5°C/W.....	5
• Changed R <sub>θ JA</sub> for RGY package from 39°C/W: to 39.3°C/W.....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV31EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI	<a href="#">Samples</a>
AM26LV31EIDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI	<a href="#">Samples</a>
AM26LV31EINSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV31EI	<a href="#">Samples</a>
AM26LV31EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	<a href="#">Samples</a>
AM26LV31EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	<a href="#">Samples</a>
AM26LV31EIRGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	<a href="#">Samples</a>
AM26LV31EIRGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF AM26LV31E :**

- Enhanced Product : [AM26LV31E-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31EINSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31EINSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV31EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV31EIRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31EIDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31EINSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26LV31EINSR	SOP	NS	16	2000	367.0	367.0	38.0
AM26LV31EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
AM26LV31EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26LV31EIRGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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