针对电流分流测量的 20MHz，二阶，隔离型三角积分调制器

查询样品: AMC1204-Q1

特性

- 符合汽车应用要求
- 符合 **AEC-Q100** 标准的下列结果
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C3B**
- 针对分流电阻器进行优化的 **±250mV** 输入电压范围
- 经认证的数字隔离：
  - 符合 **CSA**，**IEC60747-5-2** 和 **UL1577** 标准
  - 隔离电压：**4250V**
  - 工作电压：**1200V**$_{峰值}$
  - 瞬态抗扰度：**15kV/μs**
- 超长隔栅使用寿命（请参见应用报告**SLLA197**）
- 高电磁场抗扰度
  （请参见应用注释**SLLA181A**）
- 出色的 **AC** 性能
  - 信噪比 **(SNR)**：**84dB**（最小值）
  - 总谐波失真 **(THD)**：**-80dB**（最大值）
- 出色的 **DC** 精度：
  - 积分非线性 **(INL)**：**±8 LSB**（最大值）
  - 增益误差：**±2.5%**（最大值）
- 用于简化同步操作的外部时钟输入
- 可在扩展的汽车温度范围内额定运行

应用

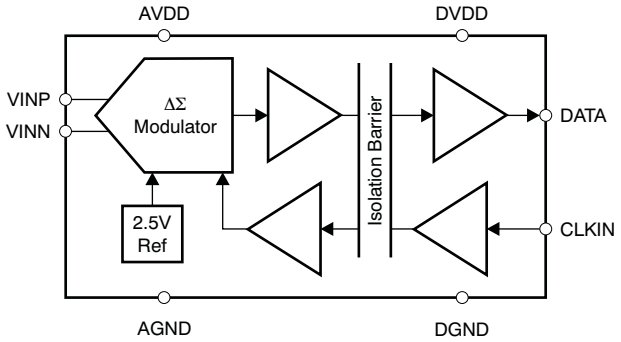
- 在下列应用中基于分流电阻器的电流感测：
  - 电机控制
  - 绿色环保能源
  - 逆变器应用
  - 不间断电源

说明

AMC1204-Q1 是一款 1 位数字输出、隔离型三角积分 (ΔΣ) 调制器，此调制器时钟频率高达 20MHz。 调制器输出的数字隔离功能由一个二氧化硅 (SiO_2) 隔栅提供，其具有极高的抗磁干扰性。 根据 UL1577，IEC60747-5-2 以及 CSA 标准或技术规范，此绝缘格栅可提供高达 4250 V$_{峰值}$的基本电气隔离。

AMC1204-Q1 可为整个隔栅上分流电阻器小信号测量提供一个单芯片解决方案。 这些类型的电阻器通常用于感测电机控制逆变器、环保能源发电系统以及其它工业应用的电流。 AMC1204-Q1 差动输入可轻易地连接至分流电阻器或其它低电平信号源。 内部基准可免除对外部组件的需要。 当与适当的外部数字滤波器配合使用时，可在 78kSPS 数据速率下获得 14 个有效位数 (ENOB)。

调制器采用 5V 模拟电源 (AVDD)，而隔离数字接口则可通过 3V，3.3V 或 5V 电源 (DVDD) 供电。 AMC1204-Q1 采用小外形尺寸 (SO)-16 (DW) 封装并且额定温度范围为 -40°C 至 125°C。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

ORDERABLE PART NUMBER(2)	MODULATOR CLOCK (MHz)	DIGITAL SUPPLY	CLOCK SOURCE	INL (LSB)	GAIN ERROR (%)	THD (dB)
AMC1204QDWRQ1	20	3 V, 3.3 V, or 5 V	External	±8	±2.5	–80

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

Over the operating ambient temperature range, unless otherwise noted.

PARAMETER		AMC1204-Q1 MIN	AMC1204-Q1 MAX	UNIT
Supply voltage, AVDD to AGND or DVDD to DGND		–0.3	6	V
Analog input voltage at VINP, VINN		AGND – 0.5	AVDD + 0.5	V
Digital input voltage at CLKIN		DGND – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins		–10	10	mA
Maximum virtual junction temperature, T_J			150	°C
Operating ambient temperature range, T_{OA}		–40	125	°C
Electrostatic discharge (ESD), all pins	Human body model (HBM) AEC-Q100 Classification Level H2	–2000	2000	V
	Charged device model (CDM) AEC-Q100 Classification Level C3B	–750	750	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		AMC1204-Q1 DW (16 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	78.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41.3	
θ_{JB}	Junction-to-board thermal resistance	50.2	
ψ_{JT}	Junction-to-top characterization parameter	11.5	
ψ_{JB}	Junction-to-board characterization parameter	41.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

REGULATORY INFORMATION

VDE/IEC	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA component acceptance notice	Recognized under 1577 component recognition program
File number: 40016131	File number: 2350550	File number: E181974

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.
The safety-limiting constraint is the operating virtual junction temperature range specified in the Absolute Maximum Ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 78.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			10	mA
T_C	Maximum case temperature				150	°C

IEC 61000-4-5 RATINGS

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Surge immunity	1.2/50 µs voltage surge and 8/20 µs current surge	±6000	V

IEC 60664-1 RATINGS

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage < 300 V_{RMS}	I-IV
	Rated mains voltage < 400 V_{RMS}	I-III
	Rated mains voltage < 600 V_{RMS}	I-III

ISOLATION CHARACTERISTICS

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IORM}	Maximum working insulation voltage per IEC		1200	V_{PEAK}
$V_{PD(t)}$	Partial discharge test voltage per IEC	t = 1s (100% production test), partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Transient overvoltage	t = 60 s (qualification test)	4250	V_{PEAK}
		t = 1 s (100% production test)	5100	V_{PEAK}
R_S	Isolation resistance	V_{IO} = 500 V at T_S	> 10^9	Ω
PD	Pollution degree		2	Degrees

ISOLATOR CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	7.9			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	7.9			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 part 1	> 400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together to create a two-terminal device, T_A < 85°C		> 10^{12}		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A < T_A max		> 10^{11}		Ω
C_{IO}	Barrier capacitance input to output	V_I = 0.8 V_{PP} at 1 MHz		1.2		pF
C_I	Input capacitance to ground	V_I = 0.8 V_{PP} at 1 MHz		3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the *Isolation Glossary* section. Techniques such as inserting grooves and/or ribs on the PCB are used to help increase these specifications.

ELECTRICAL CHARACTERISTICS

All minimum/maximum specifications at T_A = –40°C to 125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	AMC1204-Q1			UNIT
			MIN	TYP	MAX	
T_A	Specified ambient temperature range		–40		125	°C
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
INL	Integral linearity error(1)	T_A = –40°C to 85°C	–8	±2	8	LSB
		T_A = –40°C to 125°C	-16	±5	16	LSB
DNL	Differential nonlinearity(2)		–1		1	LSB
V_{OS}	Offset error(3)		–1	±0.1	1	mV
TCV_{OS}	Offset error thermal drift		–3.5	±1	3.5	µV/°C
G_{ERR}	Gain error(3)		–2.5	±0.5	2.5	%
TCG_{ERR}	Gain error thermal drift			±30		ppm/°C
PSRR	Power-supply rejection ratio			79		dB
ANALOG INPUTS						
FSR	Full-scale differential voltage input range	VINP – VINN		±320		mV
	Specified FSR		–250		250	mV
V_{CM}	Operating common-mode signal(2)		–160		AVDD	mV
C_I	Input capacitance to AGND	VINP or VINN		7		pF
C_{ID}	Differential input capacitance			3.5		pF
R_{ID}	Differential input resistance			12.5		kΩ
I_{IL}	Input leakage current	VINP – VINN = ±250 mV	–10		10	µA
		VINP – VINN = ±320 mV	–50		50	µA
CMTI	Common-mode transient immunity		15			kV/µs
CMRR	Common-mode rejection ratio	V_{IN} from 0 V to 5 V at 0 Hz		108		dB
		V_{IN} from 0 V to 5 V at 100 kHz		114		dB
EXTERNAL CLOCK						
t_{CLKIN}	Clock period		45.5	50	200	ns
f_{CLKIN}	Input clock frequency		5	20	22	MHz
$Duty_{CLKIN}$	Duty cycle	5 MHz ≤ f_{CLKIN} < 20 MHz	40	50	60	%
		20 MHz ≤ f_{CLKIN} ≤ 22 MHz	45	50	55	%
AC ACCURACY						
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz, T_A = –40°C to 105°C	70	87		dB
		f_{IN} = 1 kHz, T_A = –40°C to 125°C	69	87		dB
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, T_A = –40°C to 105°C	83	88		dB
		f_{IN} = 1 kHz, T_A = –40°C to 125°C	82	88		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz, T_A = –40°C to 105°C		–96	–70	dB
		f_{IN} = 1 kHz, T_A = –40°C to 125°C		–96	–69	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, T_A = –40°C to 105°C	72	96		dB
		f_{IN} = 1 kHz, T_A = –40°C to 125°C	71	96		dB
DIGITAL INPUTS(2)						
I_{IN}	Input current	V_{IN} = DVDD to DGND	–10		10	µA
C_{IN}	Input capacitance			5		pF
CMOS logic family			CMOS with Schmitt-trigger			
V_{IH}	High-level input voltage	DVDD = 4.5 V to 5.5 V	0.7 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage	DVDD = 4.5 V to 5.5 V	–0.3		0.3 DVDD	V

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified 500 mV input range.
(2) Ensured by design.
(3) Maximum values, including temperature drift, are ensured over the full specified temperature range.

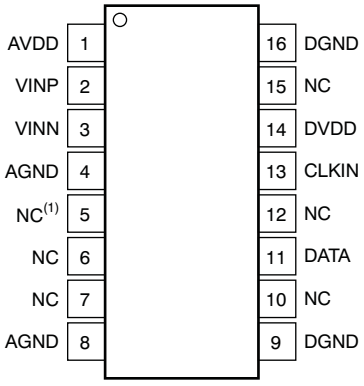
ELECTRICAL CHARACTERISTICS (continued)

All minimum/maximum specifications at T_A = –40°C to 125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	AMC1204-Q1			UNIT
			MIN	TYP	MAX	
LVCMOS logic family				LVCMOS		
V_{IH}	High-level input voltage	DVDD = 2.7 V to 3.6 V	2		DVDD + 0.3	V
V_{IL}	Low-level input voltage	DVDD = 2.7 V to 3.6 V	–0.3		0.8	V
DIGITAL OUTPUTS(2)						
C_{OUT}	Output capacitance			5		V
C_{LOAD}	Load capacitance				30	V
CMOS logic family				CMOS		
V_{OH}	High-level output voltage	DVDD = 4.5 V, I_{OH} = –100 µA	4.4			V
V_{OL}	Low-level output voltage	DVDD = 4.5 V, I_{OL} = 100 µA			0.5	V
LVCMOS logic family				LVCMOS		
V_{OH}	High-level output voltage	I_{OH} = 20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA, 2.7 V ≤ DVDD ≤ 3.6 V	DVDD – 0.4			V
		I_{OH} = –4 mA, 4.5 V ≤ DVDD ≤ 5.5 V	DVDD – 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	V
POWER SUPPLY						
AVDD	High-side supply voltage		4.5	5	5.5	V
DVDD	Controller-side supply voltage		2.7	3.3	5.5	V
I_{AVDD}	High-side supply current	4.5 V ≤ AVDD ≤ 5.5 V		11	16	mA
I_{DVDD}	Controller-side supply current	2.7 V ≤ DVDD ≤ 3.6 V		2	4	mA
		4.5 V ≤ DVDD ≤ 5.5 V		2.8	5	mA
P_D	Power dissipation	AVDD = 5.5 V, DVDD = 3.6 V		61.6	102.4	mW

PIN CONFIGURATION

DW PACKAGE
SO-16
(TOP VIEW)



(1) NC = no internal connection.

PIN DESCRIPTIONS

PIN NAME	PIN NO.	FUNCTION	DESCRIPTION
AVDD	1	Power	High-side power supply
VINP	2	Analog input	Noninverting analog input
VINN	3	Analog input	Inverting analog input
AGND	4, 8 (1)	Power	High-side ground
DGND	9, 16	Power	Controller-side ground
DATA	11	Digital output	Modulator data output
CLKIN	13	Digital input	Modulator clock input
DVDD	14	Power	Controller-side power supply
NC	5, 6, 7, 10, 12, 15	—	No internal connection; can be tied to any potential or left unconnected

(1) Both pins are connected internally via a low-impedance path; thus, only one of the pins must be tied to the ground plane.

TIMING INFORMATION

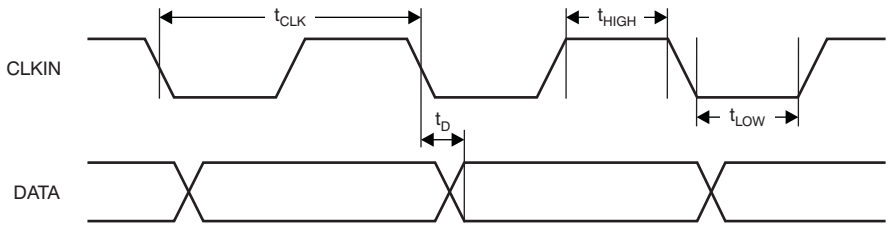


Figure 1. Modulator Output Timing

TIMING CHARACTERISTICS FOR Figure 1

Over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLKIN clock period	45.5	50	200	ns
t_{HIGH}	CLKIN clock high time	20	25	120	ns
t_{LOW}	CLKIN clock low time	20	25	120	ns
t_D	Delayed falling edge of CLKIN to DATA valid	2		15	ns

TYPICAL CHARACTERISTICS

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

INTEGRAL NONLINEARITY vs INPUT SIGNAL AMPLITUDE

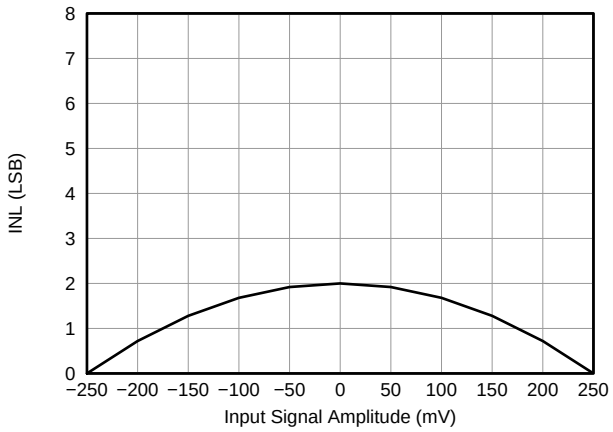


Figure 2.

INTEGRAL NONLINEARITY vs TEMPERATURE

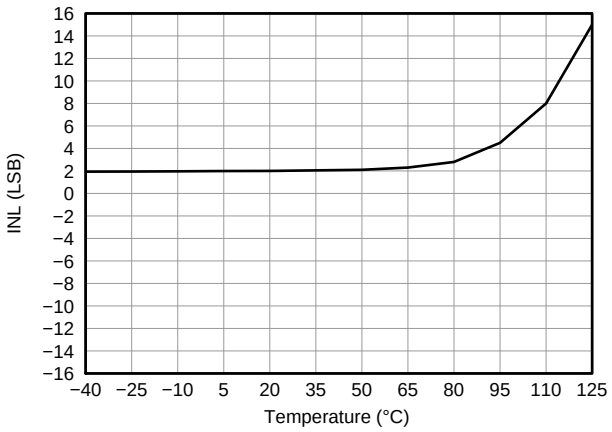


Figure 3.

OFFSET ERROR vs ANALOG SUPPLY VOLTAGE

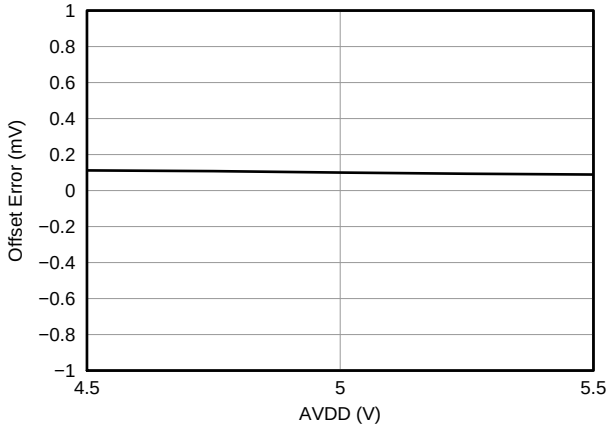


Figure 4.

OFFSET ERROR vs TEMPERATURE

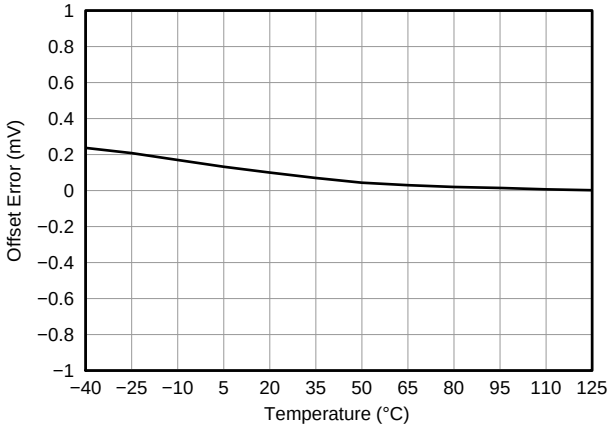


Figure 5.

OFFSET ERROR vs CLOCK FREQUENCY

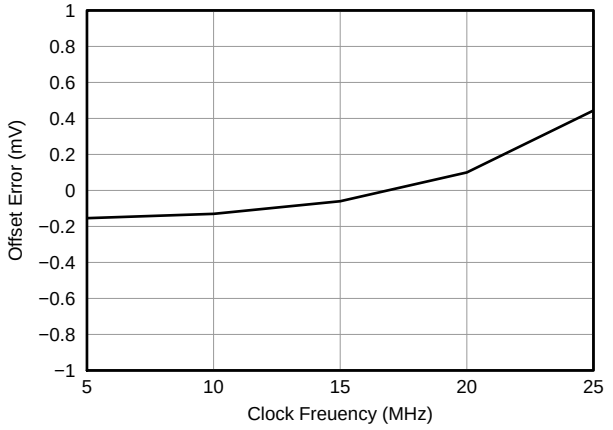


Figure 6.

OFFSET ERROR vs CLOCK DUTY CYCLE

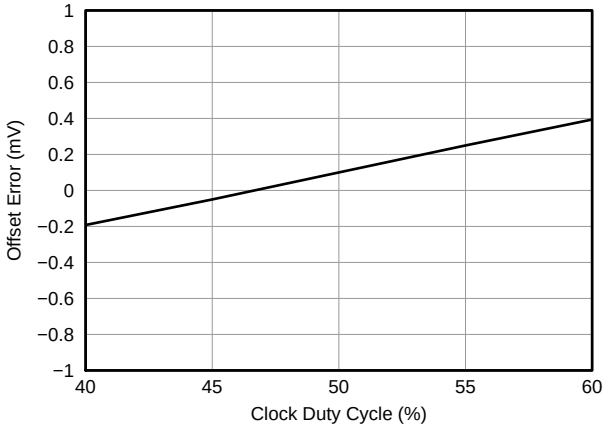


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

GAIN ERROR vs ANALOG SUPPLY VOLTAGE

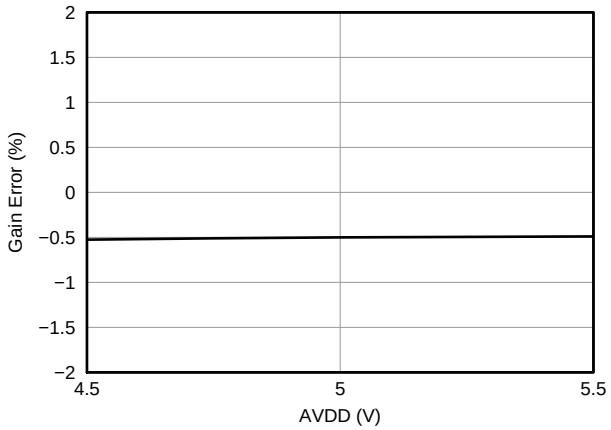


Figure 8.

GAIN ERROR vs TEMPERATURE

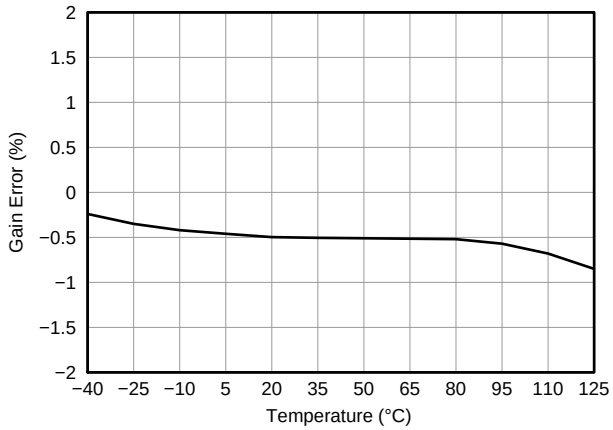


Figure 9.

GAIN ERROR vs CLOCK FREQUENCY

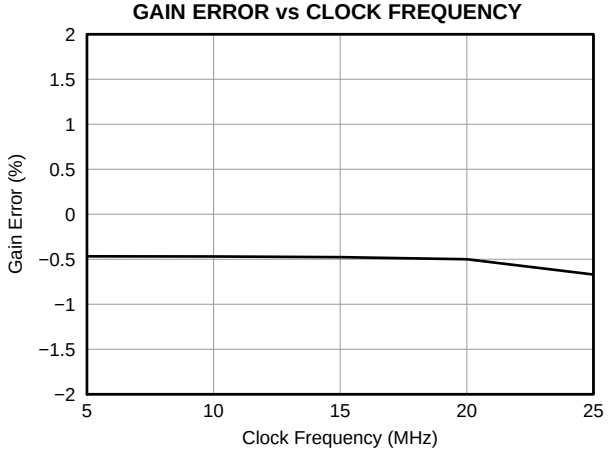


Figure 10.

GAIN ERROR vs CLOCK DUTY CYCLE

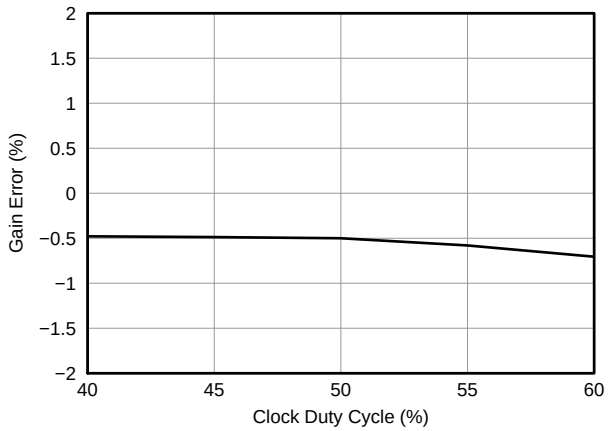


Figure 11.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

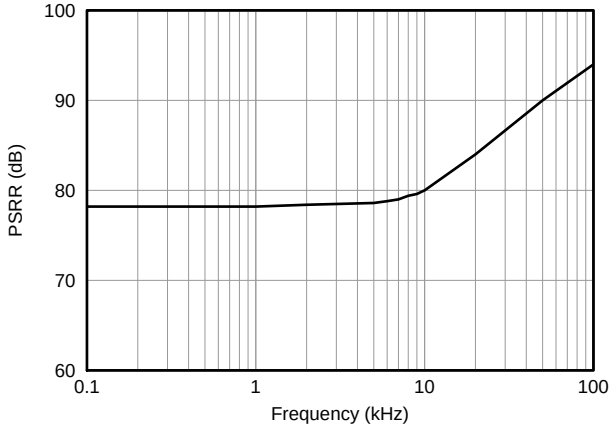


Figure 12.

COMMON-MODE REJECTION RATIO vs INPUT SIGNAL FREQUENCY

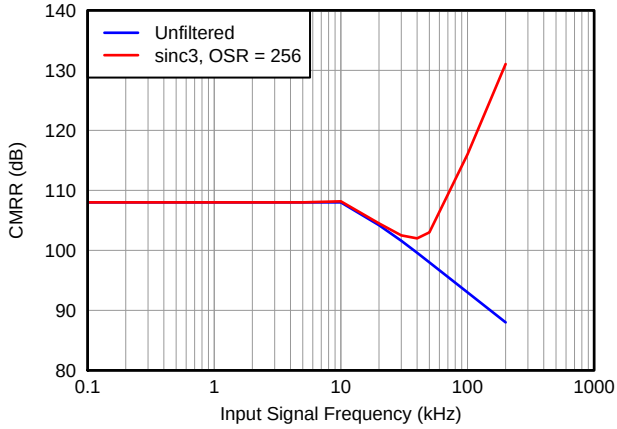


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

SINAD AND SNR vs ANALOG SUPPLY VOLTAGE

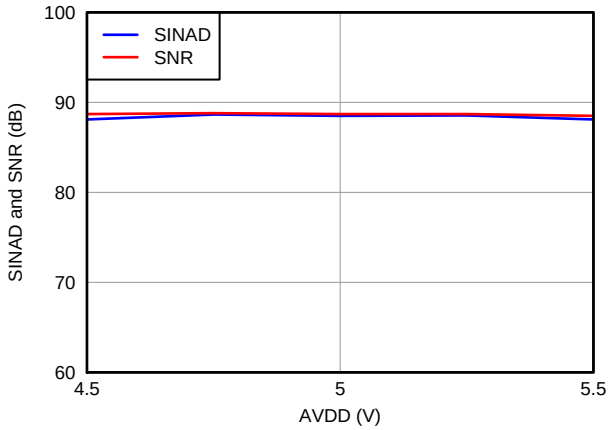


Figure 14.

SINAD AND SNR vs TEMPERATURE

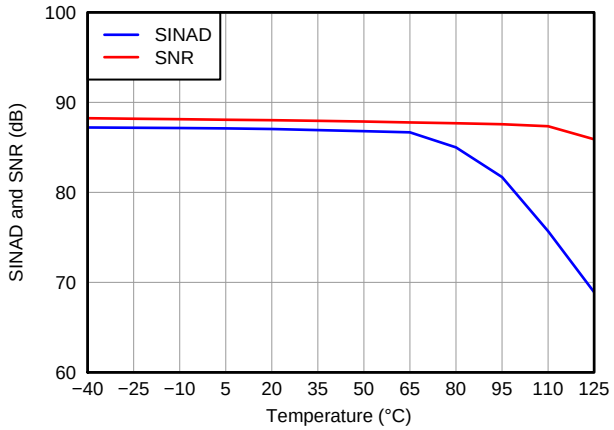


Figure 15.

SINAD AND SNR vs INPUT SIGNAL FREQUENCY

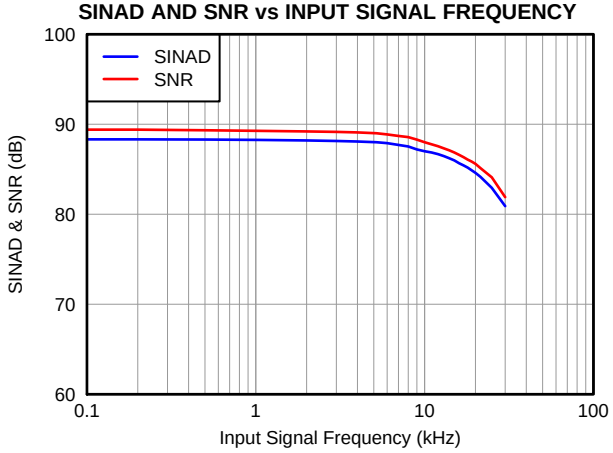


Figure 16.

SINAD AND SNR vs INPUT SIGNAL AMPLITUDE

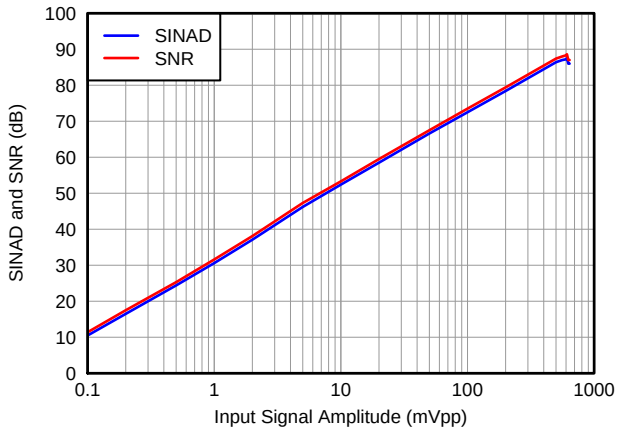


Figure 17.

SINAD AND SNR vs CLOCK FREQUENCY

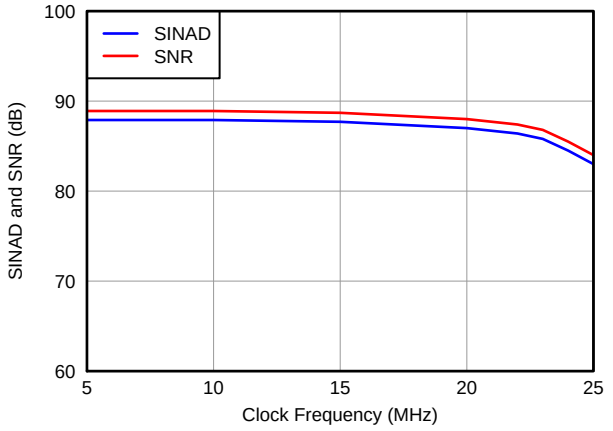


Figure 18.

SINAD AND SNR vs CLOCK DUTY CYCLE

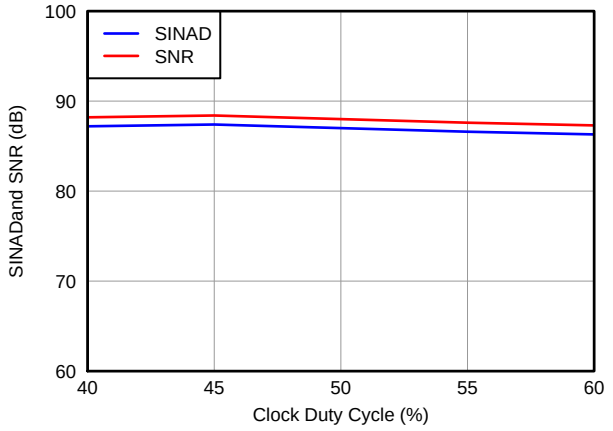


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs ANALOG SUPPLY VOLTAGE

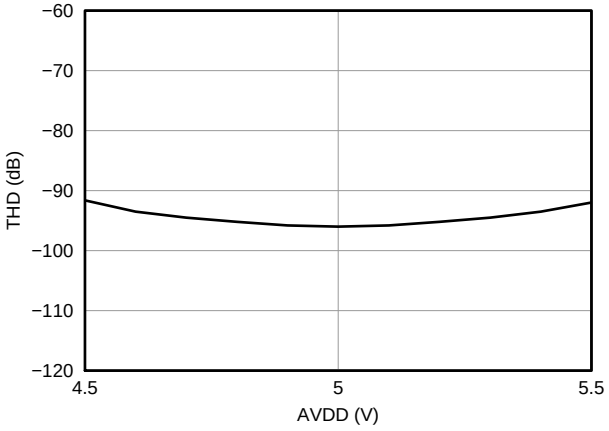


Figure 20.

TOTAL HARMONIC DISTORTION vs TEMPERATURE

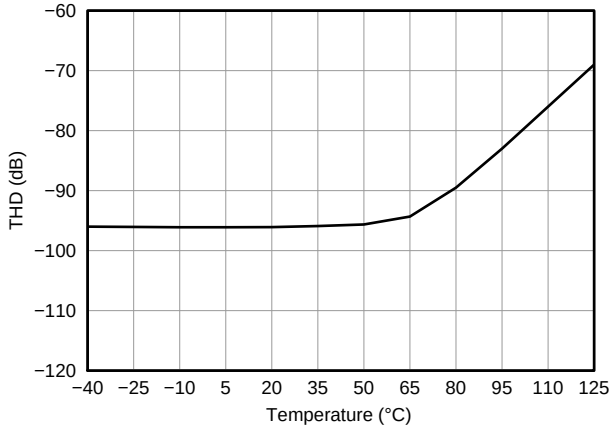


Figure 21.

TOTAL HARMONIC DISTORTION vs INPUT SIGNAL FREQUENCY

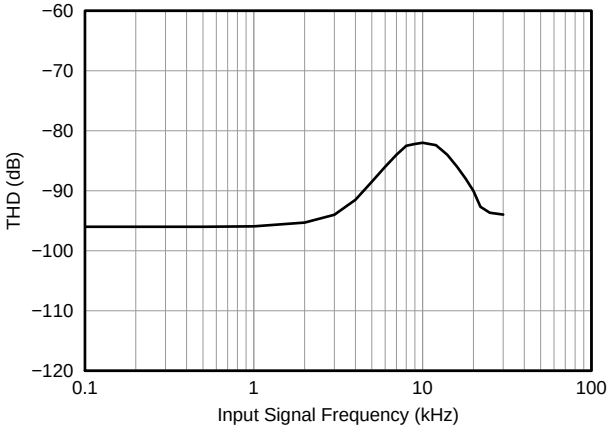


Figure 22.

TOTAL HARMONIC DISTORTION vs INPUT SIGNAL AMPLITUDE

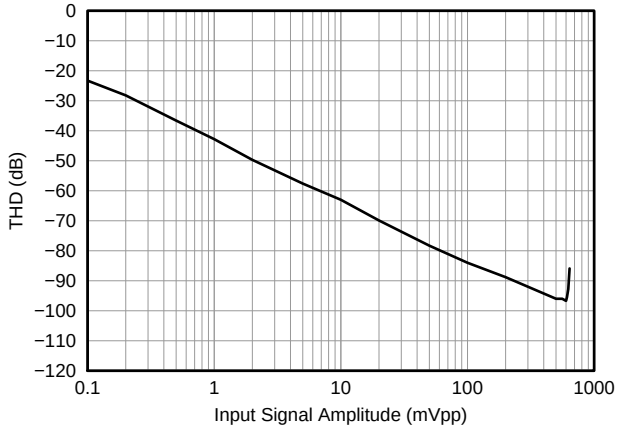


Figure 23.

TOTAL HARMONIC DISTORTION vs CLOCK FREQUENCY

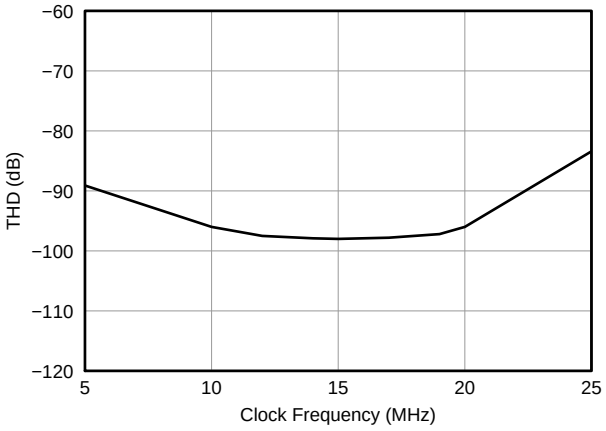


Figure 24.

TOTAL HARMONIC DISTORTION vs CLOCK DUTY CYCLE

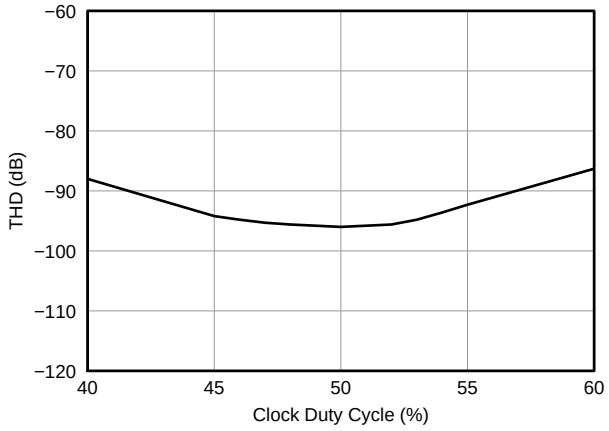


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE vs ANALOG SUPPLY VOLTAGE

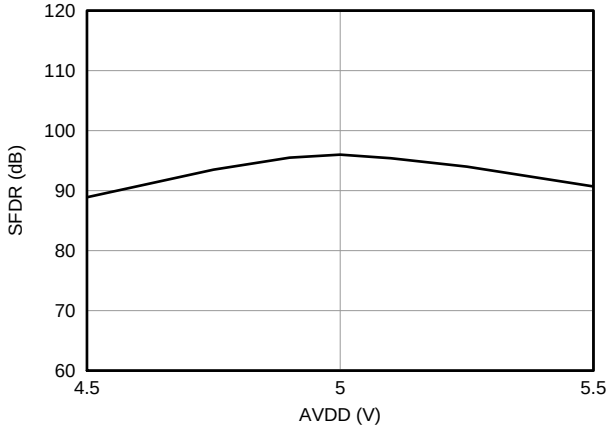


Figure 26.

SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

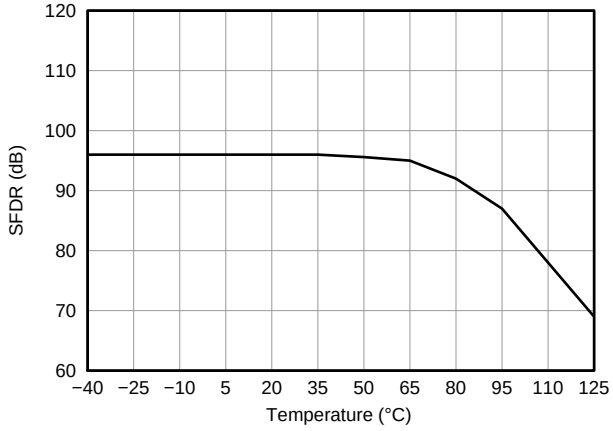


Figure 27.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT SUGNAL FREQUENCY

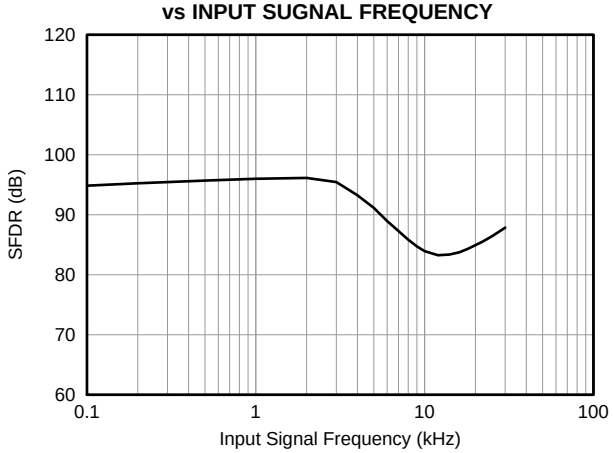


Figure 28.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL AMPLITUDE

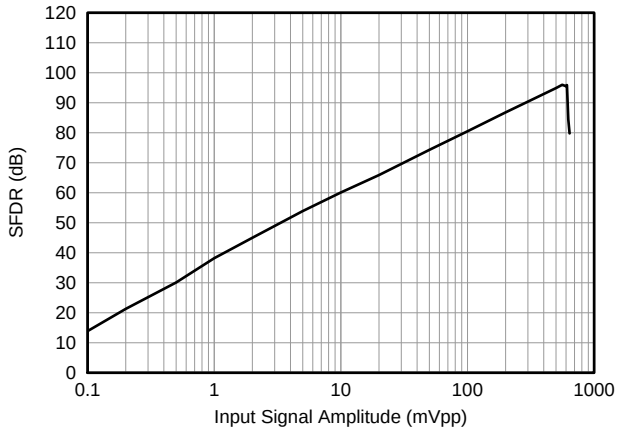


Figure 29.

SPURIOUS-FREE DYNAMIC RANGE vs CLOCK FREQUENCY

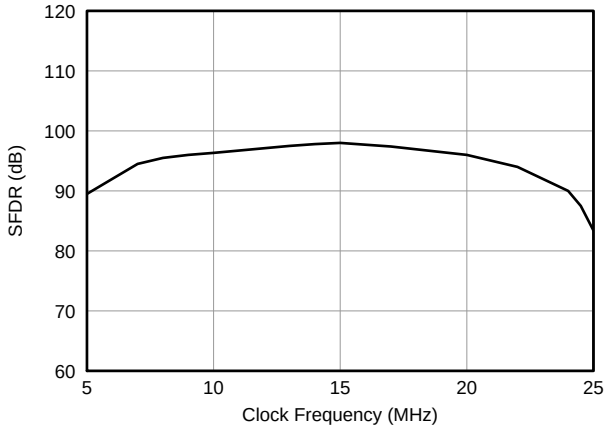


Figure 30.

SPURIOUS-FREE DYNAMIC RANGE vs CLOCK DUTY CYCLE

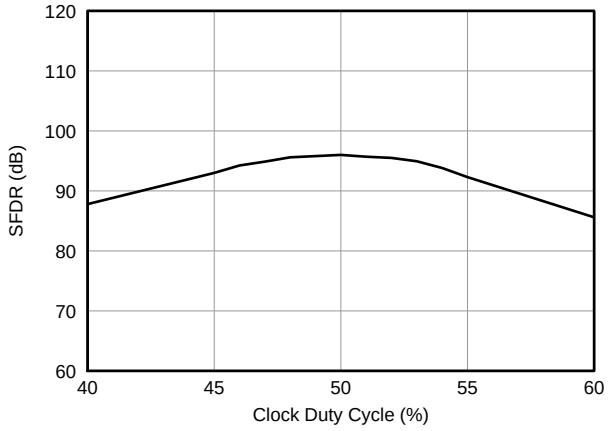


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

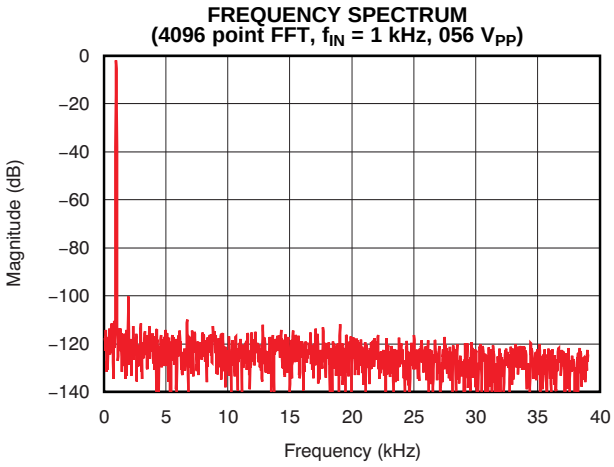


Figure 32.

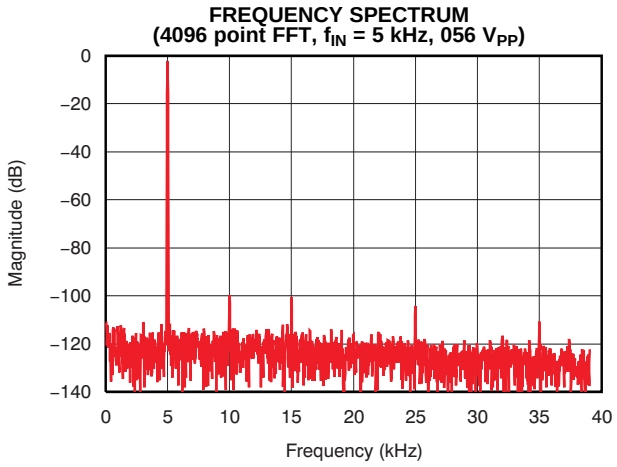


Figure 33.

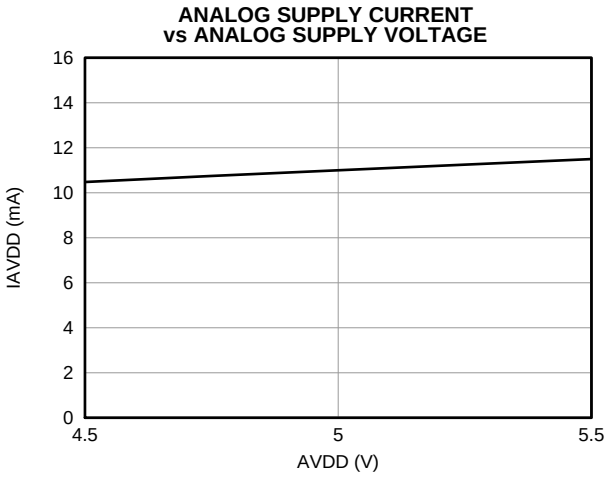


Figure 34.

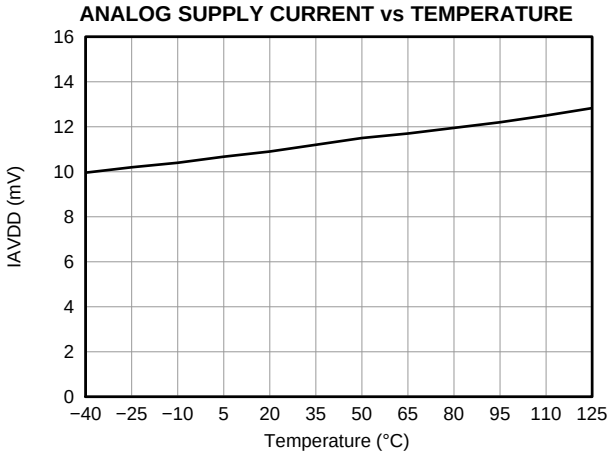


Figure 35.

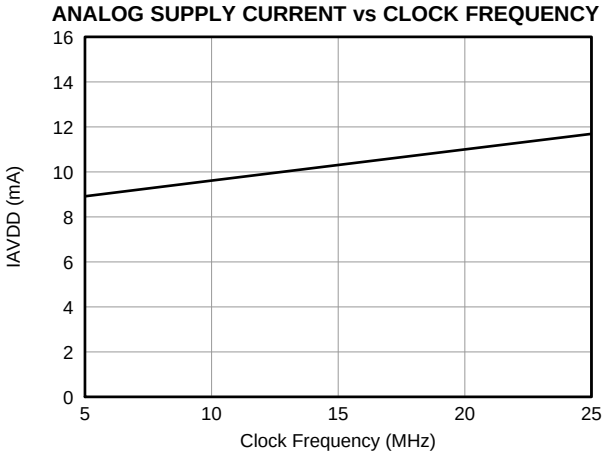


Figure 36.

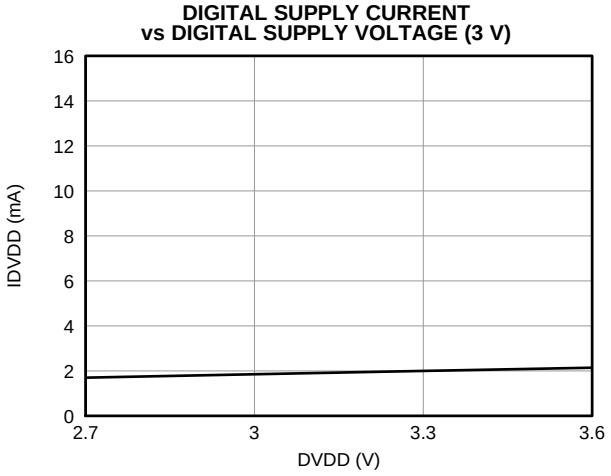


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

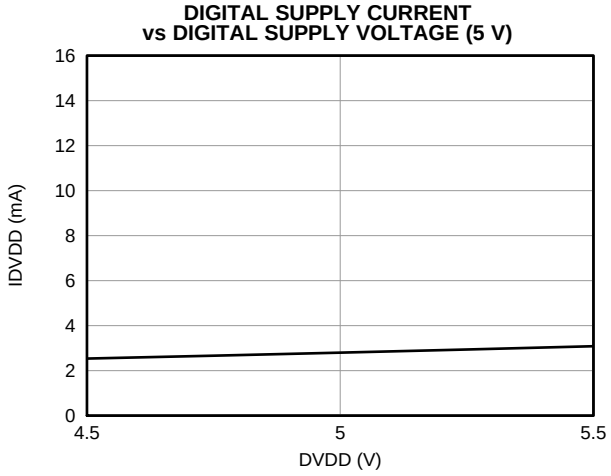


Figure 38.

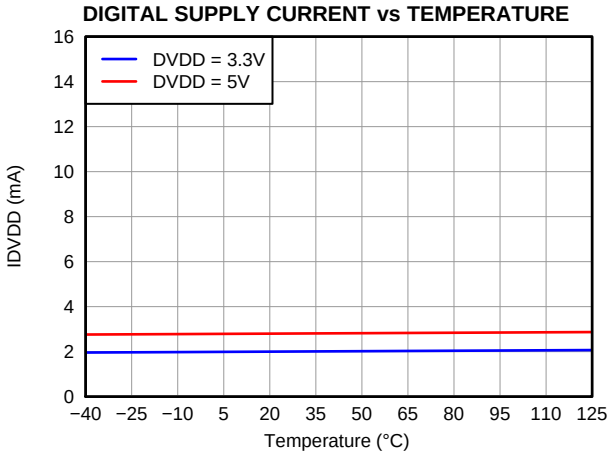


Figure 39.

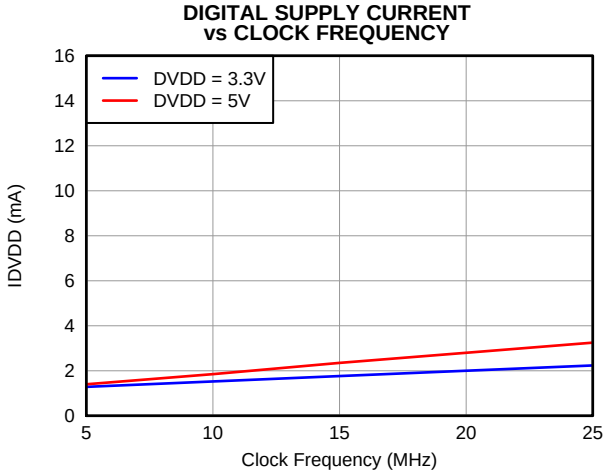


Figure 40.

GENERAL DESCRIPTION

The AMC1204-Q1 is a single-channel, second-order, delta-sigma (ΔΣ) modulators designed for medium- to high-resolution analog-to-digital conversions. The isolated output of the converter (DATA) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

Figure 41 shows a detailed block diagram of the AMC1204-Q1. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the application report *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181A, available for download at www.ti.com). The external clock input simplifies the synchronization of multiple current sense channels on system level. The extended frequency range of up to 20 MHz supports higher performance levels compared to the other solutions available on the market.

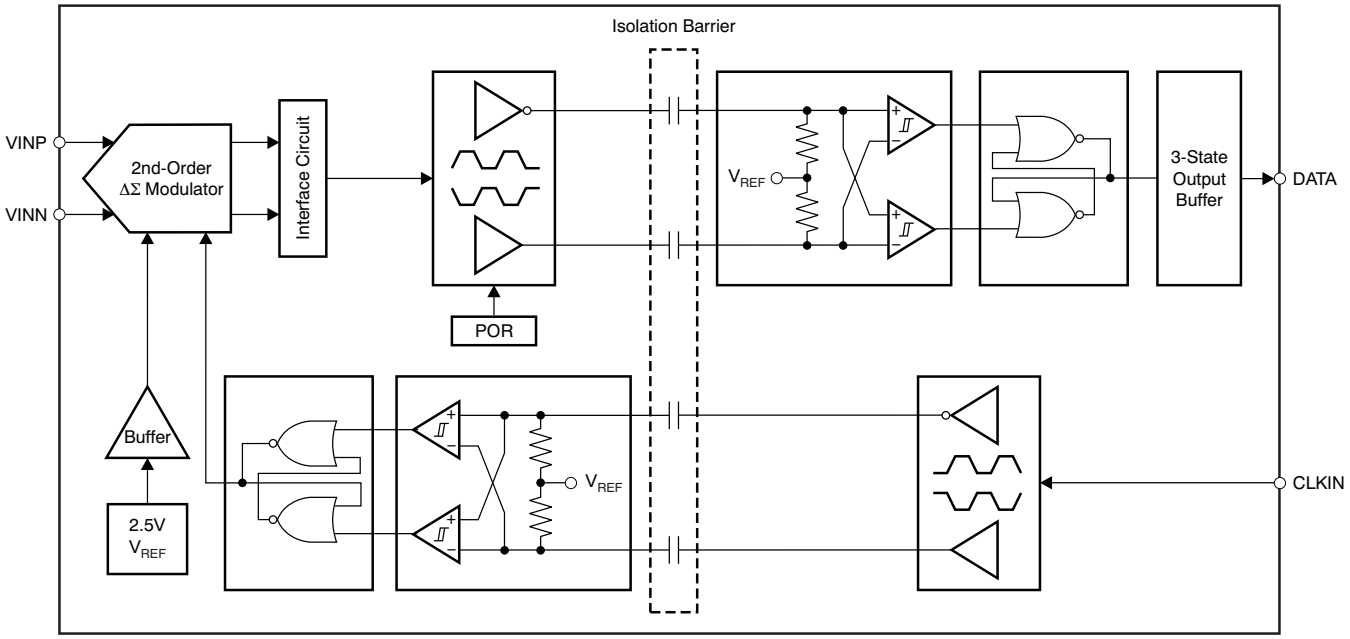


Figure 41. Detailed Block Diagram

THEORY OF OPERATION

The differential analog input of the AMC1204-Q1 is implemented with a switched-capacitor circuit. This switched-capacitor circuit implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The externally-provided clock source at the CLKIN pin is used by the capacitor circuit and the modulator and should be in the range of 5 MHz to 22 MHz. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, accurately representing the analog input voltage over time, appears at the output of the converter at the DATA pin.

ANALOG INPUT

The AMC1204-Q1 measures the differential input signal V_{IN} = (VINP – VINN) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged. Figure 42 shows the simplified schematic of the ADC input circuitry; the right side of Figure 42 illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit.

In Figure 42, the S_1 switches close during the input sampling phase. With the S_1 switches closed, C_{DIFF} charges to the voltage difference across VINP and VINN. For the discharge phase, both S_1 switches open first and then both S_2 switches close. C_{DIFF} discharges approximately to AGND + 0.8 V during this phase. This two-phase sample/discharge cycle repeats with a period of $t_{CLKIN} = 1/f_{CLKIN}$. f_{CLKIN} is the operating frequency of the modulator. The capacitors C_{IP} and C_{IN} are of parasitic nature and caused by bonding wires and the internal ESD protection structure.

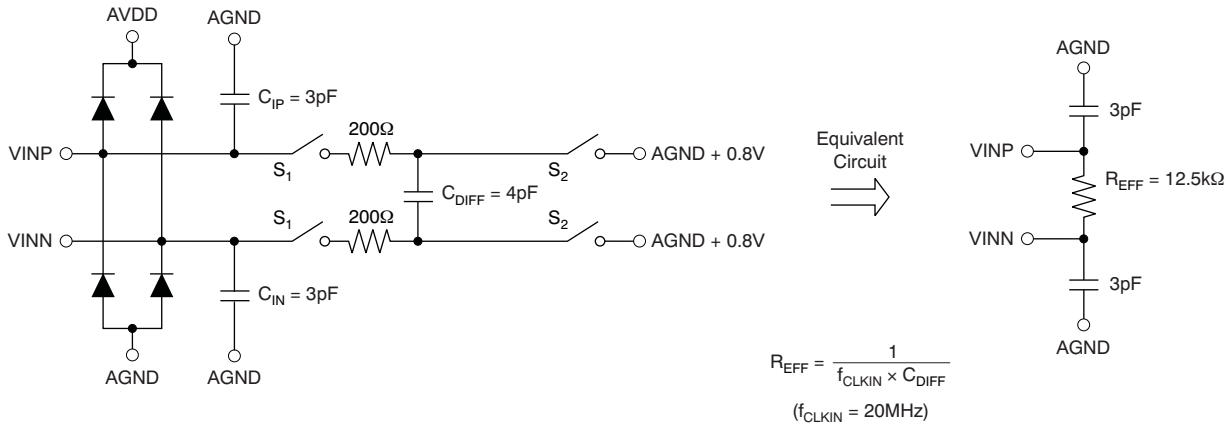


Figure 42. Equivalent Analog Input Circuit

The input impedance becomes a consideration in designs with high input signal source impedance. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect, however, depends on the desired system performance. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (105 dB), and excellent power-supply rejection.

There are two restrictions on the analog input signals VINP and VINN. First, if the input voltage exceeds the range AGND – 0.5 V to AVDD + 0.3 V, the input current must be limited to 10 mA because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV.

MODULATOR

The modulator topology of the AMC1204-Q1 is fundamentally a second-order, switched-capacitor, ΔΣ modulator, such as the one conceptualized in Figure 43. The analog input voltage ($X_{(t)}$) and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage (X_2) at the input of the first integrator or modulator stage. The output of the first integrator is further differentiated with the DAC output; the resulting voltage (X_3) feeds the input of the second integrator stage. When the value of the integrated signal (X_4) at the output of the second stage equals the comparator reference voltage, the output of the comparator switches from high to low, or vice versa, depending on its previous state. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage (X_6), causing the integrators to progress in the opposite direction, while forcing the value of the integrator output to track the average of the input.

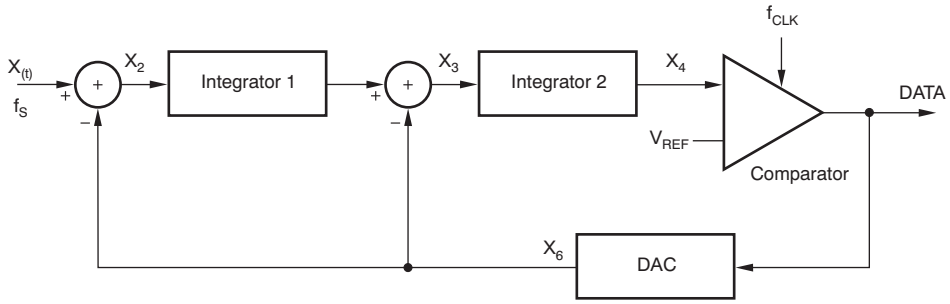


Figure 43. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 44; therefore, a low-pass digital filter should be used at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (μC), or field programmable gate array (FPGA) can be used to implement the filter. Another option is to use a suitable application-specific device such as the AMC1210, a four-channel digital sinc-filter.

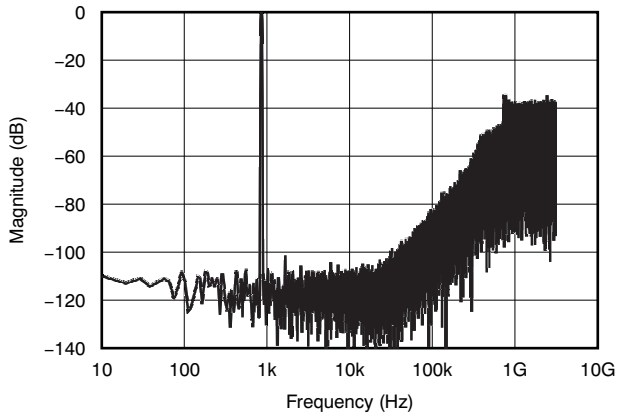


Figure 44. Quantization Noise Shaping

DIGITAL OUTPUT

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of 250 mV produces a stream of ones and zeros that are high 78.1% of the time. A differential input of –250 mV produces a stream of ones and zeros that are high 21.9% of the time. This is also the specified linear input range of the modulator with the performance as specified in this data sheet. The range between 250 mV and 320 mV (absolute values) is the non-linear range of the modulator. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320 mV or with a stream of only ones with an input greater than or equal to 320 mV. The input voltage versus the output modulator signal is shown in Figure 45.

The system clock of the AMC1204-Q1 is typically 20 MHz and is provided externally at the CLKIN pin. The data are synchronously provided at 20 MHz at the DATA output pin. The data are changing at the falling edge of CLKIN; for more details see the Timing Information section.

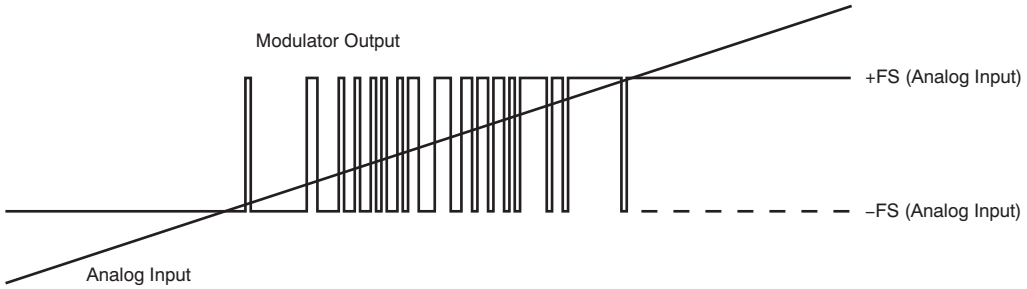


Figure 45. Analog Input versus AMC1204-Q1 Modulator Output

FILTER USAGE

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 1:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (1)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates). For an oversampling rate (OSR) in the range of 16 to 256, this filter is a good choice. All the characterization in this document is also done with a sinc^3 filter with OSR = 256 and an output word width of 16 bits.

In a sinc^3 filter response (shown in Figure 46 and Figure 47), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3 dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type with different frequency response. Performance can be improved, for example, by using a cascaded filter structure. The first decimation stage could be built of a sinc^3 filter with a low OSR and the second stage using a high-order filter.

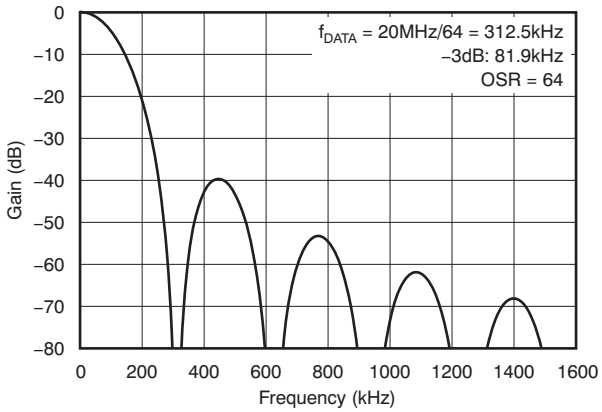


Figure 46. Frequency Response of the Sinc^3 Filter

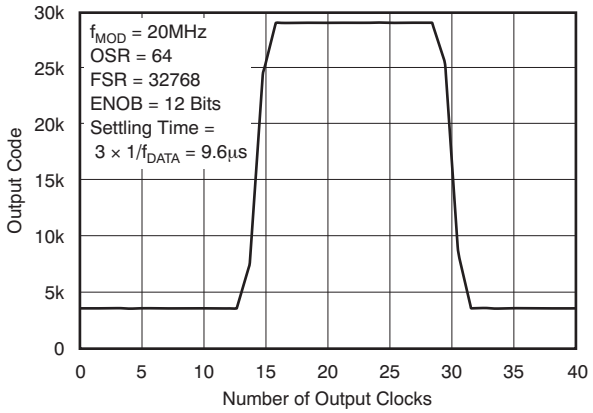


Figure 47. Pole Response of the Sinc^3 Filter

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 48 illustrates the ENOB of the AMC1204-Q1 with different oversampling ratios. In this data sheet, this number is calculated from SNR using Equation 2:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (2)$$

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter depends on its order; that is, a sinc^3 filter requires three data clocks for full settling (with $f_{DATA} = f_{CLK}/OSR$). Therefore, for overcurrent protection, filter types other than sinc^3 might be a better choice; an alternative is the sinc^2 filter. Figure 49 compares the settling times of different filter orders with sincfast being a modified sinc^2 filter with behavior as shown in Equation 3.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 (1 + z^{-2OSR}) \quad (3)$$

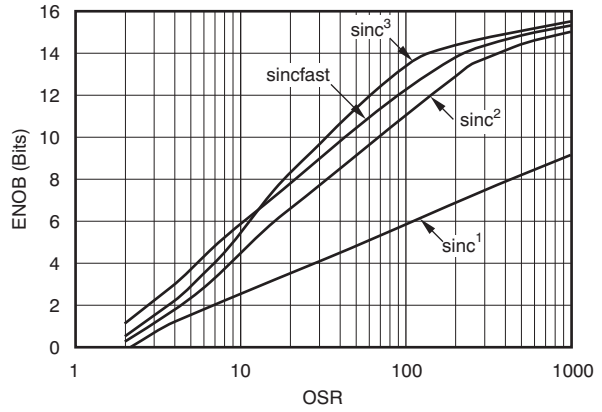


Figure 48. Measured Effective Number of Bits versus Oversampling Ratio

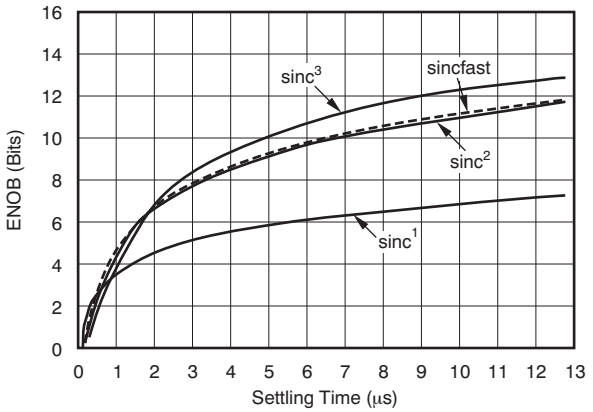


Figure 49. Measured Effective Number of Bits versus Settling Time

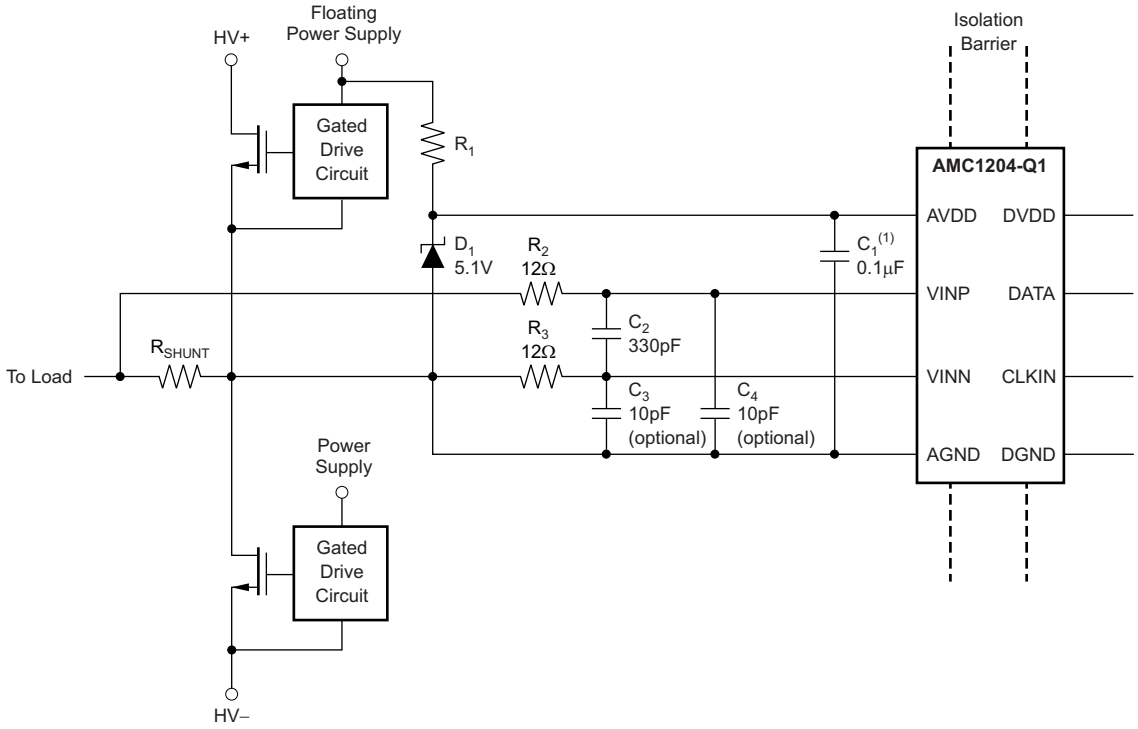
An example code for an implementation of a sinc^3 filter in an FPGA follows. For more information, see the application note *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications (SBAA094)*, available for download at www.ti.com.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5 : out std_logic_vector(23 downto 0));
end FLT;

architecture RTL of FLT is
  signal DN0, DN1, DN3, DN5 : std_logic_vector(23 downto 0);
  signal CN1, CN2, CN3, CN4 : std_logic_vector(23 downto 0);
  signal DELTA1 : std_logic_vector(23 downto 0);
begin

process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;

process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;

process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;

CN3 <= DN0 - DN1;
CN4 <= CN3 - DN3;
CN5 <= CN4 - DN5;

end RTL;
```

APPLICATION INFORMATION

A typical operation of the AMC1204-Q1 in a motor control application is shown in Figure 50. Measurement of the motor phase current is done via the shunt resistor R_{SHUNT} (in this case, a two-terminal shunt). For better performance, the differential signal is filtered using RC filters (components R_2, R_3, and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors—mismatch in values of these capacitors leads to a common-mode error at the input of the modulator.

The high-side power supply (AVDD) for the AMC1204-Q1 is derived from the power supply of the upper gate driver. For lowest cost, a zener diode can be used to limit the voltage to 5 V ±10%. A decoupling capacitor of 0.1 µF is recommended for filtering this power-supply path. This capacitor (C_1 in Figure 50) should be placed as close as possible to the AVDD pin for best performance. If better filtering is required, an additional 1 µF to 10 µF capacitor can be used. The floating ground reference AGND is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the AMC1204-Q1. If a four-terminal shunt is used, the inputs of AMC1204-Q1 are connected to the inner leads, while AGND is connected to one of the outer leads of the shunt. Both digital signals, CLKIN and DATA, can be directly connected to a digital filter (for example, the AMC1210); see Figure 51.



(1) Place C_1 close to the AMC1204-Q1.

Figure 50. Typical Application Diagram

Figure 51 shows an example of two AMC1204-Q1 devices and one ADS1209 (a dual-channel, 10 MHz, non-isolated modulator) connected to an AMC1210, building the entire analog front-end of a resolver-based motor control application.

For detailed information on the ADS1209 and AMC1210, visit the respective device product folders at www.ti.com.

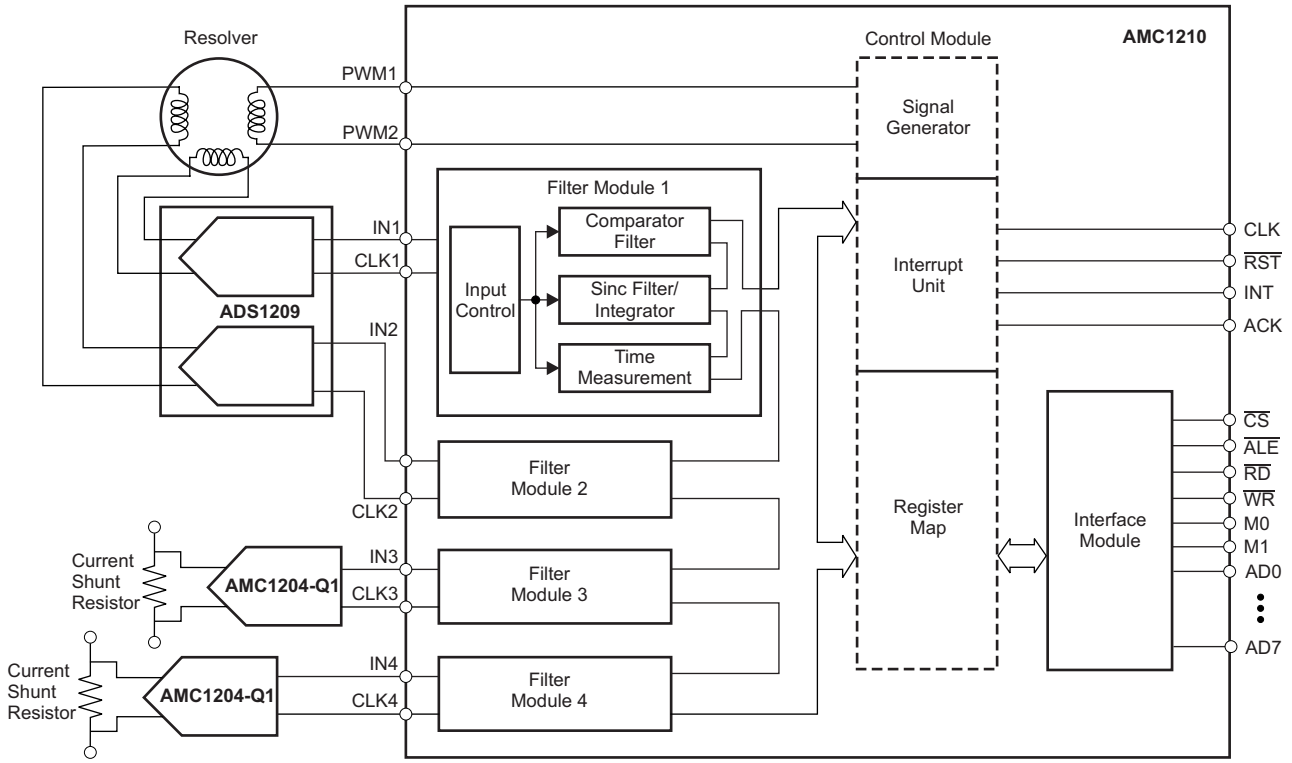


Figure 51. Example of a Resolver-Based Motor Control Analog Front-End

A layout recommendation showing the critical placement of the decoupling capacitor on the high-side and placement of the other components required by the AMC1204-Q1 is presented in Figure 52.

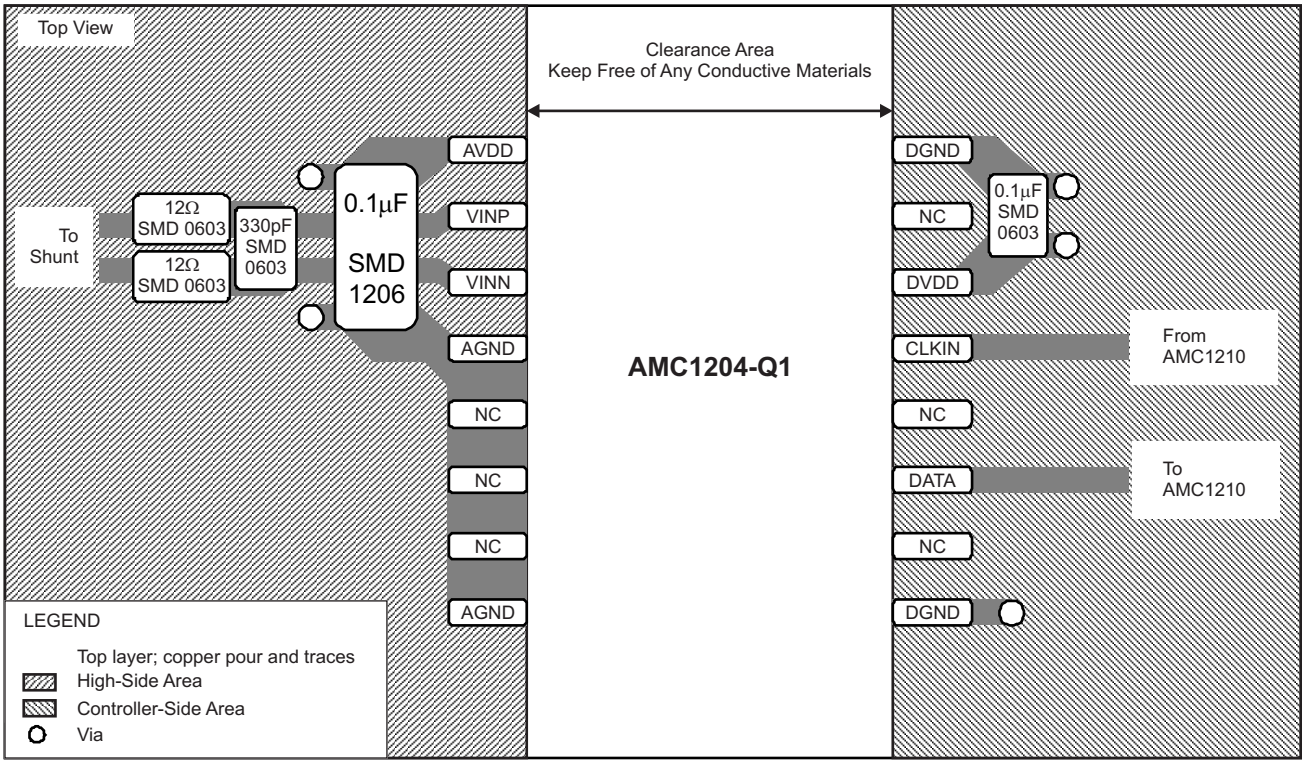
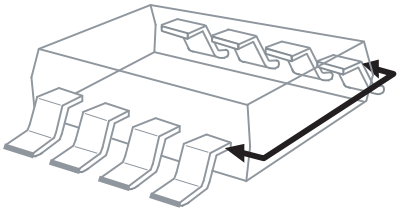


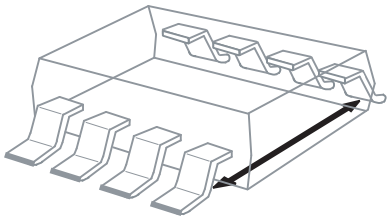
Figure 52. Recommended Layout

ISOLATION GLOSSARY

Creepage Distance: The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance: The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to-Output Barrier Capacitance: The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to-Output Barrier Resistance: The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit: An internal circuit directly connected to an external supply mains or other equivalent source that supplies the primary circuit electric power.

Secondary Circuit: A circuit with no direct connection to primary power that derives its power from a separate isolated source.

Comparative Tracking Index (CTI): CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface. The higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as tracking.

Insulation:

Operational insulation—Insulation needed for the correct operation of the equipment.

Basic insulation—Insulation to provide basic protection against electric shock.

Supplementary insulation—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation—Insulation comprising both basic and supplementary insulation.

Reinforced insulation—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence on device performance.

Pollution Degree 2—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3—Conductive pollution, or dry nonconductive pollution that becomes conductive because of condensation, occurs. Condensation is to be expected.

Pollution Degree 4—Continuous conductivity occurs as a result of conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category—This section is directed at insulation coordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

1. Signal Level: Special equipment or parts of equipment.
2. Local Level: Portable equipment, etc.
3. Distribution Level: Fixed installation.
4. Primary Supply Level: Overhead lines, cable systems.

Each category should be subject to smaller transients than the previous category.

REVISION HISTORY

Changes from Revision A (October, 2012) to Revision B **Page**

- 将 $V_{峰值}$从 4000 改为 4250。 1
- 将 $V_{峰值}$从 4000 改为 4250。 1
- Changed $V_{IOTM}$with t = 60 s (qualification test) test condition from 4000 to 4250. 4
- Changed V_{IOTM} with t = 1 s (100% production test) test condition from 4000 to 5100. 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1204QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1204Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

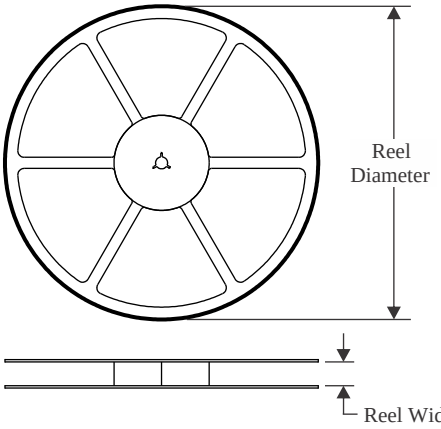
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

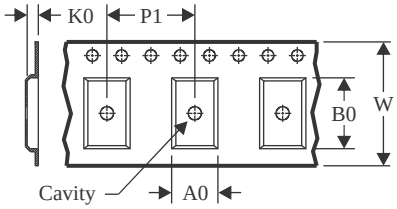
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

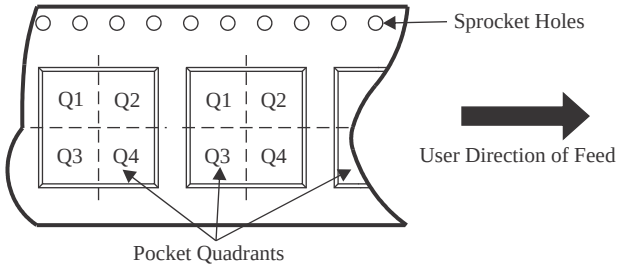


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

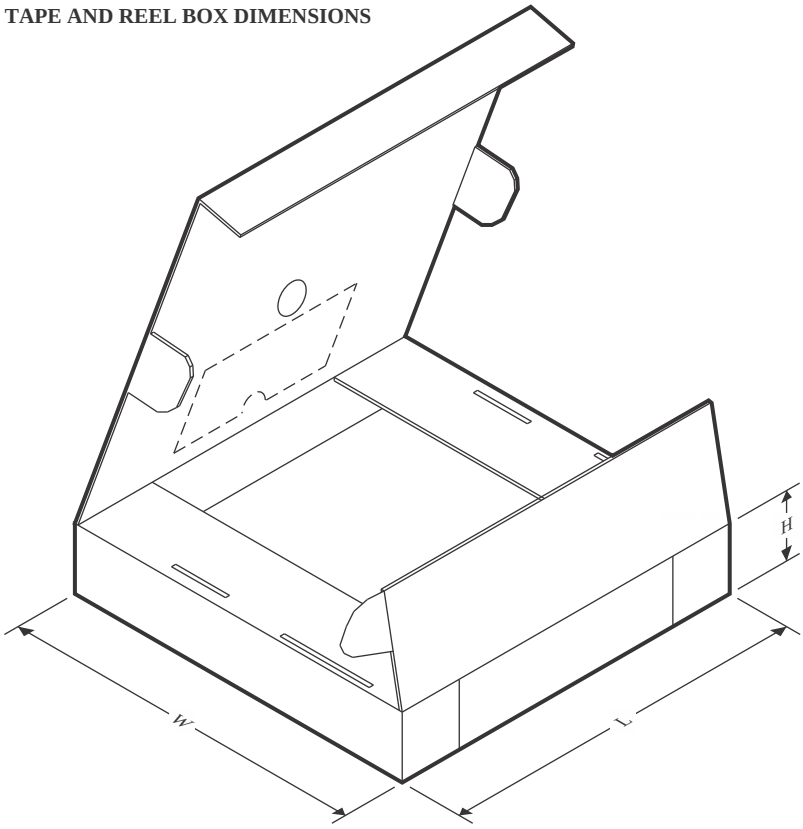
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1204QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1204QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

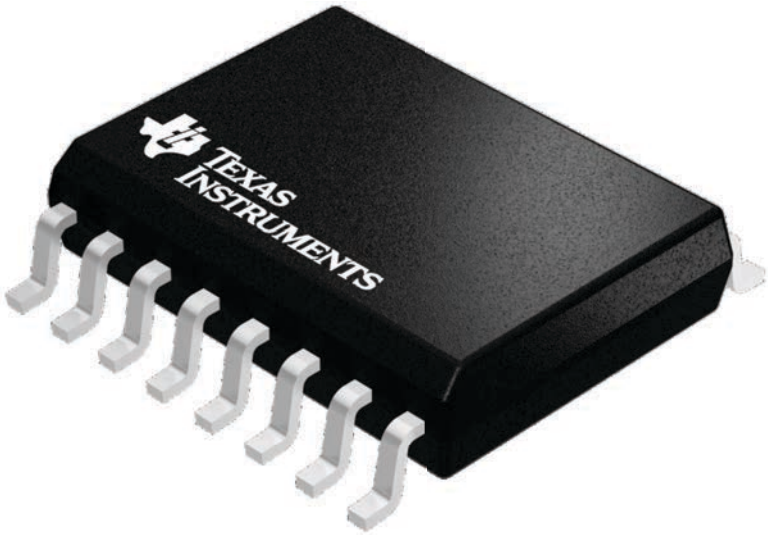
DW 16

SOIC - 2.65 mm max height

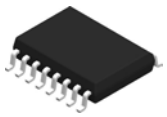
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

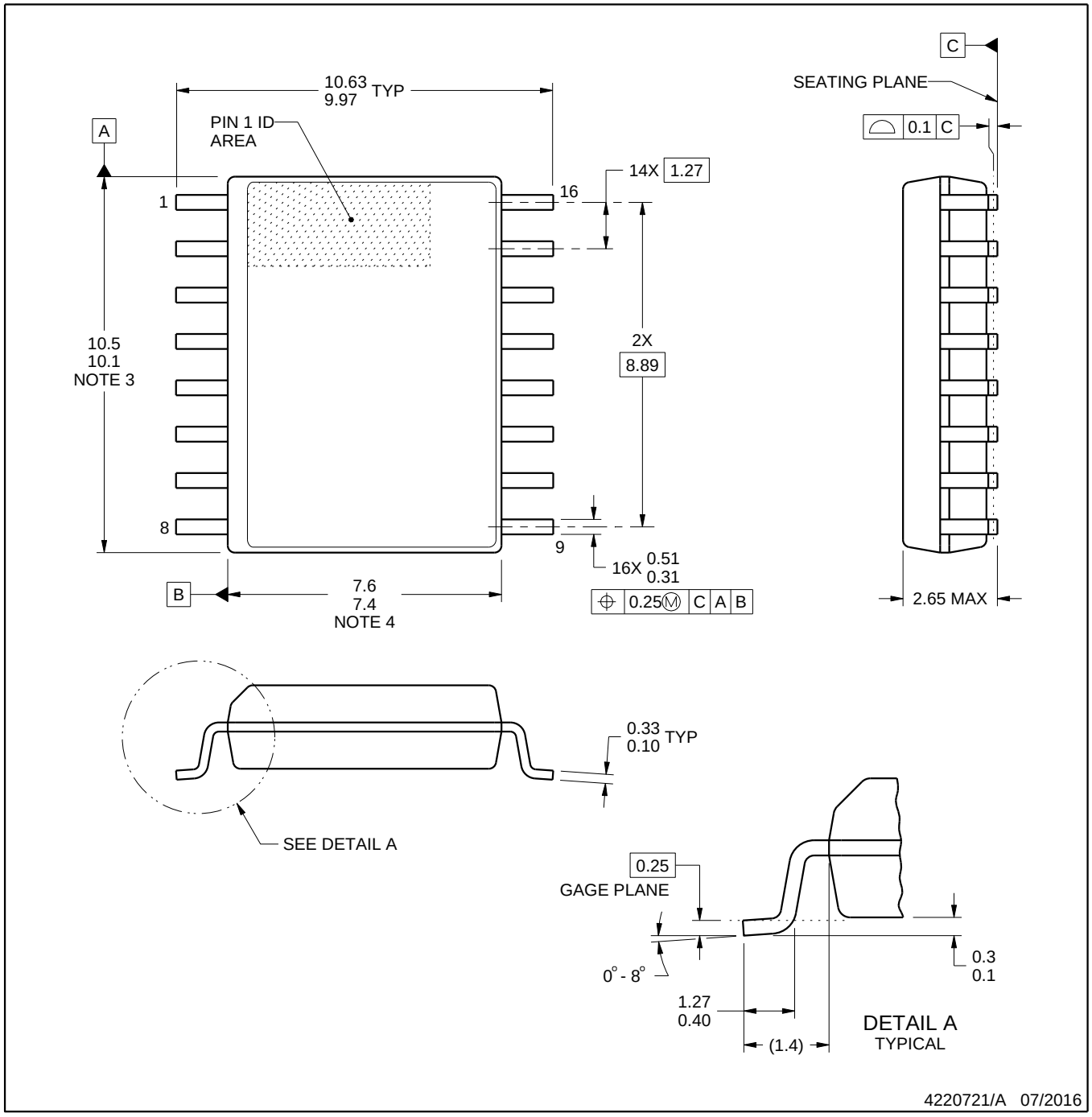


PACKAGE OUTLINE

DW0016A

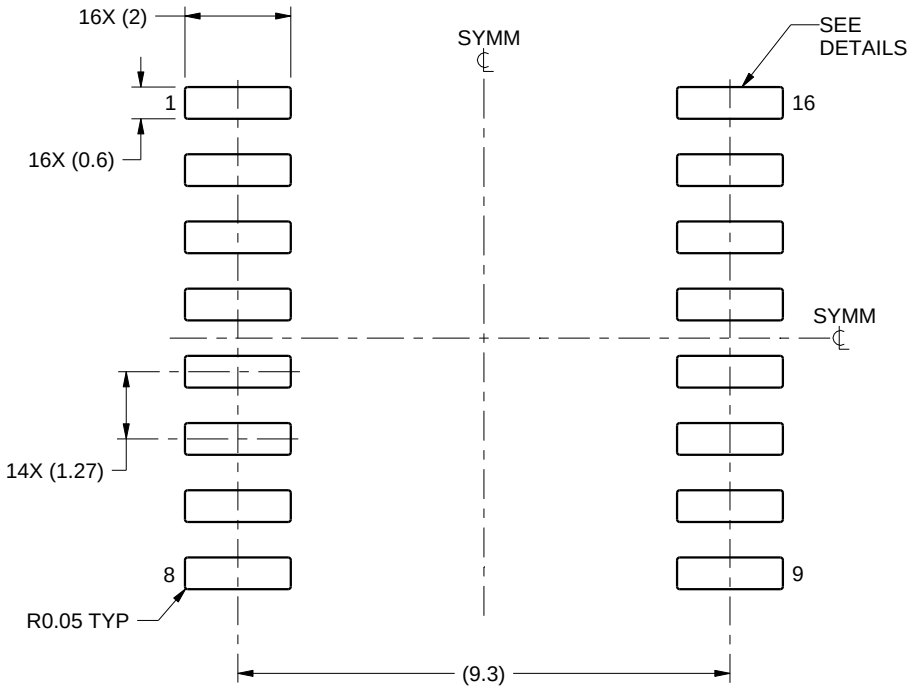
SOIC - 2.65 mm max height

SOIC

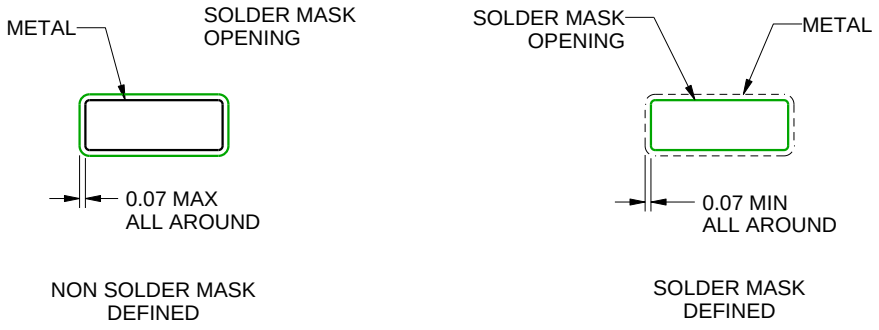


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

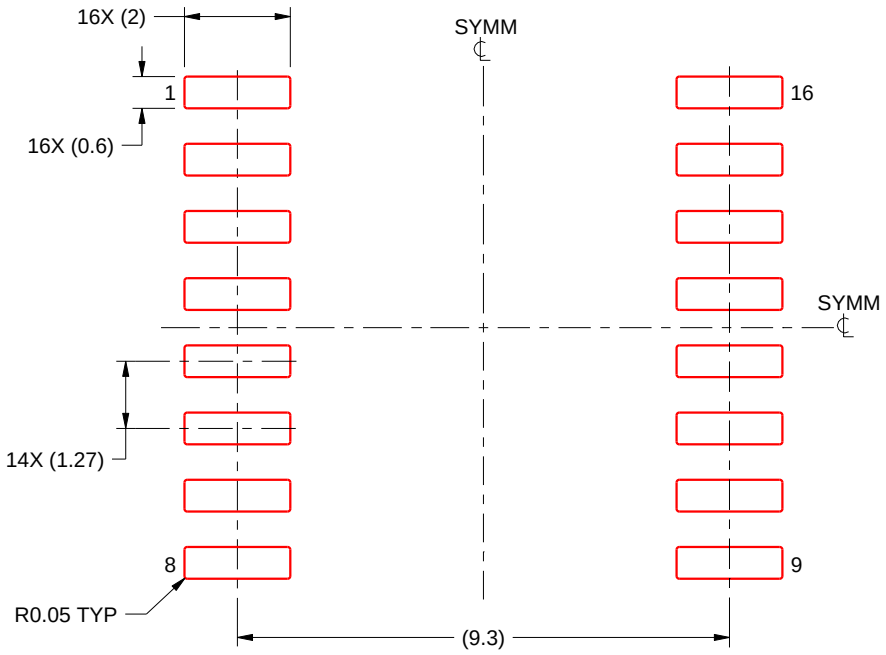


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



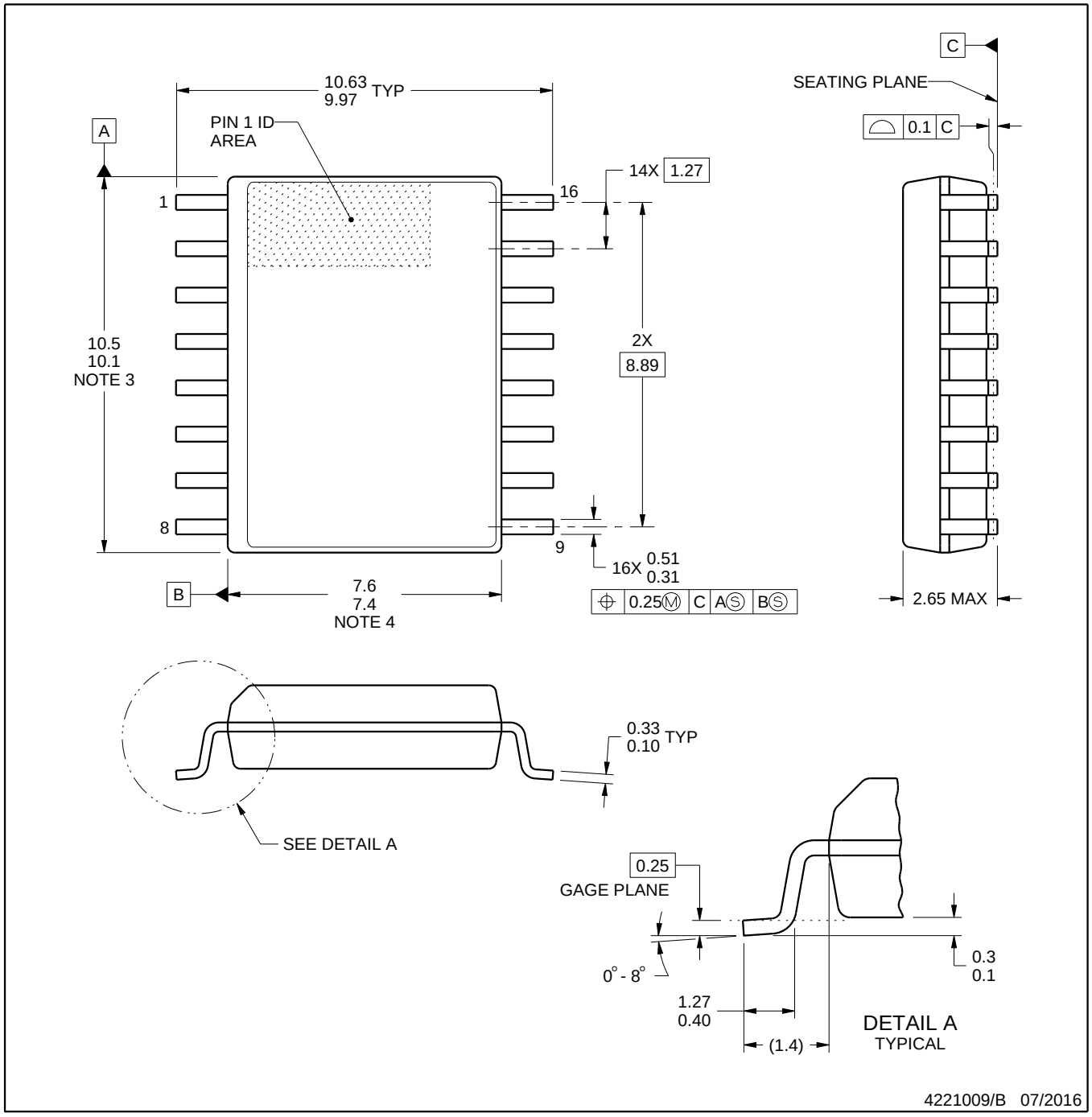
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

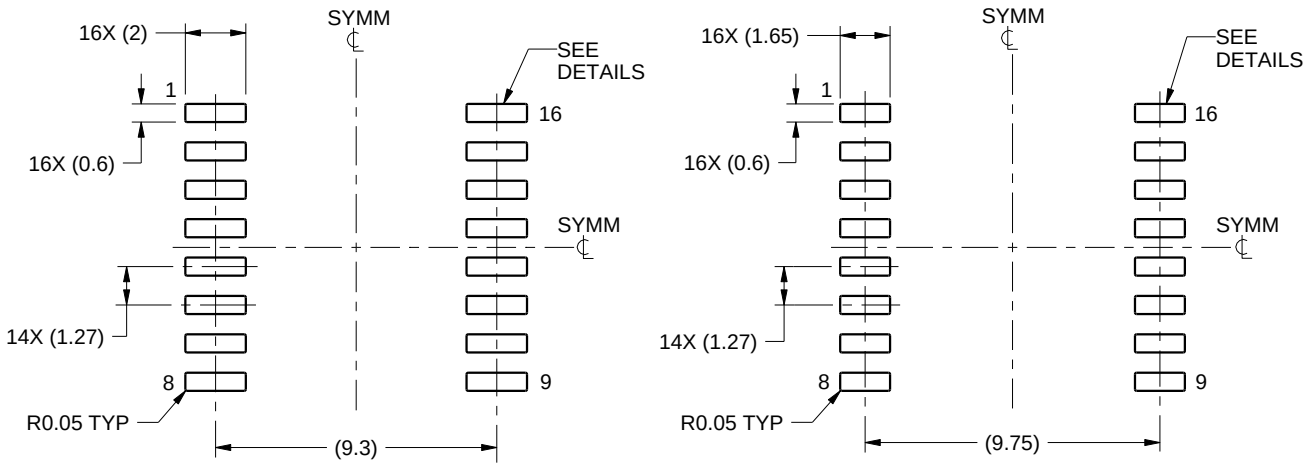
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

SOIC



NOTES:

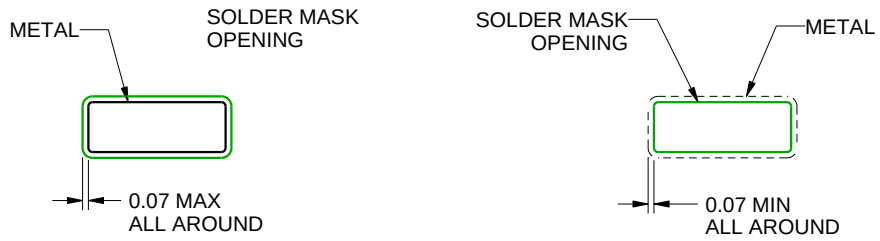
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

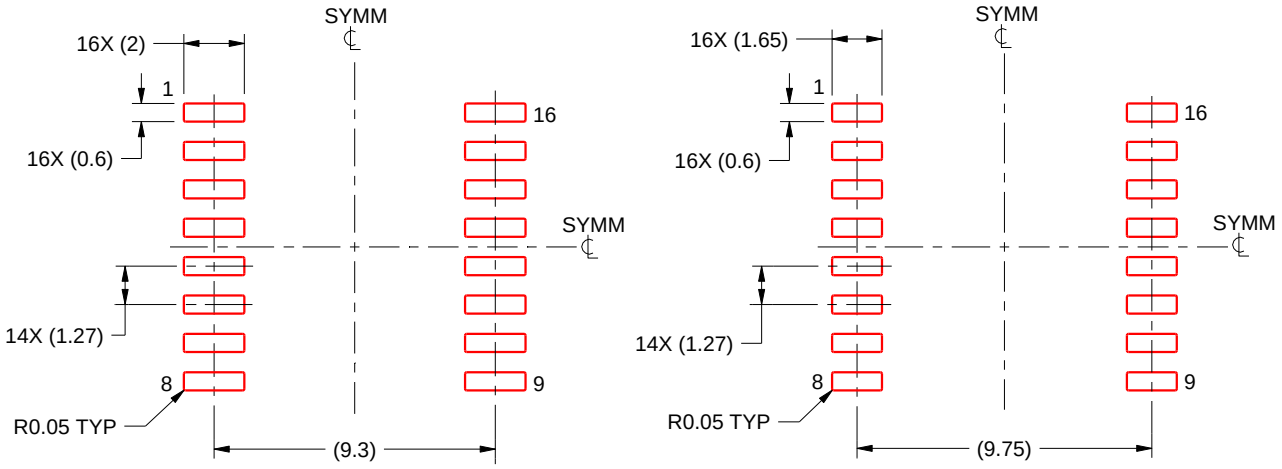
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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