TEXAS INSTRUMENTS

BUF20800-Q1

ZHCS348C – AUGUST 2011 – REVISED AUGUST 2018

具有两个可编程 VCOM 通道的 BUF20800-Q1 18 通道可编程伽马电压发生器

1 特性

- 符合汽车类应用的 应用
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4
- 低电源电流：900μA/通道
- 模拟电源电压：7V 至 18V
- 数字电源电压：2V 至 5.5V
- 18 通道伽马校正
- 2 通道可编程 V_{COM}：50mA I_{OUT}
- 10 位分辨率
- 轨至轨输出
- I²C 接口
  - 3.4MHz 高速模式
- 提供演示板和软件

2 应用

- 替代基于电阻器的伽马解决方案
- TFT-LCD 基准驱动器
- 动态伽马控制

3 说明

BUF20800-Q1 是一款可编程电压基准发生器，专为 TFT-LCD 面板中的伽马校正而设计。它提供 18 个用于伽马校正的可编程输出和 2 个用于 V_{COM} 调节的通道（每个具有 10 位分辨率）。

所有通道都可以使用支持高速数据传输（高达 3.4MHz）的 I²C 接口进行编程。该可编程性替代了传统的更改电阻器值以优化各种伽马电压的耗时过程，使设计人员能够很快地为面板确定正确的伽马电压。无需硬件更改即可轻松实现所需的更改。

BUF20800-Q1 使用 TI 的最新小几何尺寸模拟 CMOS 工艺，从而使其成为适用于大批量生产（而不仅仅是评估）的极具竞争力的选择。

如需更低的通道数，请联系您的当地销售或营销代表。

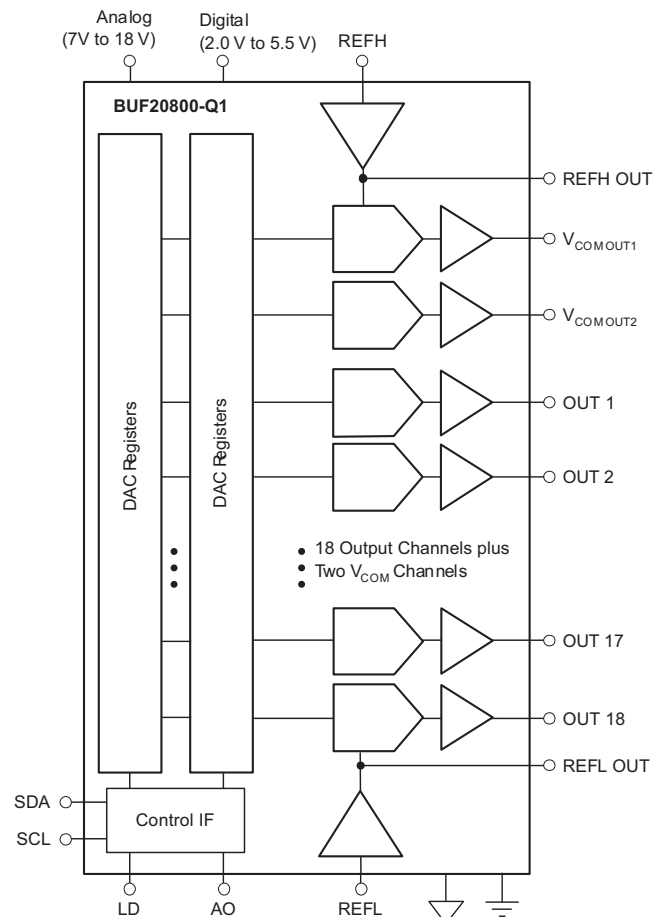BUF20800-Q1 采用具有PowerPAD™的 HTSSOP-38 封装。其额定温度范围为 −40°C 至 +105°C。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
BUF20800-Q1	HTSSOP (38)	9.80mm × 9.60mm

相关产品

特性	产品
12 通道可编程缓冲器，10 位	BUF12800
可编程 V_{COM}	BUF01900
11、6、4 通道伽马校正缓冲器，18V 电源	BUFxx704
高速 V_{COM}，1 通道和 2 通道	SN10501
完整的 LCD 直流/直流解决方案	TPS65100

简化框图

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(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

English Data Sheet: SBOS571
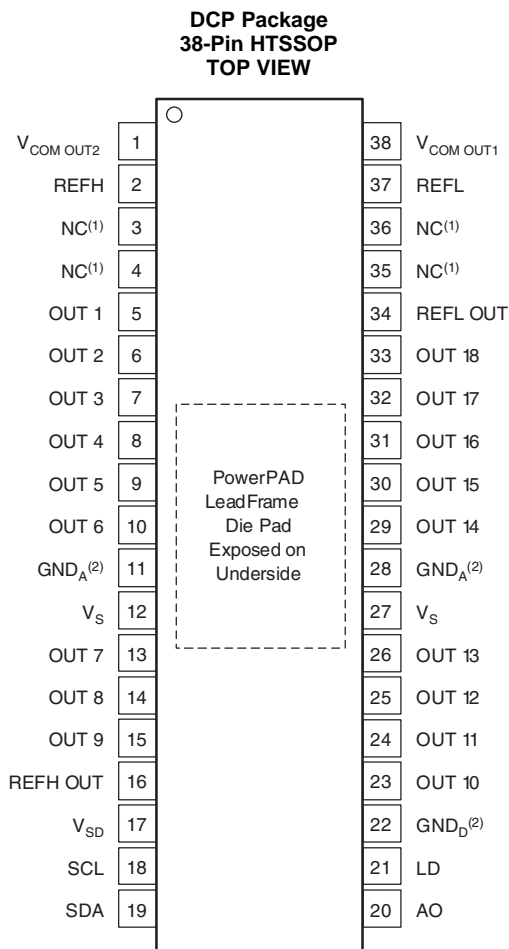
目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (January 2018) to Revision C   **Page**

- Changed OUT1-9 high output swing MIN number from "17.7" to "17.6" 6
- Added OUT1-9 high output swing for T_A = +25°C" 6

Changes from Revision A (November 2017) to Revision B   **Page**

- Added INL spec over temperature 6
- Added R1 and R2 callouts and corrected capacitor '10mF' value to '10µF' in Typical Application Configuration 22

Changes from Original (August 2011) to Revision A   **Page**

- 根据新的 TI 标准重新设置了格式：添加了器件信息 表、引脚配置和功能 部分、规格 部分、特性 说明 部分、器件功 能模式 部分、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 1
- Changed to "Code 978" from "Code 1023" 6
- Changed to "Code 32" from "Code 00" 6
- Added MAX value for "OUT 10-18 output swing : low " parameter 6

5 Pin Configuration and Functions

DCP Package
38-Pin HTSSOP
TOP VIEW

Left pin	No.		No.	Right pin
$V_{COM\ OUT2}$	1		38	$V_{COM\ OUT1}$
REFH	2		37	REFL
NC(1)	3		36	NC(1)
NC(1)	4		35	NC(1)
OUT 1	5		34	REFL OUT
OUT 2	6		33	OUT 18
OUT 3	7		32	OUT 17
OUT 4	8		31	OUT 16
OUT 5	9		30	OUT 15
OUT 6	10		29	OUT 14
GND_A(2)	11		28	GND_A(2)
V_S	12		27	V_S
OUT 7	13		26	OUT 13
OUT 8	14		25	OUT 12
OUT 9	15		24	OUT 11
REFH OUT	16		23	OUT 10
V_{SD}	17		22	GND_D(2)
SCL	18		21	LD
SDA	19		20	AO

PowerPAD LeadFrame Die Pad Exposed on Underside

(1) NC denotes no connection

(2) GND_D and GND_A are internally connected and must be at the same voltage potential.

Pin Functions

PIN NAME	NO.	I/O	DESCRIPTION
A0	20	I	Two-wire serial interface address select pin
GND_A	28	—	Analog ground. Must be connected to digital ground GND_D.
	11		
GND_D	22	—	Digital ground. Must be connected to analog ground GND_A.
LD	21		Output latch pin
NC	3	—	No connection. Leave this pin floating.
	4		
	35		
	36		
OUT1	5	O	DAC output 1
OUT2	6	O	DAC output 2
OUT3	7	O	DAC output 3
OUT4	8	O	DAC output 4
OUT5	9	O	DAC output 5

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT6	10	O	DAC output 6
OUT7	13	O	DAC output 7
OUT8	14	O	DAC output 8
OUT9	15	O	DAC output 9
OUT10	23	O	DAC output 10
OUT11	24	O	DAC output 11
OUT12	25	O	DAC output 12
OUT13	26	O	DAC output 13
OUT14	29	O	DAC output 14
OUT15	30	O	DAC output 15
OUT16	31	O	DAC output 16
OUT17	32	O	DAC output 17
OUT18	33	O	DAC output 18
REFH	2	I	Reference voltage REFH input
REFH OUT	16	O	Reference voltage REFH output
REFL	37	I	Reference voltage REFL input
REFL OUT	34	O	Reference voltage REFL output
SCL	18	I	Serial clock input; open drain.
SDA	19	I/O	Serial data I/O; open drain.
VCOMOUT1	38	O	VCOM channel 1
VCOMOUT2	1	O	VCOM channel 2
VS	12	I	Analog supply
	27		
VSD	17	I	Digital supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1].

PARAMETER			MINIMUM	MAXIMUM	UNIT
V_S	Supply voltage			19	V
V_{SD}	Supply voltage			6	V
	Signal input terminals, SCL, SDA, AO, LD	Voltage	−0.5	6	V
		Current	±10		mA
	Output Short-Circuit [2]		Continuous		
T_A	Operating temperature		−40	+105	°C
T_{stg}	Storage temperature		−65	+150	°C
T_J	Junction temperature			125	°C
	Latch-up per JESD78B		Class 1		

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short-circuit to ground, one channel at a time.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±750	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Analog supply	7		18	V
VSD	Digital supply	2		5.5	V
REFH	Reference high	4		VS – 0.2	V
REFL	Reference low	GND + 0.2		VS – 4	V
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature			125	°C

6.4 Thermal Information

THERMAL METRIC [1]		BUF20800-Q1	UNIT
		DCP Package (HTSSOP Family)	
		38 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At T_A = 25°C, V_S = 18 V, V_{SD} = 5 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

	PARAMETER	CONDITIONS	BUF20800-Q1 MIN	BUF20800-Q1 TYP	BUF20800-Q1 MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
	OUT 1−9 output swing: high	Sourcing 10 mA, V_{REFH} = 17.8 V, Code 1023, T_A = −40°C to +105°C	17.6			V
		Sourcing 10 mA, V_{REFH} = 17.8 V, Code 1023, T_A = +25°C	17.7	17.8		
	OUT 10−18 output swing: high	Sourcing 10 mA, V_{REFH} = 17.8 V, Code 978, T_A = −40°C to +105°C	16.8	17.2		
	OUT 1−9 output swing: low	Sinking 10 mA, V_{REFL} = 0.2 V, Code 32, T_A = −40°C to +105°C		0.6	1.0	V
	OUT 10−18 output swing: low	Sinking 10 mA, V_{REFL} = 0.2 V, Code 00, T_A = −40°C to +105°C		0.2	0.4	
	VCOM buffer output swing: high	Sourcing 50 mA, V_{REFH} =17.8 V, T_A = −40°C to +105°C	13	15.5		V
	VCOM buffer output swing: low	Sinking 50 mA, V_{REFL} = 0.2 V, T_A = −40°C to +105°C		1	2.0	V
I_O	Output current [(1)](#)	All Channels, Code 512, Sinking/Sourcing	40	45		mA
INL	Integral nonlinearity	No Load, V_{REFH} = 17 V, V_{REFL} = 1 V		0.3	1.5	Bits
		No Load, V_{REFH} = 17 V, V_{REFL} = 1 V, T_A = −40°C to 105°C			2.5	
DNL	Differential nonlinearity	No Load, V_{REFH} = 17 V, V_{REFL} = 1 V		0.3	1	Bits
	Gain error			0.12		%
t_D	Program to out delay			5		μs
	Output accuracy	No Load, V_{REFH} = 17 V, V_{REFL} = 1 V		±20	±50	mV
		No Load, V_{REFH} = 17 V, V_{REFL} = 1 V, T_A = −40°C to +105°C		±25		mV
RI_{NH}	Input resistance at V_{REFH} and V_{REFL}			100		MΩ
REG	Load regulation, All References	V_{OUT} = V_S/2, I_{OUT} = 5 mA to −5 mA Step		0.5	1.5	mV/mA
	40 mA, All Channels	V_{OUT} = V_S/2, $I_{SINKING}$ = 40 mA, $I_{SOURCING}$ = 40 mA		0.5	1.5	mV/mA
ANALOG POWER SUPPLY						
V_S	Operating range		7		18	V
I_S	Total analog supply current	No Load		18	28	mA
		Outputs at Reset Values, No Load, Two-Wire Bus Inactive, T_A = −40°C to +105°C			28	mA
DIGITAL						
V_{IH}	Logic 1 input voltage		0.7 × V_{SD}			V
V_{IL}	Logic 0 input voltage				0.3 × V_{SD}	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 3 mA		0.15	0.4	V
	Input leakage			±0.01	±10	μA
f_{CLK}	Clock frequency	Standard/Fast Mode, T_A = −40°C to +105°C			400	kHz
		High-Speed Mode, T_A = −40°C to +105°C			3.4	MHz

(1) See typical characteristic graph Output Voltage vs Output Current

Electrical Characteristics (continued)

At T_A = 25°C, V_S = 18 V, V_{SD} = 5 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

	PARAMETER	CONDITIONS	BUF20800-Q1			UNIT
			MIN	TYP	MAX	
DIGITAL POWER SUPPLY						
V_{SD}	Operating range		2.0		5.5	V
I_{SD}	Digital supply current [2]	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		25	50	μA
		Outputs at Reset Values, No Load, Two-Wire Bus Inactive, T_A = –40°C to +105°C		100		μA
TEMPERATURE RANGE						
	Operating temperature range	Junction Temperature < +125°C	–40		+105	°C
	Storage temperature range		–65		+150	°C
$θ_{JA}$	Thermal resistance, HTSSOP-38: Junction-to-Ambient			30		°C/W
$θ_{JC}$	Thermal resistance, HTSSOP-38: Junction-to-Case			15		°C/W

(2)   See typical characteristic graph Digital Supply Current vs Temperature

6.6 Typical Characteristics

At T_A = 25°C, V_S = 18 V, V_{SD} = 5 V, V_{REFH} = 17 V, V_{REFL} = 1 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.
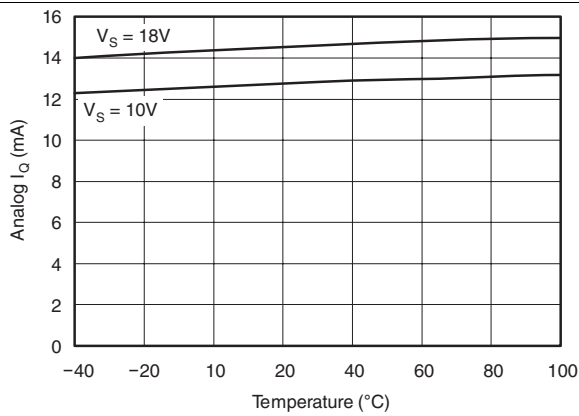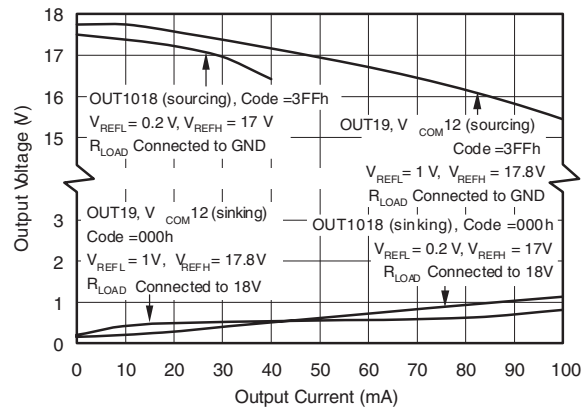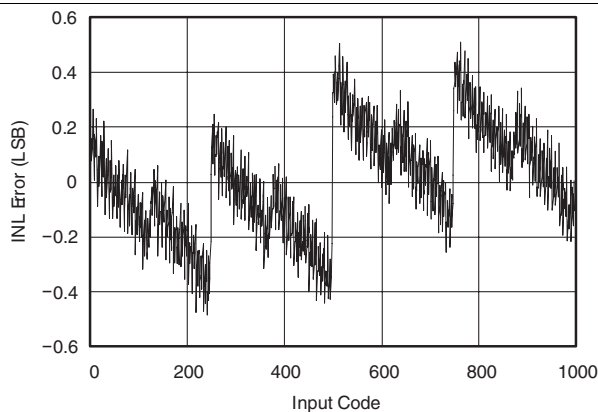

Figure 1. Analog Supply Current vs Temperature
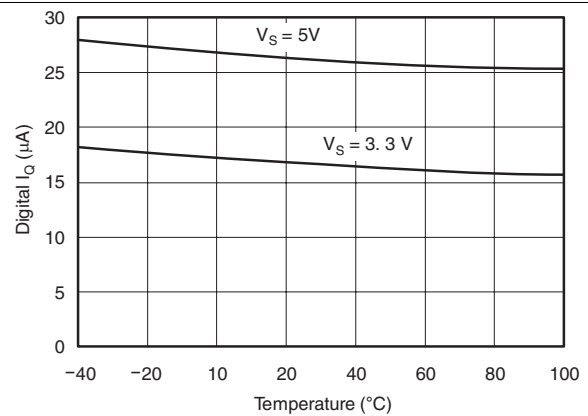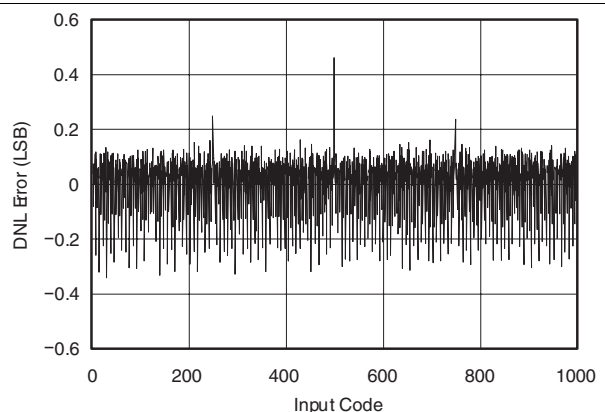

Figure 2. Digital Supply Current vs Temperature
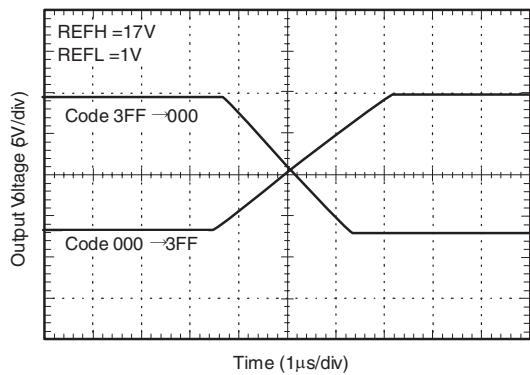
Figure 3. Full−scale Output Swing

Figure 4. Output Voltage vs Output Current

Figure 5. Integral Nonlinearity Error vs Input Code



Figure 6. Differential Nonlinearity Error vs Input Code

7 Detailed Description

7.1 Overview

The BUF20800-Q1 programmable voltage reference allows fast, easy adjustment of 18 programmable reference outputs and two channels for V_{COM} adjustment, each with 10-bit resolution. It offers very simple, time-efficient adjustment of the gamma reference and V_{COM} voltages. The BUF20800-Q1 is programmed through a high-speed, standard, two-wire interface. The BUF20800-Q1 features a double-register structure for each DAC channel to simplify the implementation of dynamic gamma control. This structure allows pre-loading of register data and rapid updating of all channels simultaneously.

Buffers 1−9 are able to swing to within 200mV of the positive supply rail, and to within 0.6V of the negative supply rail. Buffers 10−18 are able to swing to within 0.8V of the positive supply rail and to within 200mV of the negative supply rail.

The BUF20800-Q1 can be powered using an analog supply voltage from 7V to 18V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to or simultaneously with the analog supply to avoid excessive current and power consumption; damage to the device may occur if it is left connected only to the analog supply for extended periods of time. Figure 7 shows the power supply timing requirements.
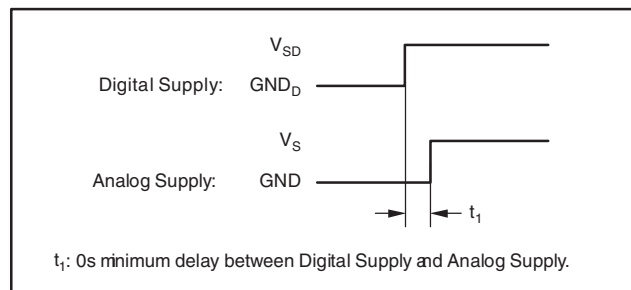
Figure 7. Power Supply Timing Requirements

Figure 14 shows the BUF20800-Q1 in a typical configuration. In this configuration, the BUF20800-Q1 device address is 74h. The output of each digital-to-analog converter (DAC) is immediately updated as soon as data are received in the corresponding register (LD = 0).

For maximum dynamic range, set $V_{REFH} = V_S − 0.2$ V and $V_{REFL} = GND + 0.2$ V.

7.2 Functional Block Diagram

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7.3 Feature Description

7.3.1 General-call Reset and Power-up

The BUF20800-Q1 responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF20800-Q1 acknowledges both bytes. Upon receiving a General Call Reset, the BUF20800-Q1 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

Feature Description (continued)

The BUF20800-Q1 automatically performs a reset upon power up. As part of the reset, all outputs are set to $(V_{REFH} - V_{REFL})/2$. Other reset values are available as a custom modification—contact your TI representative for details.

The BUF20800-Q1 resets all outputs to $(V_{REFH} - V_{REFL})/2$ after sending the device address, if a valid DAC address is sent with bits D7 to D5 set to '100'. If these bits are set to '010', only the DAC being addressed in this most significant byte (MSB) and the following least significant byte (LSB) will be reset.

7.3.2 Output Voltage

Buffer output values are determined by the reference voltages (VREFH and VREFL) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = [\frac{V_{REFH} - V_{REFL}}{1024} \times \text{Decimal Value of Code}] + V_{REFL}$$

(1)

The valid voltage ranges for the reference voltages are:

$4V \leq V_{REFH} - V_S \leq 0.2\ V$ and $0.2\ V \leq V_{REFL} \leq V_S - 4\ V$ (2)

The BUF20800-Q1 outputs are capable of a full-scale voltage output change in typically 5 μs—no intermediate steps are required.

7.3.3 Output Latch

Updating the DAC register is not the same as updating the DAC output voltage, because the BUF20800-Q1 features a double-buffered register structure. There are three methods for latching transferred data from the storage registers into the DACs to update the DAC output voltages.

Method 1 requires externally setting the latch pin (LD) LOW, LD = LOW, which will update each DAC output voltage whenever its corresponding register is updated.

Method 2 externally sets LD = HIGH to allow all DAC output voltages to retain their values during data transfer and until LD = LOW, which will then simultaneously update the output voltages of all DACs to the new register values. Use this method to transfer a future data set in advance to prepare for a very fast output voltage update.

Method 3 uses software control. LD is maintained HIGH, and all DACs are updated when the master writes a 1 in bit 15 of any DAC register. The update will occur after receiving the 16-bit data for the currently-written register.

The General Call Reset and the power-up reset will update the DAC regardless of the state of the latch pin.

7.3.4 Programmable VCOM

The V_{COM} channels of the BUF20800-Q1 can swing to 2V from the positive supply rail while sourcing 50 mA and to 1 V above the negative rail while sinking 50 mA (see Figure 4, typical characteristic *Output Voltage vs Output Current*). To store the gamma and the V_{COM} values, an external EEPROM is required. During power-up of the LCD panel, the timing controller can then read the EEPROM and load the values into the BUF20800-Q1 to generate the desired V_{COM} voltages, as illustrated in Figure 10 and Figure 8. The V_{COM} channels can be programmed independently from the gamma channels.

Feature Description (continued)
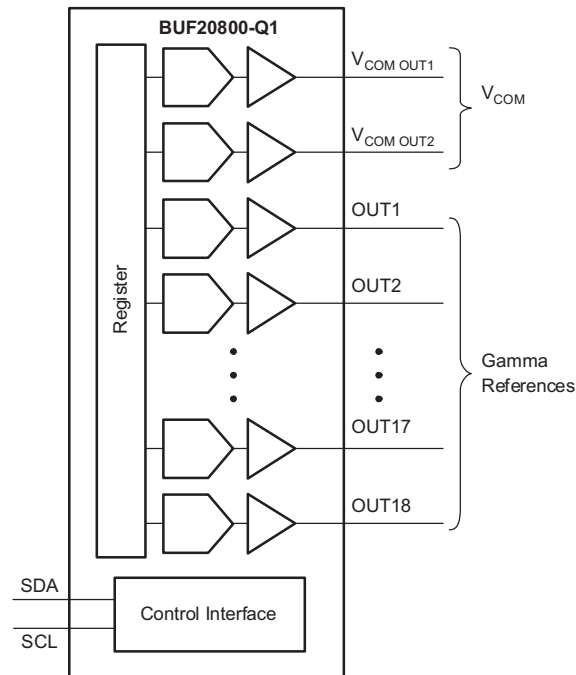

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Figure 8. BUF20800-Q1 Used for Programmable V$_{COM}$

7.3.5 REFH and REFL Input range

Best performance and output swing range of the BUF20800-Q1 are achieved by applying REFH and REFL voltages that are slightly below the power-supply voltages. Most specifications have been tested at REFH = V$_s$ − 200mV and REFL = GND + 200mV. The REFH internal buffer is designed to swing very closely to V$_s$ and the REFL internal buffer to GND. However, there is a finite limit on how close they can swing before saturating. To avoid saturation of the internal REFH and REFL buffers, the REFH voltage should not be greater than V$_s$ −100mV and REFL voltage should not be lower than GND + 100mV. Figure 9 shows the swing capability of the REFH and REFL buffers.

The other consideration when trying to maximize the output swing capability of the gamma buffers is the limitation in the swing range of output buffers (OUT1−18, V$_{COM1}$, and V$_{COM2}$), which depends on the load current. A typical load in the LCD application is 5−10mA. For example, if OUT1 is sourcing 10mA, the swing is typically limited to about V$_s$ − 200mV. The same applies to OUT18, which typically limits at GND + 200mV when sinking 10mA. An increase in output swing can only be achieved for much lighter loads. For example, a 3mA load typically allows the swing to be increased to approximately V$_s$ − 100mV and GND + 100mV.

Connecting REFH directly to V$_s$ and REFL directly to GND does not damage the BUF20800-Q1. As discussed above however, the output stages of the REFH and REFL buffers will saturate. This condition is not desirable and can result in a small error in the measured output voltages of OUT1−18, V$_{COM1}$, and V$_{COM2}$. As described above, this method of connecting REFH and REL does not help to maximize the output swing capability.

Feature Description (continued)
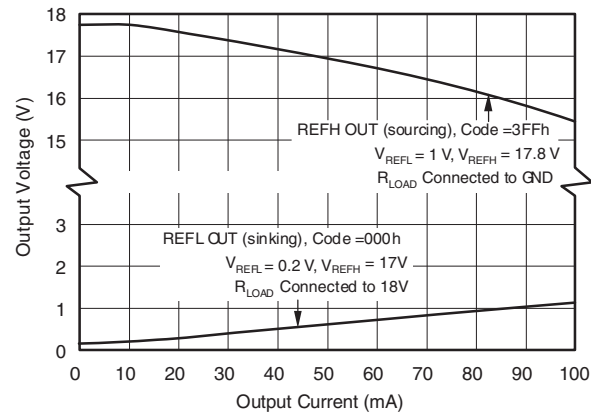
Figure 9. Reference Buffer Output Voltage vs Output Current

## 7.4 Device Functional Modes

7.4.1 Replacement of Traditional Gamma Buffer

Traditional gamma buffers rely on a resistor string (often using expensive 0.1% resistors) to set the gamma voltages. During development, the optimization of these gamma voltages can be time-consuming. Programming these gamma voltages with the BUF20800-Q1 can significantly reduce the time required for gamma voltage optimization. The final gamma values can be written into an external EEPROM to replace a traditional gamma buffer solution. During power-up of the LCD panel, the timing controller reads the EEPROM and loads the values into the BUF20800-Q1 to generate the desired gamma voltages. Figure 10a shows the traditional resistor string; Figure 10b shows the more efficient alternative method using the BUF20800-Q1.

BUF20800-Q1 uses the most advanced high-voltage CMOS process available today, which allows it to be competitive with traditional gamma buffers.

This technique offers significant advantages:
- It shortens development time significantly.
- It allows demonstration of various gamma curves to LCD monitor makers by simply uploading a different set of gamma values.
- It allows simple adjustment of gamma curves during production to accommodate changes in the panel manufacturing process or end-customer requirements.
- It decreases cost and space.

Device Functional Modes (continued)

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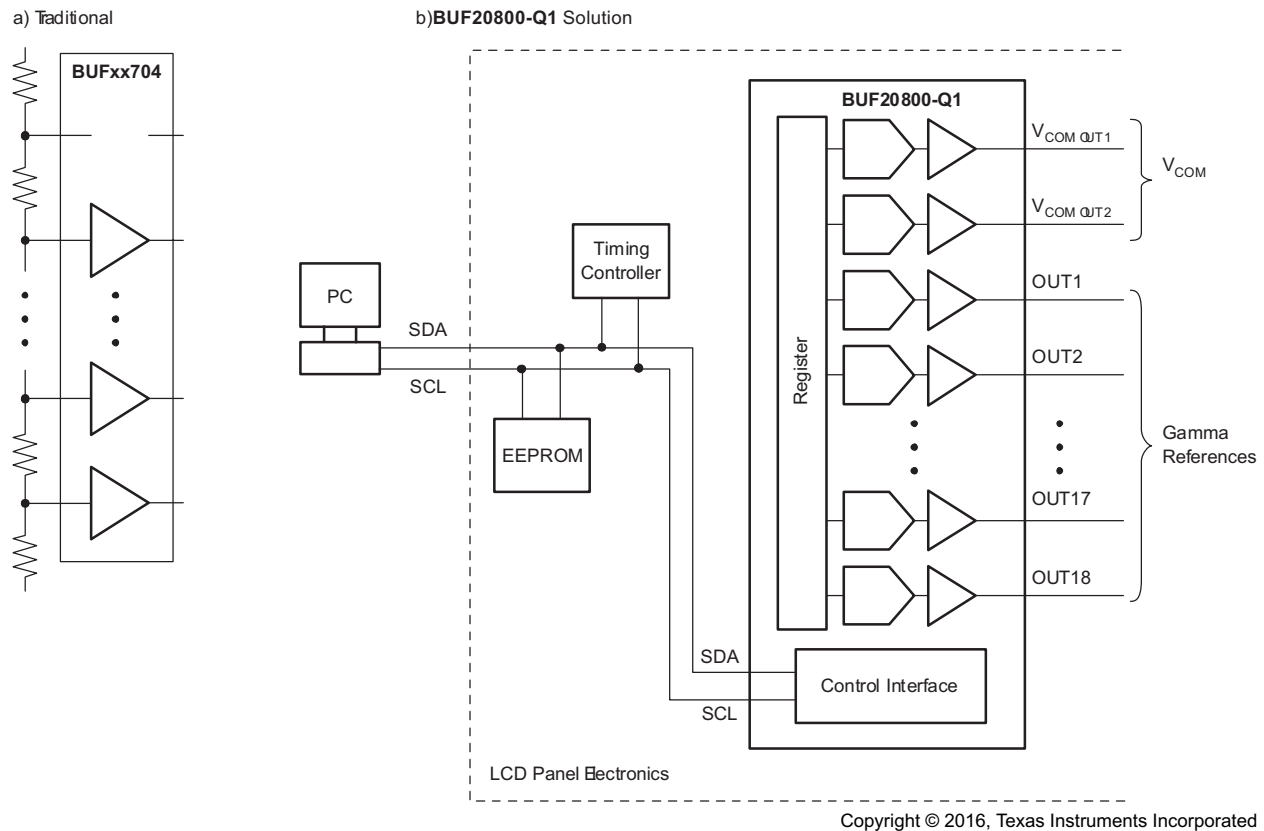
Figure 10. Replacement of the Traditional Gamma Buffer

7.4.2 Dynamic Gamma Control

Dynamic gamma control is a technique used to improve the picture quality in LCD TV applications. The brightness in each picture frame is analyzed and the gamma curves are adjusted on a frame-by-frame basis. The gamma curves are typically updated during the short vertical blanking period in the video signal. Figure 11 shows a block diagram using the BUF20800-Q1 for dynamic gamma control and V_{COM} output.

The BUF20800-Q1 is ideally suited for rapidly changing the gamma curves because of its unique topology:

* double register input structure to the DAC;
* fast serial interface;
* simultaneous updating of all DACs by software. See the Read/Write Operations to write to all registers and the Output Latch sections.

The double register input structure saves programming time by allowing updated DAC values to be pre-loaded into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC output values remain unchanged—the display is unaffected. During the vertical sync period, the DAC outputs (and therefore, the gamma voltages) can be quickly updated either by using an additional control line connected to the LD pin, or through software—writing a '1' in bit 15 of any DAC register. For the details on the operation of the double register input structure, see the Output Latch section.

Example: Update all 18 gamma registers simultaneously via software.

    Step 1: Check if LD pin is placed in HIGH state.

    Step 2: Write DAC Registers 1−18 with bit 15 always '0'.

Device Functional Modes (continued)

Step 3: Write any DAC register a second time with identical data. Make sure that bit 15 is '1'. All DAC channels will be updated simultaneously after receiving the last bit of data. (Note: this step may be eliminated by setting bit 15 of DAC 18 to '1' in the previous step.)
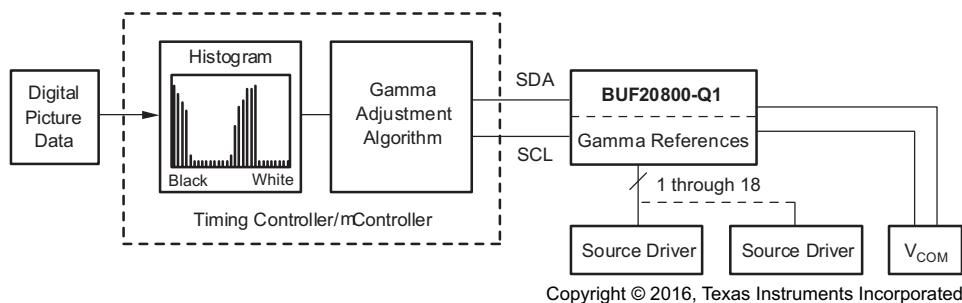

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Figure 11. Dynamic Gamma Control

7.5 Programming

7.5.1 Two-wire Bus Overview

The BUF20800-Q1 communicates through an industry standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the 9th clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF20800-Q1 can act only as a slave device; therefore, it never drives SCL. SCL is only an input for the BUF20800-Q1. Table 1 and Table 2 summarize the address and command codes, respectively, for the BUF20800-Q1.

7.5.2 Data Rates

The two-wire bus operates in one of three speed modes:
- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF20800-Q1 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with SCL = 400kHz, following the START condition; xxx are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF20800-Q1 will respond to the High-speed command regardless of the value of these last three bits. The BUF20800-Q1 will not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. On receiving a master code, the BUF20800-Q1 will switch on its Hs mode filters, and communicate at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF20800-Q1 will switch out of Hs mode with the next STOP condition.

Programming (continued)

7.5.3 Read/Write Operations

The BUF20800-Q1 is able to read from a single DAC, or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 0000 0000, which corresponds to DAC_1, through 0001 0011, which corresponds to V_{COM} OUT2.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH will perform a read transaction.

7.5.3.1 Writing

To write to a single DAC register

1. 1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D5 must be set to 0. Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10011 are valid and will be acknowledged. Table 3 shows the DAC addresses.
4. Send two bytes of data for the specified DAC register. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are used, and bits D15−D14 must not be 01), followed by the least significant byte (bits D7−D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus

The BUF20800-Q1 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register will not be updated. Updating the DAC register is not the same as updating the DAC output voltage. See the Output Latch section.

The process of updating multiple DAC registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF20800-Q1 automatically and sequentially steps through subsequent registers as additional data is sent. The process continues until all desired registers have been updated or a STOP condition is sent.

To write to multiple DAC registers:

1. 1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be updated. The BUF20800-Q1 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning), followed by the least significant byte (bits D7−D0). The first two bytes are for the DAC addressed in step 3 above. Its register is automatically updated after receiving the second byte. The next two bytes are for the following DAC. That DAC register is updated after receiving the fourth byte. This process continues until the registers of all following DACs have been updated.
5. Send a STOP condition on the bus.

The BUF20800-Q1 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data will be updated.

Programming (continued)

7.5.3.2   Reading

Reading a DAC register will return the data stored in the DAC. This data can differ from the data stored in the DAC register. See the Output Latch section.

To read the DAC value:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send the DAC address byte. Bits D7−D5 must be set to 0; Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10011 are valid and will be acknowledged.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20800-Q1 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8; only bits D9 and D8 have meaning); the next byte is the least significant byte (bits D7−D0).
7. Acknowledge after receiving the first byte.
8. Do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.
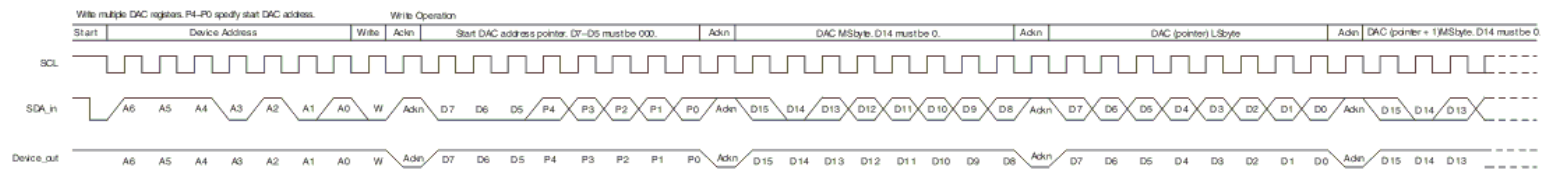
To Read Multiple DACs:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20800-Q1 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be read. The BUF20800-Q1 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20800-Q1 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, only bits D9 and D8 have meaning); the next byte is the least significant byte (bits D7−D0).
7. Acknowledge after receiving each byte of data except for the last byte. The acknowledge bit of the last byte should be HIGH to end the read operation.
8. When all desired DACs have been read, send a STOP or repeated START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.
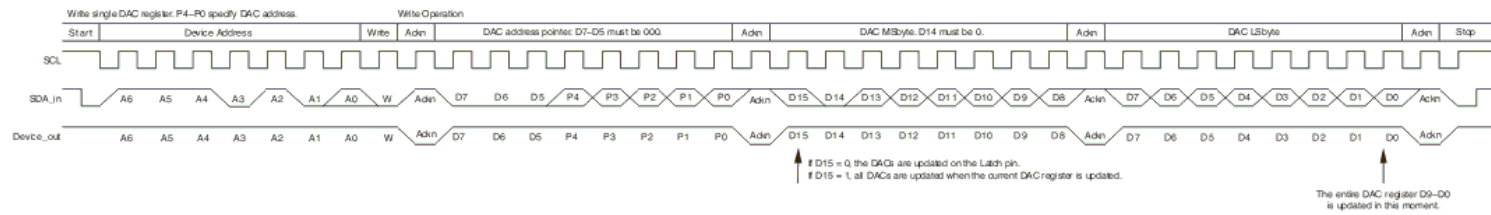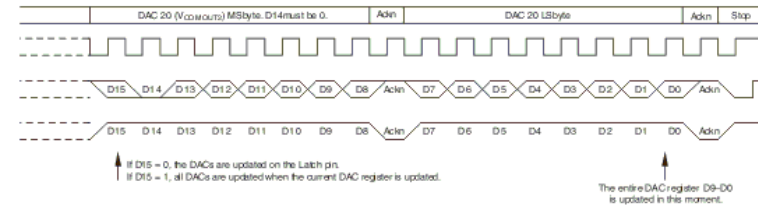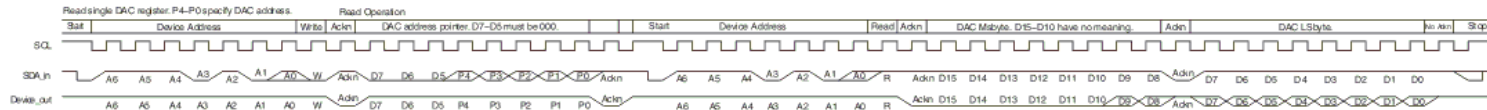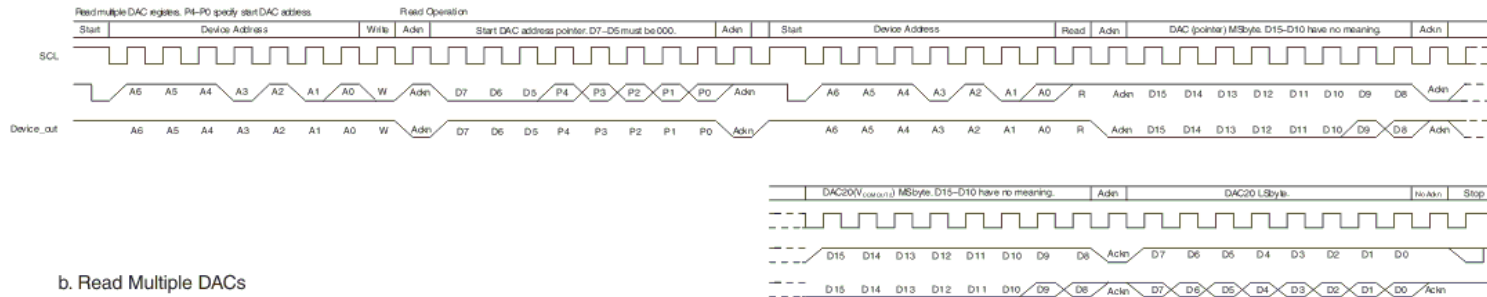
Figure 12. Timing Diagram for Write DAC Register

a. Read Single DAC

b. Read Multiple DACs

Figure 13. Timing Diagram for Read DAC Register

7.5.4 Register Maps

7.5.4.1 Addressing the BUF20800-Q1

The address of the BUF20800-Q1 is 111010x, where x is the state of the A0 pin. When the A0 pin is LOW, the device will acknowledge on address 74h (1110100). If the A0 pin is HIGH, the device will acknowledge on address 75h (1110101).

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick-Reference Table of BUF20800-Q1 Addresses

DEVICE/COMPONENT	
BUF20800-Q1 Address:	**ADDRESS**
A0 pin is LOW (device acknowledges on address 74h)	1110100
A0 pin is HIGH (device acknowledges on address 75h)	1110101

Table 2. Quick-Reference Table of Command Codes

COMMAND	CODE
General Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

7.5.5 Registers

Table 3. DAC Addresses

DAC	ADDRESS
DAC_1	0000 0000
DAC_2	0000 0001
DAC_3	0000 0010
DAC_4	0000 0011
DAC_5	0000 0100
DAC_6	0000 0101
DAC_7	0000 0110
DAC_8	0000 0111
DAC_9	0000 1000
DAC_10	0000 1001
DAC_11	0000 1010
DAC_12	0000 1011
DAC_13	0000 1100
DAC_14	0000 1101
DAC_15	0000 1110
DAC_16	0000 1111
DAC_17	0001 0000
DAC_18	0001 0001
V_{COM} OUT1	0001 0010
V_{COM} OUT2	0001 0011

8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.
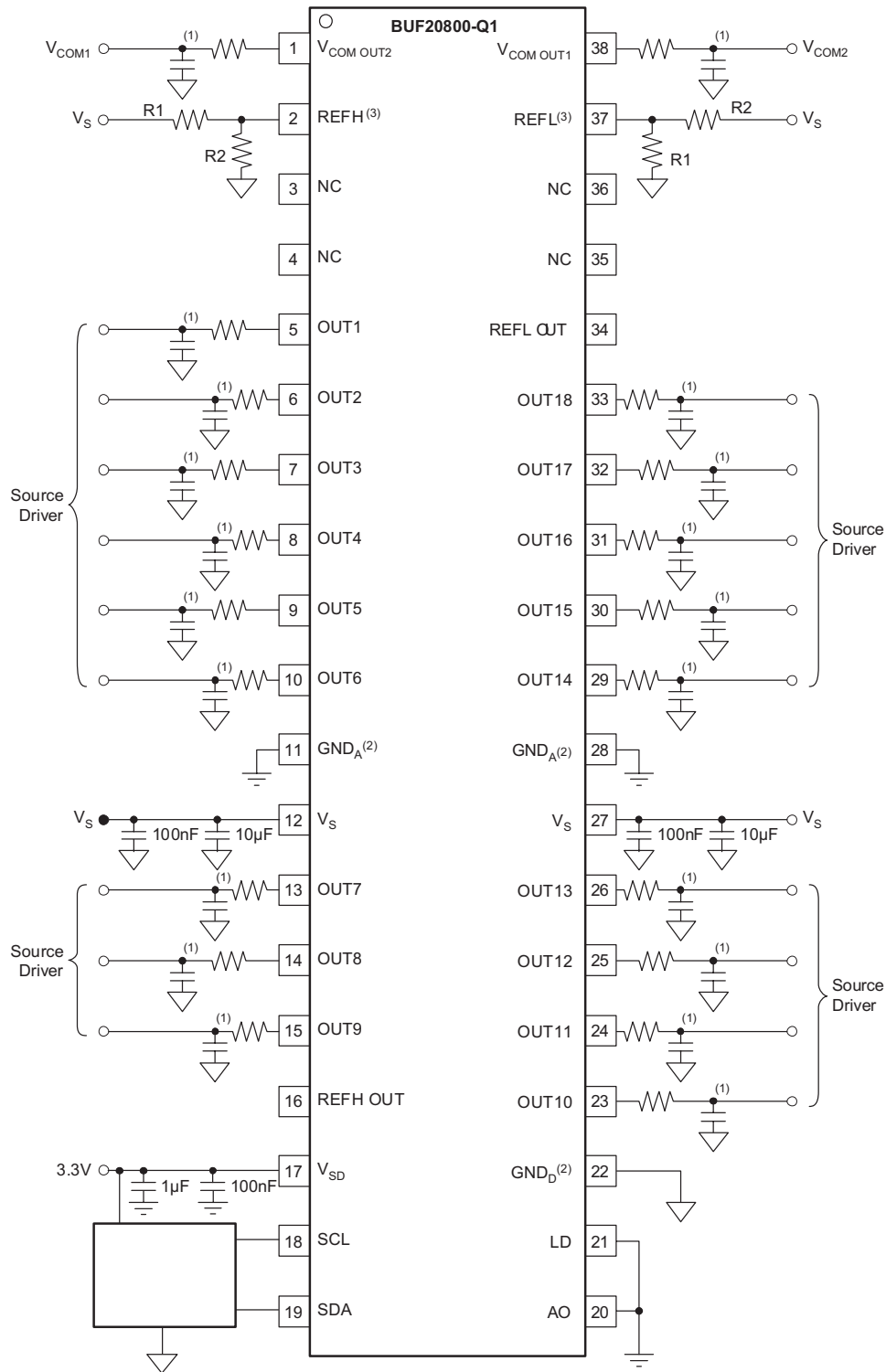
8.1 Application Information

The BUF20800-Q1 device was designed to provide 18 programmable outputs for gamma correction for the source driver IC and two VCOM channels for the common plane in LCD display applications.

8.2 Typical Application

Figure 14 shows a typical application circuit for the BUF20800-Q1 device.

Typical Application (continued)

(1) RC combination optional.
(2) GND_A and GND_D must be connected together.
(3) Connecting a capacitor to this node is not recommended.

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Figure 14. Typical Application Configuration

Typical Application (continued)

8.2.1 Design Requirements

Table 4 shows the design parameters for this design.

Table 4. Design Requirements

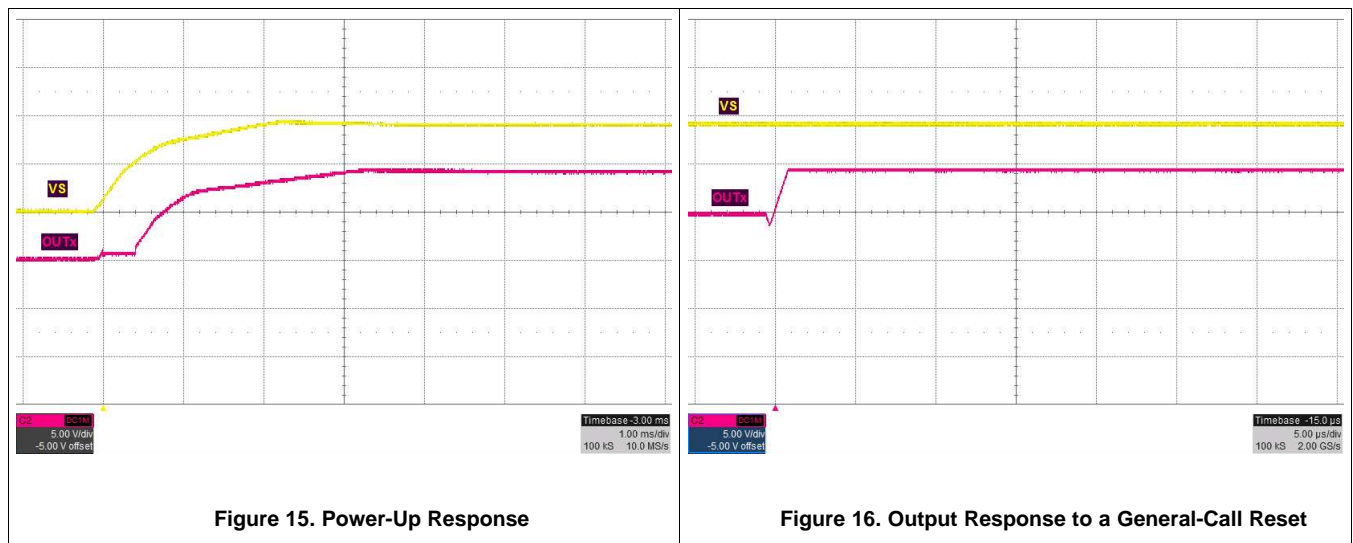| PARAMETER	SYMBOL	VALUE
Analog Input Supply Voltage	V_S	18 V
Digital Input Supply Voltage	V_{SD}	5 V
REFH Input Voltage	V_{REFH}	17.8 V
REFL Input Voltage	V_{REFL}	0.2 V

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. Connect a 10-µF capacitor in parallel to a 100-nF capacitor to all the analog input supply pins as shown in Figure 14. Connecting a 1-µF capacitor in parallel to a 100-nF capacitor is as well recommended at the digital input supply pin.

8.2.2.2 REFH and REFL Voltage Settings

The resistors R1 and R2 in Figure 14 shall be selected such as the ratio R2/(R1+R2) is close to 17/18. Use for instance R1 = 1 kΩ and R2 = 75 kΩ.

8.2.3 Application Curves

Figure 15. Power-Up Response

Figure 16. Output Response to a General-Call Reset

8.2.4 Configuration for 20 Gamma Channels

The VCOM outputs can be used as additional gamma references in order to achieve two additional gamma channels (20 total). The VCOM outputs will behave the same as the OUT1−9 outputs when sourcing or sinking smaller currents (see Figure 4). The VCOM outputs are better able to swing to the positive rail than to the negative rail. Therefore, it is better to use the VCOM outputs for higher reference voltages, as shown in Figure 17.
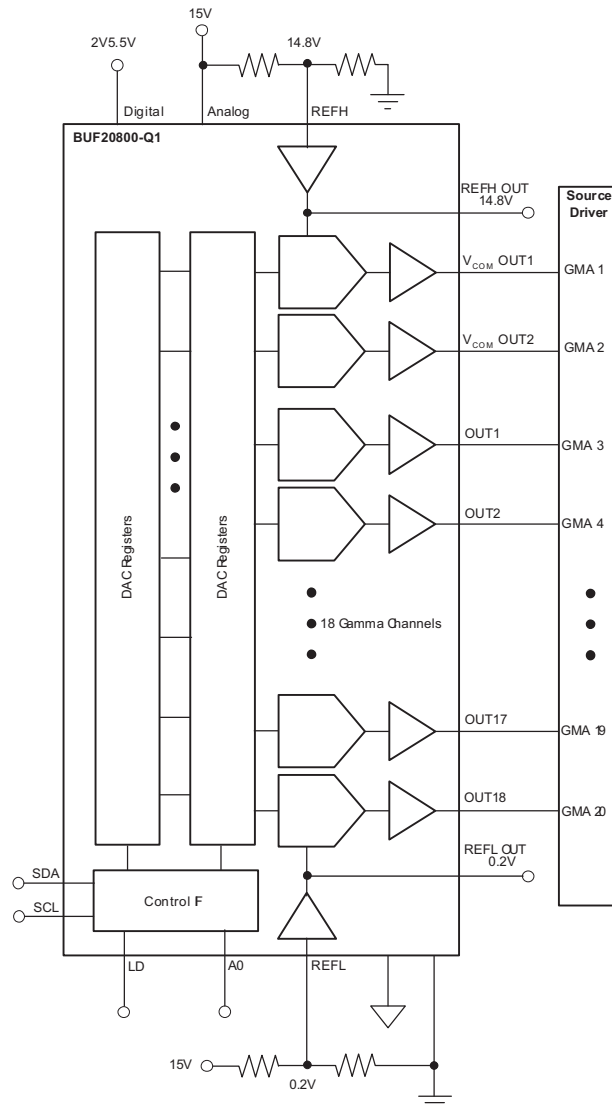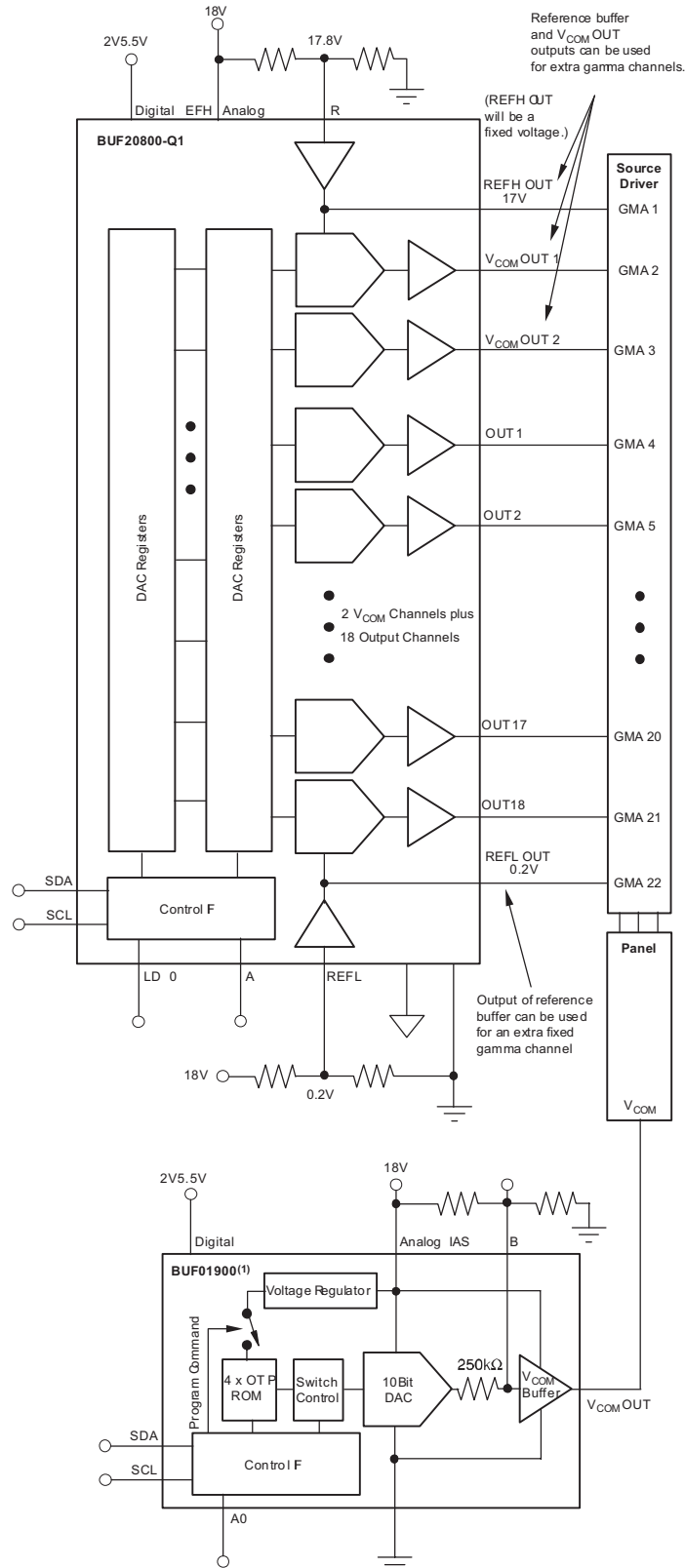
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Figure 17. 20 Gamma Channel Solution − Two V$_{COM}$ Channels Used as Additional Gamma Channels

8.2.5 Configuration for 22 Gamma Channels

In addition to the V$_{COM}$ outputs, the REFH and REFL OUT outputs can also be used as fixed gamma references. The output voltage will be set by the REFH and REFL input voltages, respectively. Therefore, REFH OUT should be used for the highest voltage gamma reference, and REFL OUT for the lowest voltage gamma reference. A 22-channel solution can be created by using all 18 outputs, the two V$_{COM}$ outputs, and both REFH/L OUT outputs for gamma references—see Figure 15. However, the REFH and REFL OUT buffers were designed to only drive light loads on the order of 5−10mA. Driving capacitive loads is not recommended with these buffers. In addition, the REFH and REFL buffers must not be allowed to saturate from sourcing/sinking too much current from REFH OUT or REFL OUT. Saturation of the REFH and REFL buffers results in errors in the voltages of OUT1−18 and V$_{COM}$ OUT1−2. The BUF01900 can be used to provide a programmable V$_{COM}$ output.

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Figure 18. 22-Channel Gamma Solution

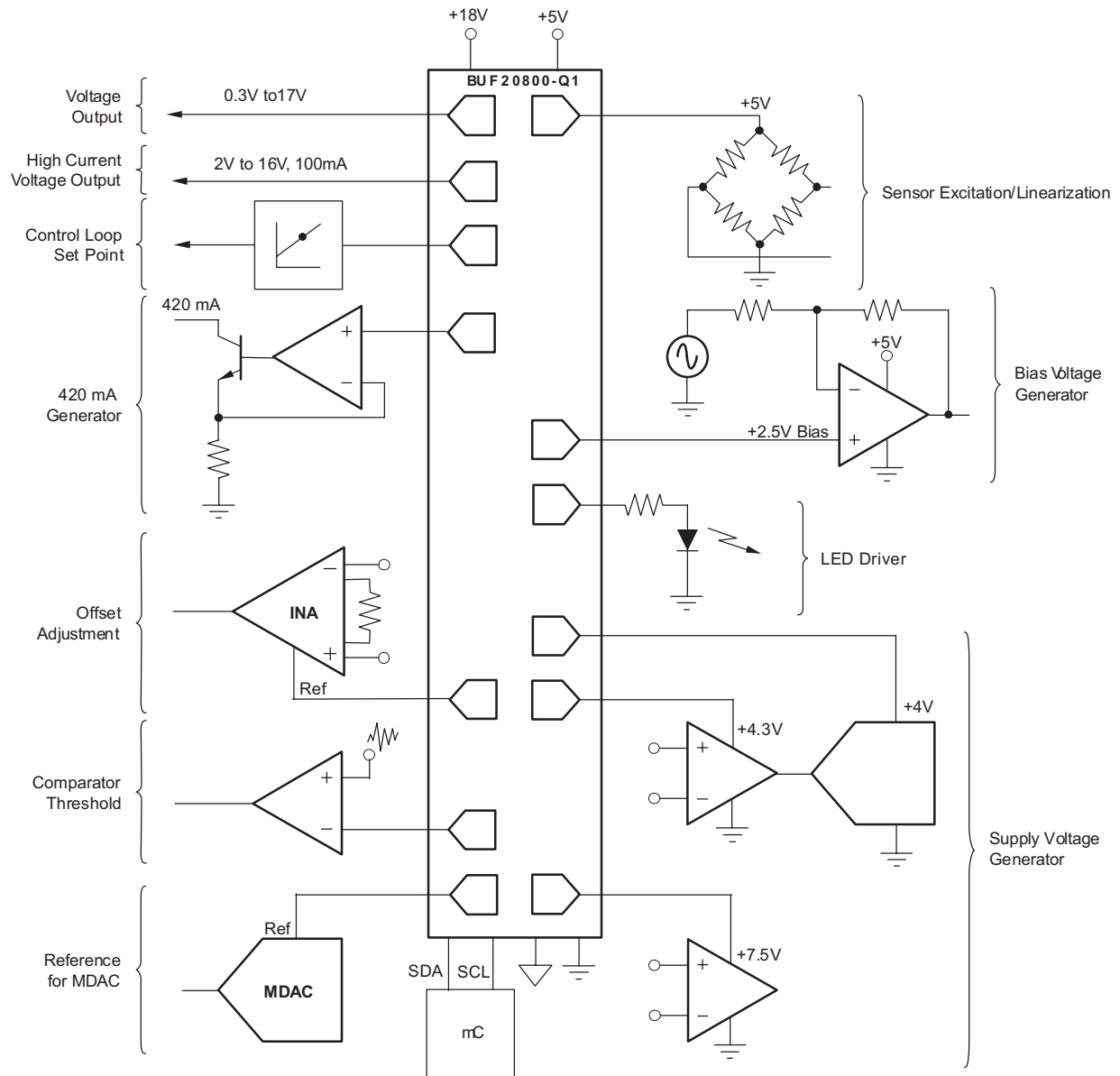### 8.2.6 The BUF20800-Q1 in Industrial Applications

The wide supply range, high output current, and very low cost make the BUF20800-Q1 attractive for a range of medium accuracy industrial applications such as programmable power supplies, multi-channel data-acquisition systems, data loggers, sensor excitation and linearization, power-supply generation, and other uses. Each DAC channel features 1LSB DNL and INL.

Many systems require different levels of biasing and power supply for various components as well as sensor excitation, control-loop set-points, voltage outputs, current outputs, and other functions. The BUF20800-Q1, with its 20 total programmable DAC channels, provides great flexibility to the entire system by allowing the designer to change all these parameters via software.

Figure 19 provides various ideas on how the BUF20800-Q1 can be used in applications. A micro-controller with two-wire serial interface controls the various DACs of the BUF20800-Q1. The BUF20800-Q1 can be used for:

- sensor excitation
- programmable bias/reference voltages
- variable power-supplies
- high-current voltage output
- 4-20mA output
- set-point generators for control loops

NOTE: The output voltages of the BUF20800-Q1 DACs will be set to (V_{REFH} − V_{REFL})/2 at power-up or reset.

Figure 19. Industrial Applications for the BUF20800-Q1

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8.2.7 Total TI Panel Solution

In addition to the BUF20800-Q1 programmable voltage reference, TI offers a complete set of ICs for the LCD panel market, including gamma correction buffers, various power-supply solutions, and audio power solutions. See Figure 20 for the total IC solution from TI.

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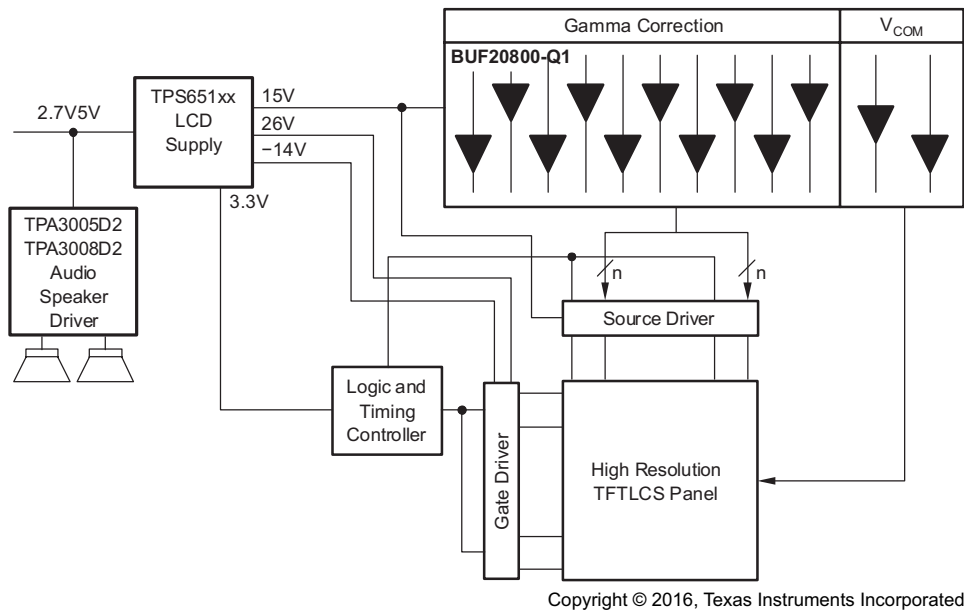
Figure 20. TI LCD Solution

9 Power Supply Recommendations

The device is designed to operate with an analog supply voltage from 7 V to 18 V, and a digital supply from 2 V to 5.5 V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. The analog and digital supplies must be well regulated and the input capacitances shown in the application circuit in Figure 14 are recommended for typical applications.

10 Layout

10.1 Layout Guidelines

10.1.1 General PowerPAD Design Considerations

The BUF20800-Q1 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, see Figure 21(a) and Figure 21(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 21(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

Layout Guidelines (continued)
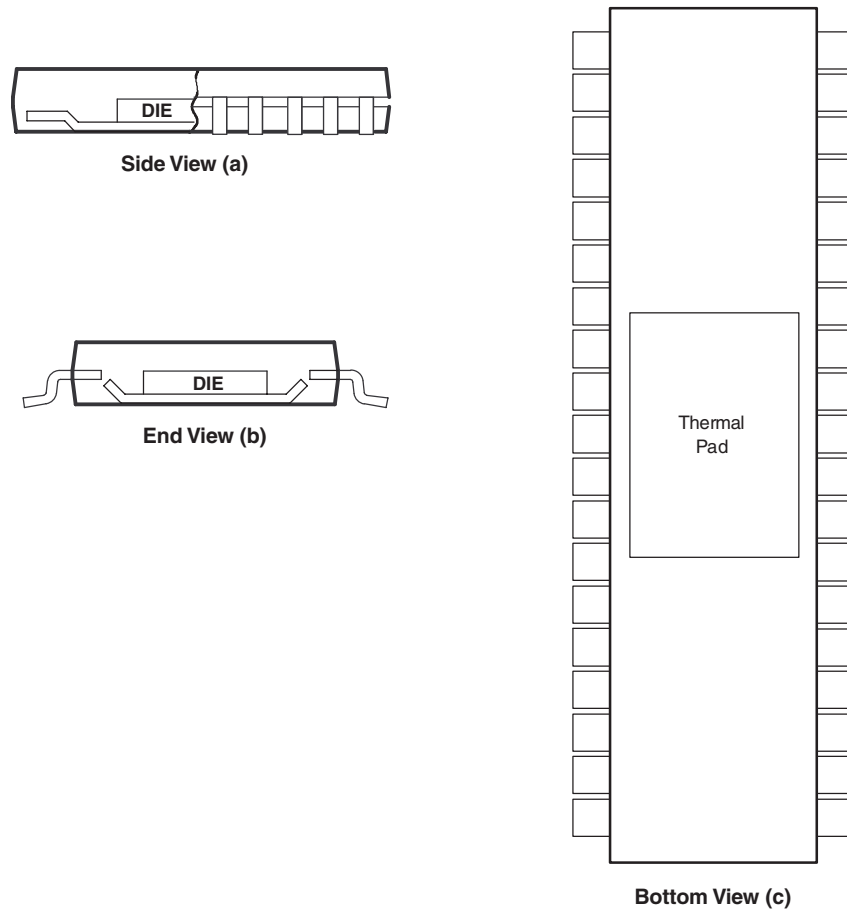
The thermal pad is electrically isolated from all terminals in the package.

Figure 21. Views of Thermally-Enhanced DCP Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. **Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation.** This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-38 DCP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An example thermal land pattern mechanical drawing is attached to the end of this data sheet.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF20800-Q1 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.

Layout Guidelines (continued)

5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF20800-Q1 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the BUF20800-Q1 IC is simply placed in position and run through the solder reflow operation as any standard surface mount component. This preparation results in a properly installed part.
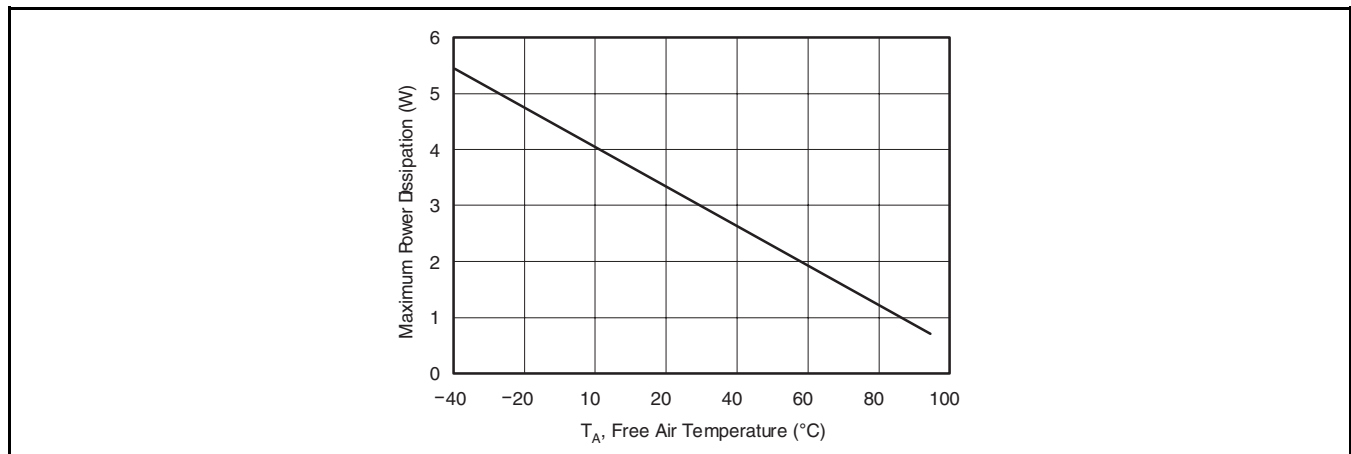
For a given θ_{JA} (listed in the Electrical Characteristics table), the maximum power dissipation is shown in Figure 22, and is calculated by Equation 3:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

where

- P_D = maximum power dissipation (W)
- T_{MAX} = absolute maximum junction temperature (+125°C)
- T_A = free-ambient air temperature (°C)　　　　　　　　　　　　　　　　　　　　　　　　　　　　(3)

**Figure 22. Maximum Power Dissipation
vs Free-Air Temperature
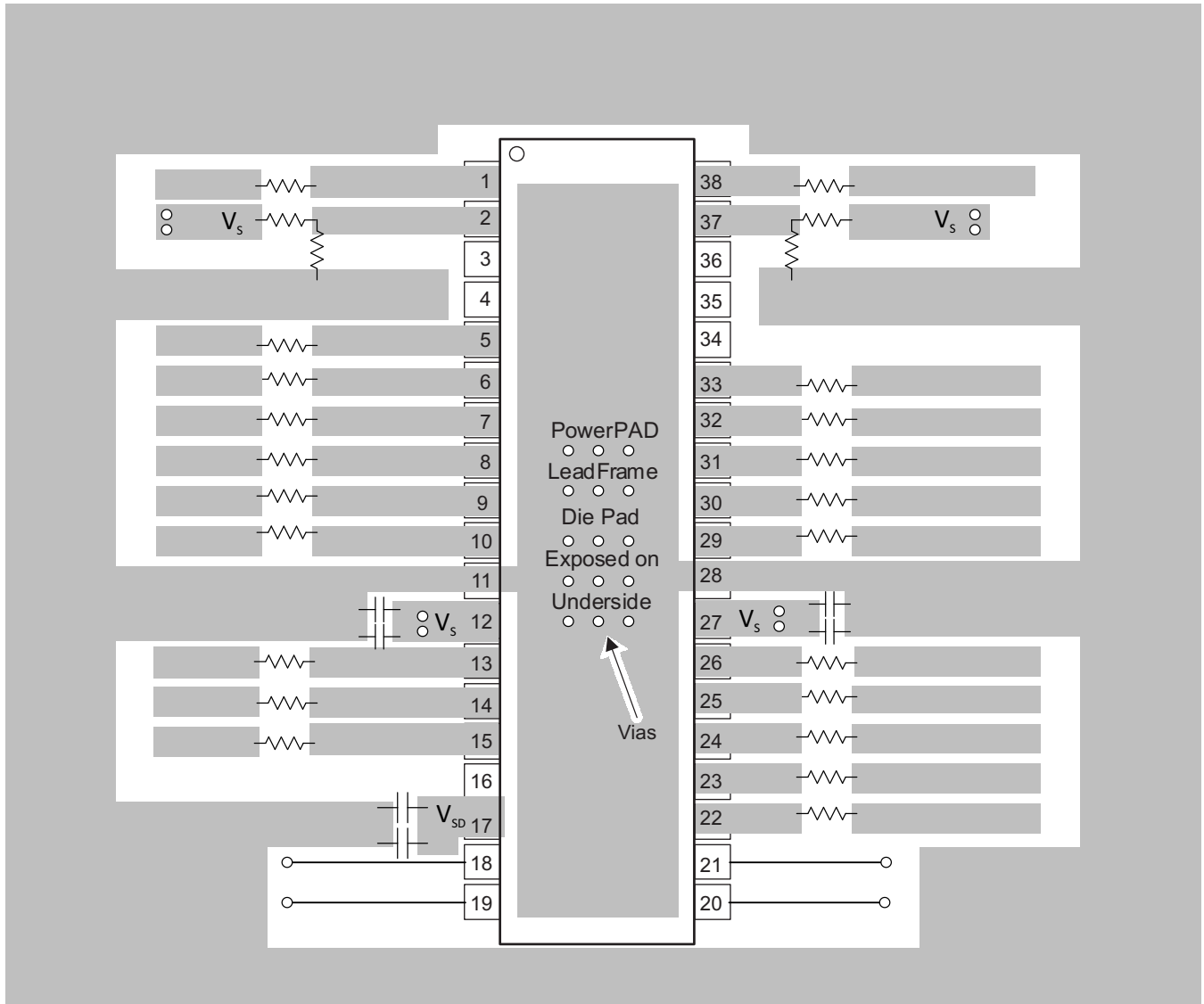(with PowerPAD soldered down)**

10.2 Layout Example

Figure 23. PCB Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 《PowerPAD 散热增强型封装》，SLMA002
- 《用伽马缓冲器驱动电容负载》，SBOA134

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表。*

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF20800ATDCPRQ1	ACTIVE	HTSSOP	DCP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	BUF20800Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF20800ATDCPRQ1	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF20800ATDCPRQ1	HTSSOP	DCP	38	2000	350.0	350.0	43.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
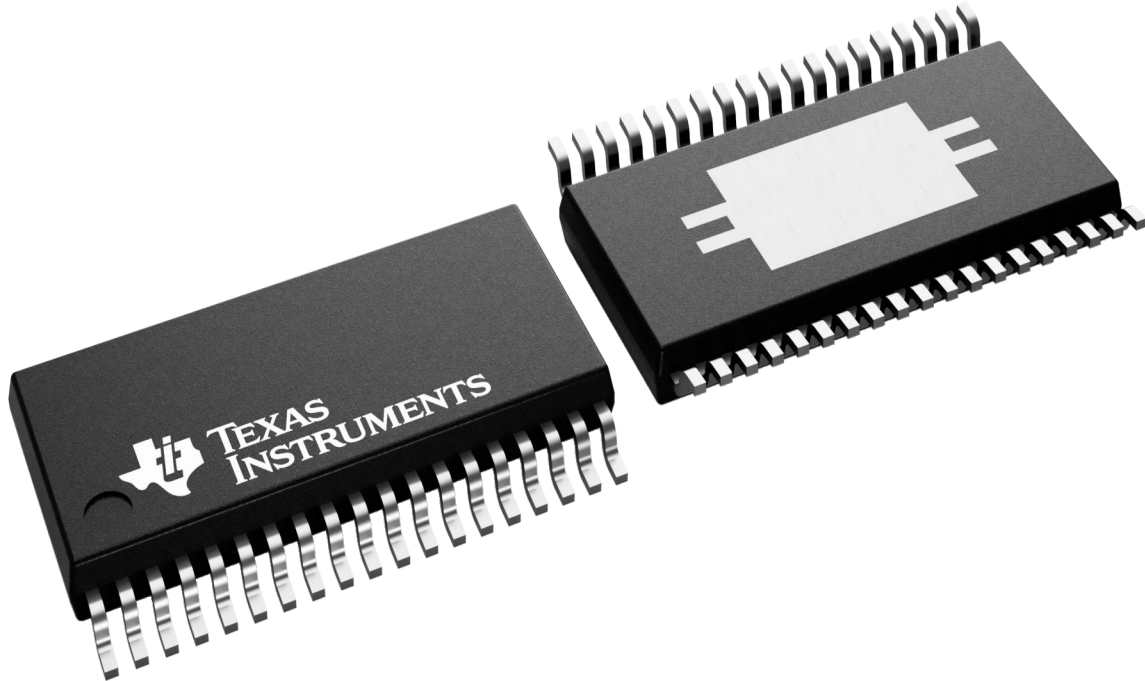
4224560/B
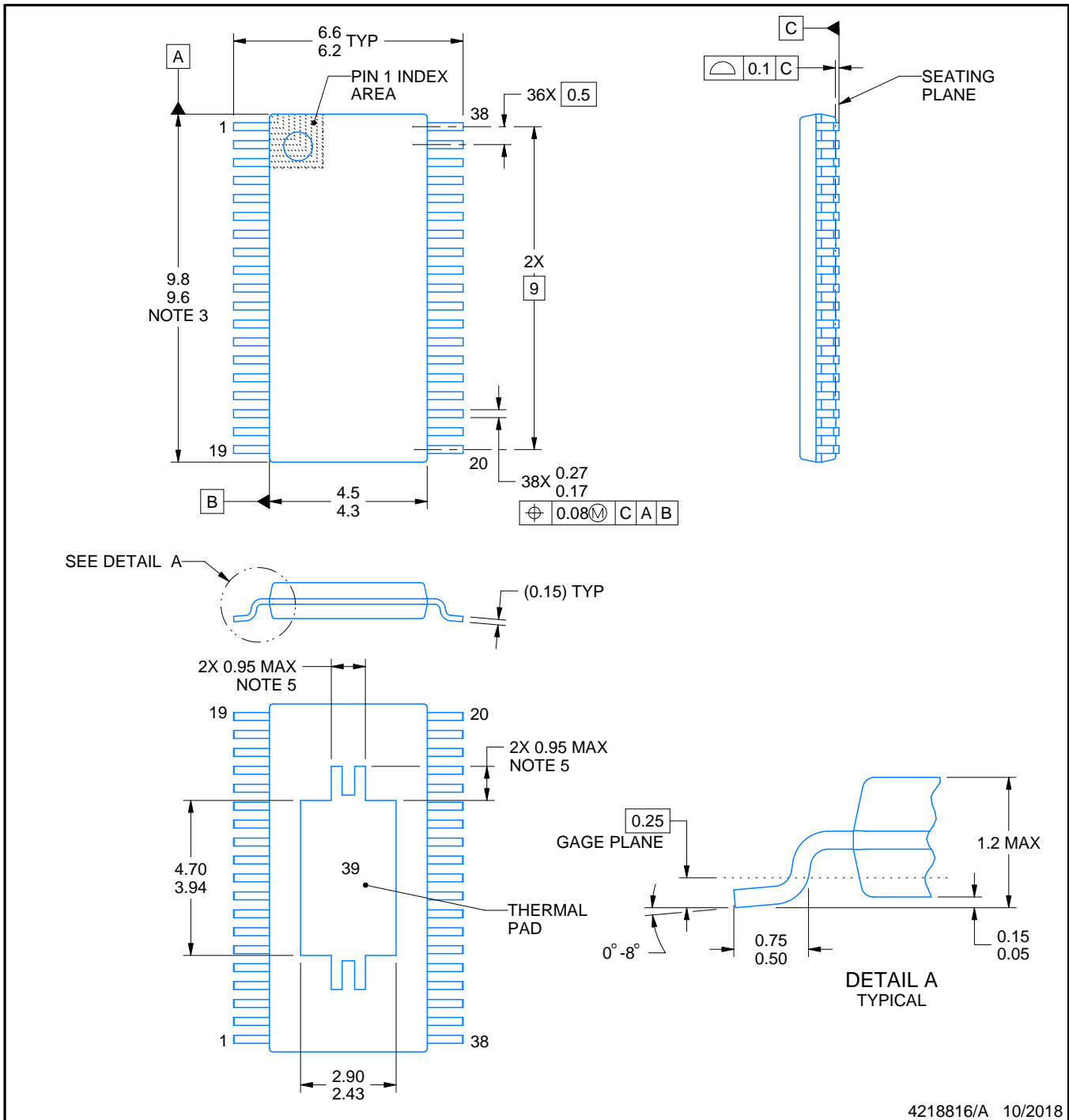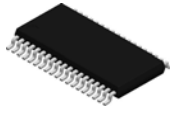
4218816/A   10/2018

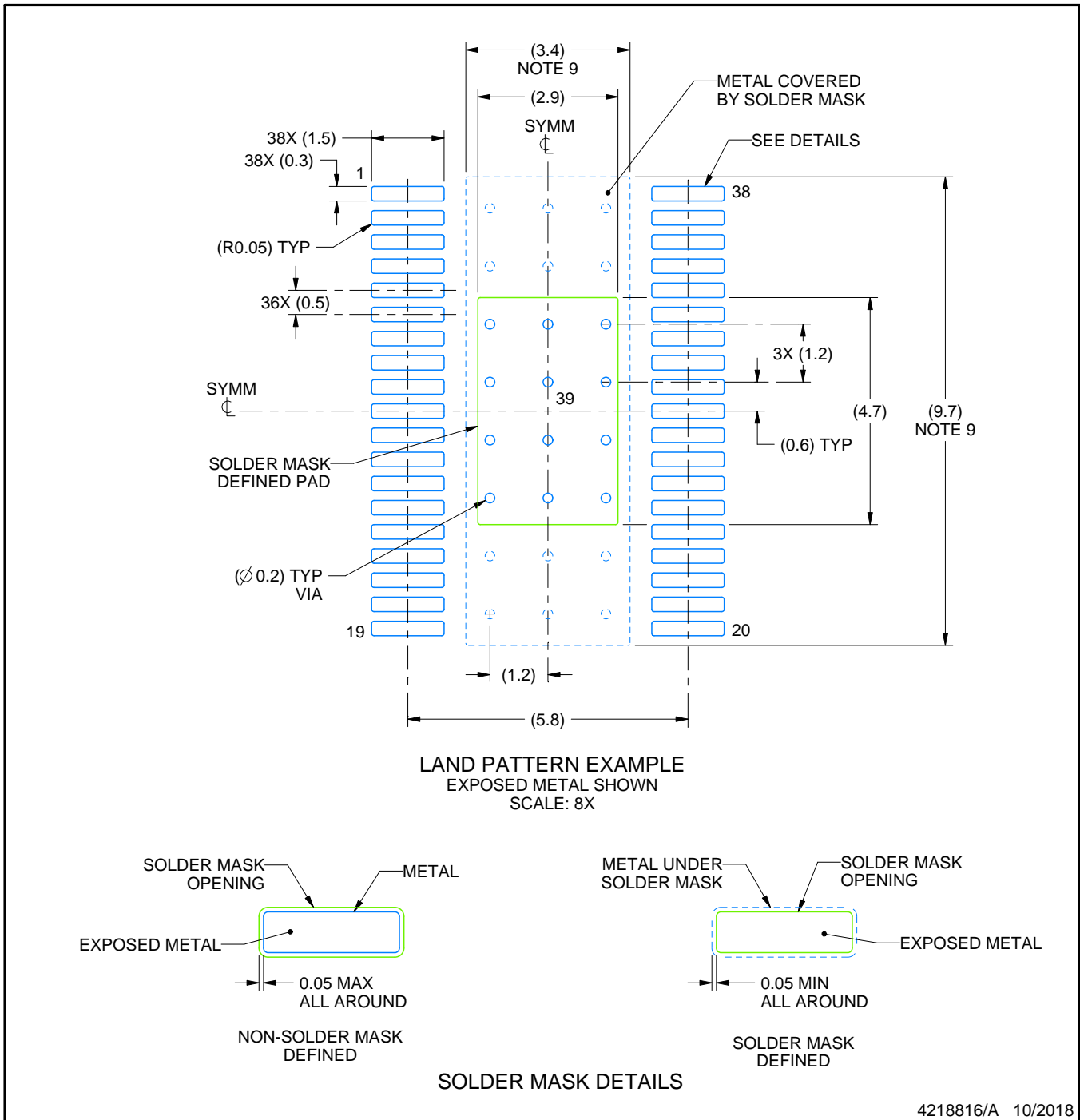PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

SOLDER MASK OPENING — METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED

METAL UNDER SOLDER MASK — SOLDER MASK OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
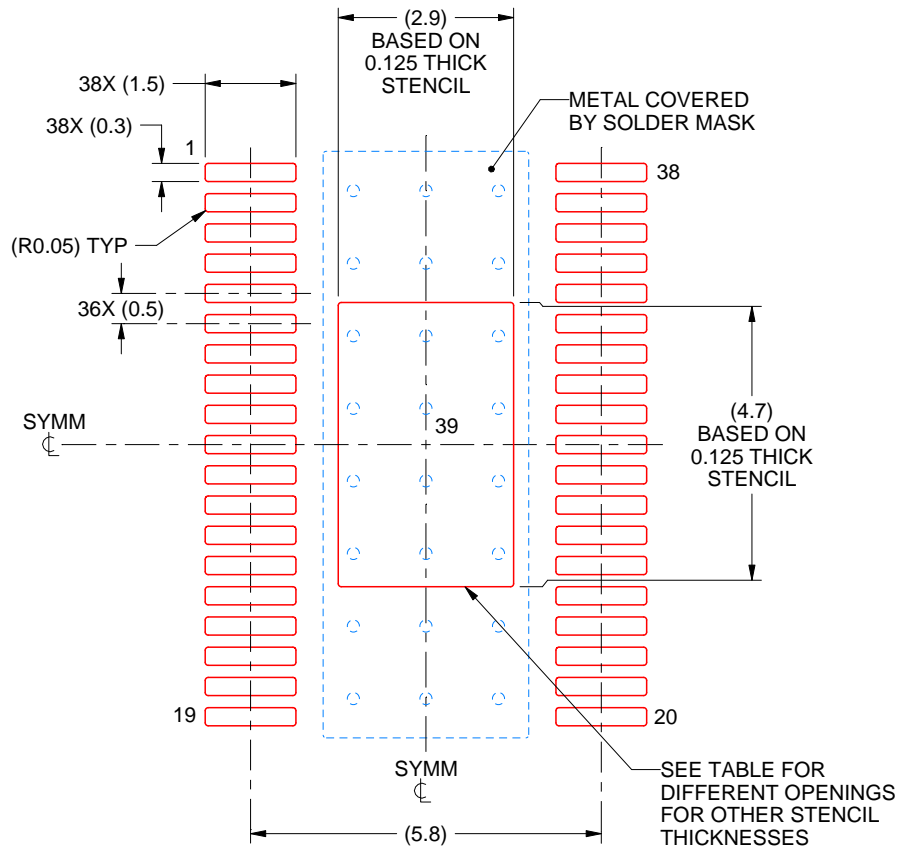
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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