CC2541-Q1 汽车用 SimpleLink™ 蓝牙®低能耗无线微控制器 (MCU)

1 器件概述

1.1 特性

- 射频
  - 2.4GHz 蓝牙低能耗专有 RF 无线 MCU
  - 支持 250kbps、500kbps、1Mbps 和 2Mbps 数据速率
  - 出色的链路预算，不使用外部前段而支持长距离应用
  - 高达 0dBm 的可编程输出功率
  - 出色的接收器灵敏度（1Mbps 时为 -94dBm）、可选择性和阻断性能
  - 适合于针对符合世界范围内的无线电频率调节系统：ETSI EN 300 328 和 EN 300 440 2 类 （欧洲），FCC CFR47 15 部分（美国），和 ARIB STD-T66（日本）
- 布局
  - 极少的外部组件
  - 6mm × 6mm 四方扁平无引线 (QFN)-40 封装
- 低功率
  - 有源模式 RX 低至：18.3mA
  - 有源模式 TX (0dBm)：18.6mA
  - 功率模式 1（4µs 唤醒）：270µs
  - 功率模式 2（睡眠定时器打开）：1µs
  - 功率模式 3（外部中断）：0.5µs
  - 宽电源电压范围（2V 至 3.6V）
- 微控制器
  - 具有代码预取功能的高性能和低功率 8051 微控制器内核
  - 256KB 系统内可编程闪存
  - 在所有功率模式下具有保持功能的 8KB RAM
  - 支持硬件调试
  - 扩展基带自动化，包括自动确认和地址解码
  - 所有功率模式中对所有相关寄存器的保持
- 外设
  - 功能强大的 5 通道直接内存访问 (DMA)
  - 红外 (IR) 生成电路
  - 通用定时器（1 个 16 位，2 个 8 位）
  - 具有捕捉功能的 32kHz 睡眠定时器
  - 精确数字接收到的数字信号强度指示器 (RSSI) 支持
  - 电池监视器和温度感应器
  - 含 8 通道和可配置分辨率的 12 位模数转换器 (ADC)
  - 高级加密标准 (AES) 安全协处理器
  - 2 个功能强大的支持几个串行协议的通用异步接收发器 (UART)
  - 23 个通用 I/O 引脚 (21 × 4mA，2 × 20mA)
  - I^2C 接口
  - 2 个具有 LED 驱动功能的 I/O 引脚
  - 安全装置定时器
  - 集成的高性能比较器
- 开发工具
  - CC2541 评估模块
  - SmartRF™ 软件
  - 提供 IAR 嵌入式 Workbench™
- 符合针对单模式蓝牙低能耗 (BLE) 解决方案的符合蓝牙4.0 协议的堆栈
  - 完全功率优化堆栈，包括控制器和主机
    - GAP - 中心设备，外设，或者广播器（包括组合角色）
    - 属性协议 (ATT) / 通用属性配置文件 (GATT) – 客户端和服务器
    - 对称式对多重处理 (SMP) - AES-128 加密和解密
    - L2CAP
  - 示例应用和配置文件
    - 针对 GAP 中心和外围作用的一般应用
    - 距离临近，加速计，简单关键字，和电池 GATT 服务
    - BLE 软件栈内支持更多应用
  - 多重配置选项
    - 单芯片配置，允许应用运行在 CC2541 上-Q1：
    - 针对外部微处理器上运行应用的网络处理器接口
  - BTool - 用于评估、开发和测试的 Windows PC 应用
  - 支持空中下载更新

1.2 应用

- 2.4GHz 蓝牙低能耗系统
- 专有 2.4GHz 系统
- 遥控门锁（被动式遥感）
- 轮胎气压监视
- 接近传感
- 接口和控制
- 诊断和维护
- 电缆更换
- 传感器节点
- 信息娱乐与媒体
- 智能手机连接
- 信标

1.3 说明

CC2541-Q1 是一款针对蓝牙低功耗和专有 2.4GHz 应用的功耗优化型无线 MCU 解决方案。 此器件可构建稳定耐用的网络节点，同时保证总物料成本低廉。 CC2541-Q1 结合了领先的 RF 收发器的出色性能以及符合行业标准的增强型 8051 MCU、系统内可编程闪存、8KB RAM 和多种其它功能强大的特性和外设。 CC2541-Q1 非常适用于需要超低功耗的系统，具体由各种工作模式指定。 运行模式间较短的转换时间进一步使低能耗变为可能。

CC2541-Q1 采用 6mm x 6mm QFN40 封装。

器件信息(1)

部件号	封装	封装尺寸
CC2541F256TRHARQ1	RHA (40)	6.00mm x 6.00mm
CC2541F256TRHATQ1	RHA (40)	6.00mm x 6.00mm

(1) 更多信息请参见 节 8，机械封装和可订购信息。

1.4 功能方框图

图 1-1 所示为 CC2541-Q1 框图。

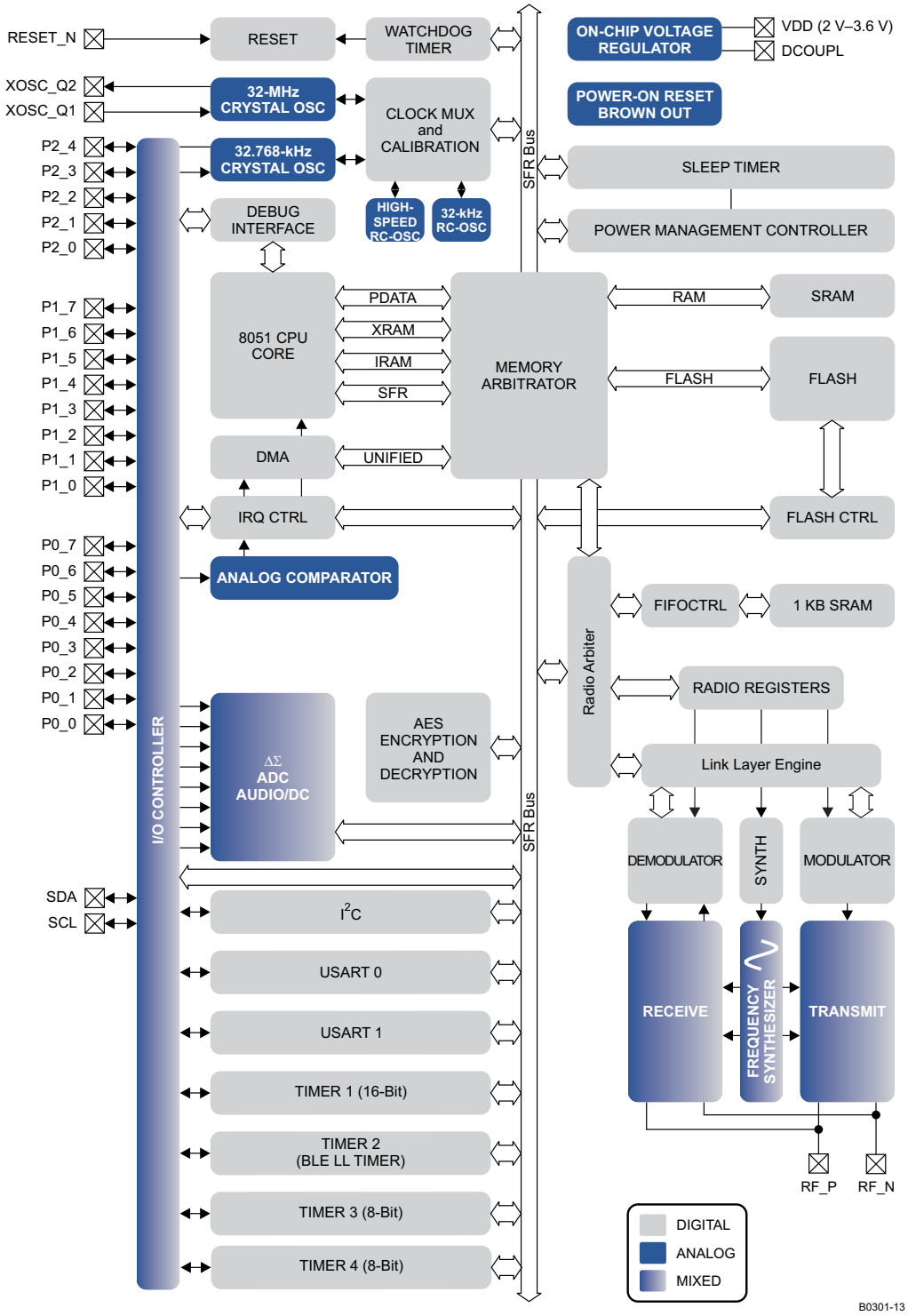


图 **1-1.** 方框图

内容

2 修订历史记录

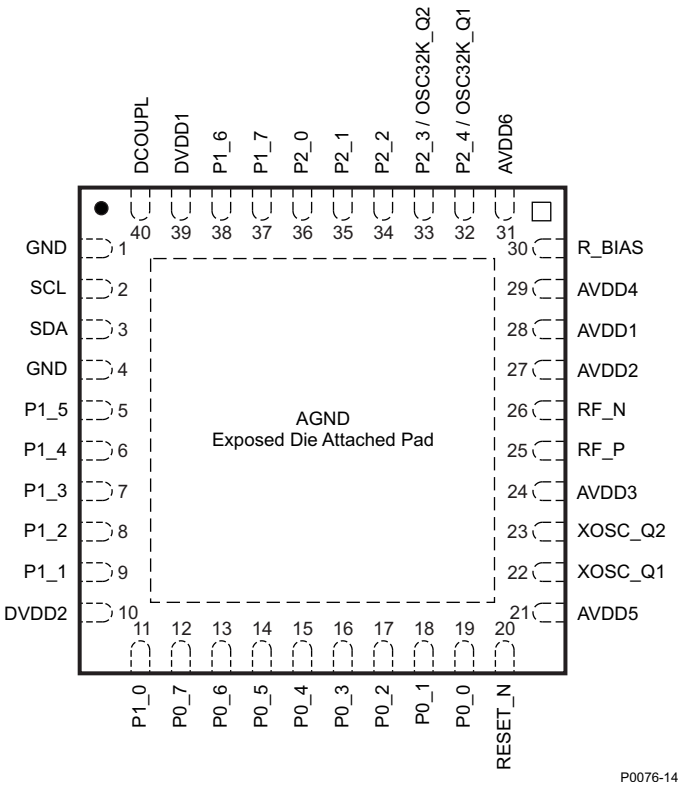
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

日期	修订版本	注释
2014 年 6 月	*	最初发布。

3 Terminal Configuration and Functions

The CC2541-Q1 pinout is shown in Figure 3-1 and a short description of the pins follows.

3.1 Pin Diagram



NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 3-1. RHA PACKAGE (TOP VIEW)

3.2 Pin Descriptions

Table 3-1. Pin Descriptions

PINS		TYPE	DESCRIPTION
NAME	NO.		
AVDD1	28	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD2	27	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD3	24	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD4	29	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD5	21	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD6	31	Power (analog)	2-V–3.6-V analog power-supply connection
DCOUPL	40	Power (digital)	1.8-V digital power-supply decoupling. Do not use for supplying external circuits.
DVDD1	39	Power (digital)	2-V–3.6-V digital power-supply connection
DVDD2	10	Power (digital)	2-V–3.6-V digital power-supply connection
GND	1	Ground pin	Connect to GND
GND	—	Ground	The ground pad must be connected to a solid ground plane.
GND	4	Ground pin	Connect to GND
P0_0	19	Digital I/O	Port 0.0
P0_1	18	Digital I/O	Port 0.1
P0_2	17	Digital I/O	Port 0.2
P0_3	16	Digital I/O	Port 0.3
P0_4	15	Digital I/O	Port 0.4
P0_5	14	Digital I/O	Port 0.5
P0_6	13	Digital I/O	Port 0.6
P0_7	12	Digital I/O	Port 0.7
P1_0	11	Digital I/O	Port 1.0 – 20-mA drive capability
P1_1	9	Digital I/O	Port 1.1 – 20-mA drive capability
P1_2	8	Digital I/O	Port 1.2
P1_3	7	Digital I/O	Port 1.3
P1_4	6	Digital I/O	Port 1.4
P1_5	5	Digital I/O	Port 1.5
P1_6	38	Digital I/O	Port 1.6
P1_7	37	Digital I/O	Port 1.7
P2_0	36	Digital I/O	Port 2.0
P2_1/DD	35	Digital I/O	Port 2.1 / debug data
P2_2/DC	34	Digital I/O	Port 2.2 / debug clock
P2_3/ OSC32K_Q2	33	Digital I/O, Analog I/O	Port 2.3/32.768 kHz XOSC
P2_4/ OSC32K_Q1	32	Digital I/O, Analog I/O	Port 2.4/32.768 kHz XOSC
RBIAS	30	Analog I/O	External precision bias resistor for reference current
RESET_N	20	Digital input	Reset, active-low
RF_N	26	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	25	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
SCL	2	I^2C clock or digital I/O	Can be used as I^2C clock pin or digital I/O. Leave floating if not used. If grounded disable pull up
SDA	3	I^2C clock or digital I/O	Can be used as I^2C data pin or digital I/O. Leave floating if not used. If grounded disable pull up
XOSC_Q1	22	Analog I/O	32-MHz crystal oscillator pin 1 or external clock input
XOSC_Q2	23	Analog I/O	32-MHz crystal oscillator pin 2

4 Specifications

4.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	VDD + 0.3 ≤ 3.9	V
Input RF level			10	dBm

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–40	125	°C
V_{ESD}	Electrostatic discharge (ESD) performance:	Human Body Model (HBM), per AEC Q100-002(1)	All pins	–1	1	kV
			All pins (Excluding pins 25 and 26)	–2	2	
		Charged Device Model (CDM), per AEC Q100-011		–500	500	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating ambient temperature range, T_A	–40		105	°C
Operating supply voltage	2		3.6	V

4.4 Thermal Characteristics for RHA Package

NAME	DESCRIPTION	°C/W	AIR FLOW (m/s)(1)
$R\Theta_{JC}$	Junction-to-case (top)	16.1	0.00
$R\Theta_{JB}$	Junction-to-board	5.5	0.00
$R\Theta_{JA}$	Junction-to-free air	30.6	0.00
Psi_{JT}	Junction-to-package top	0.2	0.00
Psi_{JB}	Junction-to-board	5.4	0.00
$R\theta_{JC}$	Junction-to-case (bottom)	1.0	0.00

(1) m/s = meters per second

4.5 Electrical Characteristics

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V, 1 Mbps, GFSK, 250-kHz deviation, ***Bluetooth*** low energy mode, and 0.1% BER

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	RX mode, standard mode, no peripherals active, low MCU activity		18.3		mA
		RX mode, high-gain mode, no peripherals active, low MCU activity		20.8		
		TX mode, –20 dBm output power, no peripherals active, low MCU activity		17.2		
		TX mode, 0 dBm output power, no peripherals active, low MCU activity		18.6		
		Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		270		µA
		Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		1		
		Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.5		
		Low MCU activity: 32-MHz XOSC running. No radio or peripherals. Limited flash access, no RAM access.		6.7		mA
I_{peri}	Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated)	Timer 1. Timer running, 32-MHz XOSC used		90		µA
		Timer 2. Timer running, 32-MHz XOSC used		90		
		Timer 3. Timer running, 32-MHz XOSC used		60		
		Timer 4. Timer running, 32-MHz XOSC used		70		
		Sleep timer, including 32.753-kHz RCOSC		0.6		
		ADC, when converting		1.2		mA

4.6 General Characteristics

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC		4		µs
Power mode 2 or 3 → Active	Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC		120		µs
Active → TX or RX	Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF		500		µs
	With 32-MHz XOSC initially on		180		µs
RX/TX turnaround	Proprietary auto mode		130		µs
	BLE mode		150		
RADIO PART					
RF frequency range	Programmable in 1-MHz steps	2379		2496	MHz
Data rate and modulation format	2 Mbps, GFSK, 500-kHz deviation 2 Mbps, GFSK, 320-kHz deviation 1 Mbps, GFSK, 250-kHz deviation 1 Mbps, GFSK, 160-kHz deviation 500 kbps, MSK 250 kbps, GFSK, 160-kHz deviation 250 kbps, MSK				

4.7 RF Receive Section

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C, VDD = 3 V, f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps, GFSK, 250-kHz Deviation, *Bluetooth* low energy Mode, 0.1% BER					
Receiver sensitivity(1)(2)	High-gain mode		–94		dBm
	Standard mode		–88		
Saturation(2)	BER < 0.1%		5		dBm
Co-channel rejection(2)	Wanted signal –67 dBm		–6		dB
In-band blocking rejection(2)	±1 MHz offset, 0.1% BER, wanted signal –67 dBm		–2		dB
	±2 MHz offset, 0.1% BER, wanted signal –67 dBm		26		
	±3 MHz offset, 0.1% BER, wanted signal –67 dBm		34		
	>6 MHz offset, 0.1% BER, wanted signal –67 dBm		33		
Out-of-band blocking rejection(2)	Minimum interferer level < 2 GHz (Wanted signal –67 dBm)		–21		dBm
	Minimum interferer level [2 GHz, 3 GHz] (Wanted signal –67 dBm)		–27		
	Minimum interferer level > 3 GHz (Wanted signal –67 dBm)		–8		
Intermodulation(2)	Minimum interferer level		–36		dBm
Frequency error tolerance(3)	Including both initial tolerance and drift. Sensitivity better than -67dBm, 250 byte payload. BER 0.1%	–250		250	kHz
Symbol rate error tolerance(4)	Maximum packet length. Sensitivity better than –67 dBm, 250 byte payload. BER 0.1%	–80		80	ppm
ALL RATES/FORMATS					
Spurious emission in RX. Conducted measurement	f < 1 GHz		–67		dBm
Spurious emission in RX. Conducted measurement	f > 1 GHz		–57		dBm

(1) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.
(2) Results based on standard-gain mode.
(3) Difference between center frequency of the received RF signal and local oscillator frequency
(4) Difference between incoming symbol rate and the internally generated symbol rate

4.8 RF Transmit Section

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting		0		dBm
	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		–20		
Programmable output power range	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		20		dB
Spurious emission conducted measurement	f < 1 GHz		–52		dBm
	f > 1 GHz		–48		dBm
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				
Optimum load impedance	Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna		70 +j30		Ω

Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

4.9 32-MHz Crystal Oscillator

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32		MHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance		6		60	Ω
C_0	Crystal shunt capacitance		1		7	pF
C_L	Crystal load capacitance		10		16	pF
	Start-up time			0.25		ms
	Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by [1]

4.10 32.768-kHz Crystal Oscillator

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32.768		kHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance			40	130	kΩ
C_0	Crystal shunt capacitance			0.9	2	pF
C_L	Crystal load capacitance			12	16	pF
	Start-up time			0.4		s

(1) Including aging and temperature dependency, as specified by [1]

4.11 32-kHz RC Oscillator

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient(2)			0.4		%/°C
Supply-voltage coefficient(3)			3		%/V
Calibration time(4)			2		ms

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.
(2) Frequency drift when temperature changes after calibration
(3) Frequency drift when supply voltage changes after calibration
(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC32K_CALDIS is set to 0.

4.12 16-MHz RC Oscillator

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency(1)			16		MHz
Uncalibrated frequency accuracy			±18%		
Calibrated frequency accuracy			±0.6%		
Start-up time			10		µs
Initial calibration time(2)			50		µs

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.
(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC_PD is set to 0.

4.13 RSSI Characteristics

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Useful RSSI range(1)	Reduced gain by AGC algorithm		64		dB
	High gain by AGC algorithm		64		
RSSI offset(1)	Reduced gain by AGC algorithm		79		dBm
	High gain by AGC algorithm		99		
Absolute uncalibrated accuracy(1)			±6		dB
Step size (LSB value)			1		dB
All Other Rates/Formats					
Useful RSSI range(1)	Standard mode		64		dB
	High-gain mode		64		
RSSI offset(1)	Standard mode		98		dBm
	High-gain mode		107		
Absolute uncalibrated accuracy(1)			±3		dB
Step size (LSB value)			1		dB

(1) Assuming CC2541-Q1 EM reference design. Other RF designs give an offset from the reported value.

4.14 Frequency Synthesizer Characteristics

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1-MHz offset from carrier		–109		dBc/Hz
	At ±3-MHz offset from carrier		–112		
	At ±5-MHz offset from carrier		–119		

4.15 Analog Temperature Sensor

Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output	Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution		1480		12-bit
Temperature coefficient			4.5		/ 1°C
Voltage coefficient			1		0.1 V
Initial accuracy without calibration			±10		°C
Accuracy using 1-point calibration			±5		°C
Current consumption when enabled			0.5		mA

4.16 Comparator Characteristics

T_A = 25°C, VDD = 3 V. All measurement results are obtained using the CC2541-Q1 reference designs, post-calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode maximum voltage			VDD		V
Common-mode minimum voltage			–0.3		
Input offset voltage			1		mV
Offset vs temperature			16		µV/°C
Offset vs operating voltage			4		mV/V
Supply current			230		nA
Hysteresis			0.15		mV

4.17 ADC Characteristics

T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage differential	VDD is voltage on AVDD5 pin	0		VDD	V
	Input resistance, signal	Simulated using 4-MHz clock speed		197		kΩ
	Full-scale signal(1)	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB(1)	Effective number of bits	Single-ended input, 7-bit setting		5.7		bits
		Single-ended input, 9-bit setting		7.5		
		Single-ended input, 10-bit setting		9.3		
		Single-ended input, 12-bit setting		10.3		
		Differential input, 7-bit setting		6.5		
		Differential input, 9-bit setting		8.3		
		Differential input, 10-bit setting		10		
		Differential input, 12-bit setting		11.5		
		10-bit setting, clocked by RCOSC		9.7		
		12-bit setting, clocked by RCOSC		10.9		
	Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD	Total harmonic distortion	Single ended input, 12-bit setting, –6 dBFS(1)		–75.2		dB
		Differential input, 12-bit setting, –6 dBFS(1)		–86.6		
	Signal to nonharmonic ratio	Single-ended input, 12-bit setting(1)		70.2		dB
		Differential input, 12-bit setting(1)		79.3		
		Single-ended input, 12-bit setting, –6 dBFS(1)		78.8		
		Differential input, 12-bit setting, –6 dBFS(1)		88.9		
CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Crosstalk	Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Offset	Midscale		–3		mV
	Gain error			0.68%		
DNL	Differential nonlinearity	12-bit setting, mean(1)		0.05		LSB
		12-bit setting, maximum(1)		0.9		
INL	Integral nonlinearity	12-bit setting, mean(1)		4.6		LSB
		12-bit setting, maximum(1)		13.3		
		12-bit setting, mean, clocked by RCOSC		10		
		12-bit setting, max, clocked by RCOSC		29		
SINAD (–THD+N)	Signal-to-noise-and-distortion	Single ended input, 7-bit setting(1)		35.4		dB
		Single ended input, 9-bit setting(1)		46.8		
		Single ended input, 10-bit setting(1)		57.5		
		Single ended input, 12-bit setting(1)		66.6		
		Differential input, 7-bit setting(1)		40.7		
		Differential input, 9-bit setting(1)		51.6		
		Differential input, 10-bit setting(1)		61.8		
		Differential input, 12-bit setting(1)		70.8		
	Conversion time	7-bit setting		20		µs
		9-bit setting		36		
		10-bit setting		68		
		12-bit setting		132		

(1) Measured with 300-Hz sine-wave input and VDD as reference.

ADC Characteristics *(continued)*

T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power consumption			1.2		mA
Internal reference VDD coefficient			4		mV/V
Internal reference temperature coefficient			0.4		mV/10°C
Internal reference voltage			1.24		V

4.18 DC Characteristics

T_A = 25°C, VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	–50		50	nA
Logic-1 input current	Input equals VDD	–50		50	nA
I/O-pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage, 4- mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4-mA pins	Output load 4 mA	2.5			V
Logic-0 output voltage, 20- mA pins	Output load 20 mA			0.5	V
Logic-1 output voltage, 20-mA pins	Output load 20 mA	2.5			V

4.19 Control Input AC Characteristics

T_A = –40°C to 105°C, VDD = 2 V to 3.6 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} $t_{SYSCLK} = 1/ f_{SYSCLK}$	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration	See item 1, Figure 4-1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip.	1			µs
Interrupt pulse duration	See item 2, Figure 4-1.This is the shortest pulse that is recognized as an interrupt request.	20			ns

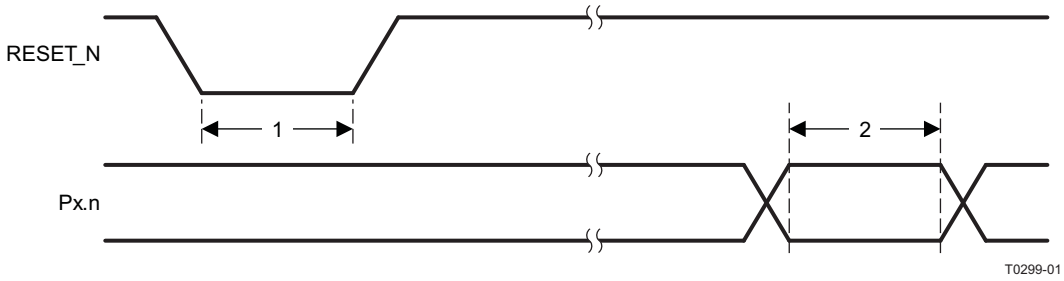


Figure 4-1. Control Input AC Characteristics

4.20 SPI AC Characteristics

T_A = –40°C to 105°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SCK period	Master, RX and TX	250			ns
		Slave, RX and TX	250			
	SCK duty cycle	Master		50%		
t_2	SSN low to SCK	Master	63			ns
		Slave	63			
t_3	SCK to SSN high	Master	63			ns
		Slave	63			
t_4	MOSI early out	Master, load = 10 pF			7	ns
t_5	MOSI late out	Master, load = 10 pF			10	ns
t_6	MISO setup	Master	90			ns
t_7	MISO hold	Master	10			ns
	SCK duty cycle	Slave		50%		ns
t_{10}	MOSI setup	Slave	35			ns
t_{11}	MOSI hold	Slave	10			ns
t_9	MISO late out	Slave, load = 10 pF			95	ns
	Operating frequency	Master, TX only			8	MHz
		Master, RX and TX			4	
		Slave, RX only			8	
		Slave, RX and TX			4	

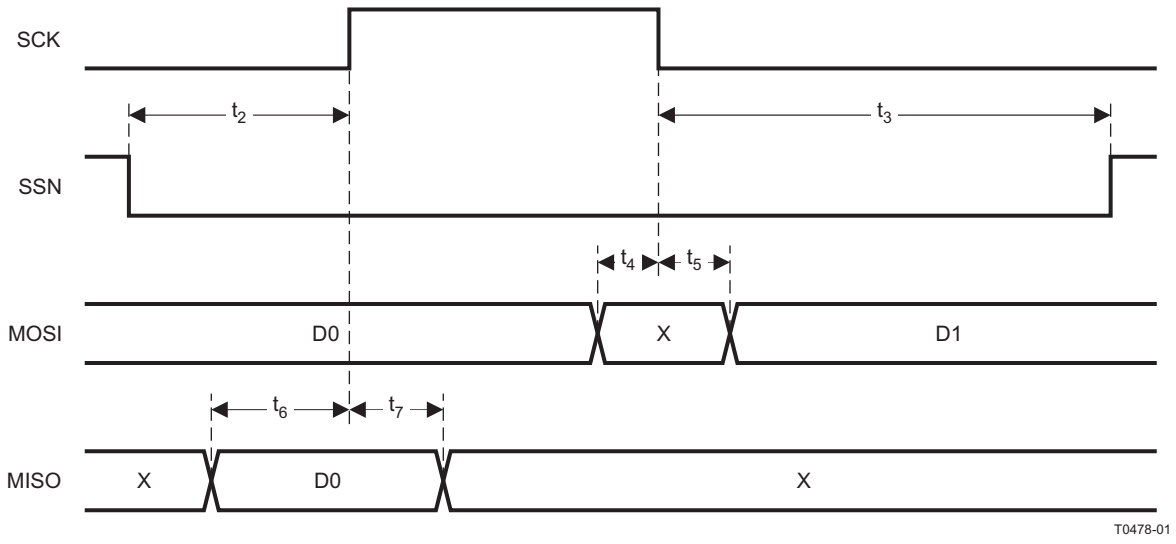


Figure 4-2. SPI Master AC Characteristics

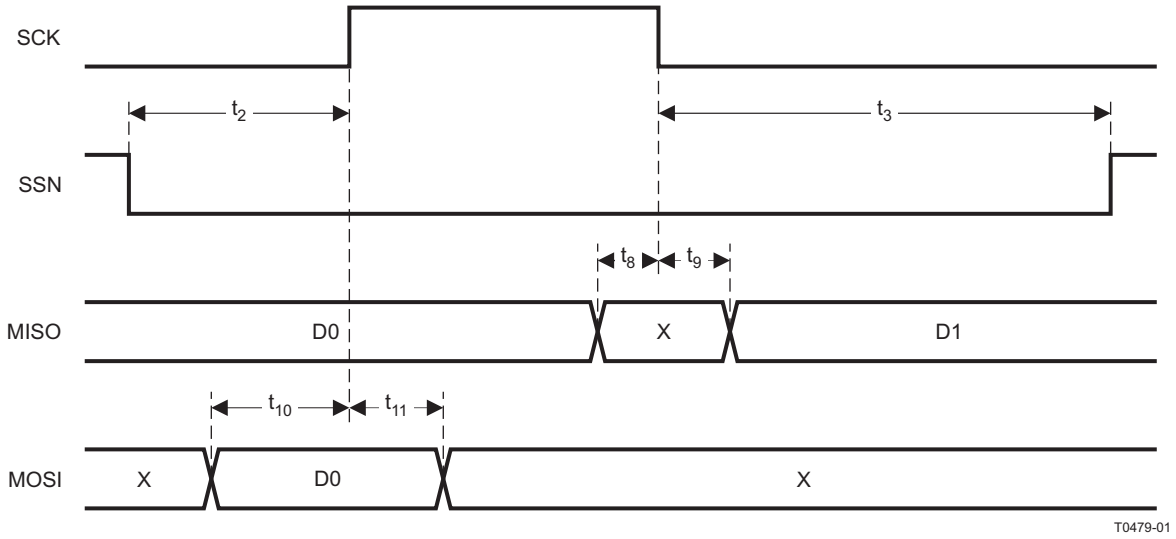


Figure 4-3. SPI Slave AC Characteristics

4.21 Debug Interface AC Characteristics

T_A = –40°C to 105°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock frequency (see Figure 4-4)				12	MHz
t_1	Allowed high pulse on clock (see Figure 4-4)		35			ns
t_2	Allowed low pulse on clock (see Figure 4-4)		35			ns
t_3	EXT_RESET_N low to first falling edge on debug clock (see Figure 4-6)		167			ns
t_4	Falling edge on clock to EXT_RESET_N high (see Figure 4-6)		83			ns
t_5	EXT_RESET_N high to first debug command (see Figure 4-6)		83			ns
t_6	Debug data setup (see Figure 4-5)		2			ns
t_7	Debug data hold (see Figure 4-5)		4			ns
t_8	Clock-to-data delay (see Figure 4-5)	Load = 10 pF			30	ns

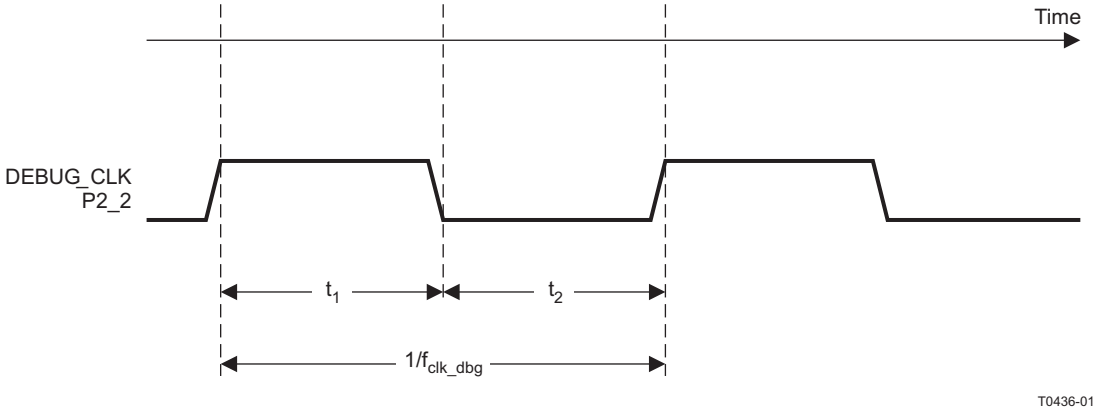


Figure 4-4. Debug Clock – Basic Timing

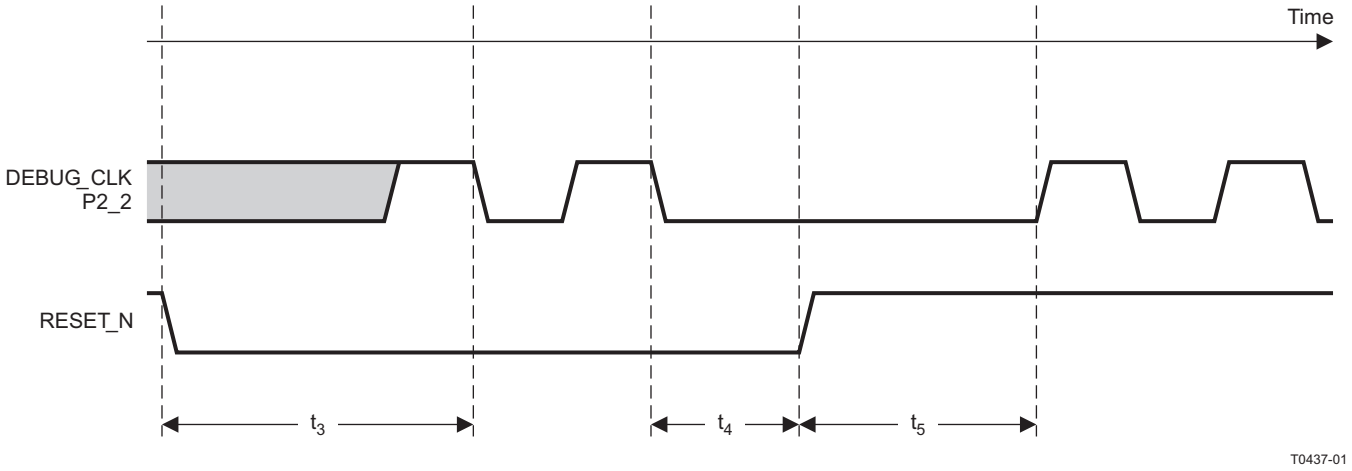


Figure 4-5. Debug Enable Timing

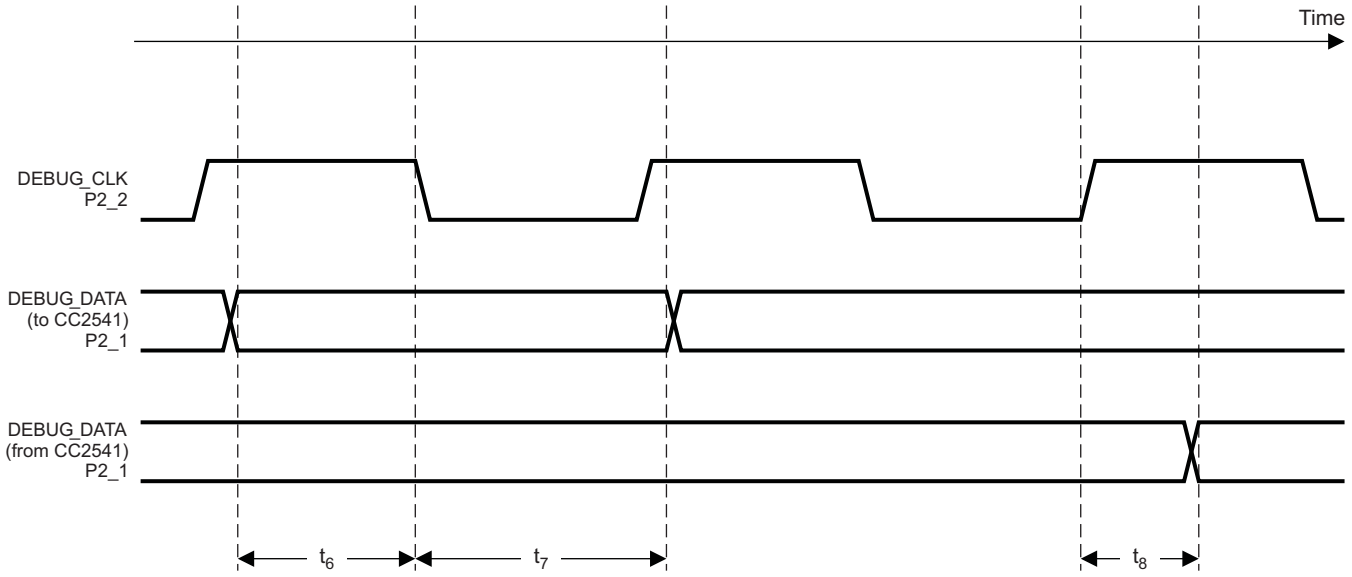


Figure 4-6. Data Setup and Hold Timing

4.22 Timer Inputs AC Characteristics

T_A = –40°C to 105°C, VDD = 2 V to 3.6 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz).	1.5			t_{SYSCLK}

4.23 Typical Characteristics

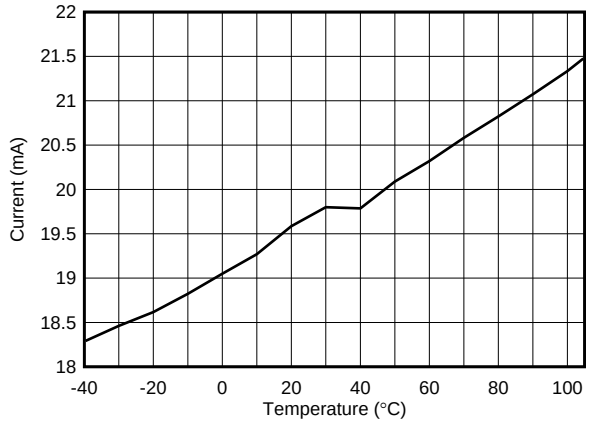


Figure 4-7. RX Current vs Temperature

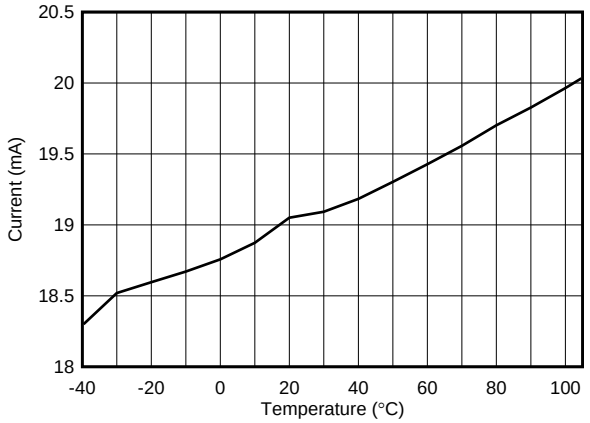


Figure 4-8. TX Current vs Temperature

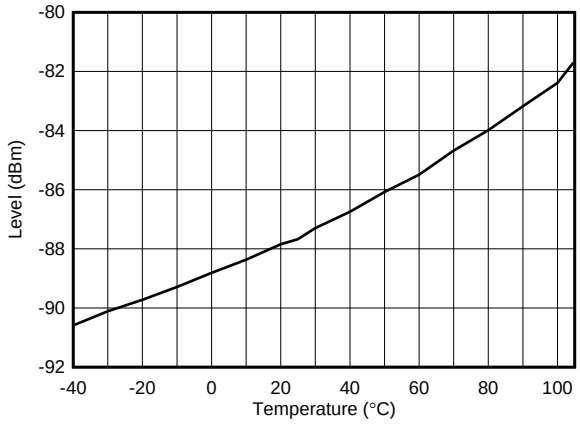


Figure 4-9. RX Sensitivity vs Temperature

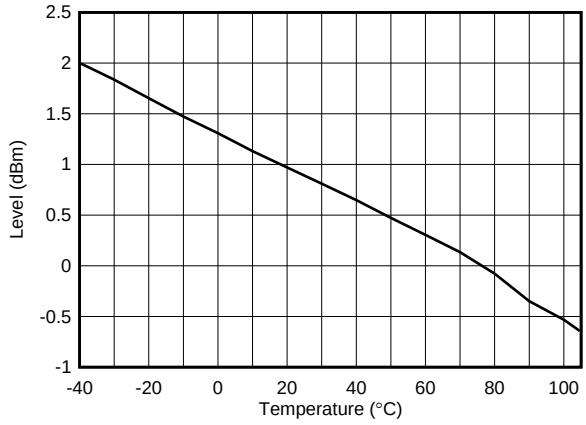


Figure 4-10. TX Power vs Temperature

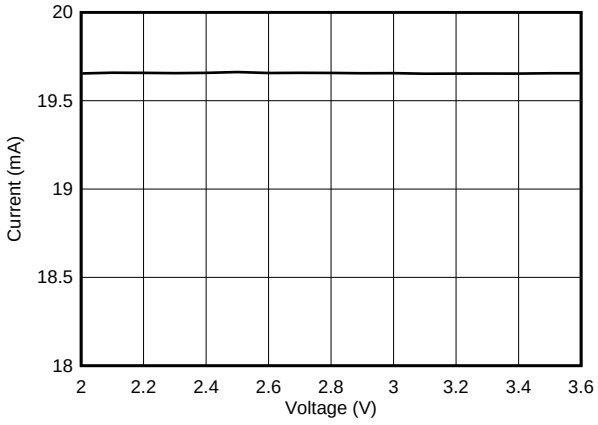


Figure 4-11. RX Current vs Supply Voltage

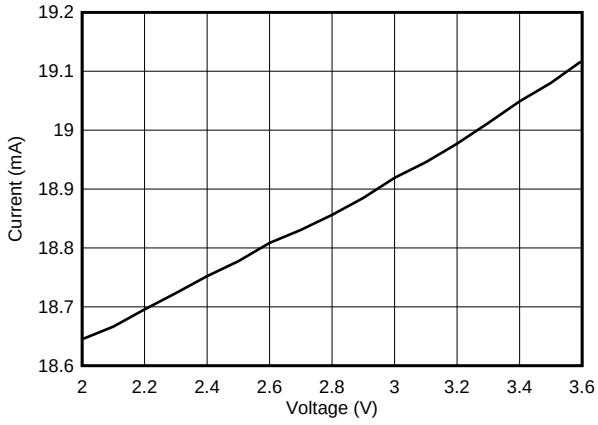
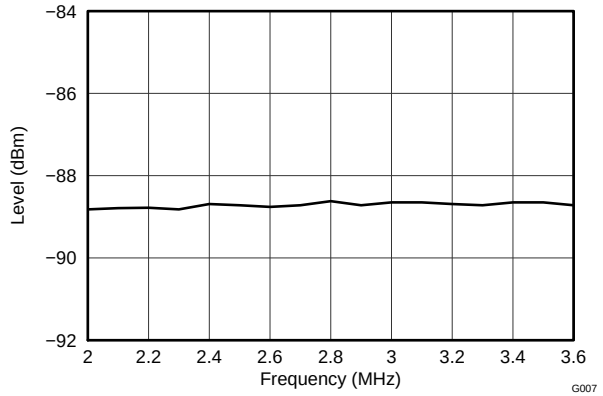


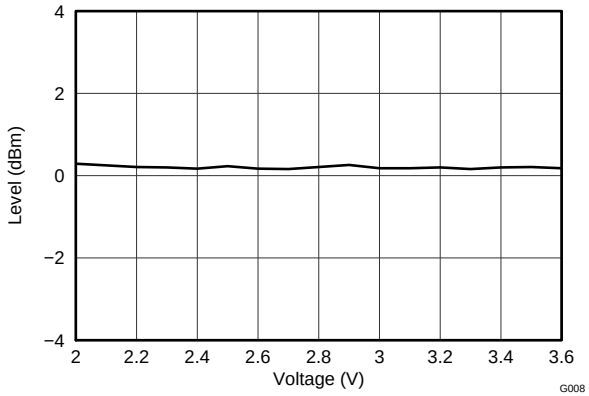
Figure 4-12. TX Current vs Supply Voltage

Typical Characteristics *(continued)*



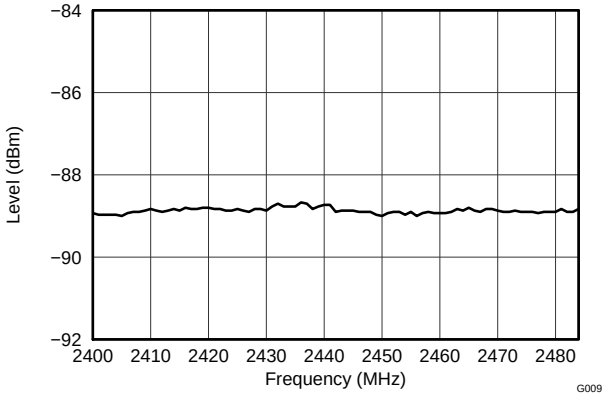
1-Mbps GFSK 250-kHz Standard Gain Setting
T_A = 25°C

Figure 4-13. RX Sensitivity vs Supply Voltage



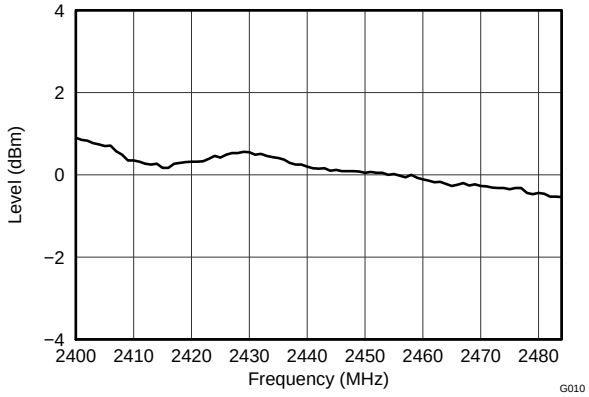
TX Power Setting = 0 dBm
T_A = 25°C

Figure 4-14. TX Power vs Supply Voltage



1-Mbps GFSK 250-kHz Standard Gain Setting
T_A = 25°C
V_{cc} = 3 V

Figure 4-15. RX Sensitivity vs Frequency



TX Power Setting = 0 dBm
T_A = 25°C
V_{cc} = 3 V

Figure 4-16. TX Power vs Frequency

Table 4-1. Output Power(1)(2)

TX POWER Setting	Typical Output Power (dBm)
0xE1	0
0xD1	–2
0xC1	–4
0xB1	–6
0xA1	–8
0x91	–10
0x81	–12
0x71	–14
0x61	–16
0x51	–18
0x41	–20

(1) Measured on Texas Instruments CC2541-Q1 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz. See SWRU191 for recommended register settings.
(2) 1 Mbsp, GFSK, 250-kHz deviation, *Bluetooth* low energy mode, 1% BER

5 Detailed Description

5.1 Functional Block Diagram

A block diagram of the CC2541-Q1 is shown in Figure 5-1. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

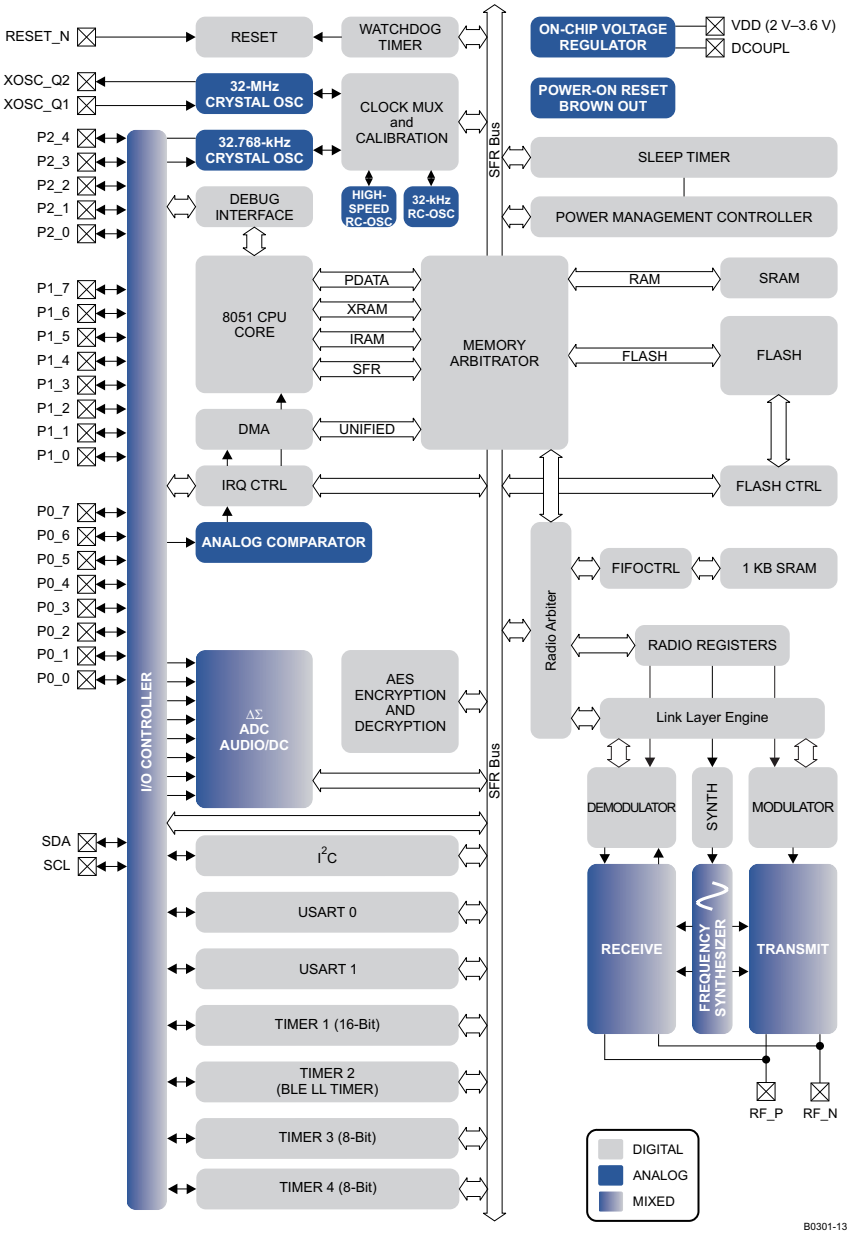


Figure 5-1. CC2541-Q1 Block Diagram

5.2 Block Descriptions

A block diagram of the CC2541-Q1 is shown in Figure 5-1. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

5.2.1 CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 5-1 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power mode 2 and mode 3).

The **256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

5.2.2 Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2541-Q1 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specfication.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2541-Q1 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.768-kHz crystal oscillator or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power mode 1 or mode 2.

A built-in **watchdog timer** allows the CC2541-Q1 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit output compare registers and two 24-bit overflow compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

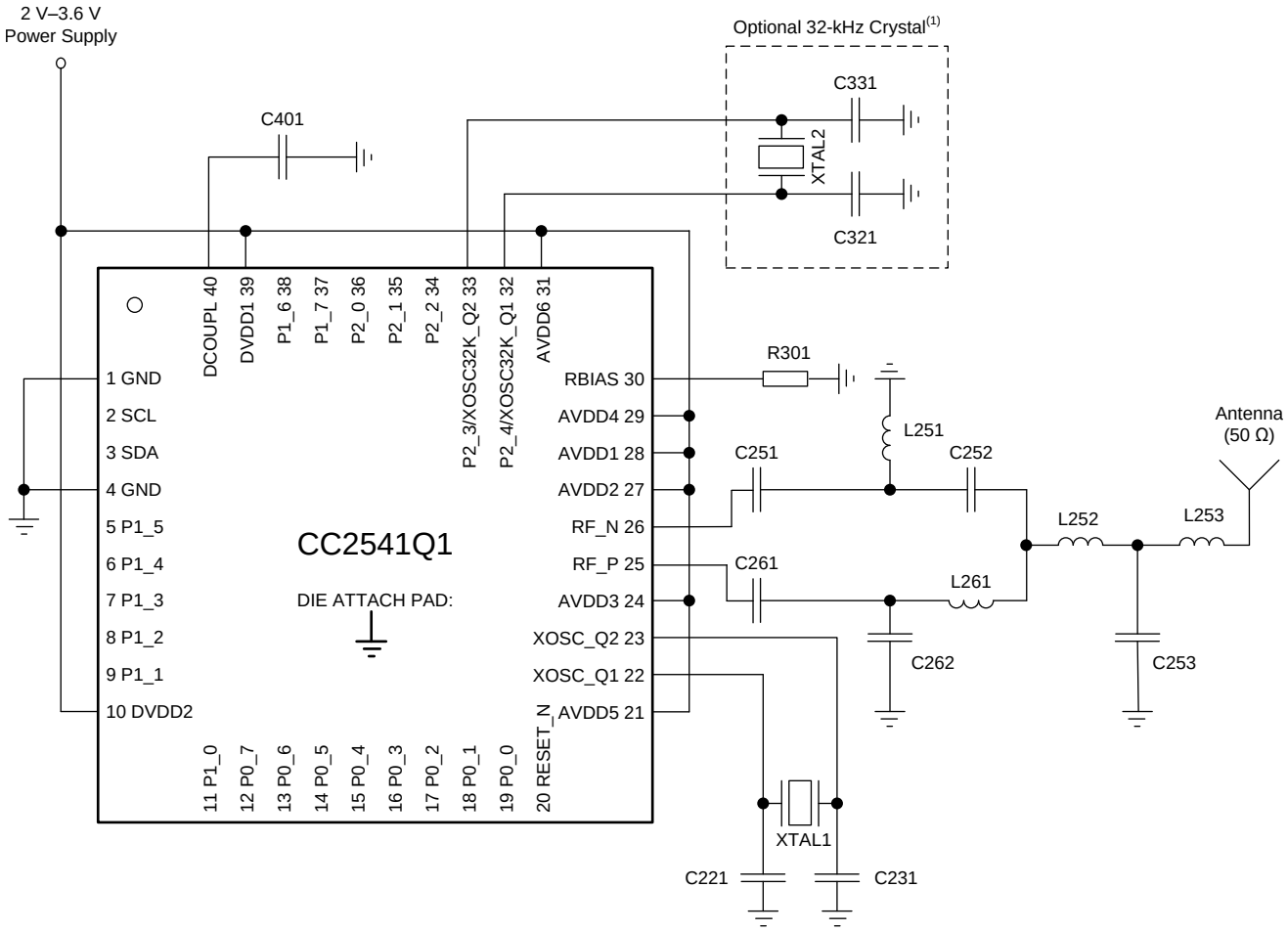
The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **I^2C** module provides a digital peripheral connection with two pins and supports both master and slave operation. I^2C support is compliant with the NXP I^2C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit device addressing modes are supported, as well as master and slave modes.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

6 Application Information

Few external components are required for the operation of the CC2541-Q1. A typical application circuit is shown in Figure 6-1.



(1) 32-kHz crystal is mandatory when running the BLE protocol stack in low-power modes, except if the link layer is in the standby state (Vol. 6 Part B Section 1.1 in [1]).
NOTE: Different antenna alternatives will be provided as reference designs.
Power supply decoupling capacitors are not shown. Digital I/O not connected

Figure 6-1. CC2541-Q1 Application Circuit

Table 6-1. Overview of External Components (Excluding Supply Decoupling Capacitors)

Component	Description	Value
C401	Decoupling capacitor for the internal 1.8-V digital voltage regulator	1 µF
R301	Precision resistor ±1%, used for internal biasing	56 kΩ

6.1 Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2541-Q1EM, for recommended balun.

6.2 Crystal

An external 32-MHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-MHz crystal oscillator. See Section 4.9 for details. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{parasitic} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{parasitic} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

6.3 On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C471) for stable operation.

6.4 Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

7 器件和文档支持

7.1 文档支持

7.1.1 相关文档

1. *Bluetooth*® Core 技术规范文档，版本 4.0
   http://www.bluetooth.com/SiteCollectionDocuments/Core_V40.zip
2. 适用于 2.4GHz IEEE 802.15.4 和 ZigBee® 应用的 CC253x 片上系统解决方案/适用于 2.4GHz 低功耗*蓝牙*应用的 CC2541-Q1 片上系统解决方案（文献编号 SWRU191）
3. CC254x 使用 TPS62730 节省电流（文献编号 SWRA365）。

7.1.1.1 其他信息

德州仪器 (TI) 为工业和消费类应用中所使用的专有应用和标准无线应用提供各种经济实用的低功耗射频解决方案。 其中包括适用于 1GHz 以下频段和 2.4GHz 频段的射频收发器、射频发送器、射频前端和片上系统以及各种软件解决方案。

此外，德州仪器 (TI) 还提供广泛的相关支持，例如开发工具、技术文档、参考设计、应用专业技术、客户支持、第三方服务以及大学计划。

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有关低功耗射频的详细信息，请参见节 7.1.1.2、节 7.1.1.3 和节 7.1.1.4。

7.1.1.2 德州仪器 (TI) 低功耗射频网站

- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

访问 www.ti.com/lprf-forum 立即体验。

7.1.1.3 德州仪器 (TI) 低功耗射频开发者网络

德州仪器 (TI) 建立了一个大型低功耗射频开发合作伙伴网络，帮助客户加快应用开发。 此网络中包括推荐的公司、射频顾问和独立设计工作室，他们可提供一系列硬件模块产品和设计服务，其中包括：

- 射频电路、低功耗射频和 ZigBee® 设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

需要有关模块、工程服务或开发工具的帮助？

请搜索低功耗射频开发者网络工具查找适合的合作伙伴。
www.ti.com/lprfnetwork

7.1.1.4 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，您能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。 低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问
www.ti.com/lprfnewsletter 立即注册

7.2 商标

SimpleLink is a trademark of Texas Instruments.
蓝牙 is a registered trademark of Bluetooth SIG, Inc..
ZigBee is a registered trademark of ZigBee Alliance.
All other trademarks are the property of their respective owners.

7.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

7.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

8 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2541F256TRHARQ1	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CC2541Q1 F256	Samples
CC2541F256TRHATQ1	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CC2541Q1 F256	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

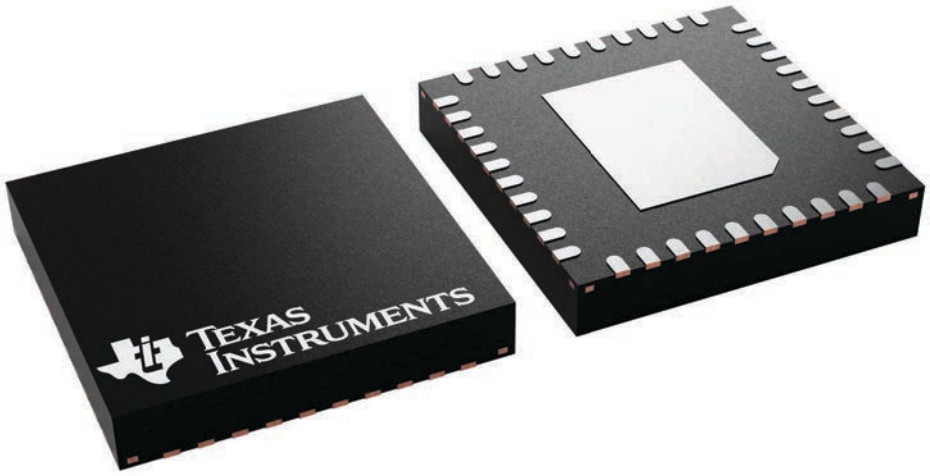
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



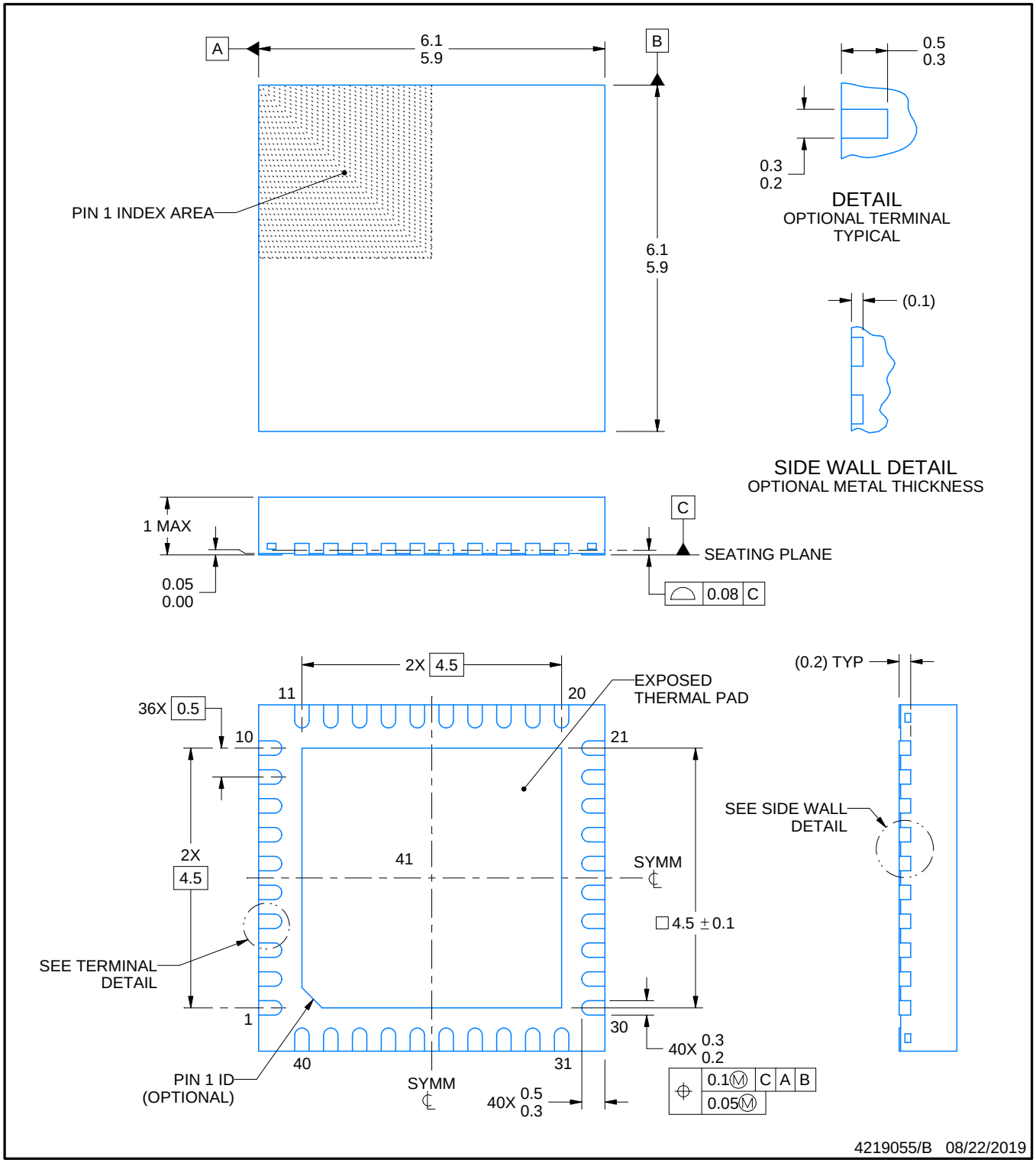
4225870/A

PACKAGE OUTLINE

RHA0040H

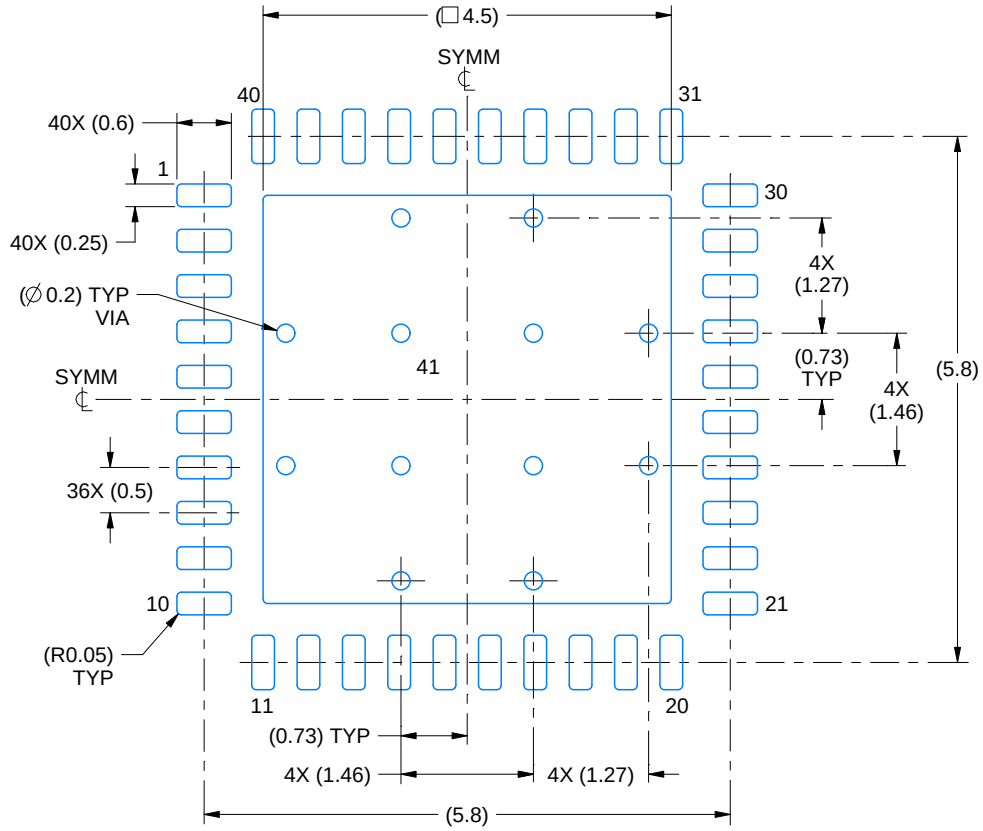
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

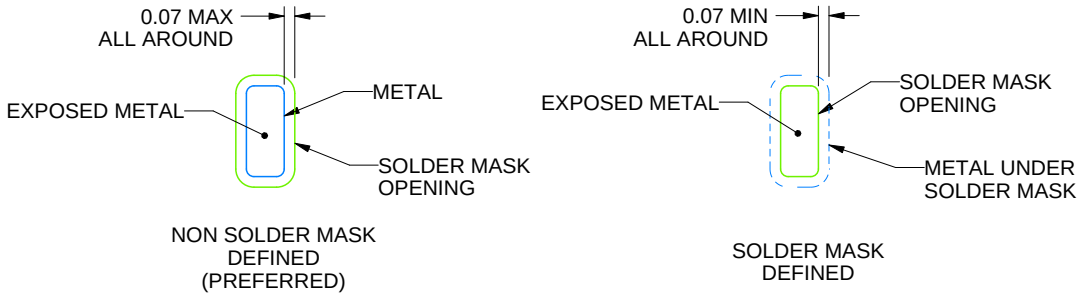


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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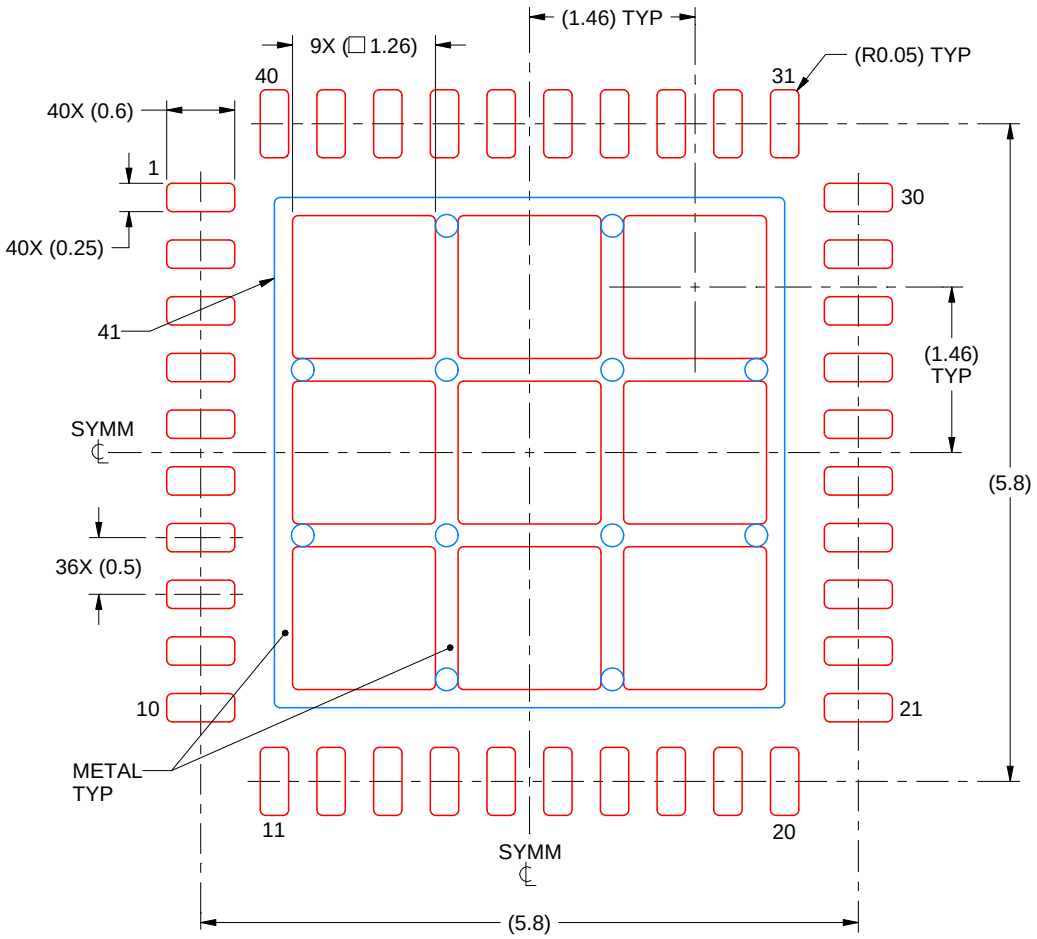
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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