CC2650MODA SimpleLink™ 低功耗 *Bluetooth*® 无线 MCU 模块

1 器件概述

1.1 特性

- 微控制器
  - 强大的 ARM® Cortex®-M3
  - EEMBC CoreMark®评分：142
  - 高达 48MHz 的时钟速度
  - 128KB 系统内可编程闪存
  - 8KB 缓存静态 RAM (SRAM)
  - 20KB 超低泄漏 SRAM
  - 2 引脚 cJTAG 和 JTAG 调试
  - 支持无线 (OTA) 升级
- 超低功耗传感器控制器
  - 可独立于系统其余部分自主运行
  - 16 位架构
  - 存储代码和数据的 2KB 超低泄漏静态随机存取存储器 (SRAM)
- 高效代码尺寸架构，ROM 中装载驱动程序、低功耗 *Bluetooth*® 控制器、 IEEE ®802.15.4 媒体接入控制 (MAC) 和引导加载程序
- 集成天线
- 外设
  - 所有数字外设引脚均可连接任意 GPIO
  - 四个通用定时器模块（8 × 16 位或 4 × 32 位，均采用脉宽调制 (PWM)）
  - 12 位模数转换器 (ADC)、200 ksps、8 通道模拟多路复用器
  - 持续时间比较器
  - 超低功耗模拟比较器
  - 可编程电流源
  - UART
  - 2 个同步串行接口 (SSI)（SPI、MICROWIRE 和 TI）
  - I^2C
  - I2S
  - 实时时钟 (RTC)
  - AES-128 安全模块
  - 真随机数发生器 (TRNG)
  - 15 个通用输入输出 (GPIO)
  - 支持八个电容感测按钮
  - 集成温度传感器
- 外部系统
  - 片上内部直流/直流转换器
  - 无需外部组件，只需电源电压
- 低功耗
  - 宽电源电压范围
    - 工作电压范围为 1.8V 至 3.8V
  - 有源模式 RX：6.2mA
  - 有源模式 TX (0dBm)：6.8mA
  - 有源模式 TX (+5dBm)：9.4mA
  - 有源模式 MCU：61µA/MHz
  - 有源模式 MCU：48.5 CoreMark/mA
  - 有源模式传感器控制器：0.4mA + 8.2µA/MHz
  - 待机电流：1µA（RTC 运行，RAM/CPU 保持）
  - 关断电流：100nA（发生外部事件时唤醒）
- 射频 (RF) 部分
  - 2.4GHz 射频收发器，符合低功耗蓝牙 (BLE) 5.1 规范及 IEEE 802.15.4 PHY 和 MAC
  - 符合 CC2650MODA RF-PHY 标准 (QDID: 88415)
  - 出色的接收器灵敏度（蓝牙低功耗对应 –97dBm，802.15.4 对应 –100dBm）、可选择性以及阻断性能
  - 最高达 +5dBm 的可编程输出功率
  - 已经过预认证，符合全球射频规范
    - ETSI RED（欧洲）
    - IC（加拿大）
    - FCC（美国）
    - ARIB STD-T66（日本）
    - JATE（日本）
- 工具和开发环境
  - 功能全面的低成本开发套件
  - 针对不同 RF 配置的多种参考设计
  - 数据包监听器 PC 软件
  - Sensor Controller Studio
  - SmartRF™Studio
  - SmartRF Flash Programmer 2
  - IAR Embedded Workbench®（用于 ARM）
  - Code Composer Studio™

1.2 应用

- 楼宇自动化
- 医疗和健康
- 电器
- 工业
- 消费类电子产品
- 接近标签
- 警报和安全
- 遥控
- 无线传感器网络

1.3 说明

该 SimpleLink™CC2650MODA 器件是一款无线微控制器 (MCU) 模块，主要适用于低功耗 *Bluetooth*® 应用。CC2650MODA 器件还适用于 ZigBee®和 6LoWPAN 以及 ZigBee RF4CE™远程控制 应用。

该模块基于 SimpleLink CC2650 无线 MCU，属于 CC26xx 系列的经济高效型超低功耗 2.4GHz RF 器件。它具有极低的有源 RF 和 MCU 电流以及低功耗模式流耗，可确保卓越的电池使用寿命，适合小型纽扣电池供电以及在能源采集型应用中 使用。

CC2650MODA 模块含有一个 32 位 ARM Cortex-M3 处理器（与主处理器工作频率同为 48MHz），并且具有丰富的外设功能集，其中包括一个独特的超低功耗传感器控制器。此传感器控制器非常适合连接外部传感器，或适合用于在系统其余部分处于睡眠模式的情况下自主收集模拟和数字数据。因此，CC2650MODA 器件成为工业、消费类电子和医疗产品中各类 应用 的理想选择。

CC2650MODA 模块已通过预认证，能够按照 FCC、IC、ETSI 和 ARIB 规范运行。在客户将此模块集成到其产品中时，这些认证能够为客户节省大量成本和精力。

蓝牙低功耗控制器和 IEEE 802.15.4 MAC 嵌入在 ROM 中，并在 ARM® Cortex®-M0 处理器上单独运行。此架构可改善系统整体性能和功耗，并释放更多闪存以供应用。

蓝牙低功耗软件堆栈 (BLE-Stack) 以及 ZigBee 软件堆栈 (Z-Stack™) 可以免费获取。

器件信息 (1)

器件型号	封装	封装尺寸
CC2650MODAMOH	MOH（模块）	16.90mm x 11.00mm

(1) 详细信息请参阅节 10。

1.4 功能框图

图 1-1 是 CC2650MODA 器件的框图。

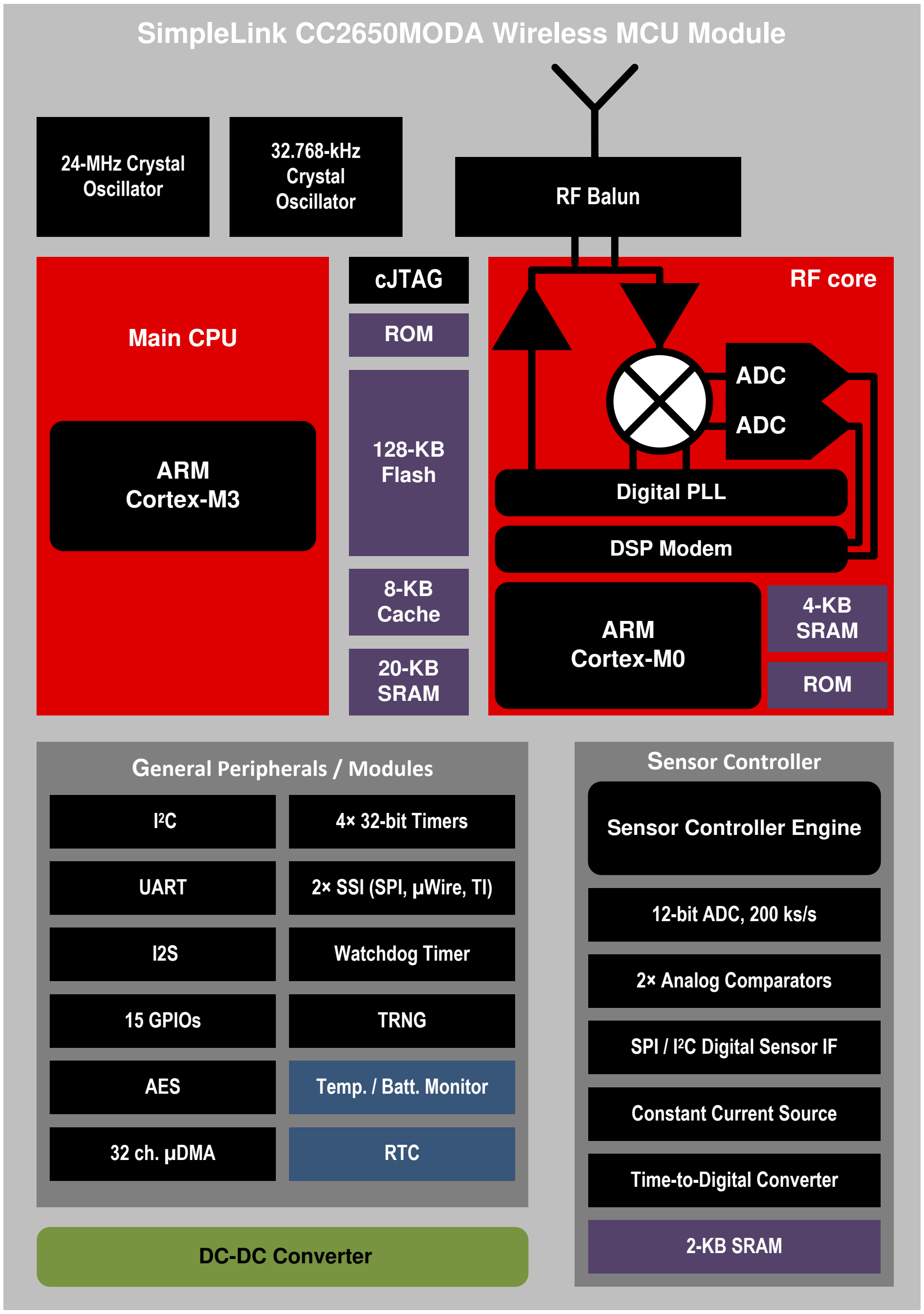


图 1-1. CC2650MODA 框图

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from July 1, 2017 to July 31, 2019	Page
• Added Module Marking section.	33
• Added Environmental Requirements and Specifications section.	36

3 Device Comparison

Table 3-1. Device Family Overview

DEVICE	PHY SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE
CC2650MODAMOH	Multiprotocol(1)	128	20	15	MOH

(1) The CC2650 device supports all PHYs and can be reflashed to run all the supported standards.

3.1 Related Products

TI's Wireless Connectivity The wireless connectivity portfolio offers a wide selection of low-power RF solutions suitable for a broad range of applications. The offerings range from fully customized solutions to turn key offerings with pre-certified hardware and software (protocol).

TI's SimpleLink™ Sub-1 GHz Wireless MCUs Long-range, low-power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands.

Companion Products Review products that are frequently purchased or used in conjunction with this product.

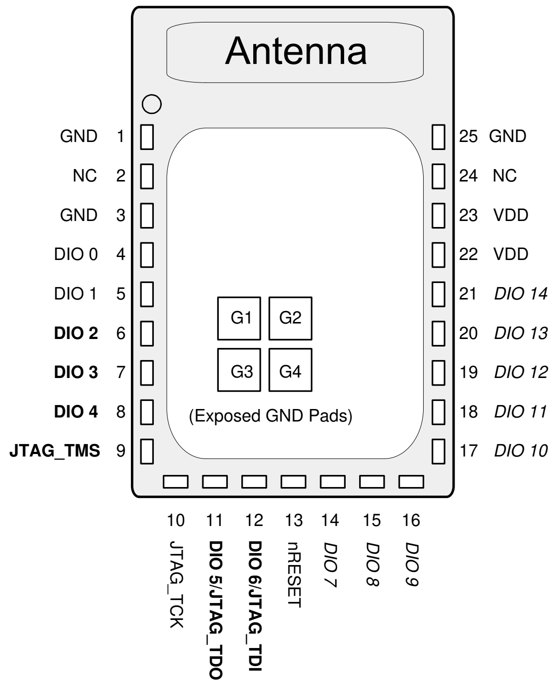
SimpleLink™ CC2650 Wireless MCU LaunchPad™ Development Kit The CC2650 LaunchPad™ development kit brings easy Bluetooth® low energy connectivity to the LaunchPad kit ecosystem with the SimpleLink ultra-low power CC26xx family of devices. This LaunchPad kit also supports development for multi-protocol support for the SimpleLink multi-standard CC2650 wireless MCU and the rest of CC26xx family of products: CC2630 wireless MCU for ZigBee®/6LoWPAN and CC2640 wireless MCU for Bluetooth low energy.

Reference Designs for CC2650MODA TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

Section 4.1 shows pin assignments for the CC2650MODA device.

4.1 Module Pin Diagram



(1) The following I/O pins marked in **bold** in the pinout have high-drive capabilities:
- DIO 2
- DIO 3
- DIO 4
- JTAG_TMS
- DIO 5/JTAG_TDO
- DIO 6/JTAG_TDI

(2) The following I/O pins marked in *italics* in the pinout have analog capabilities:
- DIO 7
- DIO 8
- DIO 9
- DIO 10
- DIO 11
- DIO 12
- DIO 13
- DIO 14

Figure 4-1. CC2650MODA MOH Package (16.9-mm × 11-mm) Module Pinout

4.2 Pin Functions

Table 4-1 describes the CC2650MODA pins.

Table 4-1. Signal Descriptions – MOH Package

PIN NAME	PIN NO.	PIN TYPE	DESCRIPTION
DIO_0	4	Digital I/O	GPIO, Sensor Controller
DIO_1	5	Digital I/O	GPIO, Sensor Controller
DIO_2	6	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	7	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_4	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_5/JTAG_TDO	11	Digital I/O	GPIO, high-drive capability, JTAG_TDO
DIO_6/JTAG_TDI	12	Digital I/O	GPIO, high-drive capability, JTAG_TDI
DIO_7	14	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_8	15	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_9	16	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_10	17	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_11	18	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_12	19	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_13	20	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
DIO_14	21	Digital I/O, Analog I/O	GPIO, Sensor Controller, analog
EGP	G1, G2, G3, G4	Power	Ground – Exposed ground pad
GND	1, 3, 25	—	Ground
JTAG_TCK	10	Digital I/O	JTAG TCKC
JTAG_TMS	9	Digital I/O	JTAG TMSC, high-drive capability
NC	2, 24	NC	Not Connected—TI recommends leaving these pins floating
nRESET	13	Digital input	Reset, active low. No internal pullup
VDD	22, 23	Power	1.8-V to 3.8-V main chip supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)]

			MIN	MAX	UNIT
VDD	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin[(3)]		–0.3	VDD + 0.3, max 4.1	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDD	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDD as reference	–0.3	VDD / 2.9	
	Input RF level			5	dBm
T_{stg}	Storage temperature		–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog capable DIO.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001[(1)]	All pins	±1000	V
		Charged device model (CDM), per JESD22-C101[(2)]	RF pins	±500	
			Non-RF pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Ambient temperature		–40	85	°C
Operating supply voltage (VDD)	For operation in battery-powered and 3.3-V systems (internal DC-DC can be used to minimize power consumption)	1.8	3.8	V

5.4 Power Consumption Summary

T_c = 25°C, V_{DD} = 3.0 V with internal DC-DC converter, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Reset. RESET_N pin asserted or VDD below Power-on-Reset threshold		100		nA
		Shutdown. No clocks running, no retention		150		nA
		Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF		1		µA
		Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF		1.2		µA
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF		2.5		µA
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF		2.7		µA
		Idle. Supply systems and RAM powered.		550		µA
		Active. Core running CoreMark		1.45 mA + 31 µA/MHz		
		Radio RX		6.2		mA
		Radio TX, 0-dBm output power		6.8		mA
		Radio TX, 5-dBm output power		9.4		mA
Peripheral Current Consumption (Adds to core current I_{core} for each peripheral unit activated)(1)						
I_{peri}	Peripheral power domain	Delta current with domain enabled		20		µA
	Serial power domain	Delta current with domain enabled		13		µA
	RF core	Delta current with power domain enabled, clock enabled, RF Core Idle		237		µA
	µDMA	Delta current with clock enabled, module idle		130		µA
	Timers	Delta current with clock enabled, module idle		113		µA
	I^2C	Delta current with clock enabled, module idle		12		µA
	I2S	Delta current with clock enabled, module idle		36		µA
	SSI	Delta current with clock enabled, module idle		93		µA
	UART	Delta current with clock enabled, module idle		164		µA

(1) I_{peri} is not supported in Standby or Shutdown.

5.5 General Characteristics

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLASH MEMORY					
Supported flash erase cycles before failure		100			k Cycles
Flash page/sector erase current	Average delta current		12.6		mA
Flash page/sector erase time(1)			8		ms
Flash page/sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash write time(1)	4 bytes at a time		8		µs

(1) This number is dependent on flash aging and will increase over time and erase cycles.

5.6 Antenna

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Polarization			Linear		
Peak Gain	2450 MHz		1.26		dBi
Efficiency	2450 MHz		57%		

5.7 1-Mbps GFSK (Bluetooth low energy) – RX

RF performance is specified in a single ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C, V_{DD} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	BER = 10^{-3}		–97		dBm
Receiver saturation	BER = 10^{-3}		4		dBm
Frequency error tolerance	Difference between center frequency of the received RF signal and local oscillator frequency.	–350		350	kHz
Data rate error tolerance		–750		750	ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 3(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		29 / 23(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		38 / 26(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		42 / 29(2)		dB
Selectivity, ±5 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		32		dB
Selectivity, Image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		23		dB
Selectivity, Image frequency ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		3 / 26(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–20		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–5		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–8		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–8		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–34		dBm
Spurious emissions, 30 MHz to 1000 MHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–71		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–62		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification

5.8 1-Mbps GFSK (Bluetooth low energy) – TX

RF performance is specified in a single ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C, V_{DD} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting			5		dBm
Output power, lowest setting			–21		dBm
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–58		dBm
	f < 1 GHz, restricted bands FCC		–57		dBm
	f > 1 GHz, including harmonics		–45		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)

5.9 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – RX

RF performance is specified in a single ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%		–100		dBm
Receiver saturation	PER = 1%		–7		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1%		35		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1%		52		dB
Channel rejection, ±15 MHz or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		57		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Spurious emissions, 30 MHz to 1000 MHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–71		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–62		dBm
Frequency error tolerance	Difference between center frequency of the received RF signal and local oscillator frequency		>200		ppm
RSSI dynamic range			100		dB
RSSI accuracy			±4		dB

5.10 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – TX

RF performance is specified in a single ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting			5		dBm
Output power, lowest setting			–21		dBm
Error vector magnitude	At maximum output power		2%		
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–58		
	f < 1 GHz, restricted bands FCC		–57		
	f > 1 GHz, including harmonics		–45		

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)

5.11 24-MHz Crystal Oscillator (XOSC_HF)(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			24		MHz
Crystal frequency tolerance(2)		–40		40	ppm
Start-up time(3)			150		µs

(1) Probing or otherwise stopping the XTAL while the DC-DC converter is enabled may cause permanent damage to the device.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance. As per Bluetooth and IEEE 802.15.4 specification
(3) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection

5.12 32.768-kHz Crystal Oscillator (XOSC_LF)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32.768		kHz
Initial crystal frequency tolerance, Bluetooth low energy applications	T_c = 25°C	–20		20	ppm
Crystal aging		-3		3	ppm/year

5.13 48-MHz RC Oscillator (RCOSC_HF)

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			48		MHz
Uncalibrated frequency accuracy			±1%		
Calibrated frequency accuracy(1)			±0.25%		
Start-up time			5		µs

(1) Accuracy relatively to the calibration source (XOSC_HF).

5.14 32-kHz RC Oscillator (RCOSC_LF)

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency			32.8		kHz
Temperature coefficient			50		ppm/°C

5.15 ADC Characteristics

T_c = 25°C, V_{DD} = 3.0 V and voltage scaling enabled, unless otherwise noted (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V_{DD}	V
	Resolution			12		Bits
	Sample rate				200	ksps
	Offset	Internal 4.3-V equivalent reference (2)		2		LSB
	Gain error	Internal 4.3-V equivalent reference (2)		2.4		LSB
DNL (3)	Differential nonlinearity			>–1		LSB
INL (4)	Integral nonlinearity			±3		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference (2), 200 ksps, 9.6-kHz input tone		9.8		Bits
		VDD as reference, 200 ksps, 9.6-kHz input tone		10		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference (2), 200 ksps, 9.6-kHz input tone		–65		dB
		VDD as reference, 200 ksps, 9.6-kHz input tone		–69		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		–71		
SINAD and SNDR	Signal-to-noise and distortion ratio	Internal 4.3-V equivalent reference (2), 200 ksps, 9.6-kHz input tone		60		dB
		VDD as reference, 200 ksps, 9.6-kHz input tone		63		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		69		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference (2), 200 ksps, 9.6-kHz input tone		67		dB
		VDD as reference, 200 ksps, 9.6-kHz input tone		72		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		73		
	Conversion time	Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles
	Current consumption	Internal 4.3-V equivalent reference (2)		0.66		mA
	Current consumption	VDD as reference		0.75		mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS™ API to include the gain or offset compensation factors stored in FCFG1.		4.3 (2) (5)		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain or offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDD as reference (Also known as *RELATIVE*) (input voltage scaling enabled)		VDD		V
	Reference voltage	VDD as reference (Also known as *RELATIVE*) (input voltage scaling disabled)		VDD / 2.82 (5)		V
	Input Impedance	200 ksps, voltage scaling enabled. Capacitive input, input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241™-2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.
(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5 depending on device, see Figure 5-24.
(4) For a typical example, see Figure 5-25.
(5) Applied voltage must be within absolute maximum ratings (see Section 5.1) at all times.

5.16 Temperature Sensor

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		–40		85	°C
Accuracy			±5		°C
Supply voltage coefficient(1)			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

5.17 Battery Monitor

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V
Accuracy			13		mV

5.18 Continuous Time Comparator

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DD}	V
External reference voltage		0		V_{DD}	V
Internal reference voltage	DCOUPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from –10 mV to +10 mV		0.72		µs
Current consumption when enabled(1)			8.6		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.19 Low-Power Clocked Comparator

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		VDD	V
Clock frequency			32		kHz
Internal reference voltage, VDD / 2			1.49–1.51		V
Internal reference voltage, VDD / 3			1.01–1.03		V
Internal reference voltage, VDD / 4			0.78–0.79		V
Internal reference voltage, DCOUPL / 1			1.25–1.28		V
Internal reference voltage, DCOUPL / 2			0.63–0.65		V
Internal reference voltage, DCOUPL / 3			0.42–0.44		V
Internal reference voltage, DCOUPL / 4			0.33–0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from –50 mV to +50 mV		<1		clock-cycle
Current consumption when enabled			362		nA

5.20 Programmable Current Source

T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25–20		µA
Resolution			0.25		µA
Current consumption(1)	Including current source at maximum programmable output		23		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.21 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DD} = 1.8 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only	1.32	1.54		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.26	0.32	V
GPIO VOH at 4-mA load	IOCURR = 1	1.32	1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		71.7		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD		21.1		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.33		V
T_A = 25°C, V_{DD} = 3.0 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR = 1		2.72		V
GPIO VOL at 4-mA load	IOCURR = 1		0.28		V
T_A = 25°C, V_{DD} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		277		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD		113		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.54		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.4		V
T_A = 25°C					
VIH	Lowest GPIO input voltage reliably interpreted as a «High»			0.8	VDD
VIL	Highest GPIO input voltage reliably interpreted as a «Low»	0.2			VDD

5.22 Thermal Resistance Characteristics for MOH Package

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\Theta_{JC}$	Junction-to-case	20.0	
$R\Theta_{JB}$	Junction-to-board	15.3	
$R\Theta_{JA}$	Junction-to-free air	29.6	0
$R\Theta_{JMA}$	Junction-to-moving air	25.0	1
Psi_{JT}	Junction-to-package top	8.8	0
Psi_{JB}	Junction-to-board	14.8	0

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.
(3) m/s = meters per second.

5.23 Timing Requirements

			MIN	NOM	MAX	UNIT
Rising supply-voltage slew rate			0		100	mV/µs
Falling supply-voltage slew rate			0		20	mV/µs
Falling supply-voltage slew rate, with low-power flash settings(1)					3	mV/µs
Positive temperature gradient in standby(2)		No limitation for negative temperature gradient, or outside standby mode			5	°C/s
CONTROL INPUT AC CHARACTERISTICS(3)						
RESET_N low duration			1			µs
SYNCHRONOUS SERIAL INTERFACE (SSI)(4)						
S1 (SLAVE)(5)	t_{clk_per}	SSIClk period	12		65024	System clocks
S2(5)	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3(5)	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDD input capacitor (see Section 7.1.1) must be used to ensure compliance with this slew rate.
(2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see Section 5.14).
(3) T_A = –40°C to +85°C, V_{DD} = 1.7 V to 3.8 V, unless otherwise noted.
(4) T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted. Device operating as slave. For SSI master operation, see Section 5.24.
(5) Refer to the SSI timing diagrams Figure 5-1, Figure 5-2, and Figure 5-3.

5.24 Switching Characteristics

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKEUP AND TIMING					
Idle → Active			14		µs
Standby → Active			151		µs
Shutdown → Active			1015		µs

Switching Characteristics *(continued)*

Measured on the TI CC2650EM-5XD reference design with T_c = 25°C, V_{DD} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS SERIAL INTERFACE (SSI) (1)					
S1 (TX only)(2) t_{clk_per} (SSIClk period)	One-way communication to SLAVE	4		65024	System clocks
S1 (TX and RX)(2) t_{clk_per} (SSIClk period)	Normal duplex operation	8		65024	System clocks
S2(2) t_{clk_high} (SSIClk high time)			0.5		t_{clk_per}
S3(2) t_{clk_low} (SSIClk low time)			0.5		t_{clk_per}

(1) Device operating as master. For SSI slave operation, see Section 5.23.
(2) Refer to SSI timing diagrams Figure 5-1, Figure 5-2, and Figure 5-3.

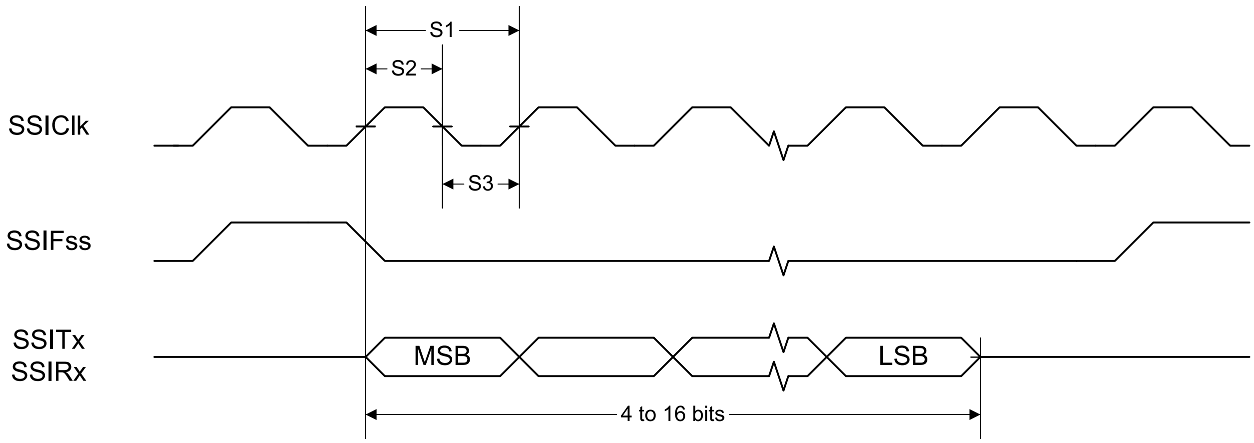


Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

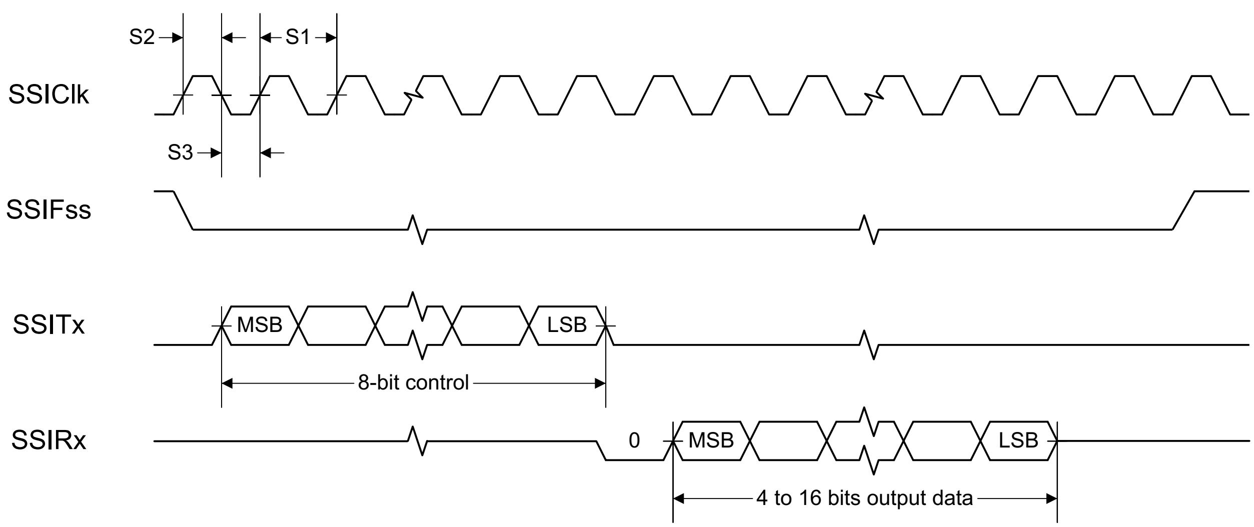


Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

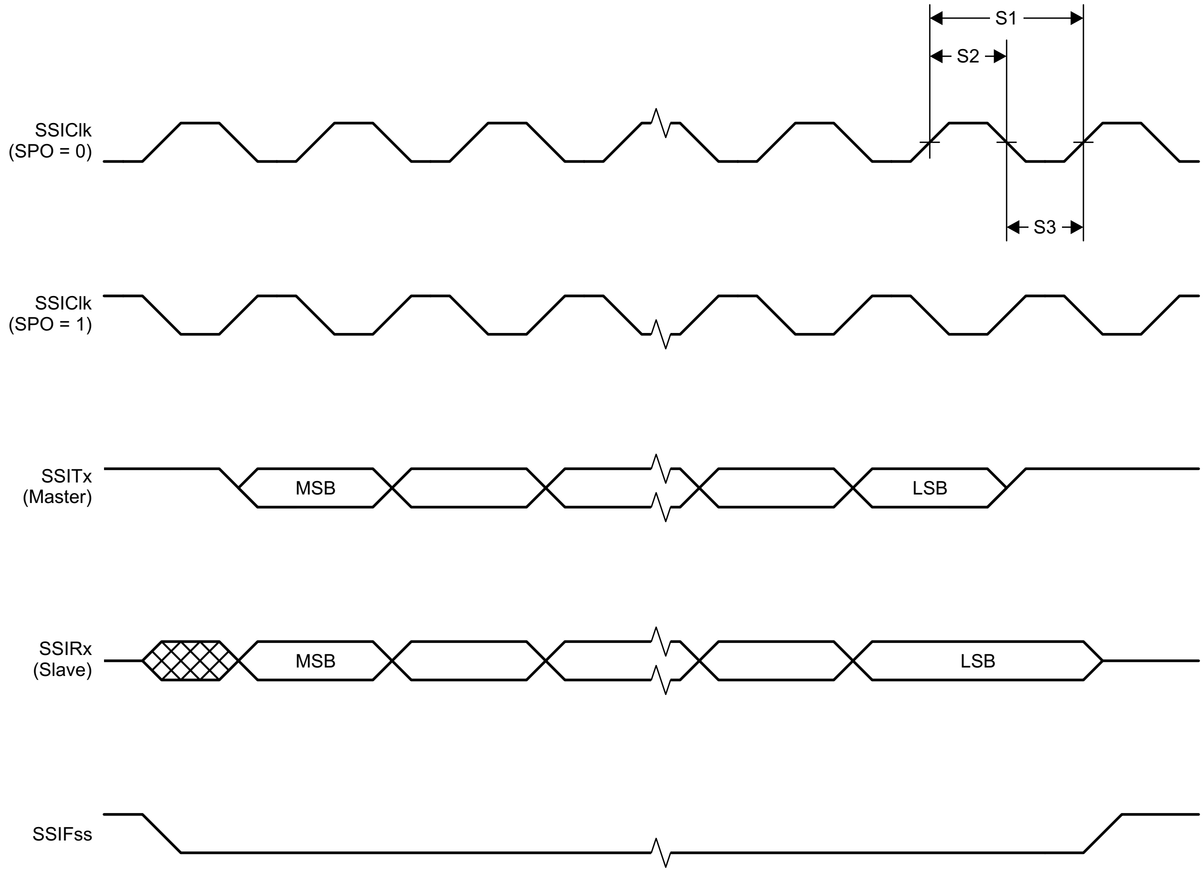


Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.25 Typical Characteristics

This section contains typical performance plots measured on the CC2650F128RHB device. They are published in the CC2650 data sheet, and the plots relevant for the CC2650MODA device are repeated here. RF performance is specified in a single-ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C and V_{DD} = 3.0 V, unless otherwise noted.

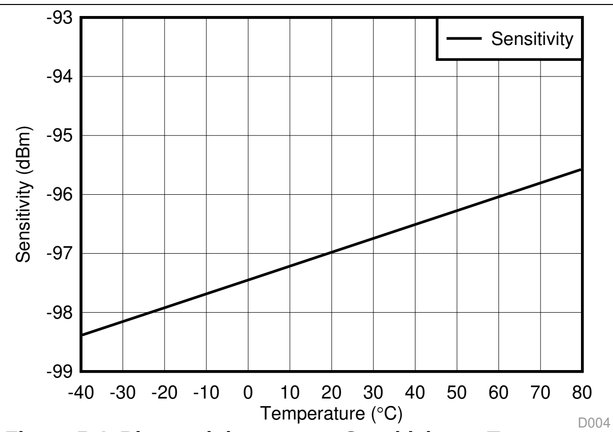


Figure 5-4. Bluetooth low energy Sensitivity vs Temperature

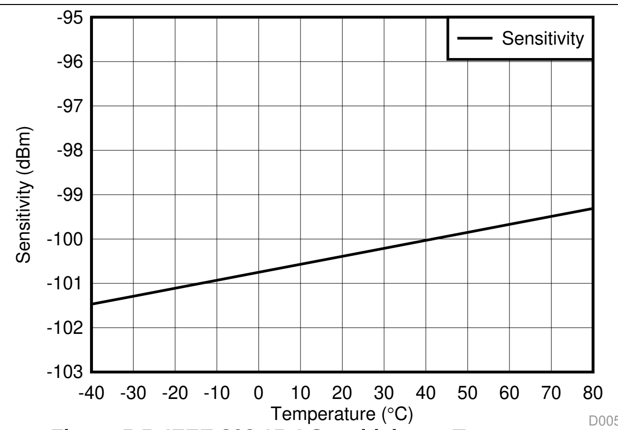


Figure 5-5. IEEE 802.15.4 Sensitivity vs Temperature

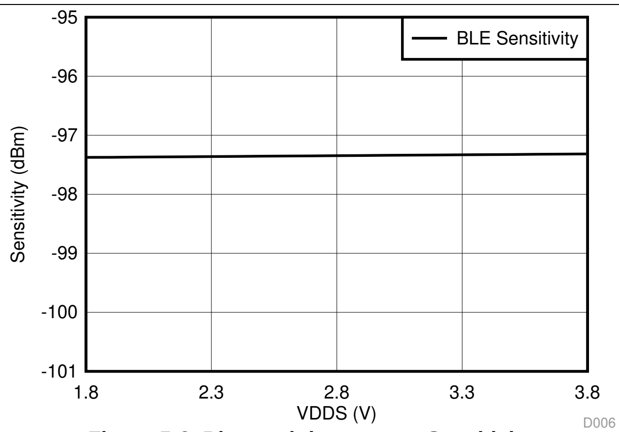


Figure 5-6. Bluetooth low energy Sensitivity vs Supply Voltage (VDD)

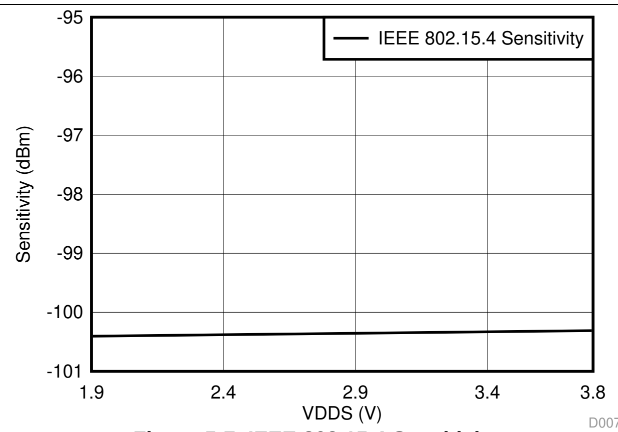


Figure 5-7. IEEE 802.15.4 Sensitivity vs Supply Voltage (VDD)

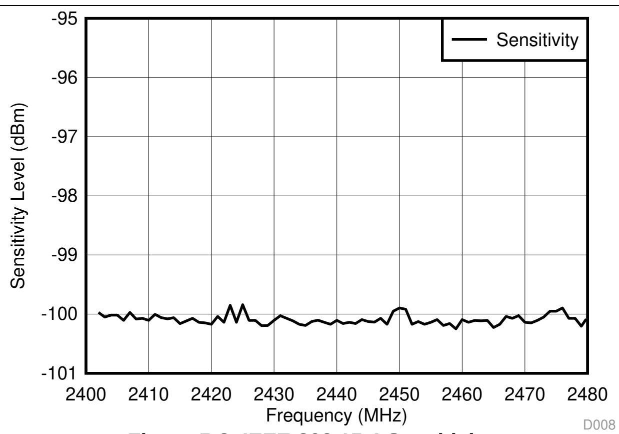


Figure 5-8. IEEE 802.15.4 Sensitivity vs Channel Frequency

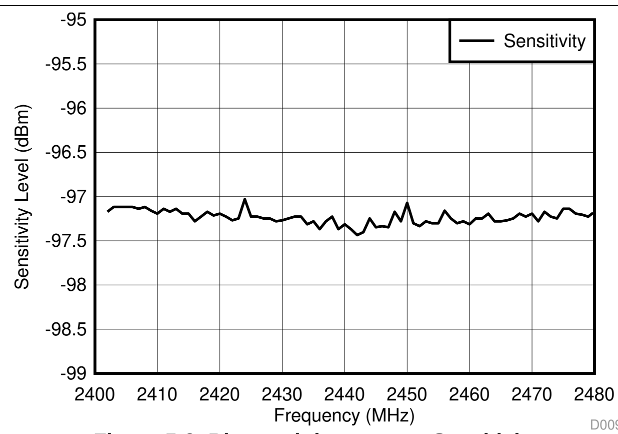


Figure 5-9. Bluetooth low energy Sensitivity vs Channel Frequency

Typical Characteristics *(continued)*

This section contains typical performance plots measured on the CC2650F128RHB device. They are published in the CC2650 data sheet, and the plots relevant for the CC2650MODA device are repeated here. RF performance is specified in a single-ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C and V_{DD} = 3.0 V, unless otherwise noted.

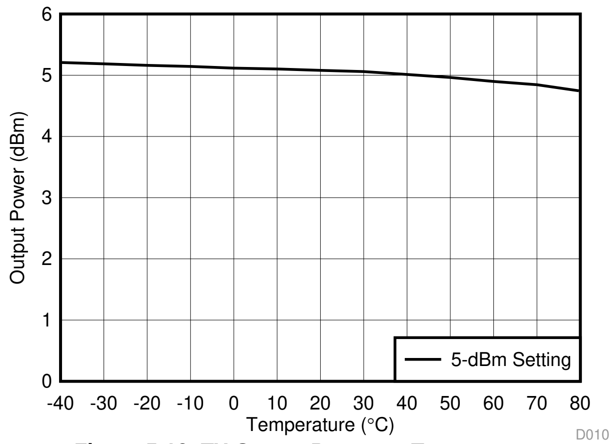


Figure 5-10. TX Output Power vs Temperature

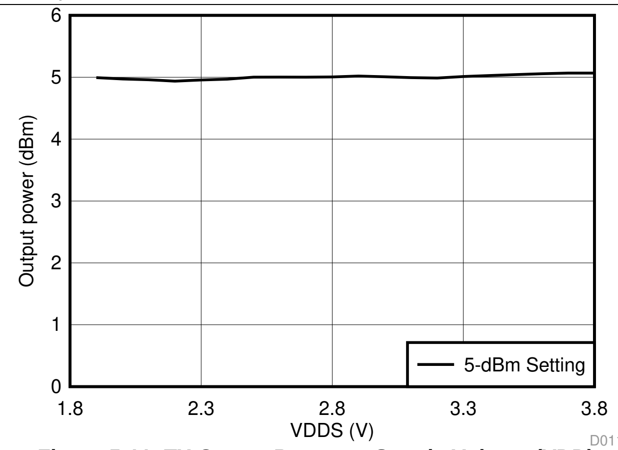


Figure 5-11. TX Output Power vs Supply Voltage (VDD)

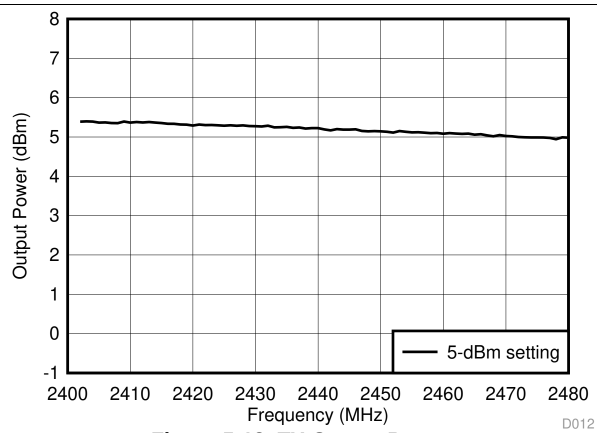


Figure 5-12. TX Output Power vs Channel Frequency

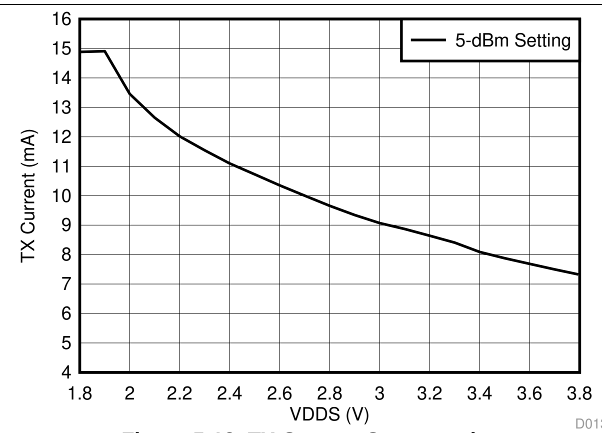


Figure 5-13. TX Current Consumption vs Supply Voltage (VDD)

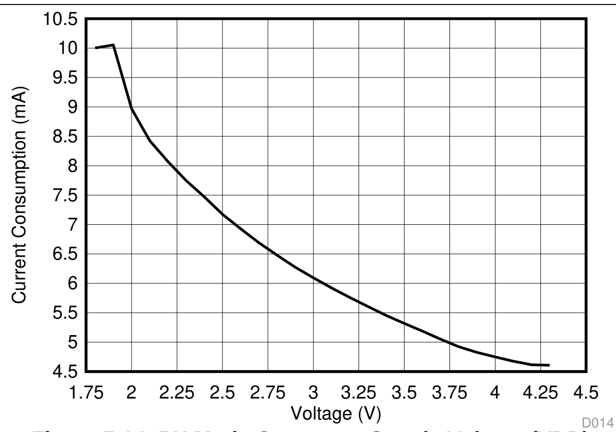


Figure 5-14. RX Mode Current vs Supply Voltage (VDD)

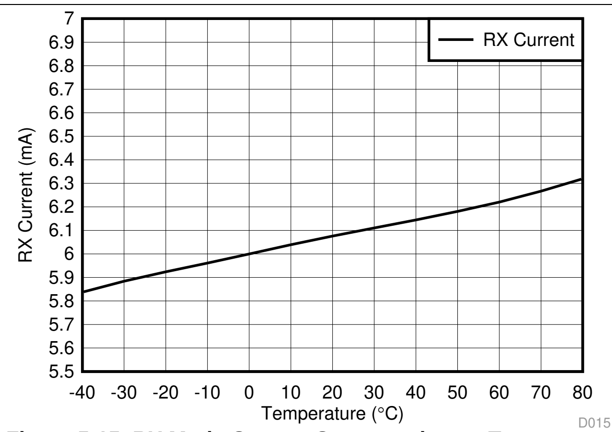


Figure 5-15. RX Mode Current Consumption vs Temperature

Typical Characteristics *(continued)*

This section contains typical performance plots measured on the CC2650F128RHB device. They are published in the CC2650 data sheet, and the plots relevant for the CC2650MODA device are repeated here. RF performance is specified in a single-ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C and V_{DD} = 3.0 V, unless otherwise noted.

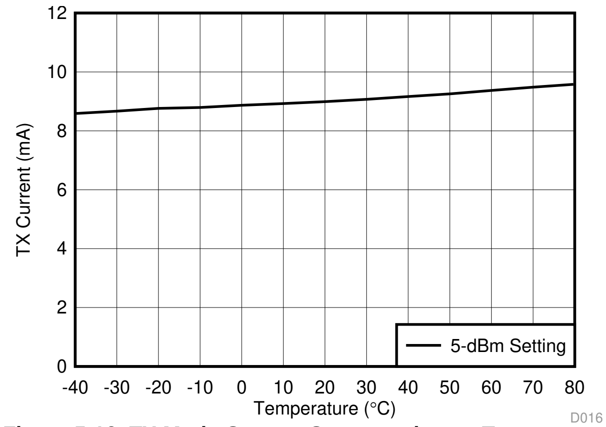


Figure 5-16. TX Mode Current Consumption vs Temperature

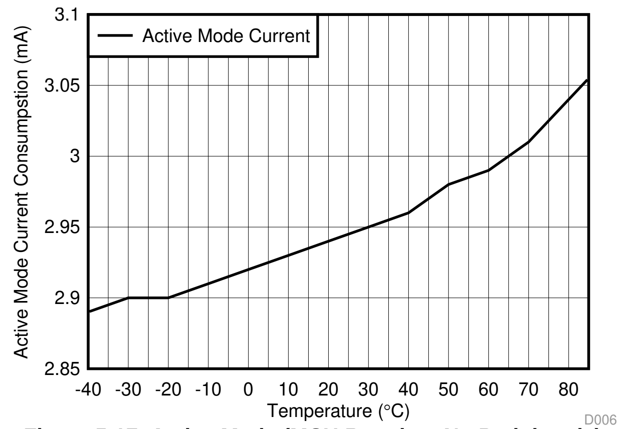


Figure 5-17. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature

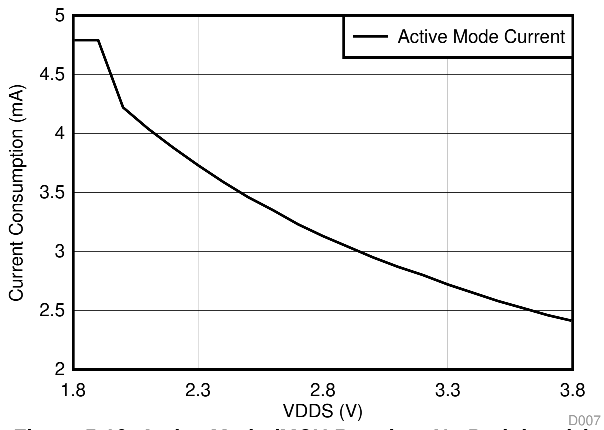


Figure 5-18. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDD)

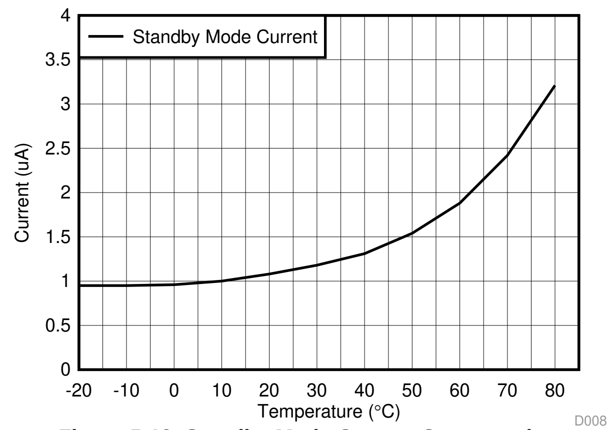


Figure 5-19. Standby Mode Current Consumption With RCOSC RTC vs Temperature

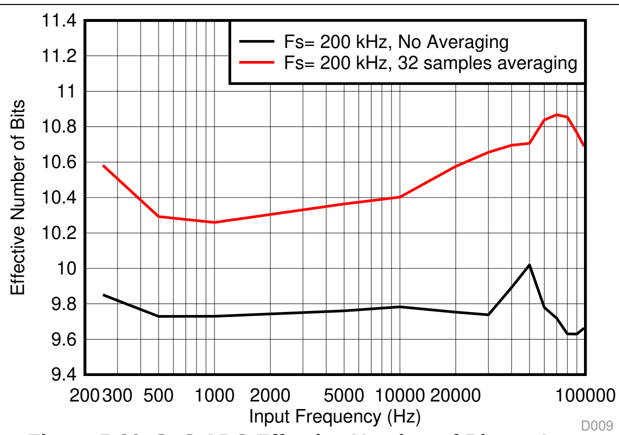


Figure 5-20. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference)

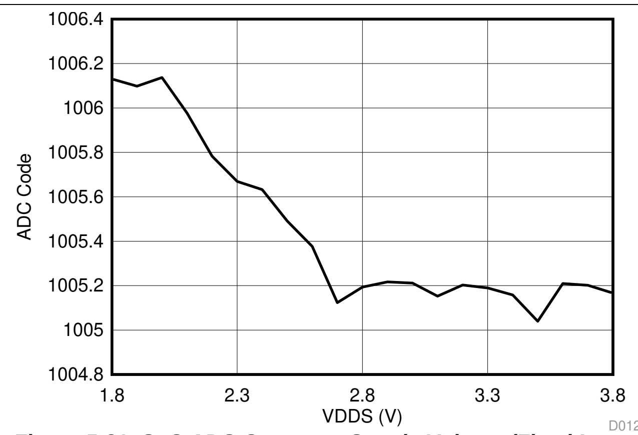


Figure 5-21. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference)

Typical Characteristics *(continued)*

This section contains typical performance plots measured on the CC2650F128RHB device. They are published in the CC2650 data sheet, and the plots relevant for the CC2650MODA device are repeated here. RF performance is specified in a single-ended 50-Ω reference plane at the antenna feeding point with T_c = 25°C and V_{DD} = 3.0 V, unless otherwise noted.

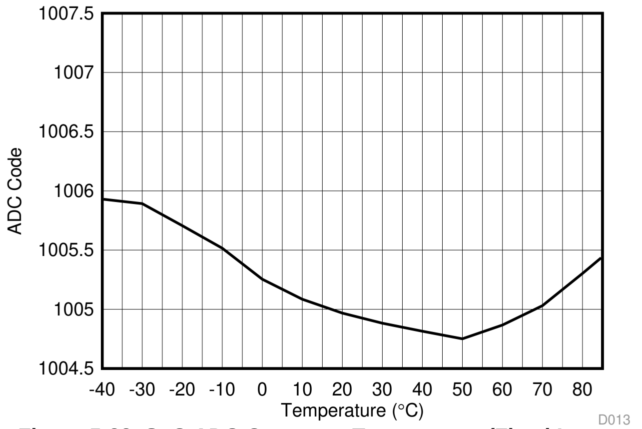


Figure 5-22. SoC ADC Output vs Temperature (Fixed Input, Internal Reference)

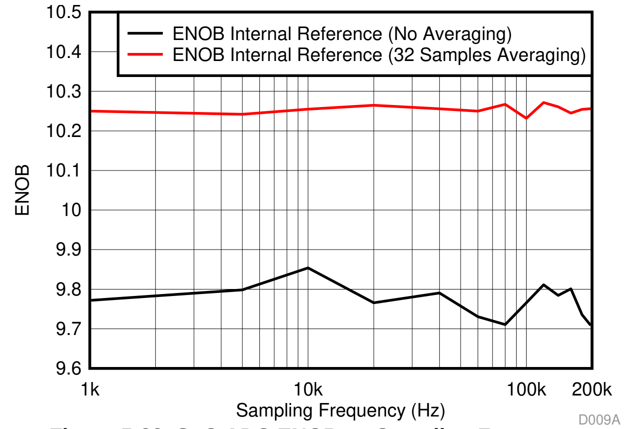


Figure 5-23. SoC ADC ENOB vs Sampling Frequency (Input Frequency = FS / 10)

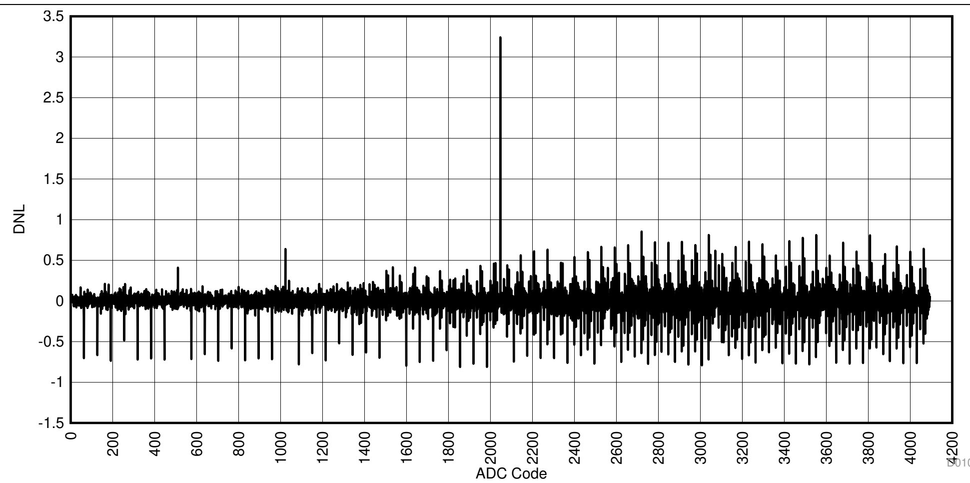


Figure 5-24. SoC ADC DNL vs ADC Code (Internal Reference)

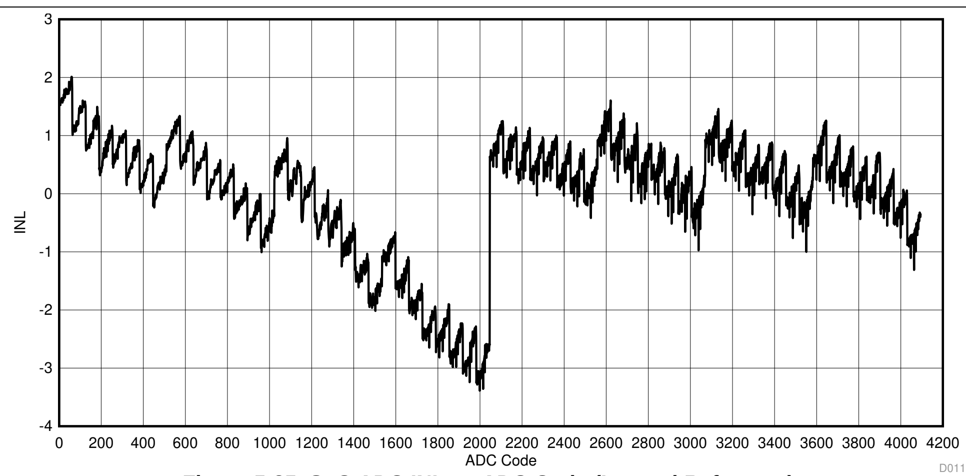


Figure 5-25. SoC ADC INL vs ADC Code (Internal Reference)

6 Detailed Description

6.1 Overview

Figure 6-1 shows the core modules of the CC2650MODA device.

6.2 Functional Block Diagram

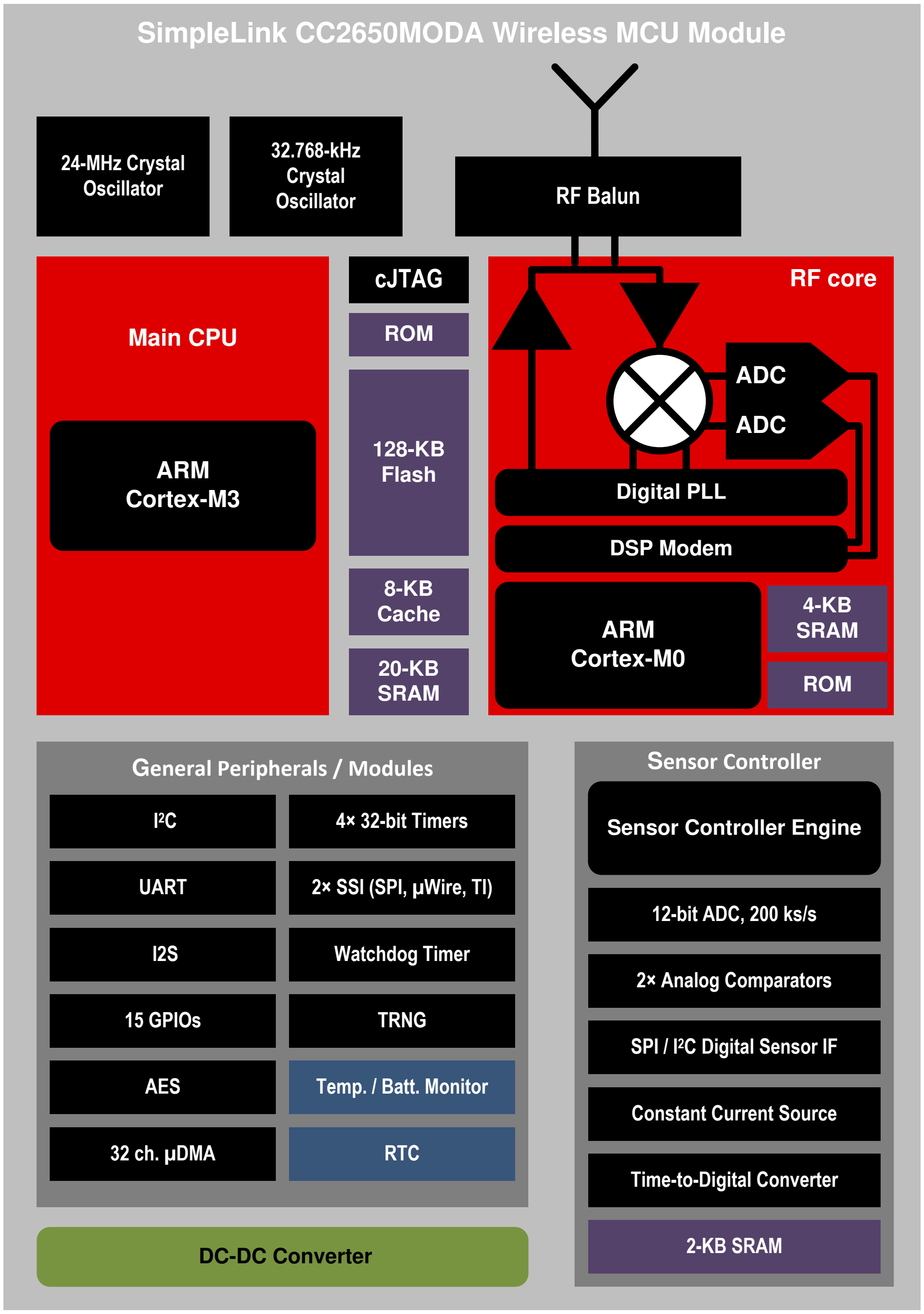


Figure 6-1. CC2650MODA Functional Block Diagram

6.3 Main CPU

The SimpleLink CC2650MODA wireless MCU contains an ARM Cortex-M3 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The Cortex-M3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Cortex-M3 features include:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low-power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.4 RF Core

The RF core contains an ARM Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high-level, command-based API to the main CPU.

The RF core can autonomously handle the time-critical aspects of the radio protocols (802.15.4 RF4CE and ZigBee, Bluetooth low energy) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The ARM Cortex-M0 processor is not programmable by customers.

6.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main Cortex-M3 CPU.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and typical use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs and bit-banged I^2C or SPI
- UART communication for sensor reading or debugging
- Capacitive sensing
- Waveform generation
- Pulse counting
- Keyboard scan
- Quadrature decoder for polling rotation sensors
- Oscillator calibration

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI/I^2C digital interface.
- The analog modules can be connected to up to eight different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1 lists the GPIOs that are connected to the Sensor Controller.

Table 6-1. GPIOs Connected to the Sensor Controller(1)

ANALOG CAPABLE	16.9 × 11 MOH DIO NUMBER
Y	14
Y	13
Y	12
Y	11
Y	9
Y	10
Y	8
Y	7
N	4
N	3
N	2
N	1
N	0

(1) Up to 13 pins can be connected to the Sensor Controller. Up to eight of these pins can be connected to analog modules

6.6 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8KB of cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI-RTOS kernel, Driverlib and lower layer protocol stack software (802.15.4 MAC and Bluetooth low energy Controller). The ROM also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.7 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.8 Power Management

To minimize power consumption, the CC2650MODA device supports a number of power modes and power-management features (see Table 6-2).

Table 6-2. Power Modes

MODE	SOFTWARE-CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.45 mA + 31 µA/MHz	550 µA	1 µA	0.15 µA	0.1 µA
Wake-up time to CPU active (1)	–	14 µs	151 µs	1015 µs	1015 µs
Register retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
High-speed clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-speed clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake up on RTC	Available	Available	Available	Off	Off
Wake up on pin edge	Available	Available	Available	Available	Off
Wake up on reset pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled (2)	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead
(2) The Brown Out Detector is disabled between recharge periods in STANDBY. Lowering the supply voltage below the BOD threshold between two recharge periods while in STANDBY may cause the BOD to lock the device upon wake-up until a Reset or POR releases it. To avoid this, TI recommends that STANDBY mode is avoided if there is a risk that the supply voltage (VDD) may drop below the specified operating voltage range. For the same reason, it is also good practice to ensure that a power cycling operation, such as a battery replacement, triggers a Power-on-reset by ensuring that the VDD decoupling network is fully depleted before applying supply voltage again (for example, inserting new batteries).

In active mode, the application Cortex-M3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 6-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake event, RTC event, or sensor-controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain and the Sensor Controller. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin, defined as a *wake from Shutdown pin*, wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU, which means that the main CPU does not have to wake up, for example, to execute an ADC sample or poll a digital sensor over SPI. The main CPU saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the sensor controller and choose which peripherals are controlled and which conditions wake up the main CPU.

6.9 Clock Systems

The CC2650MODA device supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. Bluetooth low energy requires a slow-speed clock with better than ±500-ppm accuracy if the device is to enter any sleep mode while maintaining a connection. The internal 32-kHz RC oscillator can in some use cases be compensated to meet the requirements. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48 MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768 kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.10 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities (marked in **bold** in Section 4).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps.

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I^2C interface is used to communicate with devices compatible with the I^2C standard. The I^2C interface is capable of 100-kHz and 400-kHz operation, and can serve as both I^2C master and I^2C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data transfer tasks from the Cortex-M3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except in Shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

6.11 System Architecture

Depending on the product configuration, CC26xx can function either as a Wireless Network Processor (WNP—an IC running the wireless protocol stack, with the application running on a separate MCU), or as a System-on-Chip (SoC), with the application and protocol stack running on the ARM Cortex-M3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

6.12 Certification

The CC2650MODA module is certified to the standards listed in Table 6-3 (with IDs where applicable).

Table 6-3. CC2650MODA List of Certifications

REGULATORY BODY	SPECIFICATION	ID (IF APPLICABLE)
FCC (USA)	Part 15C:2015 + MPE FCC 1.1307 RF Exposure (Bluetooth)	FCC ID: ZAT26M1
	Part 15C:2015 + MPE FCC 1.1307 RF Exposure (802.15.4)	
IC (Canada)	RSS-102 (MPE) and RSS-247 (Bluetooth)	ID: 451H-26M1
	RSS-102 (MPE) and RSS-247 (IEEE 802.15.4)	
ETSI/CE (Europe)	EN 300 328 V2.1.1 (Bluetooth)	
	EN 300 328 V2.1.1 (802.15.4)	
	EN 62479:2010 (MPE)	
	Draft EN 301 489-1 V2.2.0 (2017-03)	
	Draft EN 301 489-1 V3.2.0 (2017-03)	
	EN 55024:2010 + A1:2015	
	EN 55032:2015 + AC:2016-07	
	EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013	
Japan MIC	ARIB STD-T66	No: 201-160413/00
	JATE	D 16 0093 201/00

6.12.1 Regulatory Information Europe

Hereby, Texas Instruments Inc. declares that the radio equipment type CC2650MODA is in compliance with Directive 2014/53/EU.

The full text of the EU Declaration of Conformity (DoC) is available on the CC2650MODA technical documents page. The compliance has been verified in the operating frequency band of 2400 MHz to 2483.5 MHz. Developers and integrators that incorporate the CC2650MODA RF Module in any end products are responsible for obtaining applicable regulatory approvals for such end product.

NOTE

The CC2650MODA has been tested in the 2400-GHz to 2483.5-GHz ISM frequency band at 3.3 V with a maximum peak power of 5.056-dBm EIRP across the temperature range –40°C to +85°C and tolerance.

6.12.2 Federal Communications Commission Statement

You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference and
2. This device must accept any interference received, including interference that may cause undesired operation of the device.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be colocated or operating with any other antenna or transmitter.

6.12.3 Canada, Industry Canada (IC)

This device complies with Industry Canada licence-exempt RSS standards.

Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence

L'exploitation est autorisée aux deux conditions suivantes:

1. l'appareil ne doit pas produire de brouillage, et
2. l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

IC RF Radiation Exposure Statement:

To comply with IC RF exposure requirements, this device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas étre co-localisés ou fonctionnant en conjonction avec une autre antenne ou transmetteur.

6.12.4 Japan (JATE ID)

JATE ID is D 16 0093 201

For units already sold and marked with JATE ID: D 16 0086 201, please publicize to users that the JATE ID: D 16 0086 201 should be read as D 16 0093 201 (for example, clients web page, by software update, or similar).

6.13 End Product Labeling

This module is designed to comply with the FCC statement, FCC ID: ZAT26M1. The host system using this module must display a visible label indicating the following text:

"Contains FCC ID: ZAT26M1"

This module is designed to comply with the IC statement, IC: 451H-26M1. The host system using this module must display a visible label indicating the following text:

"Contains IC: 451H-26M1"

6.14 Manual Information to the End User

The OEM integrator must be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product that integrates this module.

NOTE

Operation outside of test conditions as documented in this datasheet is not supported and may void TI's warranty. Should the user choose to configure the CC2650MODA to operate outside of the test conditions, the device must be operated inside a protected and controlled environment, such as an RF shielded chamber and user must ensure compliance with regulatory requirements.

The end user's manual must include all required regulatory information and warnings as shown in this document.

6.15 Module Marking

Figure 6-2 shows the marking for the SimpleLink™ CC2650MODA module.

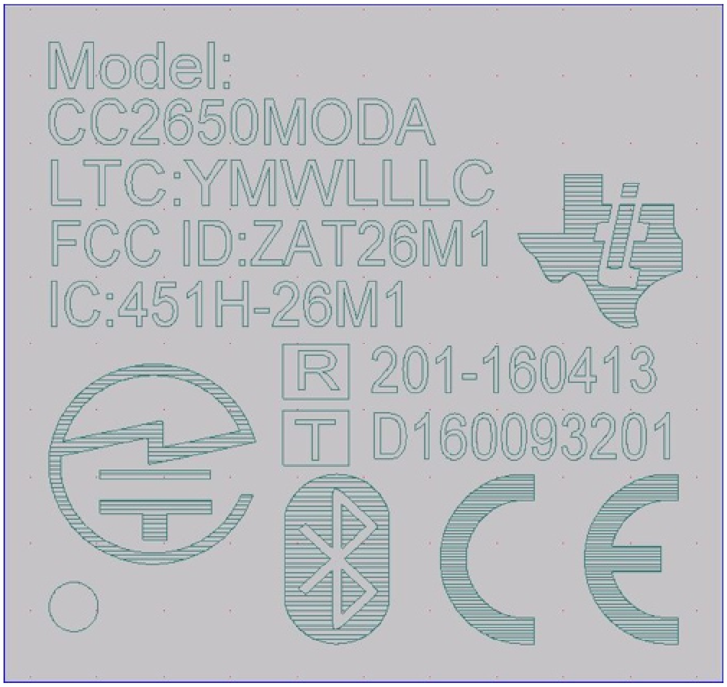


Figure 6-2. SimpleLink CC2650MODA Module Marking

Table 6-4. Module Descriptions

MARKING	DESCRIPTION
CC2650MODA	Model
YMWLLLC	LTC (lot trace code): • Y = Year • M = Month • WLLLLC = Reserved for internal use
ZAT26M1	FCC ID: single modular FCC grant ID
451H-26M1	IC: single modular IC grant ID
	MIC compliance mark
R 201-160413	JATE ID: Japan module grant ID
T D160093201	ARIB STD-T66 ID: Japan modular grant ID
	Bluetooth compliance mark
CE	CE compliance mark

7 Application, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

NOTE

TI does not recommend the use of conformal coating or similar material on the module. This coating can lead to localized stress on the solder connections inside the module and impact the module reliability. Use caution during the module assembly process to the final PCB to avoid the presence of foreign material inside the module.

7.1 Application Information

7.1.1 Typical Application Circuit

No external components are required for the operation of the CC2650MODA device. Figure 7-1 shows the application circuit.

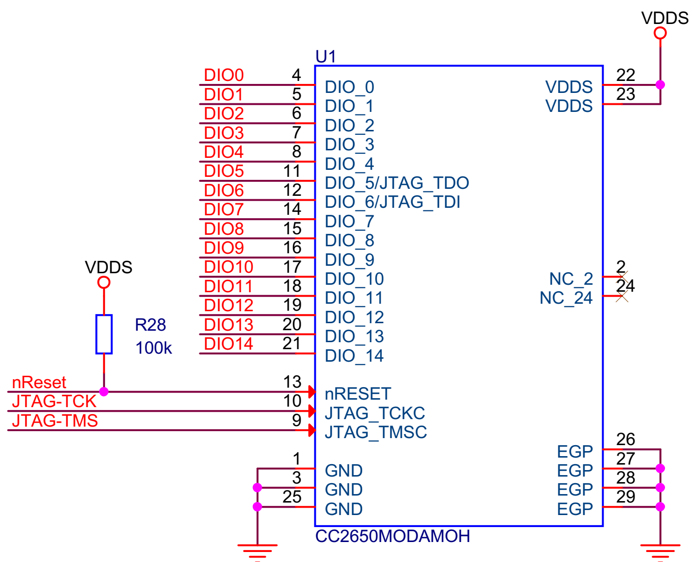


Figure 7-1. CC2650MODA Application Circuit

7.2 Layout

7.2.1 Layout Guidelines

Use the following guidelines to lay out the CC2650MODA device:

- The module must be placed close to the edge of the PCB.
- TI recommends leaving copper clearance on all PCB layers underneath the antenna area, as shown in Figure 7-2 and Figure 7-3.
- TI recommends using a generous amount of ground vias to stitch together the ground planes on different layers. Several ground vias should be placed close to the exposed ground pads of the module.
- No external decoupling is required.
- The reset line should have an external pullup resistor unless the line is actively driven. Placement of this component is not critical.
- TI recommends leaving a clearance in the top-side copper plane underneath the RF test pads.

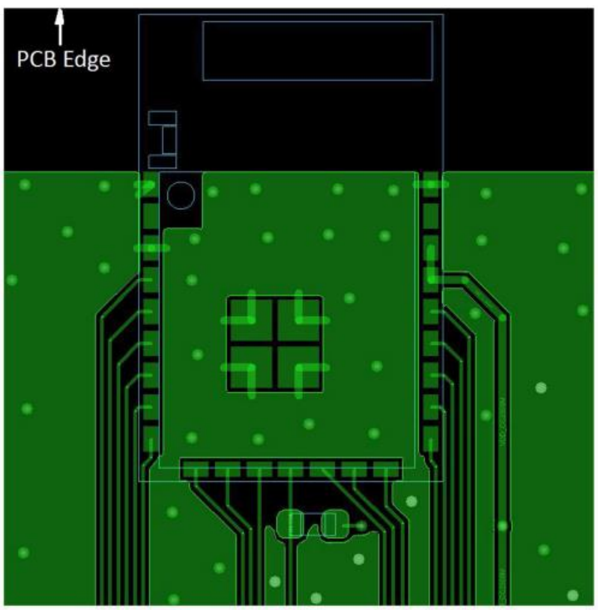


Figure 7-2. Top Layer

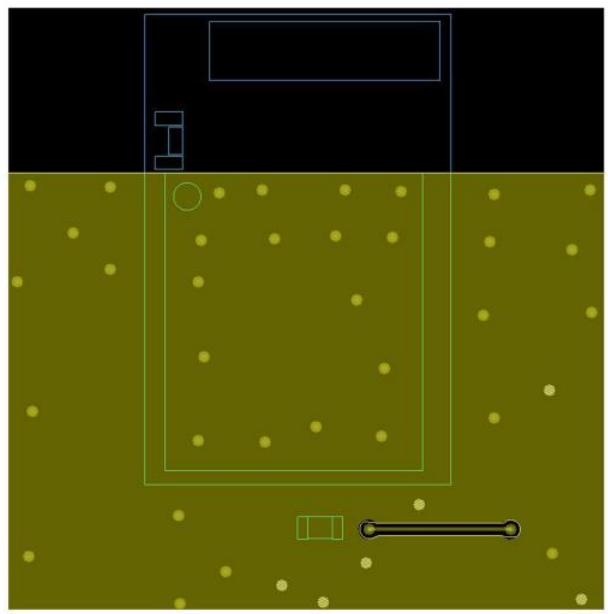


Figure 7-3. Bottom Layer

8 Environmental Requirements and Specifications

8.1 PCB Bending

The PCB follows IPC-A-600J for PCB twist and warpage < 0.75% or 7.5 mil per inch.

8.2 Handling Environment

8.2.1 Terminals

The product is mounted with motherboard through land-grid array (LGA). To prevent poor soldering, do not make skin contact with the LGA portion.

8.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product to malfunction.

8.3 Storage Condition

8.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product will be 12 months from the date the bag is sealed.

8.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

8.4 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12 to 24 hours

Baking times: 1 time

8.5 Soldering and Reflow Condition

- Heating method: Conventional convection or IR convection
- Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method
- Solder paste composition: Sn/3.0 Ag/0.5 Cu
- Allowable reflow soldering times: 2 times based on the reflow soldering profile (see Figure 8-1)
- Temperature profile: Reflow soldering will be done according to the temperature profile (see Figure 8-1)

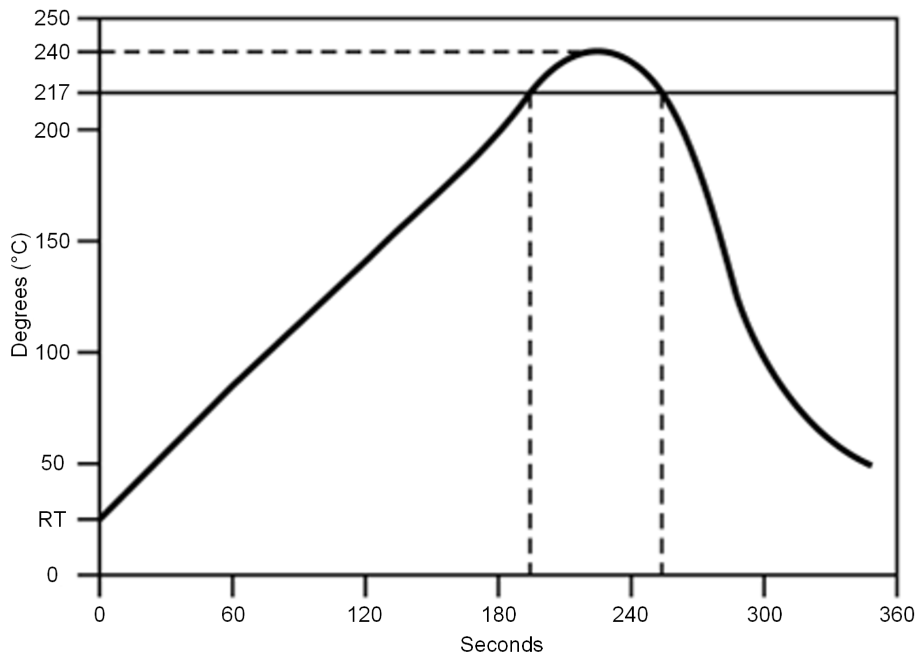


Figure 8-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)

Table 8-1. Temperature Profile

Profile Elements	Convection or IR(1)
Peak temperature range	235 to 240°C typical (260°C maximum)
Pre-heat / soaking (150 to 200°C)	60 to 120 seconds
Time above melting point	60 to 90 seconds
Time with 5°C to peak	30 seconds maximum
Ramp up	< 3°C / second
Ramp down	< -6°C / second

(1) For details, refer to the solder paste manufacturer's recommendation.

NOTE

TI does not recommend the use of conformal coating or similar material on the SimpleLink™ module. This coating can lead to localized stress on the solder connections inside the module and impact the module reliability. Use caution during the module assembly process to the final PCB to avoid the presence of foreign material inside the module.

9 器件和文档支持

9.1 器件命名规则

为了标明产品开发周期的各个产品阶段，TI 为所有部件号和/或日期代码添加了前缀。每个器件都具有以下三个前缀/标识中的一个：X、P 或无（无前缀）（例如 CC2650MODA 正在批量生产，因此未分配前缀/标识）。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如，MOH）。

要获得 MOH 封装类型的 CC2650MODA 器件部件号，请参见本文档的"封装选项附录"（TI 网站 www.ti.com.cn），或者联系您的 TI 销售代表。

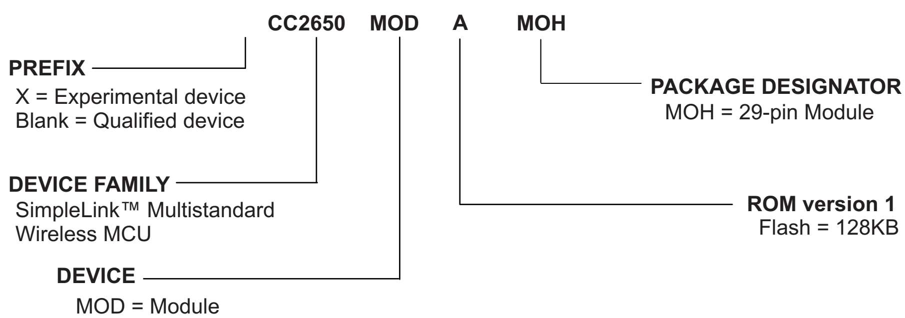


图 **9-1.** 器件命名规则

9.2 工具和软件

德州仪器 (TI) 提供大量的开发工具，其中包括评估处理器性能、生成代码、开发算法工具、以及完全集成和调试软件及硬件模块的工具。

下列产品为 CC2650MODA 器件 应用：

软件工具

SmartRF Studio 7:

SmartRF Studio 是一款 PC 应用程序，可帮助无线电系统设计人员评估早期设计过程的 RF-IC。

- 测试无线数据包收发功能，连续波收发功能
- 将相关数据写入支持的评估板或调试器，评估定制板上的 RF 性能
- 可以不搭配任何硬件使用，但此时只能生成、编辑并导出无线配置设置
- 可与德州仪器 (TI) CCxxxx 系列 RF-IC 的多款开发套件搭配使用

Sensor Controller Studio：

Sensor Controller Studio 为 CC26xx 传感器控制器提供开发环境。此传感器控制器是 CC26xx 系列中的一款专用功率优化型 CPU，可独立于系统 CPU 状态自主执行简单的后台任务。

- 允许使用 C 语言这类编程语言实现传感器控制器任务算法
- 输出传感器控制器接口驱动程序，其中整合了生成的传感器控制器机械代码和相关定义
- 通过使用集成传感器控制器任务测试和调试功能实现快速开发这有助于实现有效的传感器数据和算法验证可视化。

IDE 和编译器

Code Composer Studio：

- 带有项目管理工具和编辑器的集成开发环境
- Code Composer Studio (CCS) 6.1 及更高版本内置对 CC26xx 系列器件的支持功能。
- 优先支持的 XDS 调试器：XDS100v3、XDS110 和 XDS200
- 与 TI-RTOS 高度集成，支持 TI-RTOS 对象视图

IAR ARM Embedded Workbench

- 带有项目管理工具和编辑器的集成开发环境
- IAR EWARM 7.30.3 及更高版本内置对 CC26xx 系列器件的支持功能。
- 广泛的调试器支持，支持 XDS100v3、XDS200、IAR I-Jet 和 Segger J-Link
- 带有项目管理工具和编辑器的集成开发环境
- 适用于 TI-RTOS 的 RTOS 插件

有关 CC2650MODA 平台开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com.cn。有关售价和供货情况的信息，请联系最近的 TI 销售办事处或授权分销商。

9.3 文档支持

如需接收文档更新通知，请访问 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

以下文档对 CC2650MODA 器件进行了介绍。www.ti.com.cn 网站上提供了这些文档的副本。

符合性声明

《CC2650MODA EU 符合性声明 (DoC)》

勘误表

《CC2630 和 CC2650 SimpleLink™ 无线 MCU 勘误表》

技术参考手册

《CC13x0、CC26x0 SimpleLink™ 无线 MCU》

应用报告

《在 CC2650 模块 上运行独立 低功耗 Bluetooth® 应用》

《如何认证 Bluetooth(R) 低功耗产品》

用户指南

《CC2650 模块 BoosterPack™ 入门指南》

白皮书

《应该选择哪种 TI Bluetooth® 解决方案？》

更多文献

《借助经认证无线模块简化射频设计挑战》

9.4 德州仪器 (TI) 低功耗射频网站

TI 的低功耗射频网站提供所有最新产品、应用和设计笔记、FAQ 部分、新闻资讯以及活动更新。转至无线连接：TI 的 SimpleLink™ 低于 1GHz 无线 MCU。

9.5 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，您能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问：www.ti.com.cn/lprfnewsletter 立即注册

9.6 社区资源

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德州仪器 **(TI)** 嵌入式处理器 **Wiki** 此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

低功耗射频在线社区 TI E2E 支持社区的无线连接
- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

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- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

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9.11 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 机械、封装和可订购信息

10.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

10.2 PACKAGE OPTION ADDENDUM

10.2.1 PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
CC2650MODAMOHR	ACTIVE	QFM	MOH	29	1200	Green (RoHS & no Sb/Br)	ENIG	3, 250°C	–40 to 85	CC2650MODA

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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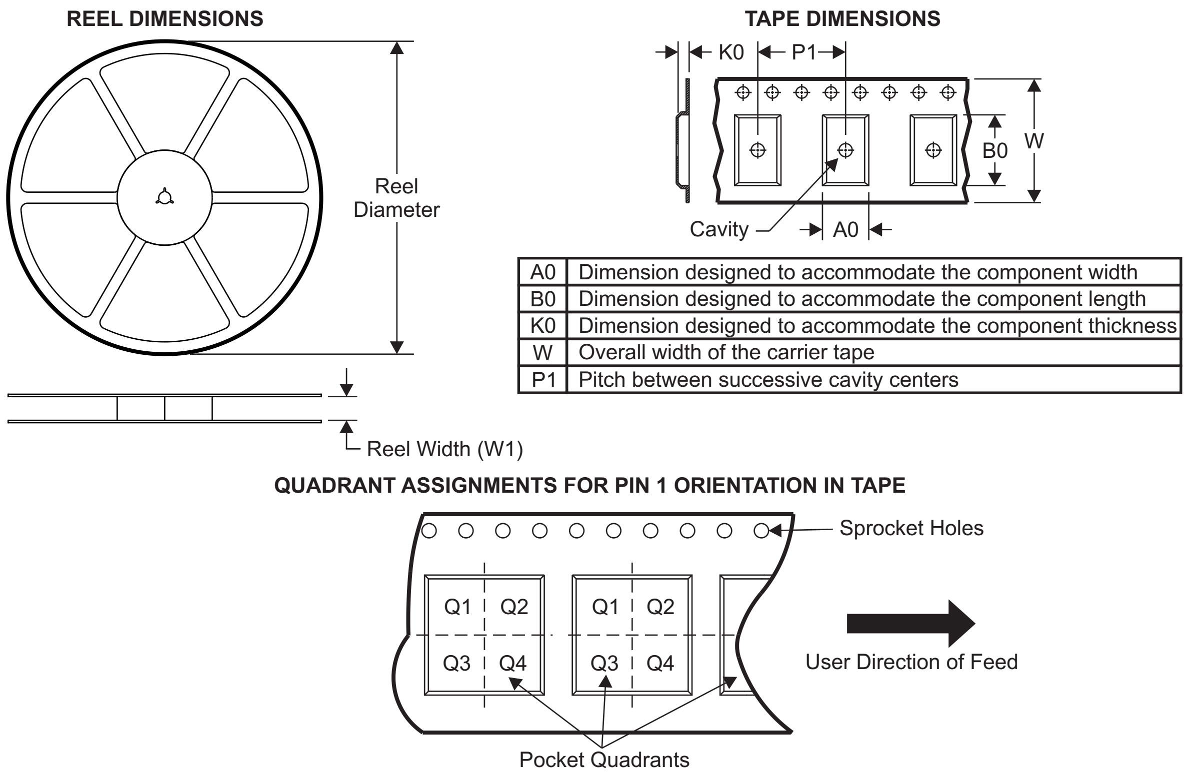
10.3 PACKAGE MATERIALS INFORMATION

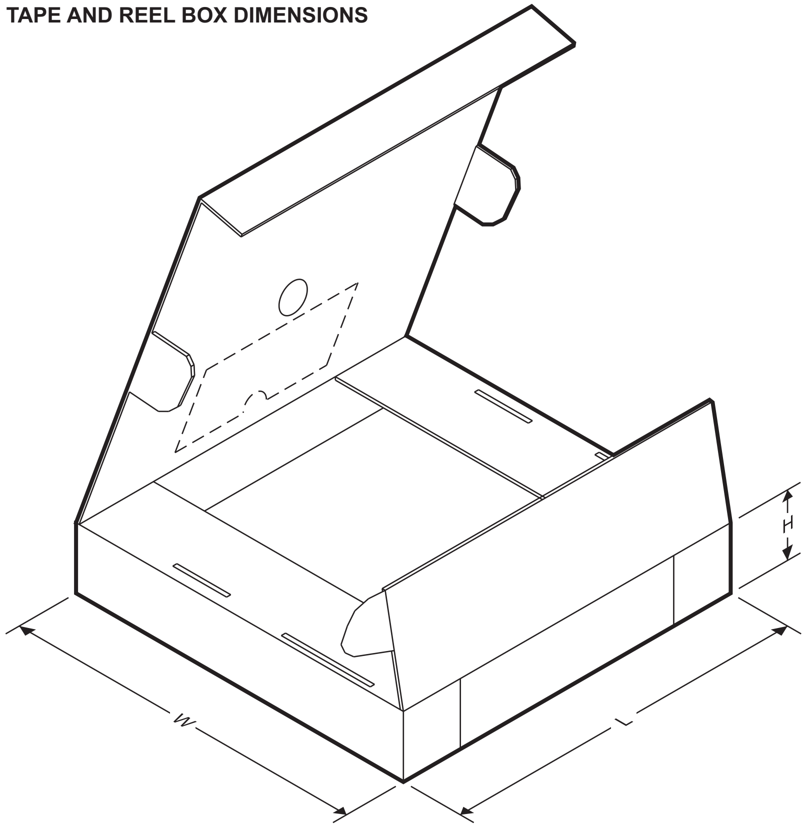
10.3.1 TAPE AND REEL INFORMATION



All dimensions are nominal.

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2650MODAMOHR	QFM	MOH	29	1200	330	32.5	11.4	17.4	2.9	16	32	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2650MODAMOHR	QFM	MOH	29	1200	352	348	56

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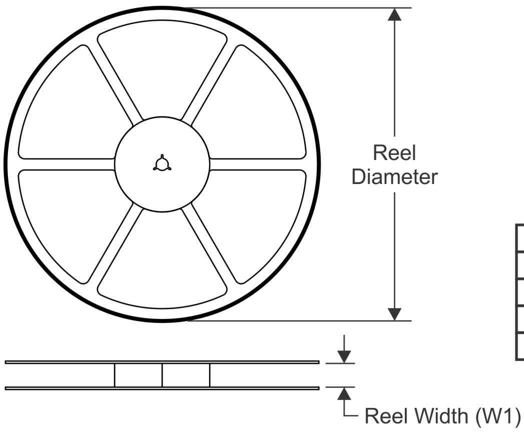
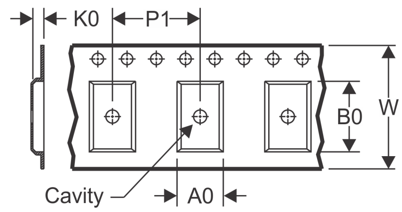
TAPE AND REEL INFORMATION

REEL DIMENSIONS

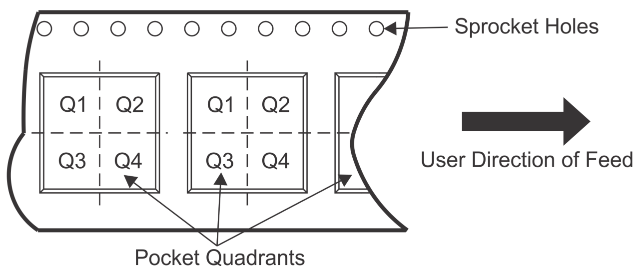


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

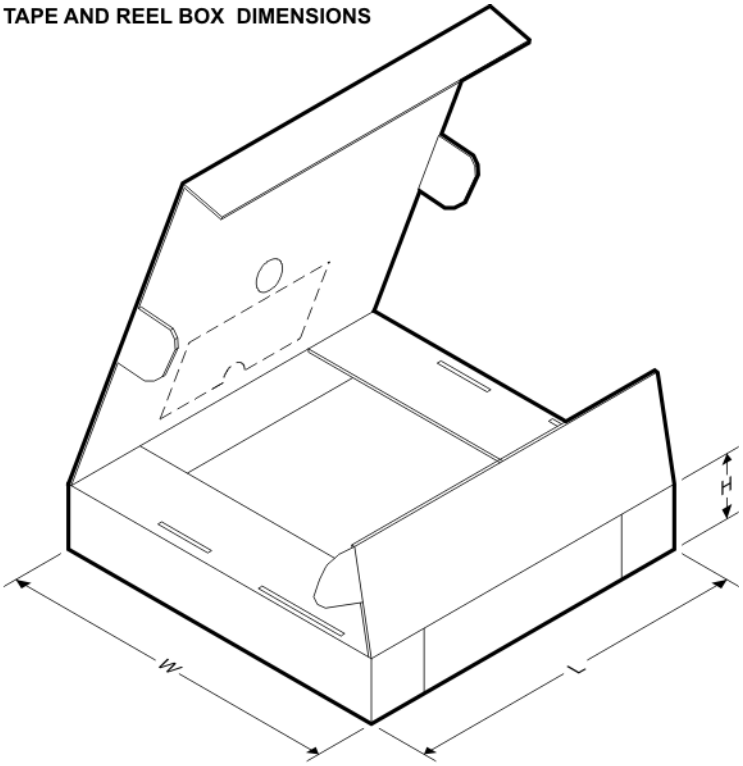
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

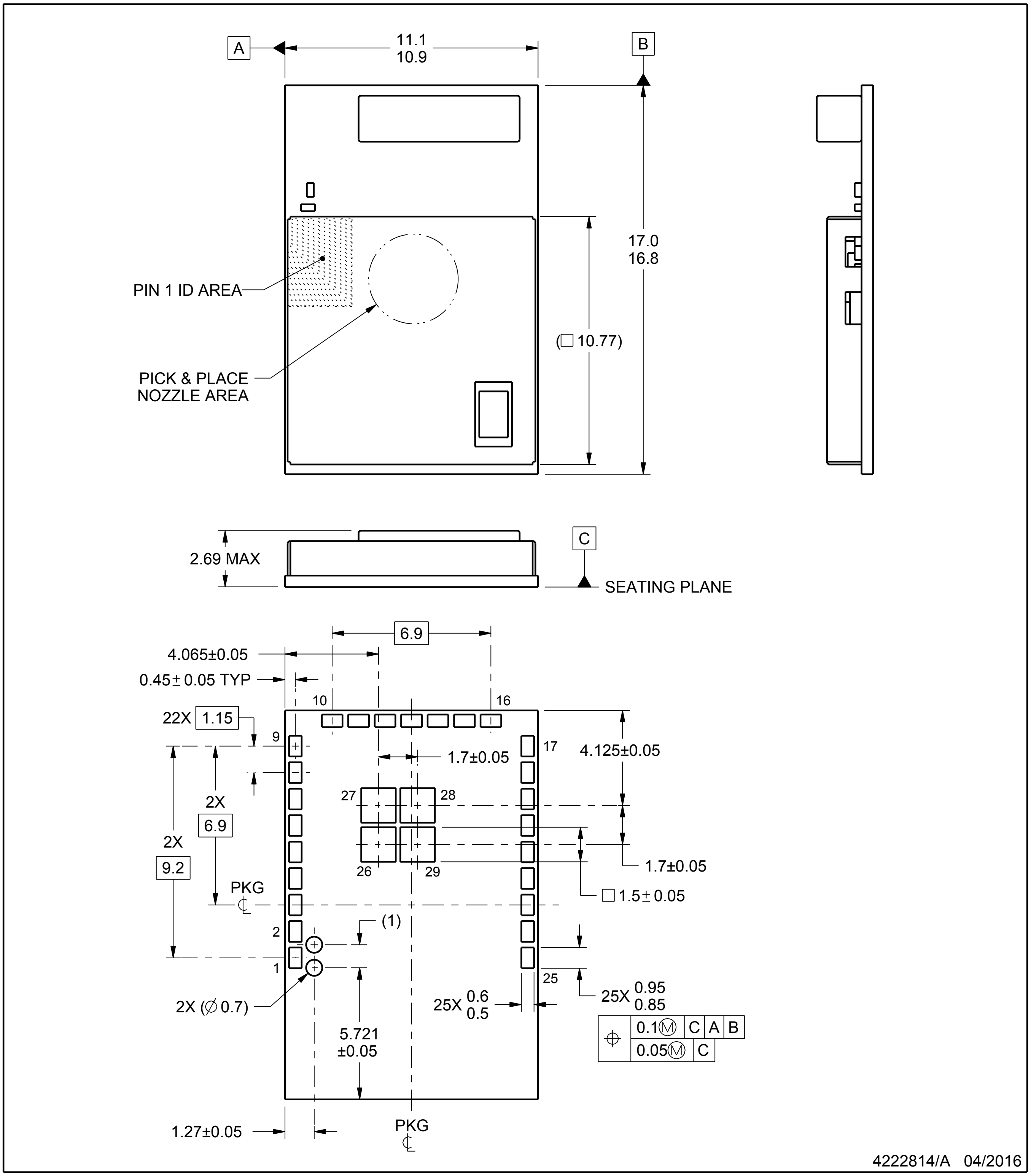
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2650MODAMOHR	QFM	MOH	29	1200	330.0	32.4	11.4	17.4	2.9	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



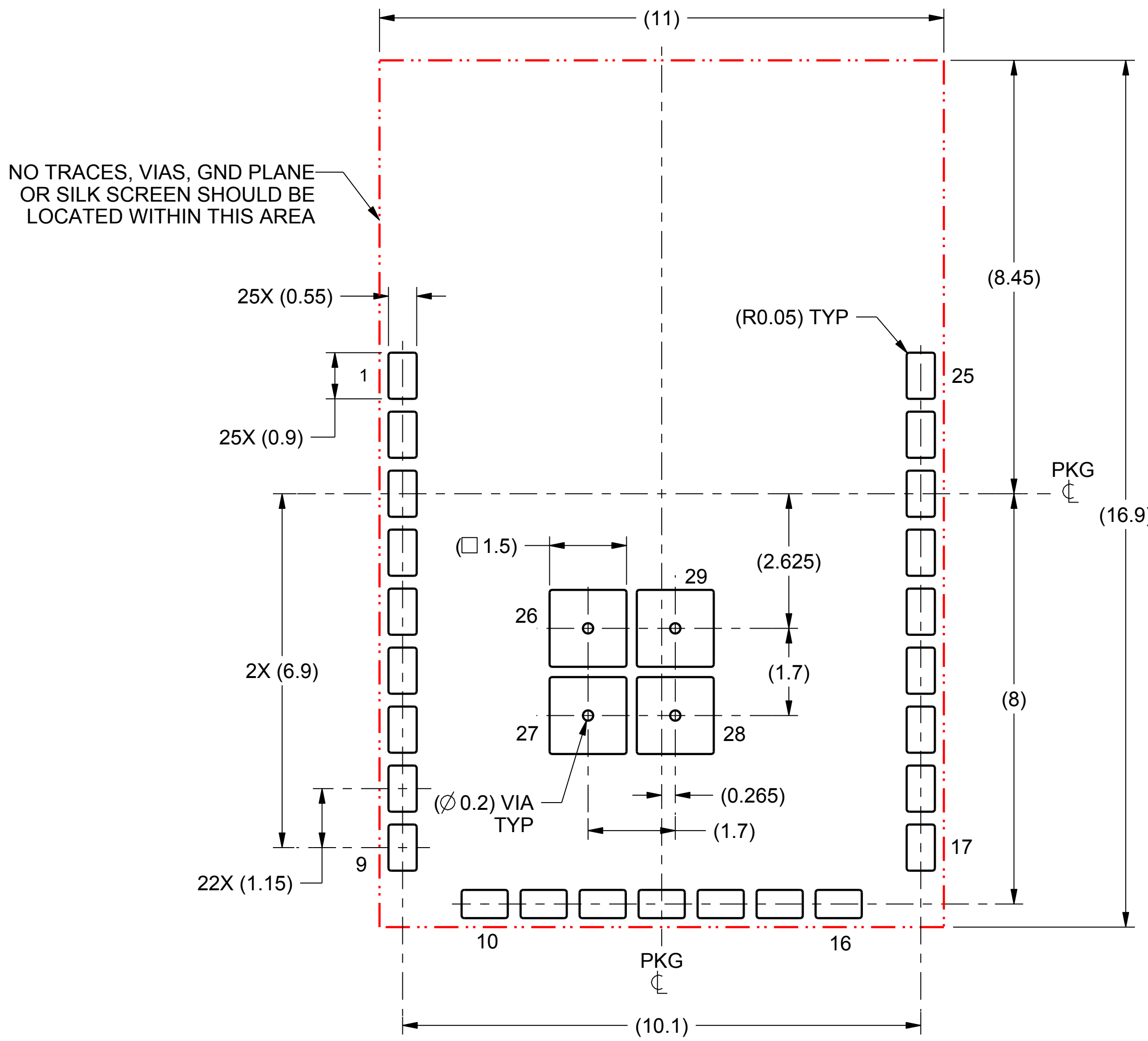
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2650MODAMOHR	QFM	MOH	29	1200	383.0	353.0	58.0

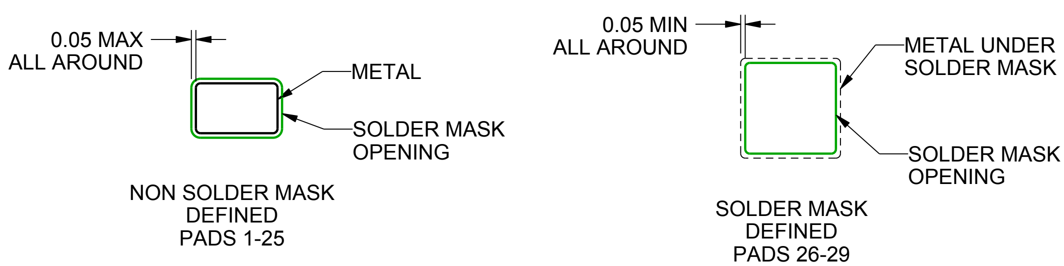


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:7X

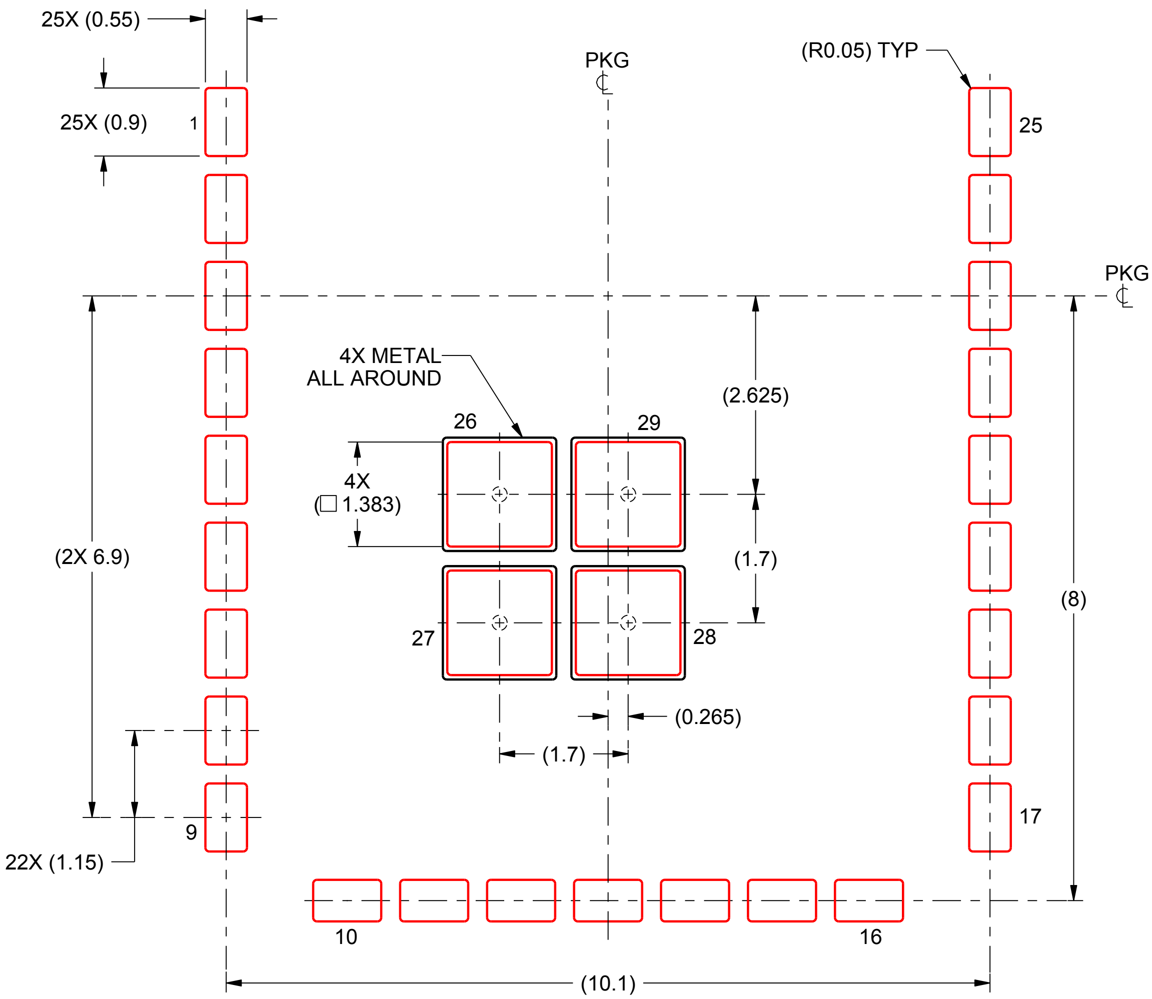


SOLDER MASK DETAILS

4222814/A 04/2016

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 26-29: 85%
SCALE:10X

4222814/A 04/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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