

CC330x SimpleLink™ Wi-Fi 6 和低功耗 Bluetooth® 配套 IC

1 特性

关键特性

- Wi-Fi 6 (802.11ax)
- CC330x1 器件中的低功耗 Bluetooth® 5.4
- 能够运行 TCP/IP 堆栈的任何处理器或 MCU 主机的配套 IC
- 集成 2.4GHz PA，适用于输出功率高达 +20.5dBm 的完整无线解决方案。
- 工作温度：-40°C 至 +105°C
- 应用吞吐量高达 50Mbps

扩展特性

- Wi-Fi 6
 - 2.4GHz、20MHz、单空间流
 - 支持 IEEE 802.11 b/g/n/ax 的 MAC、基带和射频收发器
 - 目标唤醒时间 (TWT)、OFDMA、MU-MIMO (下行链路)、基本服务集着色和触发帧，可提高效率
 - 基于硬件的加密和解密，支持 WPA2 和 WPA3
 - 出色的互操作性
 - 支持 4 位 SDIO 或 SPI 主机接口
- 低功耗蓝牙 5.4
 - LE 编码 PHY (远距离)、LE 2M PHY (高速) 和广播扩展
 - 主机控制器接口 (HCI) 传输，具有 UART 或共享 SDIO 的选项
- 增强的安全性
 - 安全主机接口
 - 固件身份验证
 - 防回滚保护
- 多角色支持 (例如，并发 STA 和 AP)，可连接不同射频通道 (Wi-Fi 网络) 上的 Wi-Fi 设备
- 可选天线分集或选择
- 3 线或 1 线 PTA，用于与额外 2.4GHz 无线电 (例如 Thread 或 Zigbee) 在外部共存
- 电源管理
 - V_{MAIN} 、 V_{IO} 、 V_{pp} : 1.8V
 - V_{PA} : 3.3V
- 时钟源
 - 40MHz XTAL 快速时钟
 - 内部慢速时钟或外部 32.768kHz 慢速时钟
- 小封装尺寸
 - 易于设计，采用 40 引脚 5mm x 5mm 四方扁平无引线 (QFN) 封装，间距为 0.4mm

2 应用

- 电网基础设施
 - 电量计
 - 串式逆变器
 - 微型逆变器
 - 能量存储电源转换系统 (PCS)
 - 电动汽车充电基础设施
- 楼宇和家居自动化
 - HVAC 控制器
 - HVAC 网关
 - 恒温器
 - 楼宇安全网关
 - 车库门系统
 - IP 网络摄像头/可视门铃
 - 无线安防摄像头
- 电器
 - 冰箱和冷冻柜
 - 烤箱
 - 洗衣机和烘干机
 - 住宅热水器和供暖系统
 - 空气净化器和加湿器
 - 咖啡机
 - 空调室内机
 - 扫地机器人
 - 割草机器人
- 医疗
 - 输液泵
 - 电子病床和床控制器
 - 多参数患者监护仪
 - 血压监护仪
 - CPAP 呼吸机
 - 远程保健系统
 - 超声波扫描仪
 - 超声波智能探头
 - 电动牙刷
- 零售自动化和支付
- 打印机



3 说明

SimpleLink™ Wi-Fi CC33xx 系列器件兼具经济性和可靠性，可支持工程师放心地连接更多应用。CC33xx 是单芯片 Wi-Fi 6 和低功耗蓝牙 5.4 器件。CC3300 和 CC3301 是此引脚对引脚兼容系列中的首批器件。

- **CC3300** : 2.4GHz Wi-Fi 6 配套 IC。
- **CC3301** : 2.4GHz Wi-Fi 6 和低功耗蓝牙 5.4 配套 IC。

CC330x 提供 Wi-Fi 6 和 BLE，同时与 Wi-Fi 4 (802.11 b/g/n) 和 Wi-Fi 5 (802.11ac) 保持兼容。这些 CC330x 器件是德州仪器 (TI) 的第 10 代连接组合芯片。因此，CC330x 基于成熟的技术设计而成。这些器件非常适合用在通过 Linux 或 RTOS 主机运行 TCP/IP 的成本敏感型嵌入式应用中，CC330x 为物联网 (IoT) 的嵌入式设备应用带来了 Wi-Fi 6 的效率，并具有较小的 PCB 尺寸和高度优化的物料清单。

器件信息

| 器件型号 | Wi-Fi 2.4GHz SISO | 蓝牙低功耗 |
|----------------|-------------------|-------|
| CC3300ENJARSBR | ✓ | |
| CC3301ENJARSBR | ✓ | ✓ |

4 系统图

图 4-1 显示了 CC3301 的基本系统图。

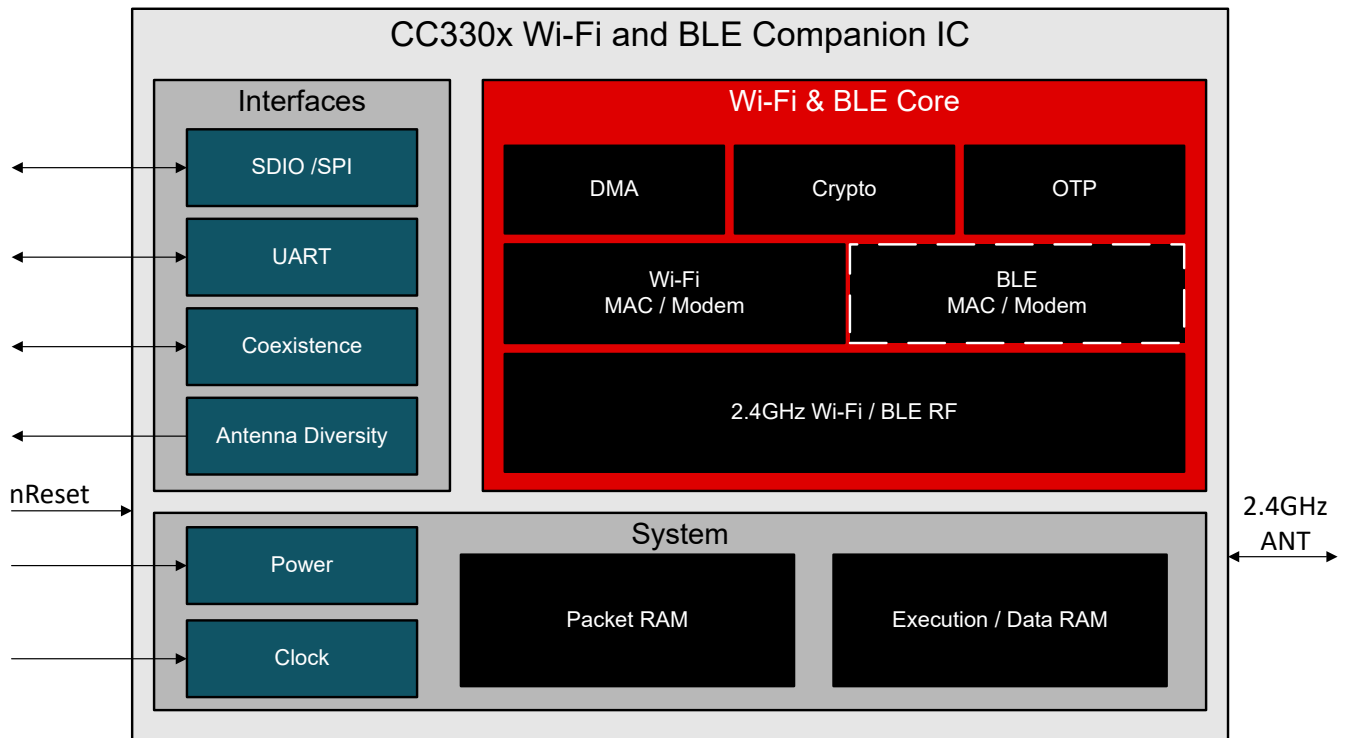


图 4-1. CC3301 系统简图

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5 Terminal Configuration and Functions

5.1 Pin Diagram

图 5-1 shows pin assignments for the 40-pin WQFN package.

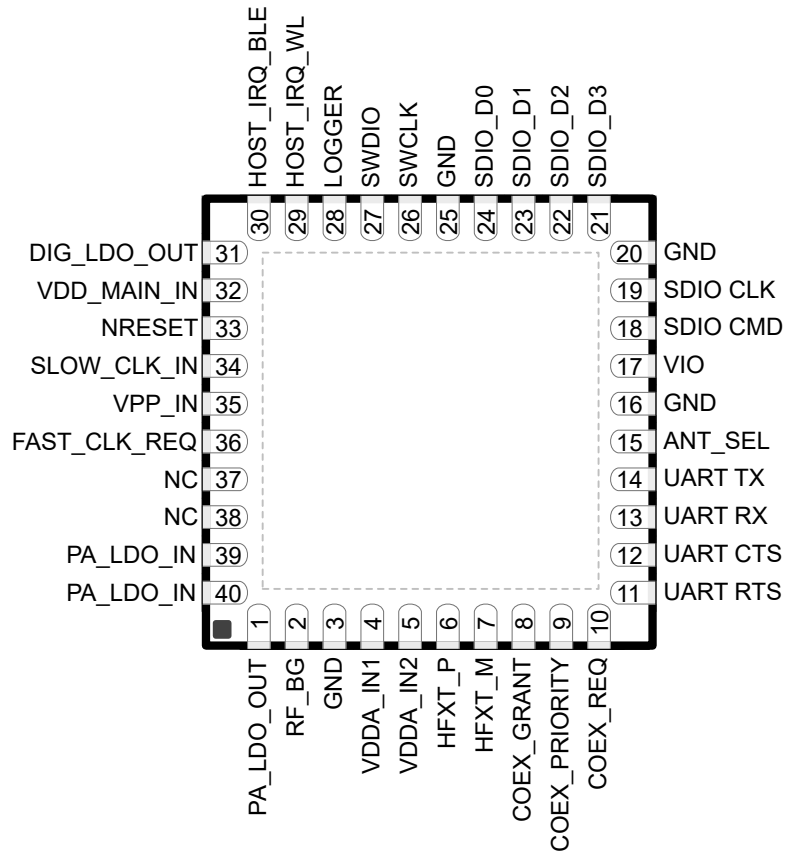


图 5-1. CC3301 Pin Diagram

5.2 Pin Attributes

表 5-1. Pin Attributes

| PIN | SIGNAL NAME | TYPE | DIR (I/O) | VOLTAGE LEVEL | SHUTDOWN STATE | STATE AFTER POWER-UP | DESCRIPTION |
|-----|----------------------------|---------|-----------|-----------------|----------------|----------------------|---|
| 1 | PA_LDO_OUT | Analog | | | | | RF power amplifier LDO output |
| 2 | RF_BG | RF | I/O | | | | Bluetooth Low Energy and WLAN 2.4-GHz RF port |
| 3 | GND | GND | | | | | GND |
| 4 | VDDA_IN1 | POW | | | | | 1.8 V supply for analog domain |
| 5 | VDDA_IN2 | POW | | | | | 1.8 V supply for analog domain |
| 6 | HFXT_P | Analog | | Sine | | | XTAL_P |
| 7 | HFXT_M | Analog | | | | | XTAL_N |
| 8 | COEX_GRANT ² | Digital | O | V _{IO} | PD | PD | External coexistence interface - grant |
| 9 | COEX_PRIORITY ² | Digital | I | V _{IO} | PU | PU | External coexistence interface - priority |
| 10 | COEX_REQ ² | Digital | I | V _{IO} | PU | PU | External coexistence interface - request |
| 11 | UART RTS | Digital | O | V _{IO} | PU | PU | Device RTS signal - flow control for BLE HCI |
| 12 | UART CTS | Digital | I | V _{IO} | PU | PU | Device CTS signal - flow control for BLE HCI |
| 13 | UART RX | Digital | I | V _{IO} | PU | PU | UART RX for BLE HCI |
| 14 | UART TX | Digital | O | V _{IO} | PU | PU | UART TX for BLE HCI |
| 15 | ANT_SEL ² | Digital | O | V _{IO} | PD | PD | Antenna select control line |
| 16 | GND | GND | | | | | GND |
| 17 | VIO | POW | | | | | 1.8 V IO supply |
| 18 | SDIO CMD | Digital | I/O | V _{IO} | HiZ | HiZ | SDIO command or SPI PICO |
| 19 | SDIO CLK | Digital | I | V _{IO} | HiZ | HiZ | SDIO clock or SPI clock |
| 20 | GND | GND | | | | | GND |
| 21 | SDIO D3 | Digital | I/O | V _{IO} | HiZ | PU | SDIO data D3 or SPI CS |
| 22 | SDIO D2 | Digital | I/O | V _{IO} | HiZ | HiZ | SDIO data D2 |
| 23 | SDIO D1 | Digital | I/O | V _{IO} | HiZ | HiZ | SDIO data D1 |
| 24 | SDIO D0 | Digital | I/O | V _{IO} | HiZ | HiZ | SDIO data D0 or SPI POCI |
| 25 | GND | GND | | | | | GND |
| 26 | SWCLK | Digital | I | V _{IO} | PD | PD | Serial wire debug clock |
| 27 | SWDIO | Digital | I/O | V _{IO} | PU | PU | Serial wire debug I/O |
| 28 | LOGGER ³ | Digital | O | V _{IO} | PU | PU | Tracer (UART TX debug logger) |
| 29 | HOST_IRQ_WL ³ | Digital | O | V _{IO} | PD | 0 | Interrupt request to host for WLAN |

表 5-1. Pin Attributes (续)

| PIN | SIGNAL NAME | TYPE | DIR (I/O) | VOLTAGE LEVEL | SHUTDOWN STATE | STATE AFTER POWER-UP | DESCRIPTION |
|-----|---------------------------|---------|-----------|-----------------|----------------|----------------------|--|
| 30 | HOST_IRQ_BLE ³ | Digital | O | V _{IO} | PD | PD | Interrupt request to host for BLE (in shared SDIO mode) |
| 31 | DIG_LDO_OUT | Analog | O | | | | Digital LDO output to decoupling capacitor |
| 32 | VDD_MAIN_IN | POW | | | | | 1.8 V supply input for SRAM and digital |
| 33 | nRESET | Digital | I | V _{IO} | PD | PD | Reset line for enabling or disabling device (active low) |
| 34 | SLOW_CLK_IN | Digital | I | V _{IO} | PD | PD | 32.768-kHz RTC clock input |
| 35 | VPP_IN | POW | | | | | 1.8 V OTP programming input supply |
| 36 | FAST_CLK_REQ | Digital | O | V _{IO} | PD | PD | Fast clock request from the device |
| 37 | NC | NC | | | | | Connect to GND |
| 38 | NC | NC | | | | | Connect to GND |
| 39 | PA_LDO_IN | POW | | | | | 3.3 V supply for PA |
| 40 | PA_LDO_IN | POW | | | | | 3.3 V supply for PA |

1. All digital I/O's (with the exception of SDIO signals) are Hi-Z when the device is in shutdown mode with internal PU/PD according to the "shutdown state" column.
2. See software release notes for support level.
3. LOGGER and HOST_IRQ_WL pins are sensed by the device during boot, see [CC33xx Hardware Integration](#).

6 Specifications

All specifications are given at the CC3301 pins. Typical values are measured with nominal device at 25°C.

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | PINS | MIN | MAX | UNIT |
|-------------------|--|----------|-------|-----------------------|------|
| V _{PA} | V _{DD} PA Voltage | 39,40 | - 0.5 | 4.2 | V |
| V _{MAIN} | Main supply voltage for analog and digital - VDD_MAIN_IN, VDDA_IN1, VDDA_IN2 | 32, 4, 5 | - 0.5 | 2.1 | V |
| V _{IO} | VDD IO Voltage | 17 | - 0.5 | 2.1 | V |
| | Input Voltage to all digital pins | | - 0.5 | V _{IO} + 0.5 | V |
| | HFXT_P Input Voltage | 6 | - 0.5 | 2.1 | V |
| V _{PP} | VPP OTP Voltage | 35 | - 0.5 | 2.1 | V |
| T _A | Operating Ambient Temperature | | - 40 | 105 | °C |
| T _{stg} | Storage temperature | | - 55 | 155 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | | VALUE | UNIT |
|--------------------|-------------------------|---|------------|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | RF pins | ±1000 | V |
| | | | Other pins | ±2000 | |
| | | Charged device model (CDM), per AEC Q100-011 | RF pins | ±250 | |
| | | | Other pins | ±500 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | PINS | MIN | TYP | MAX | UNIT |
|-------------------|--|--------|------|-----|-----------------------|------|
| V _{MAIN} | Main supply voltage digital and analog - VDD_MAIN_IN, VDDA_IN1, VDDA_IN2 | 32,4,5 | 1.62 | 1.8 | 1.98 | V |
| V _{PA} | DC supply rail for PA | 39,40 | 3 | 3.3 | 3.6 | |
| V _{IO} | DC supply rail for input/output | 17 | 1.62 | 1.8 | 1.98 | |
| V _{PP} | DC supply rail for OTP memory | 35 | 1.62 | 1.8 | 1.98 | |
| T _A | Operating ambient temperature | | - 40 | | 85/105 ⁽¹⁾ | °C |
| | Maximum power dissipation | | | | 2 | W |

- (1) The CC3300 and CC3301 devices may operate at temperatures of up to 105°C. This allows the device to be used reliably in applications that may be exposed to higher ambient temperature over certain periods of the product's life. At temperatures higher than 85°C, the WLAN/BLE performance may degrade.

6.4 Electrical Characteristics

| PARAMETER | DESCRIPTION | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------|----------------|------------------------|-----|------------------------|------|
| V _{IH} | High Level Input Voltage | | 0.65 x V _{IO} | | V _{IO} | V |
| V _{IL} | Low Level Input Voltage | | 0 | | 0.35 x V _{IO} | |
| V _{OH} | High Level Output Voltage | at 4mA | V _{IO} - 0.45 | | V _{IO} | |
| V _{OL} | Low Level Output Voltage | at 4mA | 0 | | 0.45 | |

6.5 Thermal Resistance Characteristics

| THERMAL METRIC ⁽¹⁾ | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------------------|--|------|-----|-----|------|
| R _{θJA} | Junction-to-ambient thermal resistance (According to JEDEC EIA/JESD 51 document) | 30.5 | | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 16.7 | | | |
| R _{θJB} | Junction-to-board thermal resistance | 10 | | | |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.1 | | | |
| Ψ _{JB} | Junction-to-board characterization parameter | 10 | | | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 1.7 | | | |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 WLAN Performance: 2.4-GHz Receiver Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------|------|-------|------|------|
| Operational Frequency Range | | 2412 | | 2472 | MHZ |
| Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates | 1 Mbps DSSS | | -98 | | dBm |
| | 2 Mbps DSSS | | -95.3 | | |
| | 11 Mbps CCK | | -90 | | |
| | 6 Mbps OFDM | | -93.2 | | |
| | 54 Mbps OFDM | | -75.5 | | |
| | HT MCS0 MM 4K | | -93 | | |
| | HT MCS7 MM 4K | | -72.9 | | |
| | HE MCS0 4K | | -92.7 | | |
| Maximum input level: 8% PER for 11b rates, 10% PER for 11g/n/ax rates | 1 DSSS | | 0 | | dBm |
| | OFDM6, HT MCS0, HE MCS0 | | 0 | | |
| | OFDM54, HT MCS7, HE MCS7 | | -9 | | |
| Adjacent Channel Rejection | 1 Mbps DSSS | | 45 | | dB |
| | 11 Mbps CCK | | 39 | | |
| | 6 Mbps OFDM | | 20 | | |
| | 54 Mbps OFDM | | 3 | | |
| | HT MCS0 | | 20 | | |
| | HT MCS7 | | 3 | | |
| | HE MCS0 | | 16 | | |
| HE MCS7 | | -1 | | | |
| RSSI Accuracy | -90 dBm to -30dBm | -3 | | 3 | dB |

6.7 WLAN Performance: 2.4-GHz Transmitter Power

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|------|------|------|------|
| Operational Frequency Range | | 2412 | | 2472 | MHz |
| Maximum output power at $V_{PA} > 3.0$ V | 1 Mbps DSSS | | 20.5 | | dBm |
| | 6 Mbps OFDM | | 20.2 | | |
| | 54 Mbps OFDM | | 17.4 | | |
| | HT MCS0 MM | | 20.2 | | |
| | HT MCS7 MM | | 17.4 | | |
| | HE MCS0 | | 20.2 | | |
| | HE MCS7 | | 17.3 | | |

6.8 BLE Performance: Receiver Characteristics

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--|--|-----|-----------|-----|------|
| BLE 125Kbps (LE Coded) Receiver Characteristics | | | | | |
| Receiver sensitivity | PER <30.2% | | -102.2 | | dBm |
| Receiver saturation | PER <30.2% | | 0 | | dBm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at -79 dBm, modulated interferer in channel | | 10 | | dB |
| Selectivity, ± 1 MHz ⁽¹⁾ | Wanted signal at -79 dBm, modulated interferer at ± 1 MHz. | | 0 / 0 | | dB |
| Selectivity, ± 2 MHz ⁽¹⁾ | Wanted signal at -79 dBm, modulated interferer at ± 2 MHz. | | -37 / -30 | | dB |
| Selectivity, ± 3 MHz ⁽¹⁾ | Wanted signal at -79 dBm, modulated interferer at ± 3 MHz. | | -39 / -36 | | dB |
| Selectivity, ± 4 MHz ⁽¹⁾ | Wanted signal at -79 dBm, modulated interferer at ± 4 MHz. | | -45 / -41 | | dB |
| RSSI Accuracy | Dynamic range of -90 to -20dBm | -4 | | 4 | dB |
| BLE 500Kbps (LE Coded) Receiver Characteristics | | | | | |
| Receiver sensitivity | PER <30.2% | | -99.8 | | dBm |
| Receiver saturation | PER <30.2% | | 0 | | dBm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at -72 dBm, modulated interferer in channel. | | 10 | | dB |
| Selectivity, ± 1 MHz ⁽¹⁾ | Wanted signal at -72 dBm, modulated interferer at ± 1 MHz. | | 0 / 0 | | dB |
| Selectivity, ± 2 MHz ⁽¹⁾ | Wanted signal at -72 dBm, modulated interferer at ± 2 MHz. | | -35 / -25 | | dB |
| Selectivity, ± 3 MHz ⁽¹⁾ | Wanted signal at -72 dBm, modulated interferer at ± 3 MHz. | | -40 / -37 | | dB |
| Selectivity, ± 4 MHz ⁽¹⁾ | Wanted signal at -72 dBm, modulated interferer at ± 4 MHz. | | -45 / -40 | | dB |
| RSSI Accuracy | Dynamic range of -90 to -20dBm | -4 | | 4 | dB |
| BLE 1Mbps (LE 1M) Receiver Characteristics | | | | | |
| Receiver sensitivity ⁽²⁾ | PER <30.2%, 37-byte packets | | -99.4 | | dBm |
| Receiver sensitivity ⁽²⁾ | PER <30.2%, 255 byte-packets | | -98.1 | | dBm |
| Receiver saturation | PER <30.2% | | 0 | | dBm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer in channel | | 10 | | dB |

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--|---|-----|-----------|-----|------|
| Selectivity, ±1 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±1 MHz | | 0 / 0 | | dB |
| Selectivity, ±2 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±2 MHz. | | -35 / -28 | | dB |
| Selectivity, ±3 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±3 MHz | | -38 / -32 | | dB |
| Selectivity, ±4 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±4 MHz | | -45 / -40 | | dB |
| Out-of-band blocking | 30 MHz to 2000 MHz, Wanted signal at -67 dBm | | - 23 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz, Wanted signal at -67 dBm | | - 30 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz, Wanted signal at -67 dBm | | - 30 | | dBm |
| Out-of-band blocking | 3000 MHz to 6 GHz, Wanted signal at -67 dBm | | - 21 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level | | - 40 | | dBm |
| RSSI accuracy | Dynamic range of -90 to -20dBm | -4 | | 4 | dB |
| BLE 2Mbps (LE 2M) Receiver Characteristics | | | | | |
| Receiver sensitivity ⁽³⁾ | PER <30.2% | | -95.2 | | dBm |
| Receiver saturation | PER <30.2% | | 0 | | dBm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer in channel | | 10 | | dB |
| Selectivity, ±2 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±2 MHz. | | 0 / 0 | | dB |
| Selectivity, ±4 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±4 MHz | | -35 / -28 | | dB |
| Selectivity, ±6 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±6 MHz | | -35 / -28 | | dB |
| Alternate channel rejection, ±8 MHz ⁽¹⁾ | Wanted signal at -67 dBm, modulated interferer at ±8 MHz | | -37 / -32 | | dB |
| Out-of-band blocking | 30 MHz to 2000 MHz, Wanted signal at -67 dBm | | - 23 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz, Wanted signal at -67 dBm | | - 30 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz, Wanted signal at -67 dBm | | - 30 | | dBm |
| Out-of-band blocking | 3000 MHz to 6 GHz, Wanted signal at -67 dBm | | - 21 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level | | - 44 | | dBm |
| RSSI Accuracy | Dynamic range of -90 to -20dBm | -4 | | 4 | dB |

(1) Numbers given as C/I dB

(2) BLE 1M PHY sensitivity on channels 17 and 39 may degrade by up to 2.5 dB

(3) BLE 2M PHY sensitivity on channel 17 may degrade by up to 1.5 dB

6.9 BLE Performance - Transmitter Characteristics

The CC330X devices support BLE TX setting 0,5,10, or 20 dBm

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------------------|-------------|-----|-----|-----|------|
| Output Power, highest setting | | | 20 | | dBm |

6.10 Current Consumption - WLAN Static Modes

All results are based on measurements taken using the [RadioTool](#) evaluation application (typ values are taken with nominal devices at room temp).

| PARAMETER | TEST CONDITION | | SUPPLY | TYP | MAX | UNIT |
|------------------------------|----------------|---------------------|-------------------|-----|-----|------|
| Continuous TX ⁽¹⁾ | 1 DSSS | TX power = 20.5 dBm | V _{Main} | 92 | | mA |
| | | | V _{PA} | 250 | 290 | |
| | 6 OFDM | TX power = 20.2 dBm | V _{Main} | 105 | 170 | |
| | | | V _{PA} | 250 | 290 | |
| | 54 OFDM | TX power = 17.4 dBm | V _{Main} | 110 | | |
| | | | V _{PA} | 180 | | |
| | HT MCS0 | TX power = 20.2 dBm | V _{Main} | 105 | | |
| | | | V _{PA} | 245 | | |
| | HT MCS7 | TX power = 17.4 dBm | V _{Main} | 110 | | |
| | | | V _{PA} | 180 | | |
| | HE MCS0 | TX power = 20.2 dBm | V _{Main} | 105 | | |
| | | | V _{PA} | 240 | | |
| | HE MCS7 | TX power = 17.3 dBm | V _{Main} | 110 | | |
| | | | V _{PA} | 180 | | |
| Continuous RX | | | V _{Main} | 62 | | |
| | | | V _{PA} | 0 | | |

- (1) Peak current V_{PA} can hit 340mA during device calibration.
Peak current V_{MAIN} of 185mA including peripherals and internal cortex

6.11 Current Consumption - WLAN Use Cases

Nominal device at room temp

| MODE | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------|---|-----|-----|-----|------|
| DTIM=1 | System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~102ms) | | 637 | | µA |
| | System with 1.8V WLAN beacon reception every DTIM=1 (~102ms) | | 980 | | |
| DTIM=3 | System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~102ms) | | 371 | | |
| | System with 1.8V WLAN beacon reception every DTIM=1 (~102ms) | | 570 | | |
| DTM=5 | System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~102ms) | | 319 | | |
| | System with 1.8V WLAN beacon reception every DTIM=1 (~102ms) | | 490 | | |

6.12 Current Consumption - BLE Static Modes

| PARAMETER | TEST CONDITION | SUPPLY | TYP | MAX | UNIT |
|--------------------|-------------------|-------------------|-----|-----|------|
| TX, Max Duty Cycle | TX power = 0 dBm | V _{Main} | 102 | | mA |
| | | V _{PA} | 35 | | |
| | TX power = 10 dBm | V _{Main} | 102 | | |
| | | V _{PA} | 100 | | |
| | TX power = 20 dBm | V _{Main} | 105 | | |
| | | V _{PA} | 250 | | |
| RX | | V _{Main} | 62 | | |
| | | V _{PA} | 0 | | |

6.13 Current Consumption - Device States

Nominal device at room temp

| MODE | DESCRIPTION | SUPPLY | TYP | UNIT |
|----------|---|-------------------------------------|-----|------|
| Shutdown | External supplies are available, device held in reset (nReset is low) | V _{Main} + V _{PP} | 10 | uA |
| | | V _{PA} | 2 | |
| Sleep | Low power mode - RAM in retention | V _{Main} + V _{PP} | 330 | |
| | | V _{PA} | 2 | |

6.14 Timing and Switching Characteristics

6.14.1 Power Supply Sequencing

For proper operation of the CC330x device, perform the recommended power-up sequencing as follows:

1. All supplies (VDD_MAIN_IN, VDDA, VIO, VPA) must be available before nReset is released.
2. For an external slow clock, ensure that the clock is stable before nReset is deasserted (high).
3. The nReset pin should be held low for at least 10 us after stabilization of the external power supplies.

6.14.2 Clocking Specifications

The CC330x device uses two clocks for operation:

- A fast clock running at 40 MHz for WLAN/BLE functions
- A slow clock running at 32.768 kHz for low power modes

The slow clock can be generated internally or externally. The fast clock must be generated externally.

6.14.2.1 Slow Clock Generated Internally

In order to minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less accurate and consumes more power than sourcing the slow clock externally. For this scenario the Slow_CLK_IN pin should be left not connected.

6.14.2.2 Slow Clock Using an External Oscillator

For optimal power consumption, the slow clock can be generated externally by an oscillator or sourced from elsewhere in the system. The external source must meet the requirements listed below. This clock should be fed into the CC330x pin Slow_CLK_IN and should be stable before nReset is deasserted and device is enabled.

6.14.2.2.1 External Slow Clock Requirements

| PARAMETER | Description | MIN | TYP | MAX | UNIT |
|----------------------------|-------------------------------|----------------------|-------|----------------------|-----------|
| Input slow clock frequency | Square wave | | 32768 | | Hz |
| Frequency accuracy | Initial + temperature + aging | | | ±250 | ppm |
| Input Duty cycle | | 30 | 50 | 70 | % |
| T_r/T_f | Rise and fall time | | | 100 | ns |
| V_{IL} | Input low level | 0 | | $0.35 \times V_{IO}$ | V |
| V_{IH} | Input high level | $0.65 \times V_{IO}$ | | 1.95 | V |
| | Input impedance | 1 | | | $M\Omega$ |
| | Input capacitance | | | 5 | pF |

6.14.2.3 Fast Clock Using an External Crystal (XTAL)

The CC330x device supports a crystal-based fast clock (XTAL). The crystal is fed directly between HFXT_P and HFXT_M pins with suitable loading capacitors, and must meet the requirements below.

6.14.2.3.1 External Fast Clock XTAL Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------------------|-----|-----|--------|----------|
| Supported frequencies | | | 40 | | MHz |
| Frequency accuracy | Initial + temperature + aging | | | +/- 25 | ppm |
| Load Capacitance, C_L ⁽¹⁾ | | 5 | | 13 | pF |
| Equivalent series resistance, ESR | | | | 30 | Ω |
| Drive level | | | 100 | | uW |

- (1) Load capacitance, $C_L = [C1 \cdot C2] / [C1 + C2] + C_p$, where C1, C2 are the capacitors connected on HFXT_P and HFXT_M, respectively, and C_p is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and $C_p = 2$ pF, then $C_L = 5$ pF.

6.15 Interface Timing Characteristics

6.15.1 SDIO Timing Specifications

SDIO is the main host interface for WLAN, and it supports a maximum clock rate of 52 MHz. The CC330x device also supports shared SDIO interface for both BLE and WLAN.

6.15.1.1 SDIO Timing Diagram - Default Speed

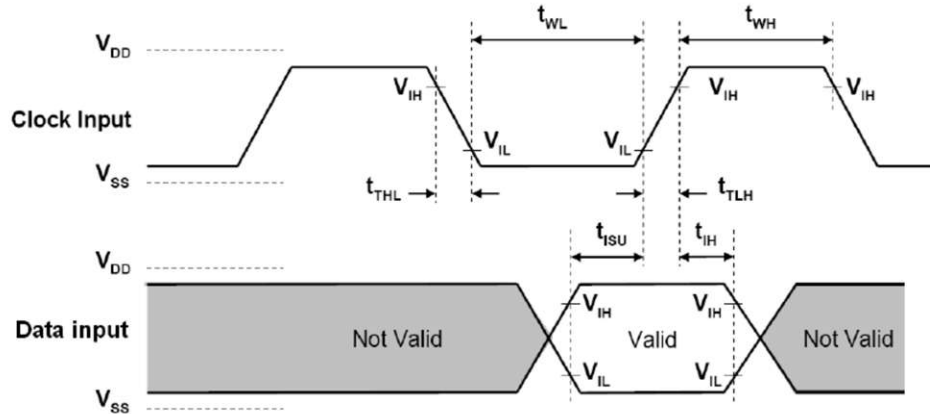


图 6-1. SDIO Default Input Timing

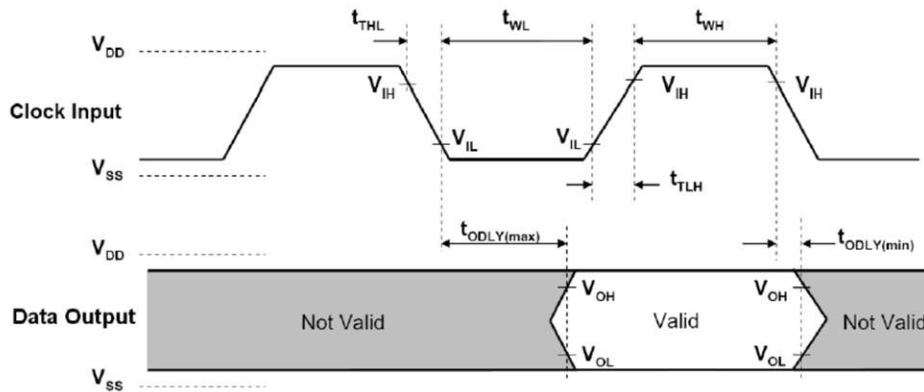


图 6-2. SDIO Default Output Timing

6.15.1.2 SDIO Timing Parameters - Default Speed

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|-------------|--------------------------------------|-----|-----|------|
| f_{clock} | Clock frequency, CLK | | 26 | MHz |
| t_{High} | High Period | 10 | | ns |
| t_{Low} | Low Period | 10 | | |
| t_{TLH} | Rise time, CLK | | 10 | |
| t_{THL} | Fall time, CLK | | 10 | |
| t_{ISU} | Setup time, input valid before CLK ↑ | 5 | | |
| t_{IH} | Hold time, input valid after CLK ↑ | 5 | | |
| t_{ODLY} | Delay time, CLK ↓ to output valid | 2 | 14 | |
| C_L | Capacitive load on outputs | 15 | 40 | |

6.15.1.3 SDIO Timing Diagram - High Speed

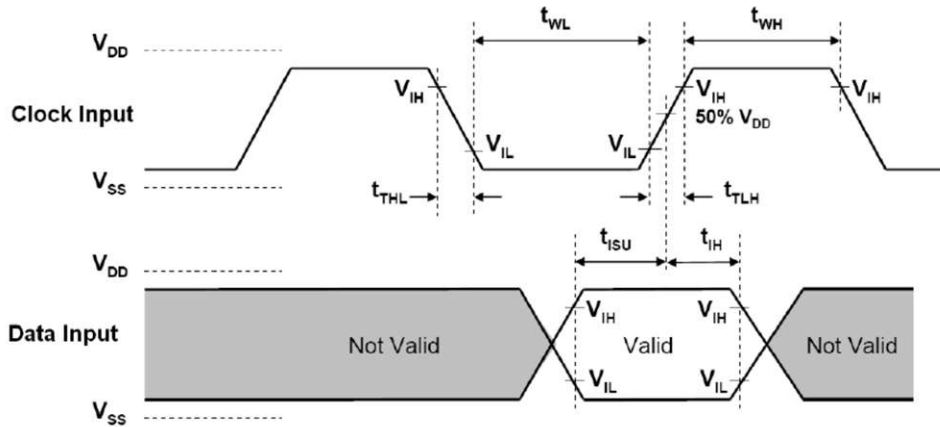


图 6-3. SDIO HS Input Timing

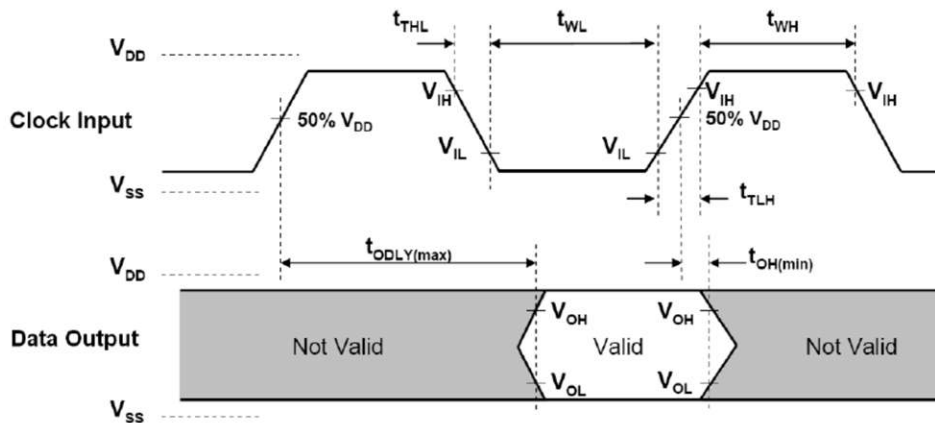


图 6-4. SDIO HS Output Timing

6.15.1.4 SDIO Timing Parameters - High Speed

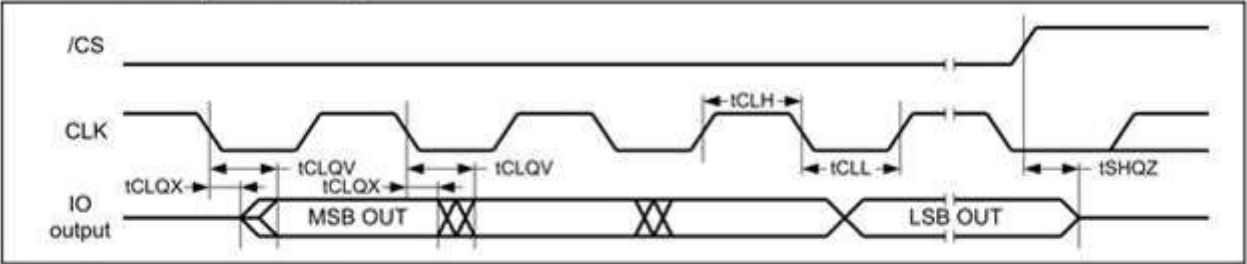
| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|--------------------|--------------------------------------|-----|-----|------|
| f_{clock} | Clock frequency, CLK | | 52 | MHz |
| t_{High} | High Period | 7 | | ns |
| t_{Low} | Low Period | 7 | | |
| t_{TLH} | Rise time, CLK | | 3 | |
| t_{THL} | Fall time, CLK | | 3 | |
| t_{ISU} | Setup time, input valid before CLK ↑ | 6 | | |
| t_{IH} | Hold time, input valid after CLK ↑ | 2 | | |
| t_{ODLY} | Delay time, CLK ↓ to output valid | 2 | 14 | |
| C_L | Capacitive load on outputs | 15 | 40 | pF |

6.15.2 SPI Timing Specifications

SPI is another host interface for WLAN. The CC330x device also supports shared SPI interface for both BLE and WLAN.

6.15.2.1 SPI Timing Diagram

9.7 Serial Output Timing



9.8 Serial Input Timing

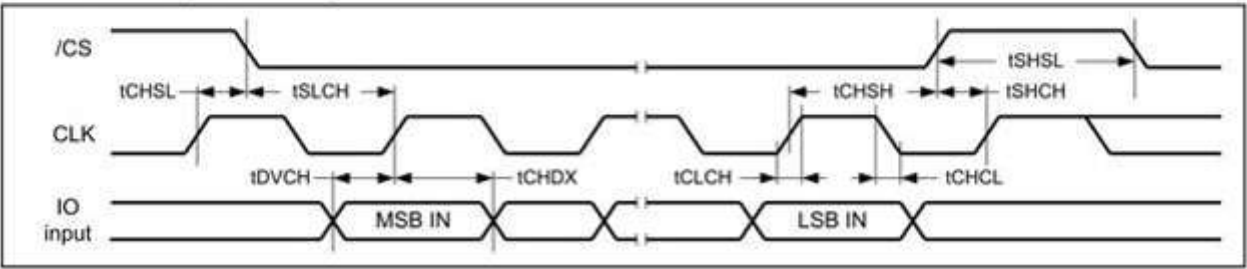


图 6-5. SPI Timing

6.15.2.2 SPI Timing Parameters

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|--|---|-----|-----|------|
| f_{clock} | Clock frequency, CLK | | 26 | MHz |
| t_{High} | High Period | 10 | | ns |
| t_{Low} | Low Period | 10 | | |
| t_{TLH} | Rise time, CLK | | 3 | |
| t_{THL} | Fall time, CLK | | 3 | |
| t_{CSsu} | CS Setup time, CS valid before CLK \uparrow | 3 | | |
| t_{ISU} | PICO, input valid before CLK \uparrow | 3 | | |
| t_{IH} | PICO Hold time, input valid after CLK \uparrow | 3 | | |
| $t_{\text{Dr}}, t_{\text{Df}} - \text{Active}$ | Delay time, CLK \uparrow/\downarrow to output valid | 2 | 10 | |
| $t_{\text{Dr}}, t_{\text{Df}} - \text{Sleep}$ | Delay time, CLK \uparrow/\downarrow to output valid | | 12 | |
| C_{L} | Capacitive load on outputs | 15 | 40 | |

6.15.3 UART 4-Wire Interface

UART is the main host interface for BLE, which supports host controller interface (HCI) transport layer.

6.15.3.1 UART Timing Parameters

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|-----------------------------|---------------------------|-------|-----|-------|------|
| Baud rate | | 37.5 | | 4364 | kbps |
| Baud rate accuracy per byte | Receive/Transmit | -2.5 | | +1.5 | % |
| Baud rate accuracy per bit | Receive/Transmit | -12.5 | | +12.5 | % |
| CTS low to TX_DATA on | | 0 | 2 | | ms |
| CTS high to TX_DATA off | Hardware flow control | | | 1 | Byte |
| CTS high pulse width | | 1 | | | bit |
| RTS low to RX_DATA on | | 0 | 2 | | ms |
| RTS high to RX_DATA off | Interrupt set to 1/4 FIFO | | | 16 | Byte |

7 Applications, Implementation, and Layout

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

图 7-1 shows the reference schematic for the CC3301 using an optimized bill of materials.

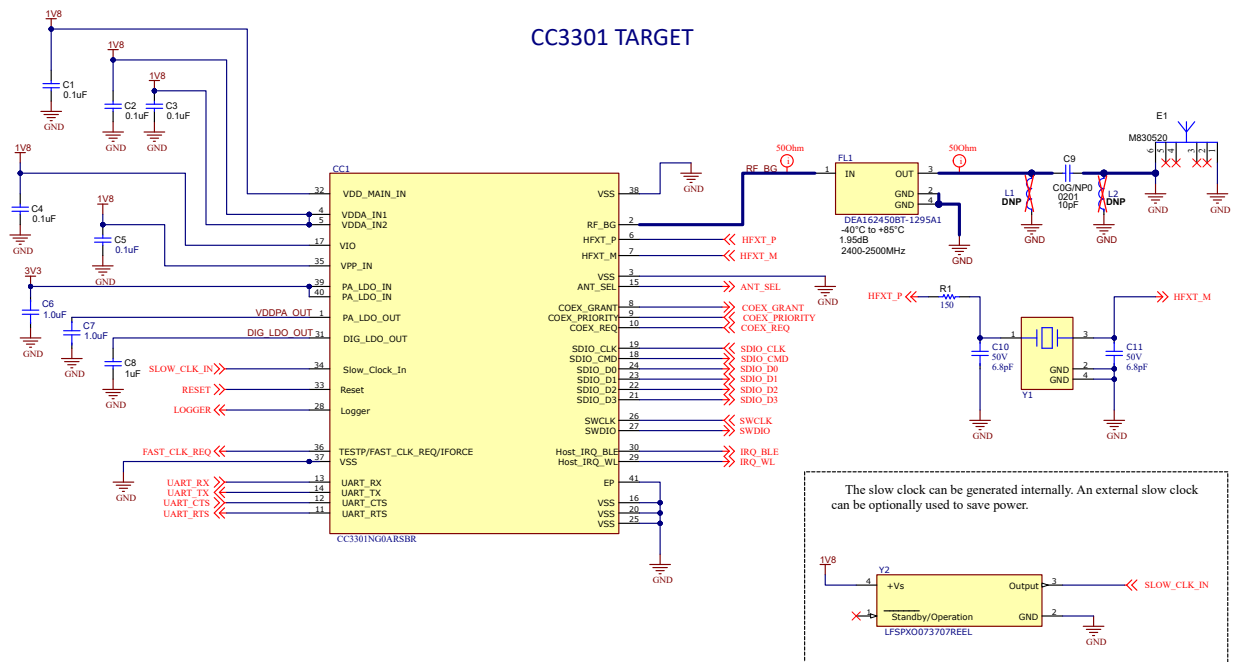


图 7-1. CC3301 Reference Schematic

1. The slow clock can be generated internally. An external slow clock can be optionally used to save power.
2. For more information on antenna selection and matching, please see the [CC33xx Hardware Integration](#).

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

8.2 器件命名规则样板文件

器件开发演变流程：

X 试验器件不一定代表最终器件的电气规范标准，并且可能不使用生产组装流程。

P 原型器件不一定是最终器件模型，并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

支持工具开发演变流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

TMDS 完全合格的开发支持产品。

X 和 P 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

器件开发演变流程：

TMX 试验器件不一定代表最终器件的电气规范标准，并且可能不使用生产组装流程。

TMP 原型器件不一定是最终器件模型，并且不一定符合最终电气标准规范。

TMS 完全合格的芯片模型的生产版本。

支持工具开发演变流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

TMDS 完全合格的开发支持产品。

TMX 和 TMP 器件和 TMDX 开发支持工具供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

生产器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件 (X 或者 P) 的故障率大于标准生产器件。由于这些器件的预期最终使用故障率仍未确定，故德州仪器 (TI) 建议请勿将这些器件用于任何生产系统。请仅使用合格的生产器件。

8.3 Tools and Software

Design Kits and Evaluation Modules

[CC330x Reference Design Files](#)

CC330x reference design CAD source files. TI recommends using this design as a reference when creating the layout in order to achieve the RF performance listed in this datasheet.

[CC3301 BoosterPack plug-in module](#)

The CC3301 BoosterPack™ plug-in module (BP-CC3301) is a test and development board that can be easily connected to TI LaunchPad™ development kits or processor boards; thus enabling rapid software development.

CC3301 M.2 card plug-in module The CC3301 M.2 card plug-in module (M2-CC3301) is a test and development board that can be easily connected to TI processor boards or other processor boards with an M.2 Key E interface support; thus enabling rapid software development.

Software

SimpleLink Wi-Fi Toolbox SimpleLink Wi-Fi Toolbox is a collection of tools to help development and testing of the CC33xx. The Wi-Fi toolbox package provides all the capabilities required to debug and monitor WLAN/Bluetooth® Low Energy firmware with a host, perform RF validation tests, run pretest for regulatory certification testing, and debug hardware and software platform integration issues.

CC33xx device drivers The CC33XX are single-chip Wi-Fi 6 and Bluetooth Low Energy 5.4 companion devices suitable for both Linux and RTOS based systems. CC33XX-SOFTWARE is a collection of software development sources aimed to facilitate quick setup, out-of-box experience, and accelerate development in Linux or RTOS environments.

8.4 Documentation Support

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

Application Reports

CC33xx Production Line Guide Texas Instruments™ provides many resources in order to assist users in quickly examining the functionality and performance of their devices. This document provides the necessary information to guide the user in production line testing for CC33xx. The device's functions can be checked using tools and software provided by Texas Instruments. Performance testing is more involved as external equipment is required for thorough examination.

SimpleLink CC33xx Security Features This document describes the CC33xx security related features, which are made available to vendors through an ecosystem that incorporates simple and concise APIs, tools, and documentation

User's Guides

CC33xx WLAN Features User's Guide This document provides information about CC33xx family of devices and Wi-Fi® features, as well as TI proprietary enhancements. The document does not provide the complete application programming interface (API) set, but a high-level overview of the features.

CC33xx Hardware Integration This document describes how to integrate the CC330x into any system and the hardware requirements for this device. Layout and schematic considerations are listed here as well, which TI highly recommends following in order to achieve the device performance listed in this datasheet.

8.5 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.6 Trademarks

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc..

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8.7 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.8 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from October 5, 2023 to December 19, 2023 (from Revision C (October 2023) to Revision D (December 2023))

| | Page |
|---|------|
| • Updated specifications data and test conditions to production values..... | 8 |
| • Updated reference schematic..... | 18 |

10 Mechanical, Packaging, and Orderable Information

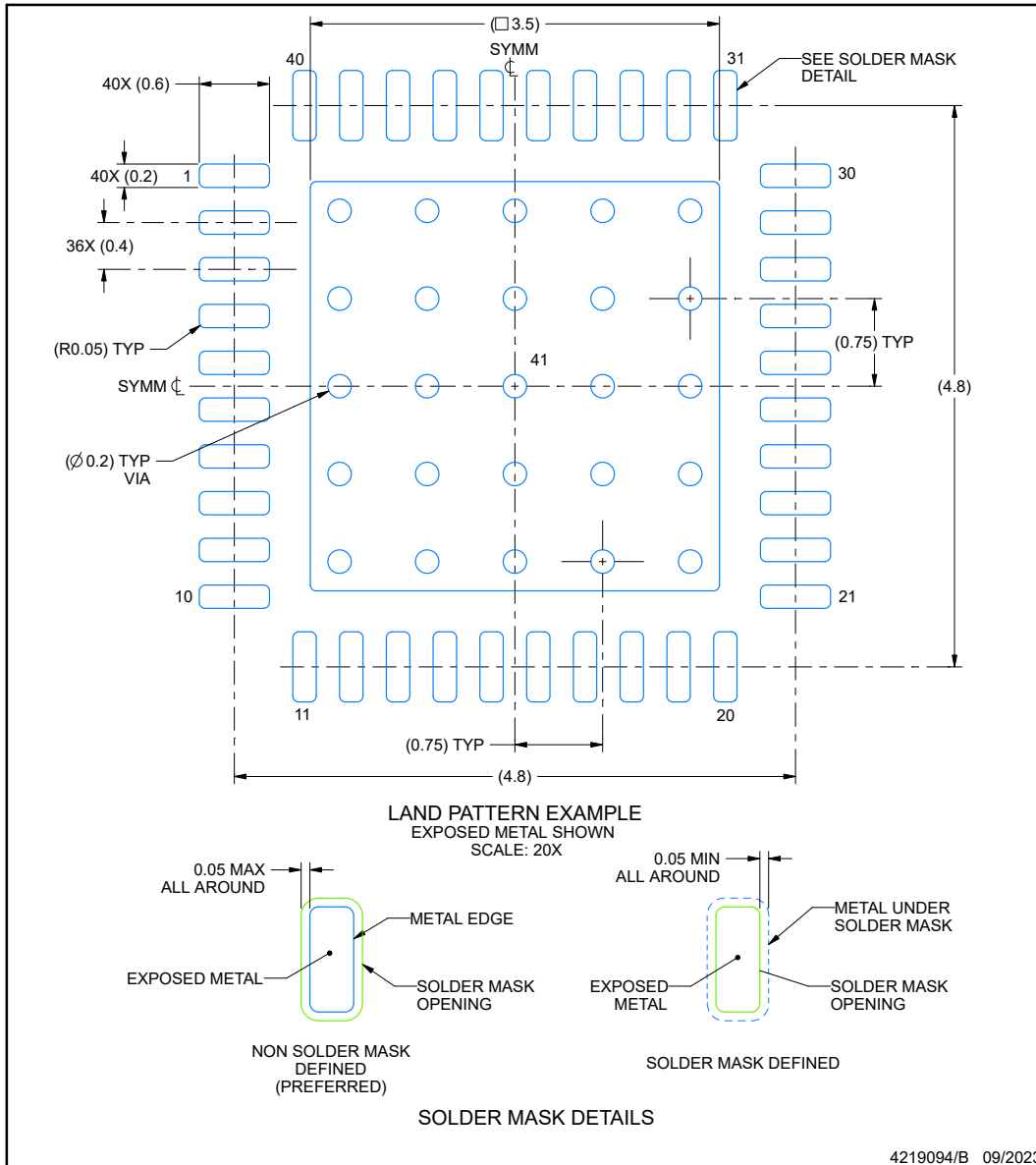
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

EXAMPLE BOARD LAYOUT

RSB0040B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

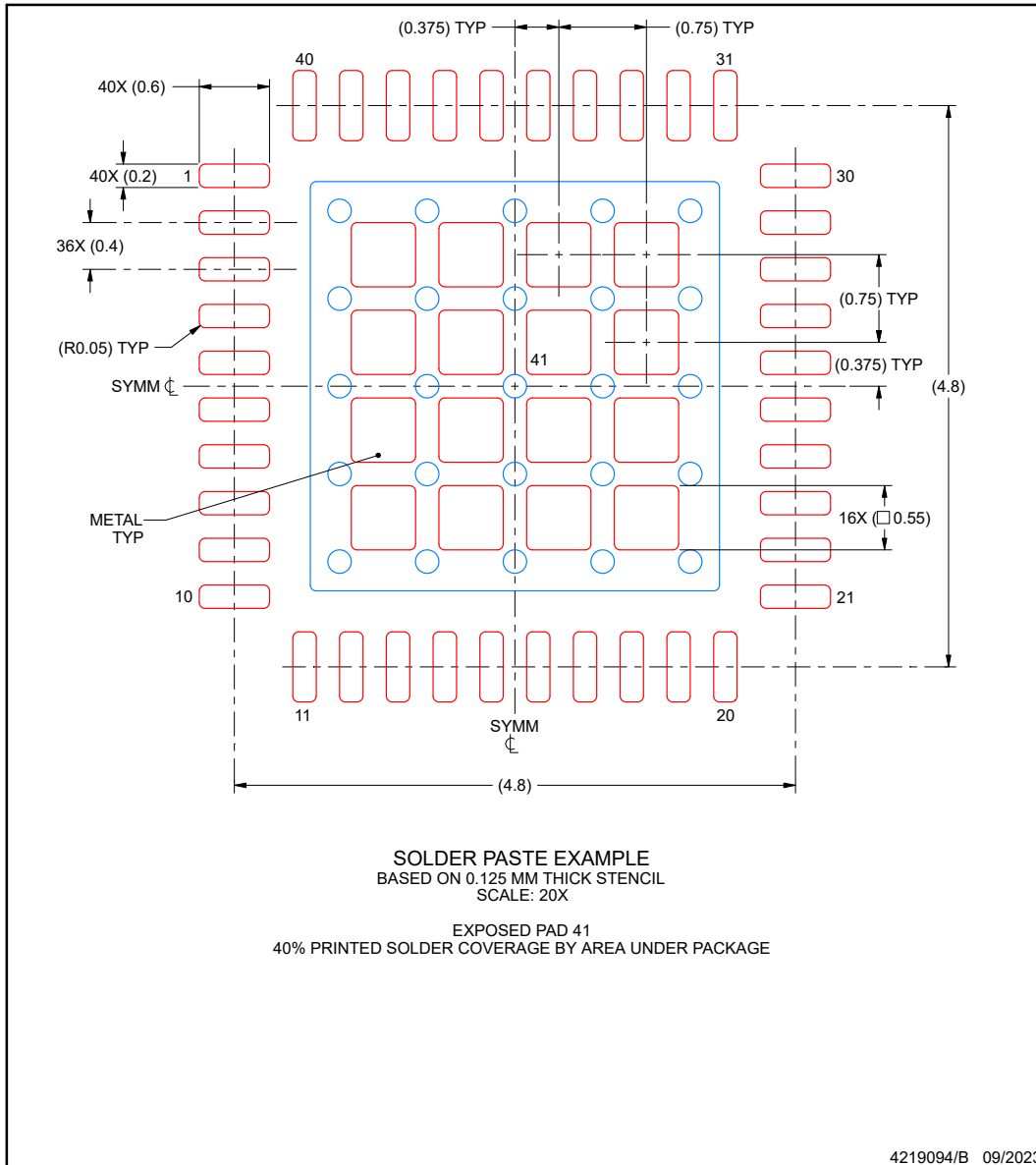
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSB0040B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC3300ENJARSBR | ACTIVE | WQFN | RSB | 40 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | CC3300 ENJA | Samples |
| CC3301ENJARSBR | ACTIVE | WQFN | RSB | 40 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | CC3301 ENJA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC3300ENJARSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| CC3301ENJARSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC3300ENJARSBR | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| CC3301ENJARSBR | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |

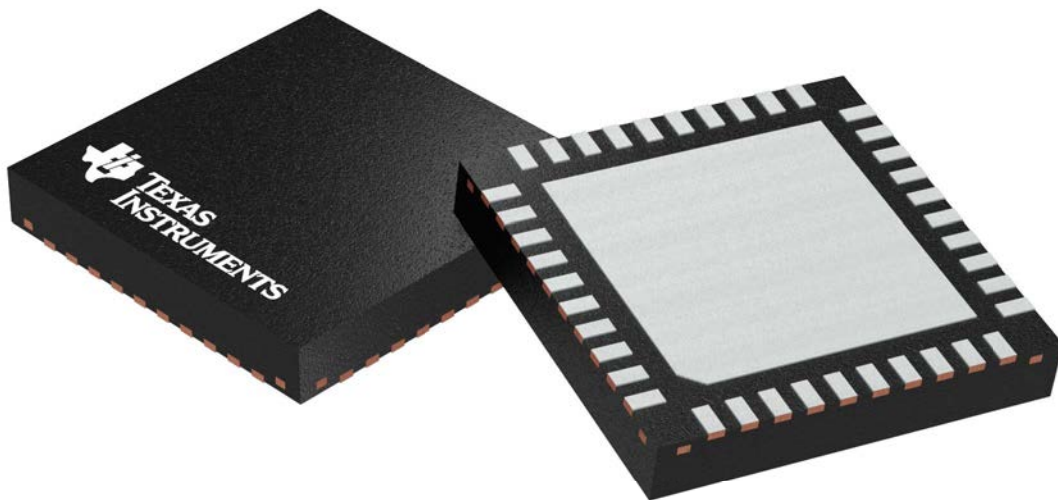
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

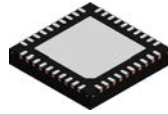
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207182/D

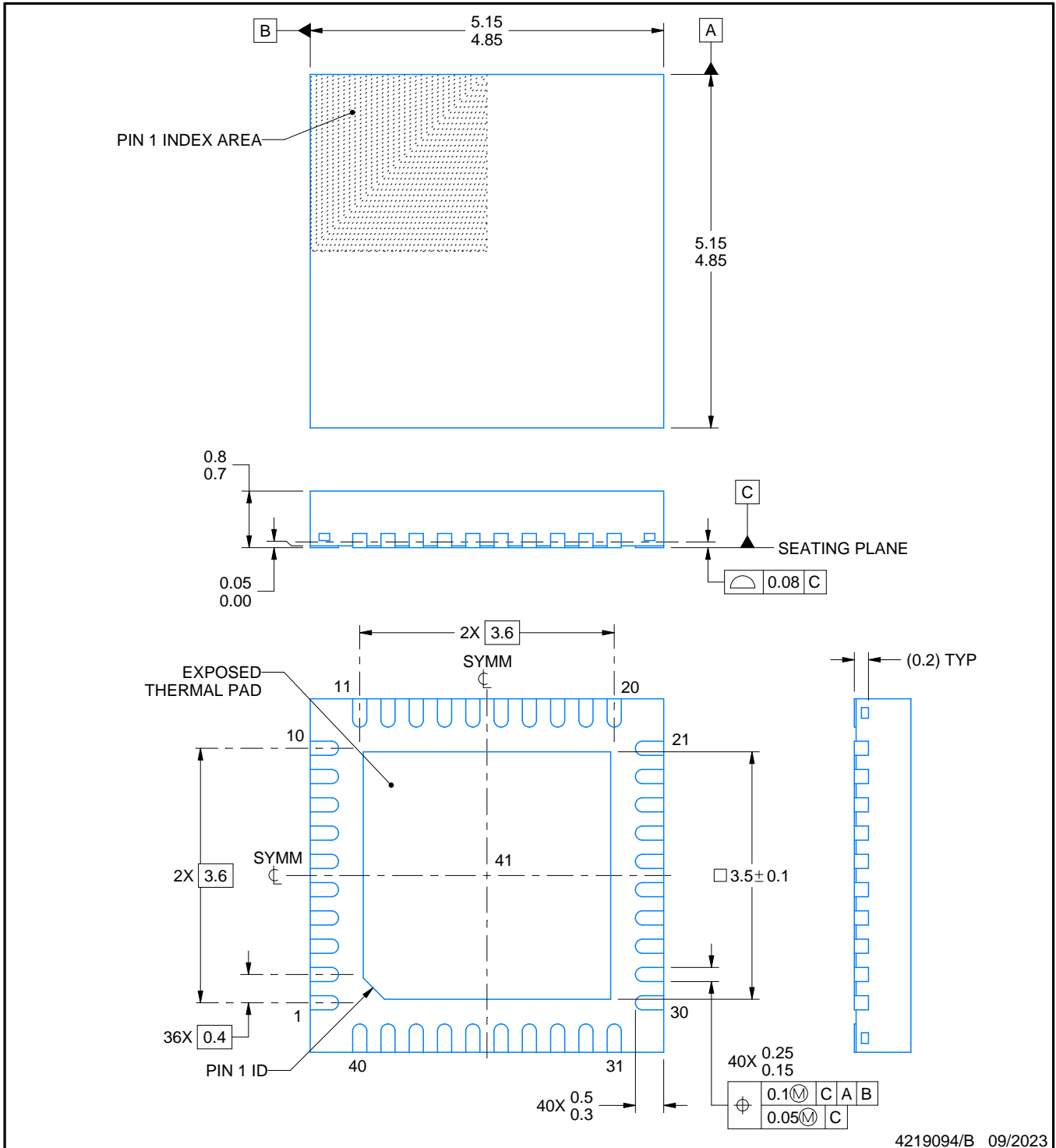
RSB0040B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

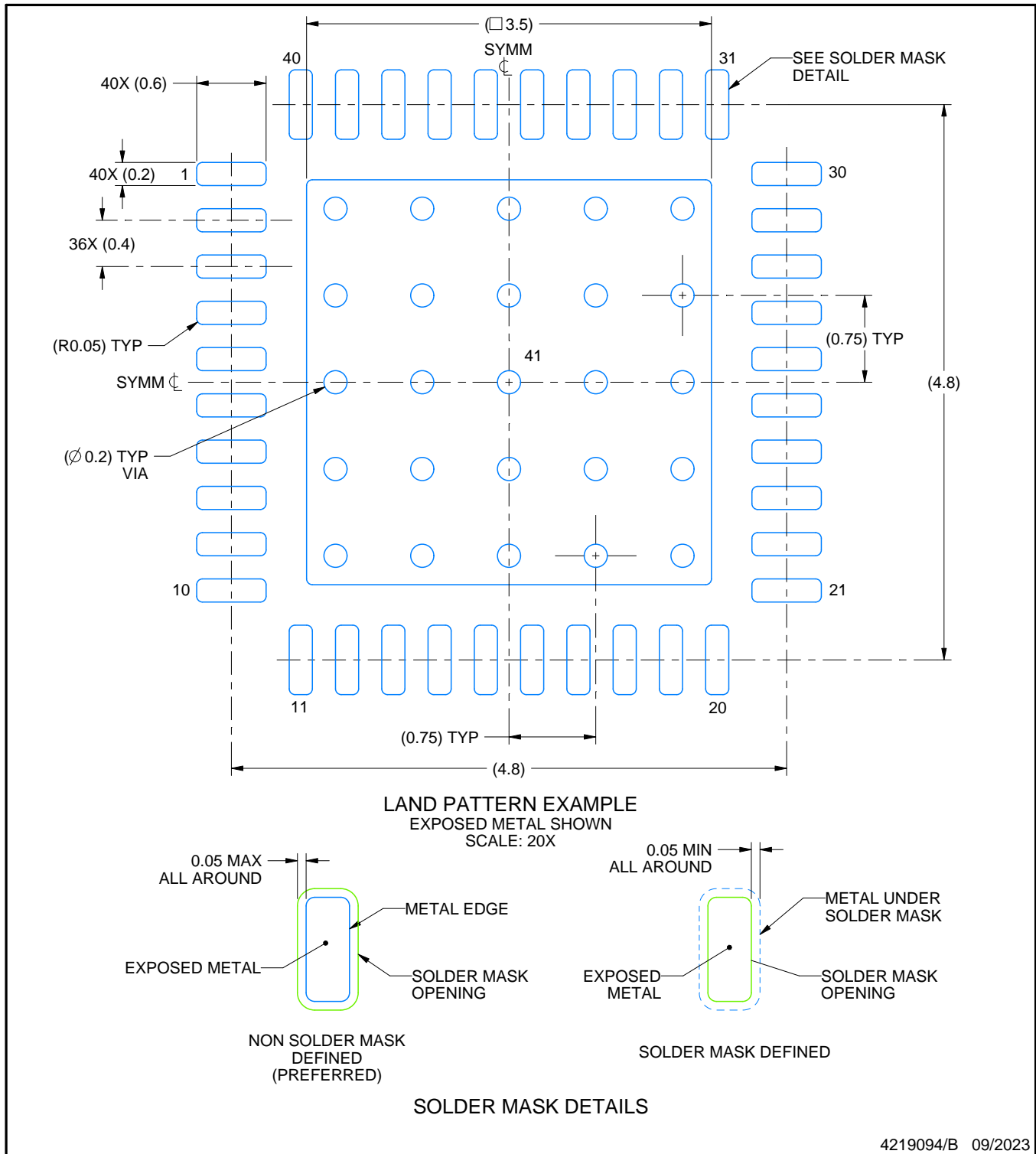
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RSB0040B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES: (continued)

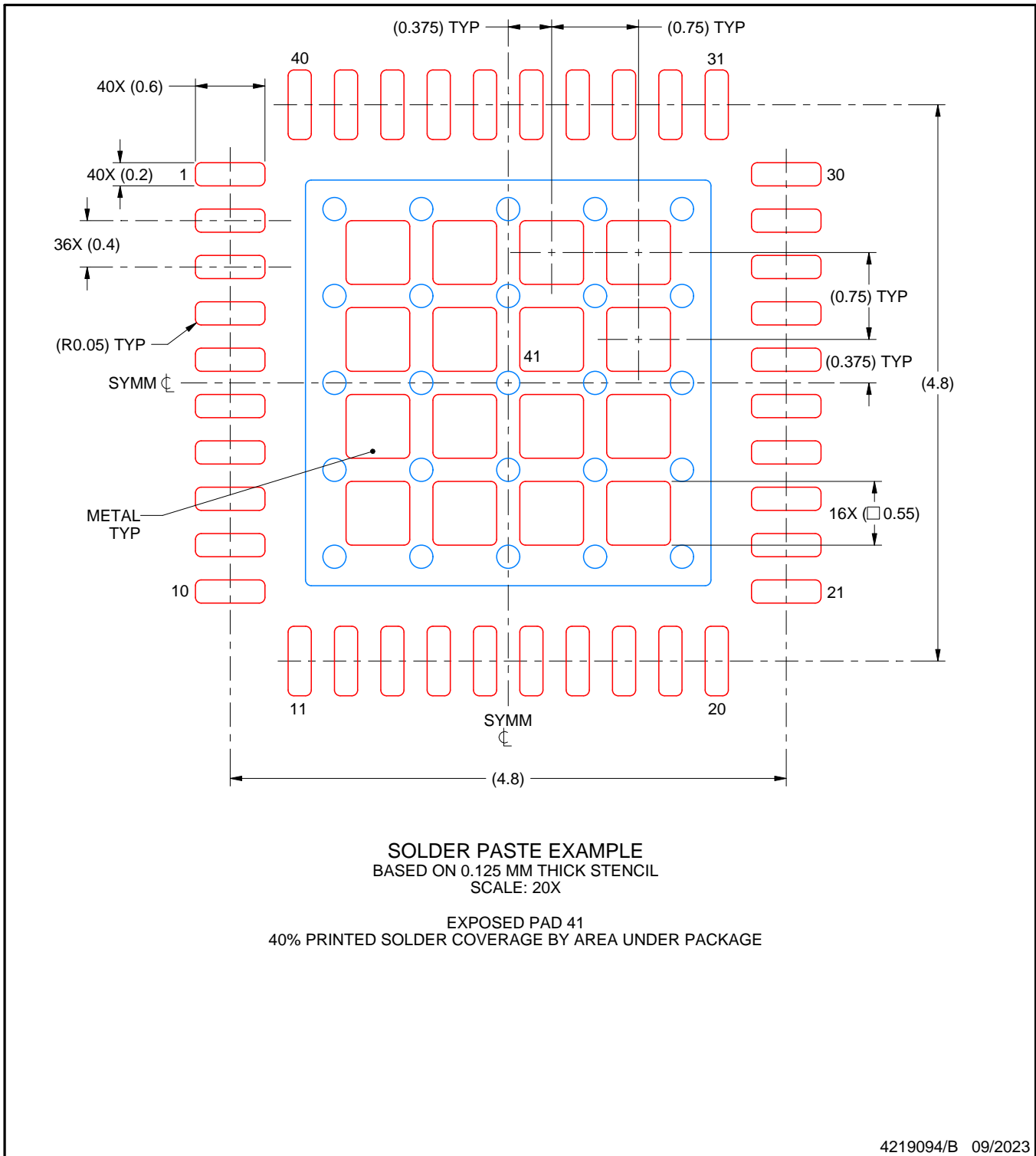
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSB0040B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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