CDx4HC688、CDx4HCT688 高速 CMOS 逻辑 8 位幅度比较器

1 特性

- 可级联
- 扇出（在温度范围内）
  - 标准输出：10 个 LSTTL 负载
  - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围：–55℃ 至 125℃
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，功耗显著降低
- HC 类型
  - 工作电压为 2V 至 6V
  - 高抗噪性：当 V_{CC} = 5V 时，N_{IL} = 30%，N_{IH} = V_{CC} 的 30%
- HCT 类型
  - 工作电压为 4.5V 至 5.5V
  - 直接 LSTTL 输入逻辑兼容，V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
  - CMOS 输入兼容性，当电压为 V_{OL}、V_{OH} 时，I_I ≤ 1 μA

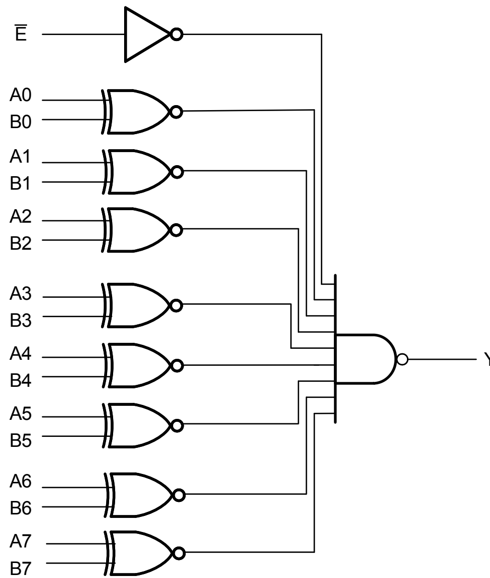
2 说明

’HC688 和 ’HCT688 是 8 位幅度比较器，专用于需要比较两个 8 位二进制字的计算机和逻辑应用。当进行比较的字相等时，输出 (Y) 为低电平，并且可用作级联应用中下一个器件的使能输入。

封装信息

器件型号	封装[1]	封装尺寸（标称值）
CD74HC688M	SOIC (20)	12.80mm × 7.50mm
CD74HCT688M	SOIC (20)	12.80mm × 7.50mm
CD74HC688E	PDIP (20)	25.40mm × 6.35mm
CD74HCT688E	PDIP (20)	25.40mm × 6.35mm
CD74HC688NSR	SO (20)	15.00mm × 5.30mm
CD74HC688PWR	TSSOP (20)	6.50mm × 4.40mm
CD54HC688F3A	CDIP (20)	26.92mm × 6.92mm
CD54HCT688F3A	CDIP (20)	26.92mm × 6.92mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SCHS196

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (February 2022) to Revision E (October 2022)	Page
• Increased R θ JA for packages: DW (58 to 109.1); N (69 to 84.6); NS (60 to 113.4); PW (83 to 131.8)............	4

Changes from Revision C (August 2003) to Revision D (February 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准..........	1

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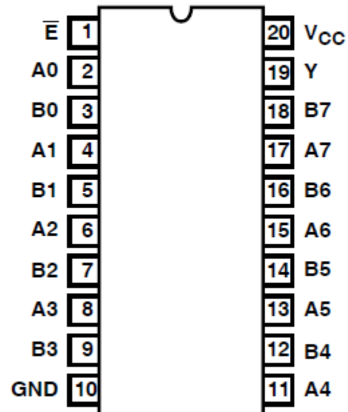
4 Pin Configuration and Functions



J, N, DW, NS, or PW package
20-Pin CDIP, PDIP, SOIC, SO, TSSOP
Top View

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5 Specifications

5.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
I_{IK}	Input diode current	For $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output diode current	For $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Output source or sink current per output pin	For $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress-only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		−55	125	℃

5.3 Thermal Information

THERMAL METRIC		DW (SOIC) 20 PINS	N (PDIP) 20 PINS	NS (SO) 20 PINS	PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	109.1	84.6	113.4	131.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	78.4	82.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	55.3	47.1	21.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = –20 μA	2	1.9			1.9		1.9		V
		I_{OH} = –20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = –20 μA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = –4 mA	4.5	3.98			3.84		3.7		
		I_{OH} = –5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	$V_I = V_{CC}$ or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	6			8		80		160	μA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = –20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = –4 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	$V_I = V_{CC}$ or GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5			8		80		160	μA
ΔI_{CC} (1)	Additional supply current per input pin	Enable inputs held at V_{CC} –2.1	4.5 to 5.5		100	252		315		343	μA
		Data inputs held at V_{CC} –2.1	4.5 to 5.5		100	126		157.5		171.5	μA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) $V_I = V_{IH}$ or V_{IL}.

5.5 Switching Characteristics

C_L = 50pF. Input t_r, t_f = 6 ns

PARAMETER		V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{PLH}, t_{PHL}	Propagation delay (图 6-1) An to output	2			170		210		255	ns
		4.5		14[3]	34		42		51	
		6			29		36		43	
t_{PLH}, t_{PHL}	Bn to output	2			170		210		255	ns
		4.5		14[3]	34		42		51	
		6			29		36		43	
t_{PLH}, t_{PHL}	$\overline{E}$ to output	2			120		150		180	ns
		4.5		9[3]	24		30		36	
		6			20		26		30	
t_{TLH}, t_{THL}	Output transition time (图 6-1)	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
C_{IN}	Input capacitance				10		10		10	pF
C_{PD}	Power dissipation capacitance[1] [2]			22[4]						pF
HCTTYPES										
t_{PLH}, t_{PHL}	Propagation delay (图 6-1) An to output	4.5		14[3]	34		42		51	ns
t_{PLH}, t_{PHL}	Bn to output	4.5		14[3]	34		42		51	ns
t_{PLH}, t_{PHL}	$\overline{E}$ to output	4.5		9[3]	24		30		36	ns
t_{TLH}, t_{THL}	Output transition time (图 6-1)	4.5			15		19		22	ns
C_{IN}	Input capacitance				10		10		10	pF
C_{PD}	Power dissipation capacitance[1] [2]	5		22[4]						pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.
(4) C_L = 15 pF.

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6 Parameter Measurement Information

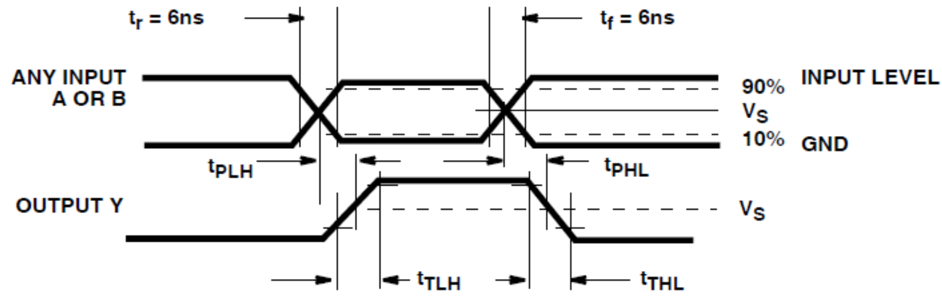


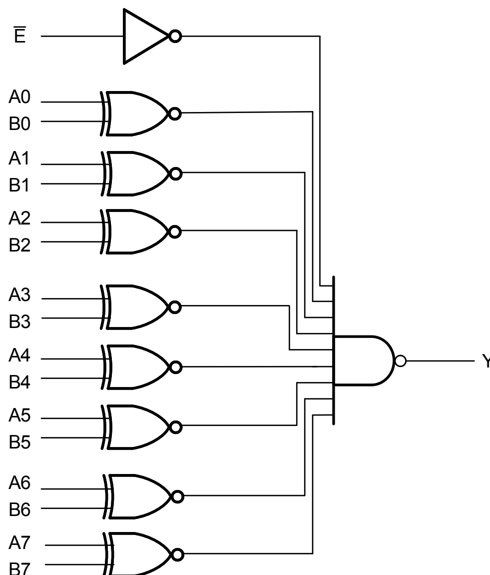
图 6-1. Propagation Delay and Transition Times

7 Detailed Description

7.1 Overview

The ’HC688 and ’HCT688 are 8-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 8-bit binary words. When the compared words are equal the output (Y) is low and can be used as the enabling input for the next device in a cascaded application.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table(1)

INPUTS		OUPUTS
A, B	Ē	Y
A = B	L	L
A ≠ B	L	H
X	H	H

(1) H = high voltage level, L = low voltage level, X = don’t care.

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8685701RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8685701RA CD54HCT688F3A	Samples
CD54HC688F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8681801RA CD54HC688F3A	Samples
CD54HCT688F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT688F	Samples
CD54HCT688F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8685701RA CD54HCT688F3A	Samples
CD74HC688E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC688E	Samples
CD74HC688M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HC688M	
CD74HC688M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC688M	Samples
CD74HC688NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC688M	Samples
CD74HC688PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ688	Samples
CD74HC688PWT	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-55 to 125	HJ688	
CD74HCT688E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT688E	Samples
CD74HCT688EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT688E	Samples
CD74HCT688M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT688M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC688, CD54HCT688, CD74HC688, CD74HCT688 :

- Catalog : CD74HC688, CD74HCT688

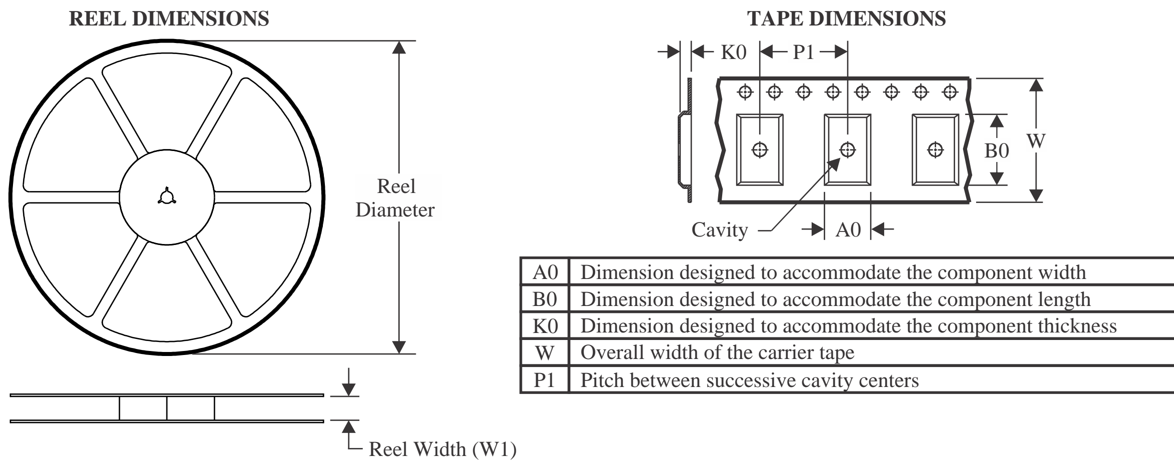
- Military : CD54HC688, CD54HCT688

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

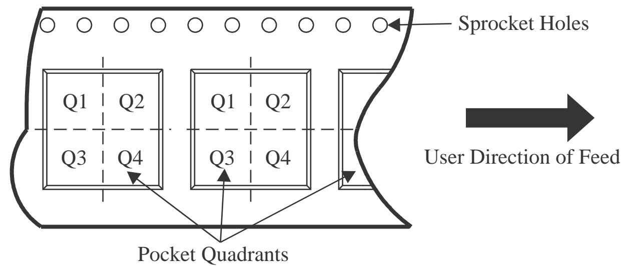
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

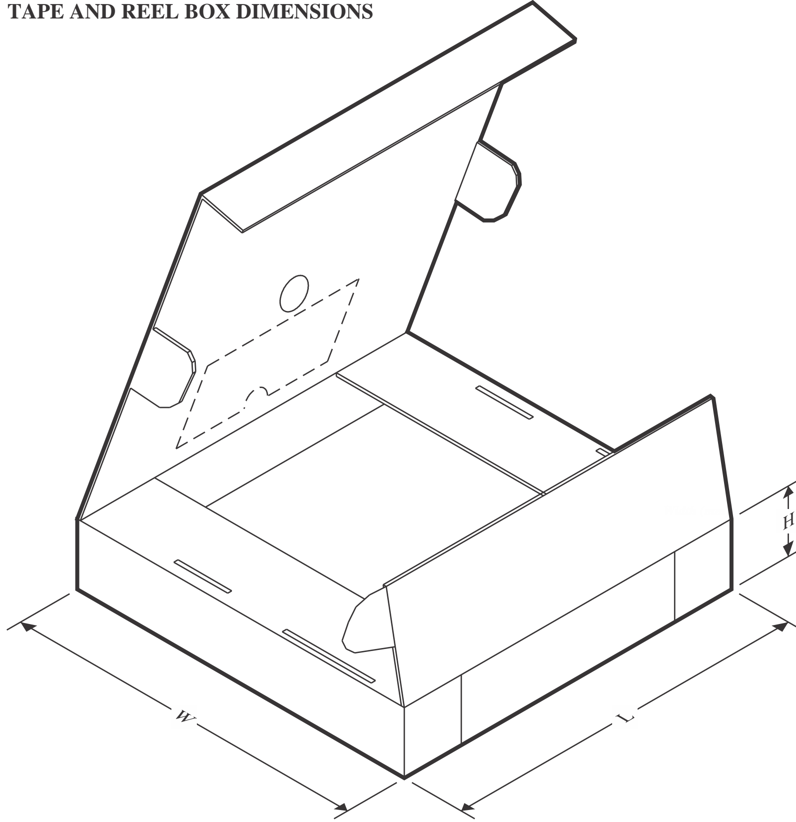
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC688M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC688NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
CD74HC688NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
CD74HC688PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CD74HC688PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CD74HCT688M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT688M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

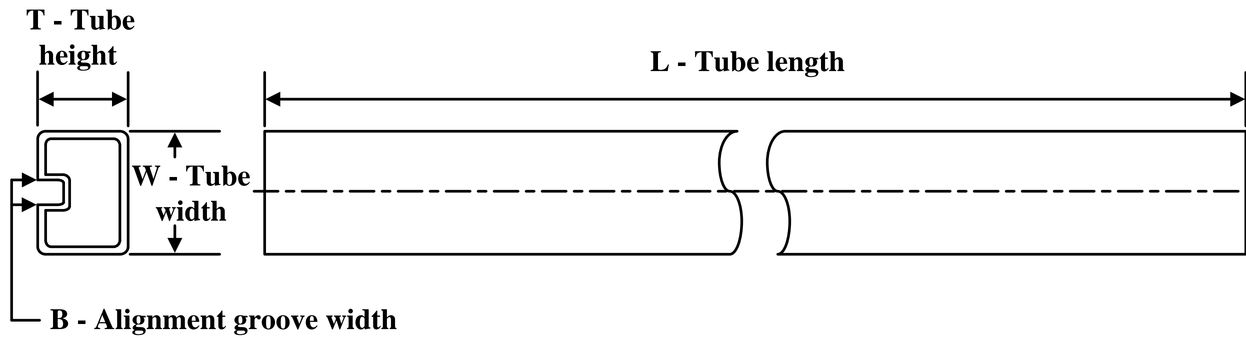
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC688M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC688NSR	SOP	NS	20	2000	367.0	367.0	45.0
CD74HC688NSR	SOP	NS	20	2000	367.0	367.0	45.0
CD74HC688PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
CD74HC688PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
CD74HCT688M96	SOIC	DW	20	2000	356.0	356.0	41.0
CD74HCT688M96	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE

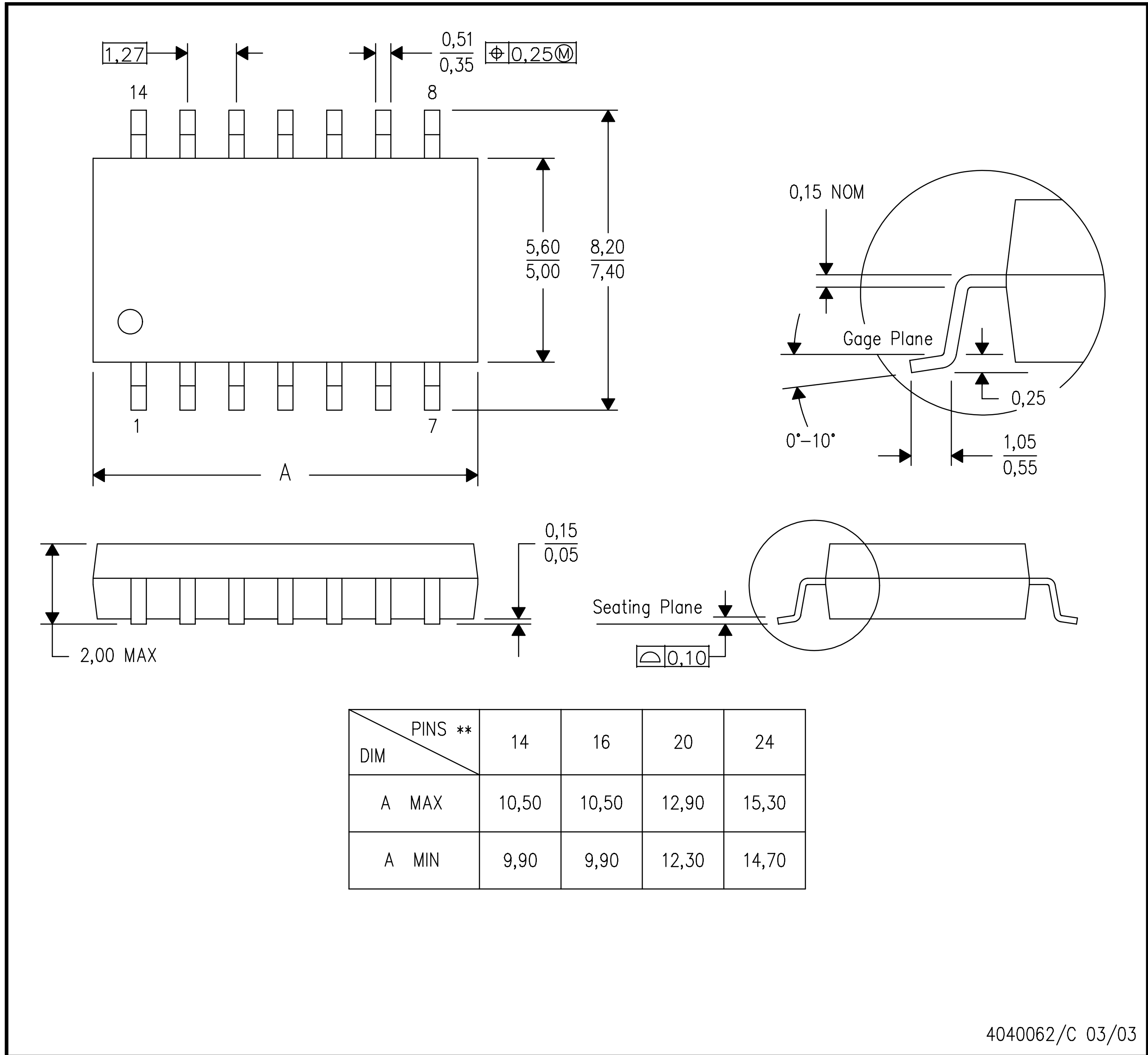


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC688E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT688E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT688EE4	N	PDIP	20	20	506	13.97	11230	4.32

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



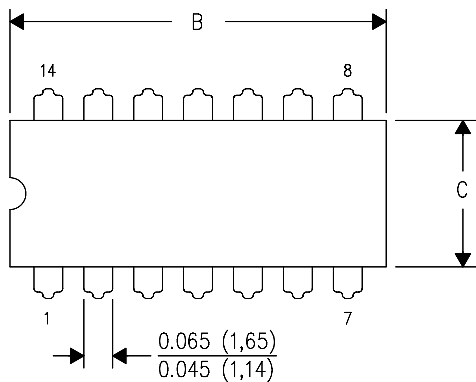
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

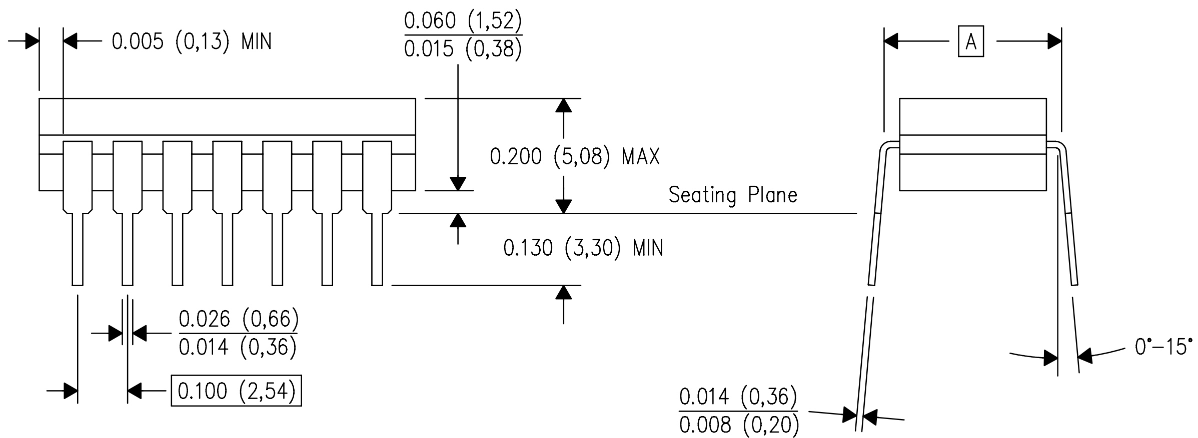
J (R-GDIP-T**)

CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

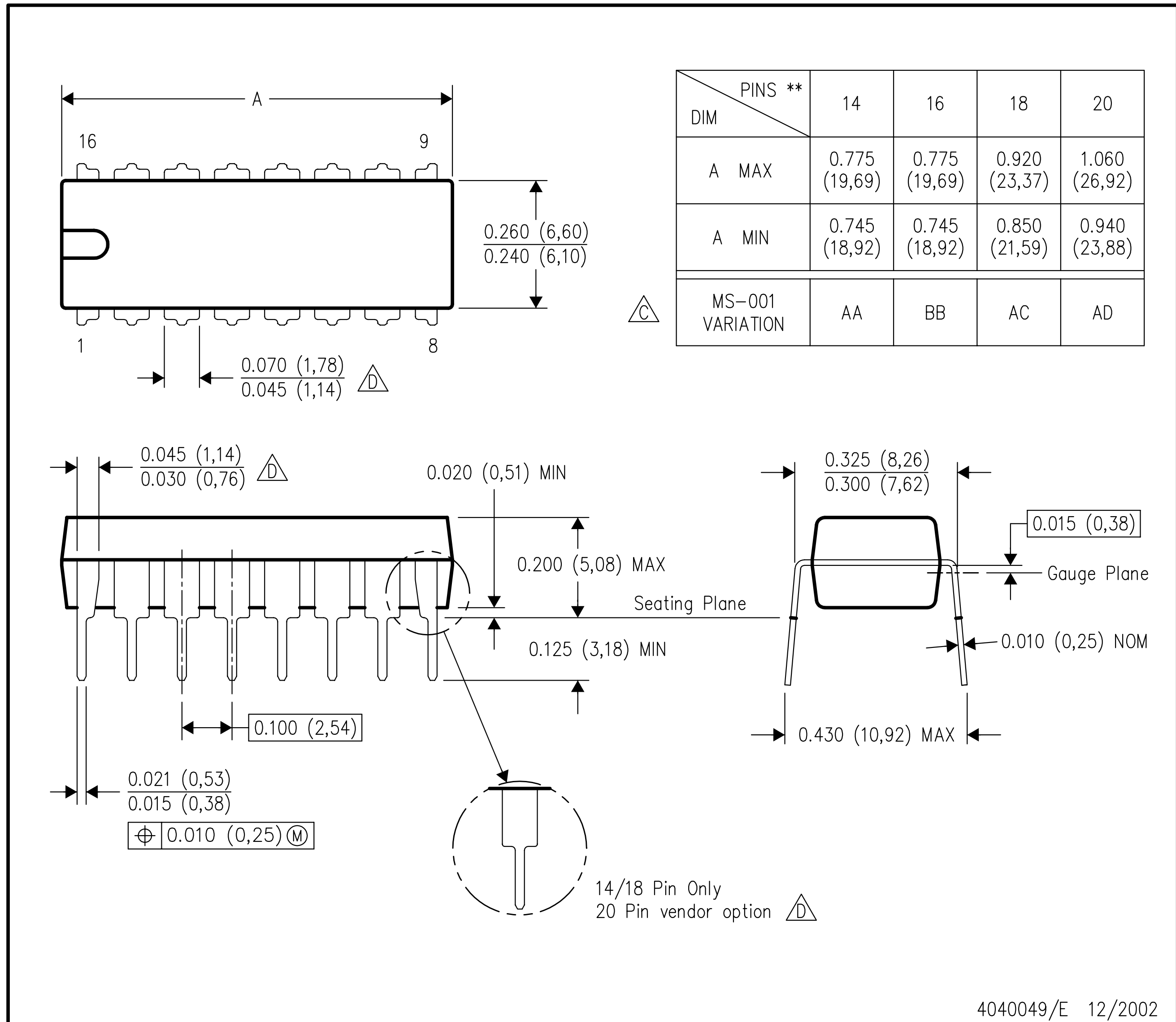


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

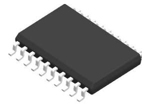
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



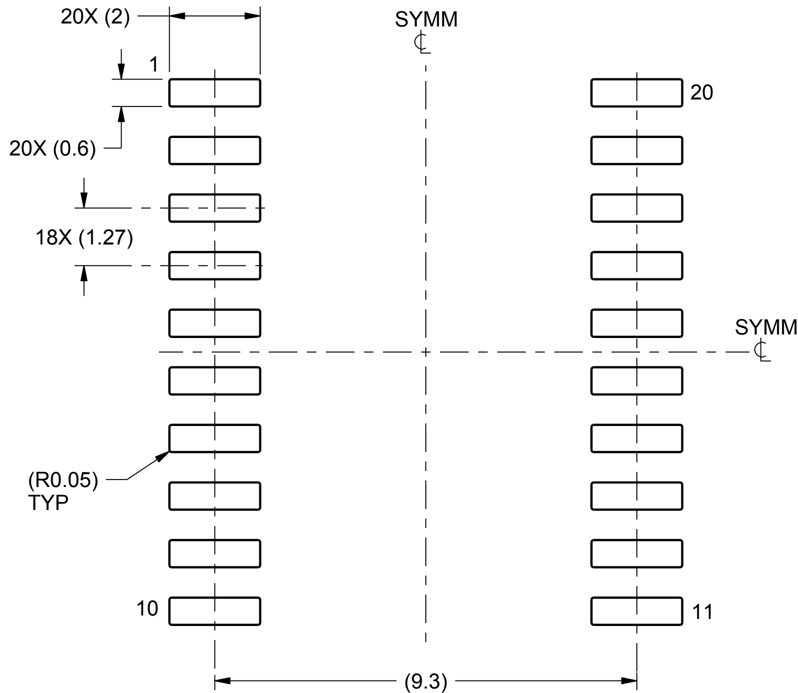
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

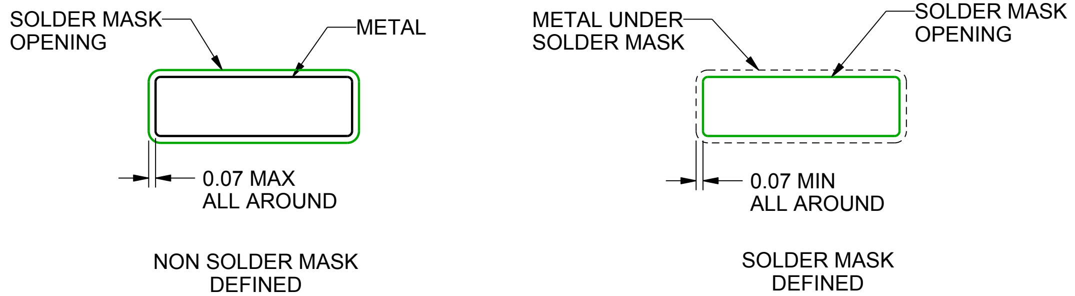


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

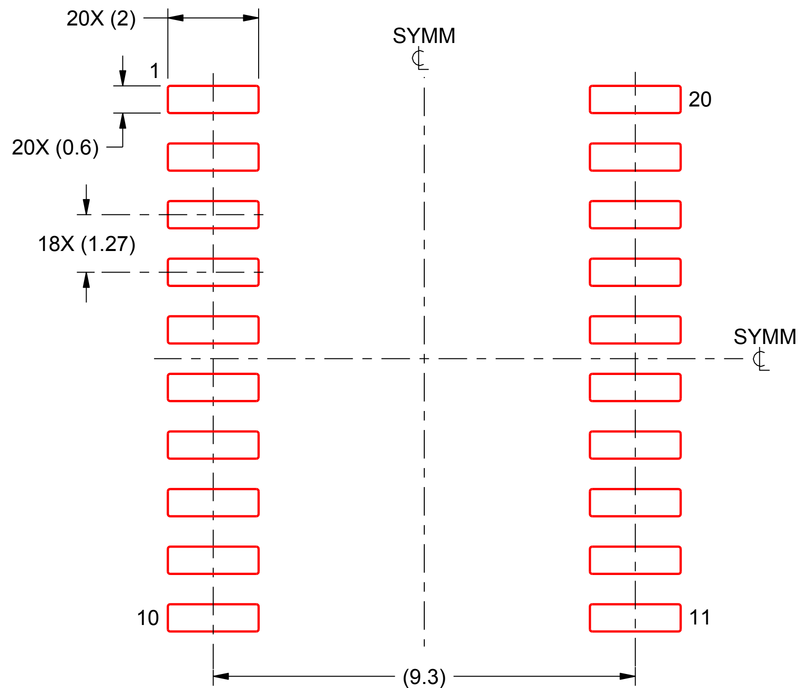
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

2X
5.85

6.6
6.4
NOTE 3

10

11

20X 0.30
0.19

0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

C

SEATING
PLANE

0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25
GAGE PLANE

0.15
0.05

0° -8°

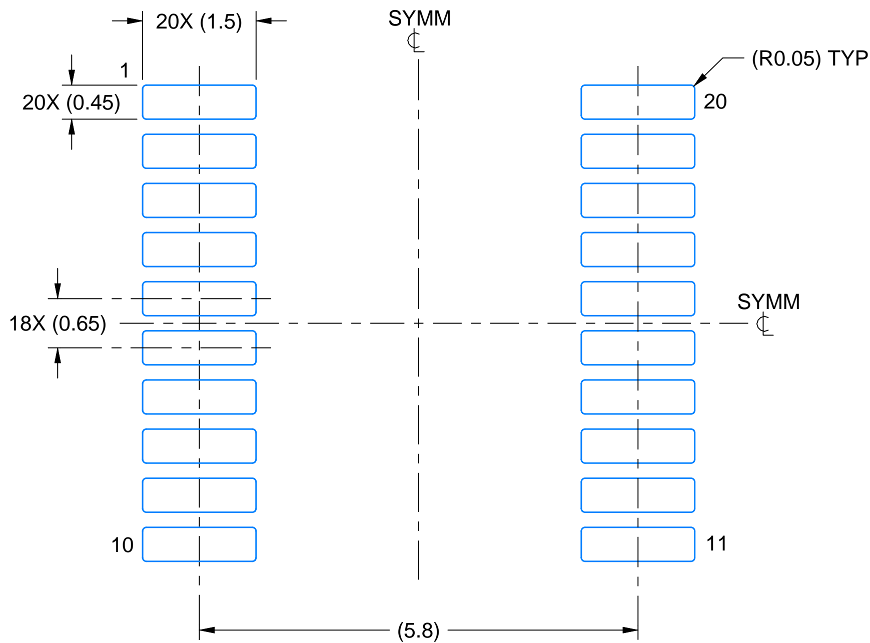
0.75
0.50

DETAIL A
TYPICAL

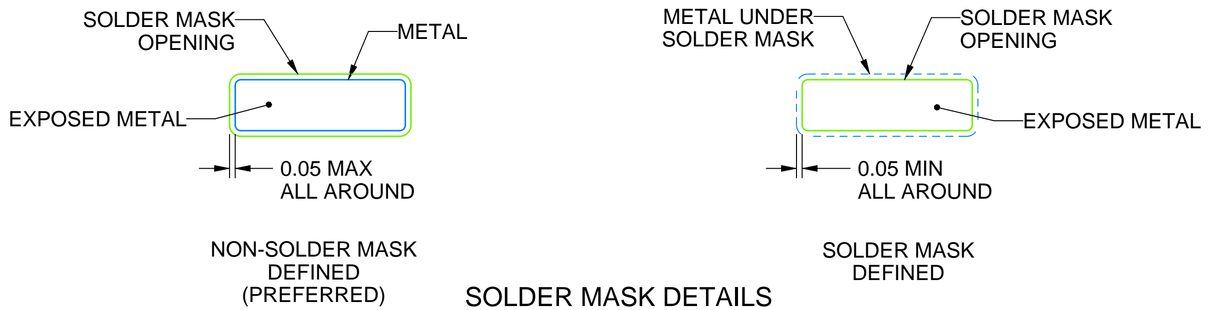
4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

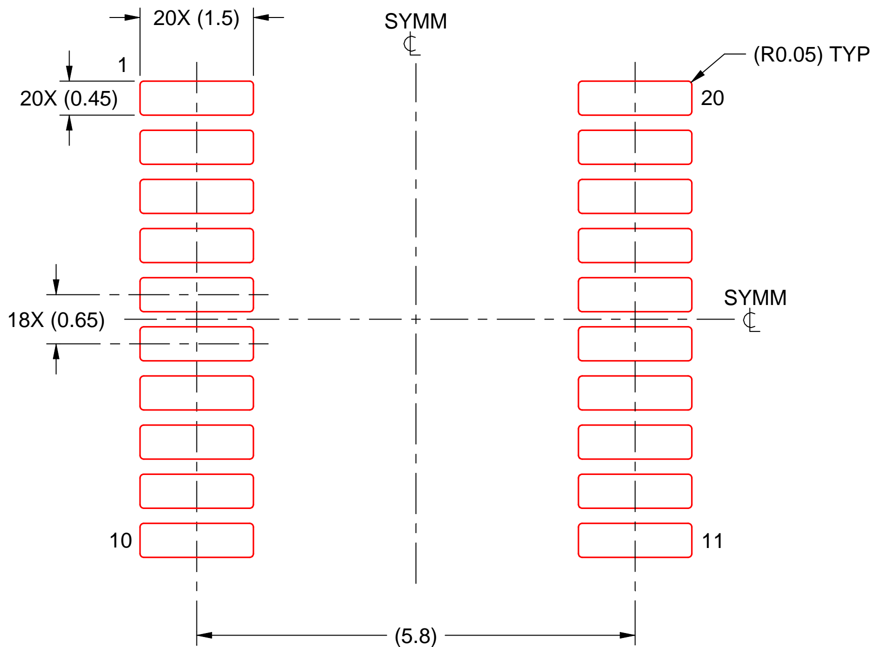
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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