CD74HCT4051-Q1 汽车级高速 CMOS 逻辑模拟多路复用器和多路信号分离器

1 特性

- 宽模拟输入电压范围：±5V（最大值）
- 低导通电阻：
  - 70Ω（典型值）(V_{CC} – V_{EE} = 4.5V)
  - 40Ω（典型值）(V_{CC} – V_{EE} = 9V)
- 低开关间串扰
- 快速开关和传播速度
- 先断后合开关
- 宽工作温度范围：
  - –40°C 至 +125°C
- 工作控制电压：4.5V 至 5.5V
- 开关电压：0V 至 10V
- 直接 LSTTL 输入逻辑兼容性
  V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
- CMOS 输入兼容性
  在 V_{OL}、V_{OH} 下 $I_I \leq 1\mu A$

2 应用

- 数字射频
- 信号门控
- 工厂自动化
- 电视
- 电器
- 可编程逻辑电路
- 传感器

3 说明

CD74HCT4051-Q1 器件是数字控制的模拟开关，它使用硅栅 CMOS 技术并借助标准 CMOS 集成电路的低功耗特性来实现与 LSTTL 接近的运行速度。

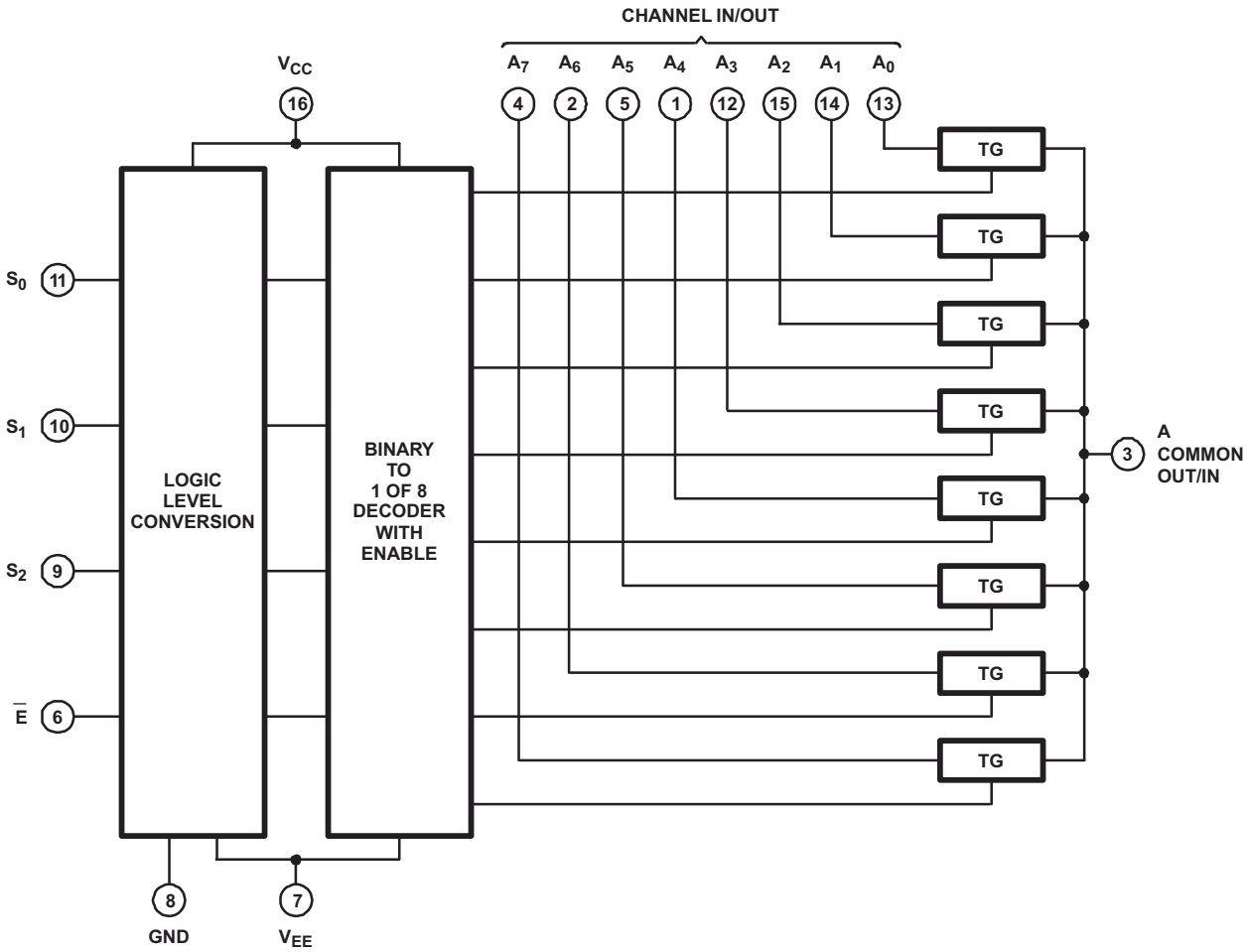
该模拟多路复用器和多路信号分离器可控制模拟电压，该电压可能会在整个电源电压范围内变化（例如，V_{CC} 变为 V_{EE}）。它是双向开关，可将任何模拟输入用作输出，反之亦然。该开关具有低导通电阻和低关断泄漏。此外，该器件还具有使能控制，当处于高电平时将禁用所有开关，将其置于关断状态。

封装信息

器件型号	封装(1)	封装尺寸(2)
CD74HCT4051-Q1	D（SOIC，16）	9.9mm × 3.9mm

(1) 有关更多信息，请参阅节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。



HCT4051 的功能方框图

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4 Pin Configuration and Functions

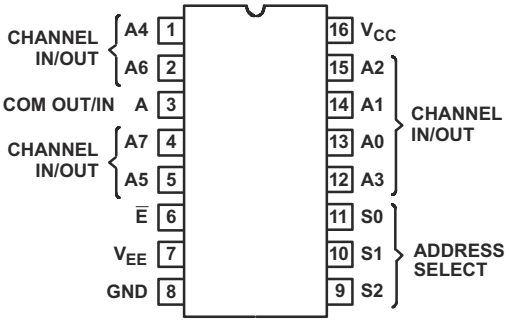

图 4-1. D Package, 16-Pin SOIC (Top View)

INPUTS				ON CHANNELS
ENABLE	S2	S1	S0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC} – V_{EE} (2)	DC Supply voltage		-0.5	10.5	V
V_{CC}			– 0.5	7	V
V_{EE}			0.5	-7	V
I_{IK}	DC input diode current	V_I < – 0.5V or V_I > V_{CC} + 0.5V	– 20	20	mA
I_{OK}	DC switch diode current	V_I < V_{EE} – 0.5V or V_I > V_{CC} + 0.5V	– 20	20	mA
	DC switch current	V_I < V_{EE} – 0.5V or V_I > V_{CC} + 0.5V	-25	25	mA
I_{CC}	DC V_{CC} or ground current		– 50	50	mA
I_{EE}	DC V_{EE} current		– 20		mA
$R_{\theta JA}$	Package thermal impedance(3)			91.6	°C/W
T_{JMAX}	Maximum junction temperature			150	°C
T_{LMAX}	Maximum lead temperature	Soldering 10 s		300	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The package thermal impedance is calculated in accordance with JESD 51-7

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range (T_A = full package temperature range)(2)		4.5		5.5	V
V_{CC} – V_{EE}	Supply voltage range (T_A = full package temperature range)(2)		2		10	V
V_{EE} (2)	Supply voltage range (T_A = full package temperature range)(3)		0		– 6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	DC input control voltage		0		V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}		V_{CC}	V
t_r , t_f	Input rise and fall times	V_{CC} = 4.5V	0		500	ns
T_A	Ambient temperature		– 40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, Literature number SCBA004.
(2) In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{on} values shown in electrical characteristics tables). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

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5.3 Electrical Characteristics: HCT Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT
CD74HCT4051-Q1									
r_{ON} ON resistance	I_O = 1mA V_I=V_{IH} or V_{IL}	V_{IS} = V_{CC} or V_{EE}	0	4.5	25°C		70	160	Ω
					–40°C to +125°C			240	
			-4.5	4.5	25°C		40	120	
					–40°C to +125°C			180	
		V_{IS} = V_{CC} to V_{EE}	0	4.5	25°C		90	180	Ω
					–40°C to +125°C			270	
			-4.5	4.5	25°C		45	130	
					–40°C to +125°C			195	
Δr_{ON} Maximum ON resistance between any two channels	Between any two channels		0	4.5	25°C		10		Ω
			-4.5	4.5	25°C		5		
I_{IZ} Switch ON/OFF leakage current	For switch OFF: When VIS = VCC, VOS = VEE; When VIS = VEE, VOS = VCC, For switch ON: All applicable combinations of VIS and VOS voltage levels V_I = V_{IH} or V_{IL}		0	6	25°C			±0.2	µA
					–40°C to 125°C			±2	
			-5	5	25°C			±0.4	
					–40°C to 125°C			±4	
I_{IL} Control input leakage current	V_I = V_{CC} or GND			5.5	25°C			±0.1	µA
					–40°C to 125°C			±1	
Quiescent Device Current, I_{CC} Max	I_O = 0 V_{IS} = V_{CC} or GND	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	0	6	25°C			12	µA
					–40°C to 125°C			160	
		When V_{IS} = V_{CC}, V_{OS} = V_{EE}	-5	5	25°C			32	
					–40°C to 125°C			320	
Quiescent Device Current, ΔI_{CC} Max(1)	Per input pin: 1 unit load, V_{IN} = V_{CC} - 2.1V			4.5V to 5.5V	25°C		100	360	µA
					–40°C to 125°C			490	

(1) For dual-supply systems, theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

5.4 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions			MIN	NOM	MAX	UNIT
t_{PD}	Switch IN to OUT	C_L = 15pF	V_{CC} = 5V	25°C		4		ns
		C_L = 50pF	V_{CC} = 4.5V	25°C			12	ns
				–40°C to +125°C			18	ns
			V_{CC} = 4.5V, V_{EE} = -4.5V	25°C			8	ns
				–40°C to +125°C			12	ns

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5.4 Switching Characteristics（续）

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions			MIN	NOM	MAX	UNIT
t_{en}	ADDRESS SEL or $\overline{E}$ to OUT	C_L = 15pF	V_{CC} = 5V	25°C		23		ns
		C_L = 50pF	V_{CC} = 4.5V	25°C			55	ns
				–40°C to +125°C			83	ns
			V_{CC} = 4.5V, V_{EE} = -4.5V	25°C			48	ns
				–40°C to +125°C			60	ns
t_{dis}	ADDRESS SEL or $\overline{E}$ to OUT	C_L = 15pF	V_{CC} = 5V	25°C		35		ns
		C_L = 50pF	V_{CC} = 4.5V	25°C			50	ns
				–40°C to +125°C			68	ns
			V_{CC} = 4.5V, V_{EE} = -4.5V	25°C			44	ns
				–40°C to +125°C			55	ns
C_I	Control			–40°C to +125°C			10	pF
C_{PD}	Power dissipation capacitance (1)					52		pF

(1) Cpd is used to determine the dynamic power consumption, per package.
PD = Cpd VCC2 fI + Σ (CL + CS) VCC2 fO
fO = output frequency
fI = input frequency
CL = output load capacitance
CS = switch capacitance
VCC = supply voltage

5.5 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter	Test Conditions	V_{EE} (V)	V_{CC} (V)	MIN	NOM	MAX	UNIT
C_I Switch input capacitance					5		pF
C_{COM} Common output capacitance					25		pF
f_{MAX} (2) Minimum switch frequency response at –3 dB(1)		-2.25	2.25		145		MHz
		-4.5	4.5		180		
THD Sine-wave distortion		-2.25	2.25		0.035		%
		-4.5	4.5		0.018		
Switch OFF signal(2) feedthrough(3)		-2.25	2.25		-73		dB
		-4.5	4.5		-75		

(1) Adjust input voltage to obtain 0 dBm at VOS for fIN = 1 MHz.
(2) VIS is centered at (VCC − VEE)/2.
(3) Adjust input for 0 dBm.

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5.6 Typical Characteristics

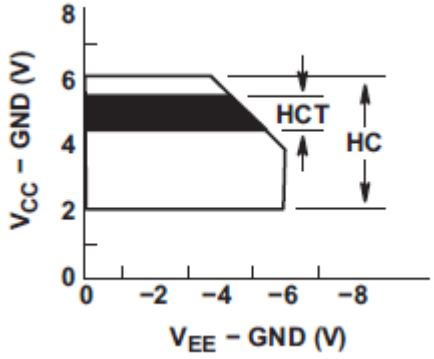

图 5-1. Recommended Operating Area as a Function of (V_{CC} - V_{EE})

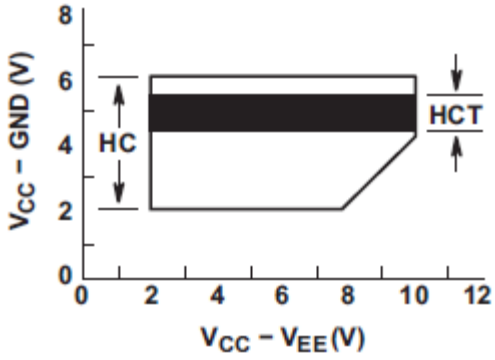

图 5-2. Recommended Operating Area as a Function of (V_{CC} - GND)

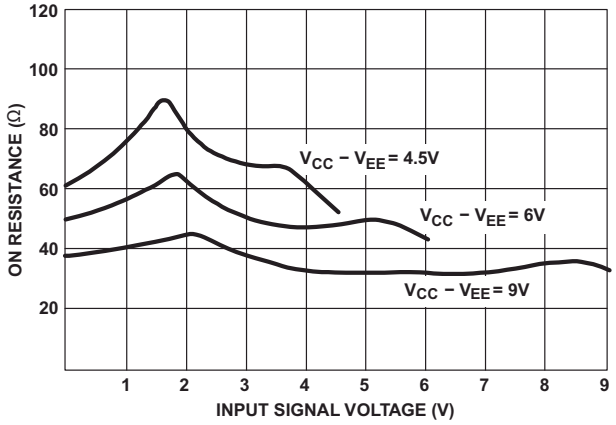

图 5-3. Typical ON Resistance vs Input Signal Voltage

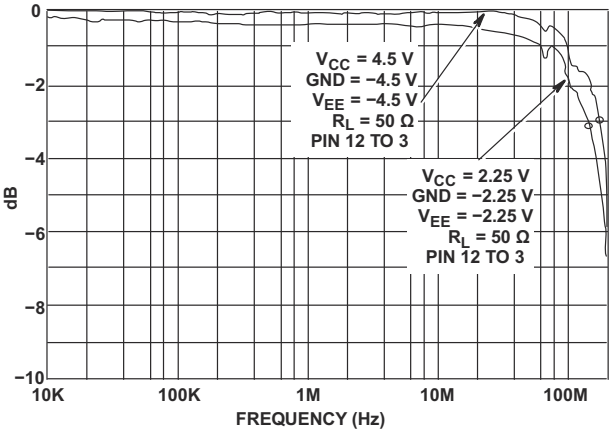

图 5-4. Channel ON Bandwidth (HC and HCT4051)

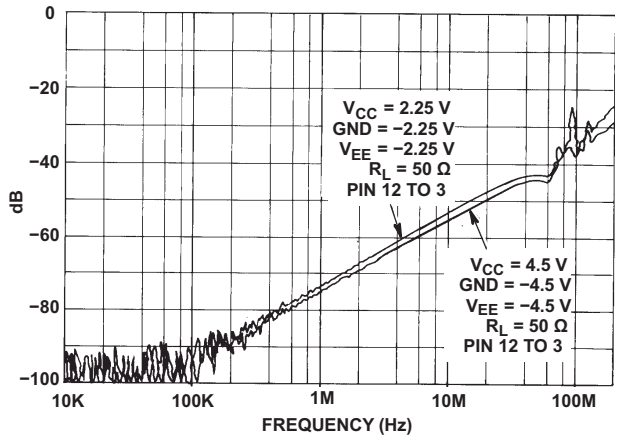

图 5-5. Channel OFF Feedthrough (HC and HCT4051)

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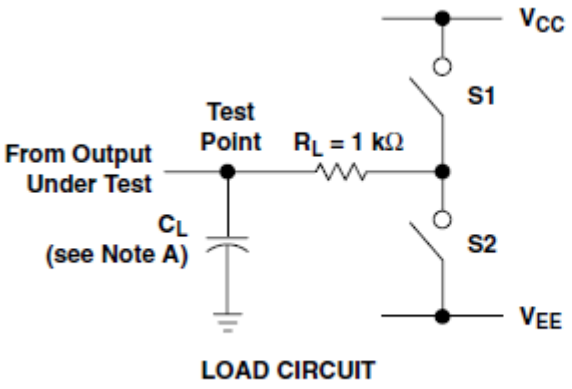
6 Parameter Measurement Information



PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open

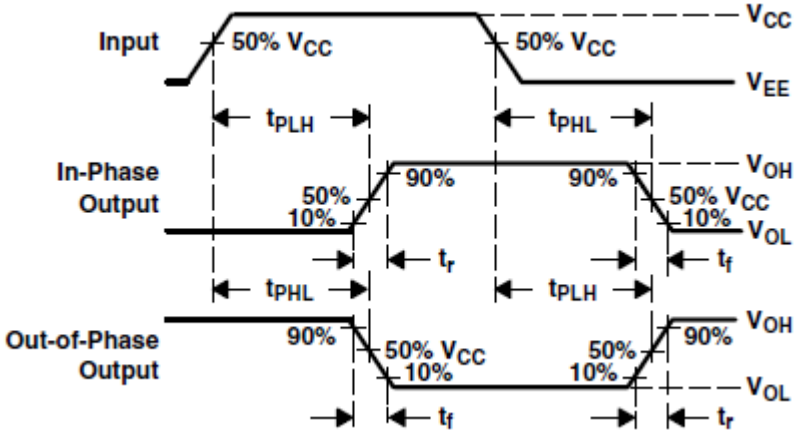


图 6-1. Propagation delay and output transition times. Waveform 1

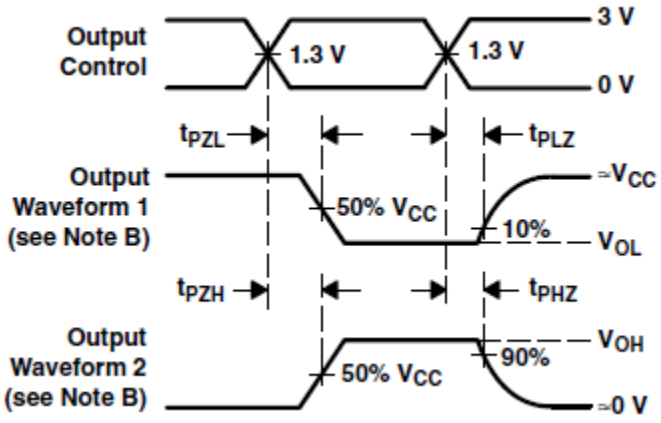


图 6-2. Output enable and disable times. Waveform 2

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

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Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50 Ω, t_r = 6ns, t_f = 6ns.
D. For clock inputs, f_{MAX} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} AND t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

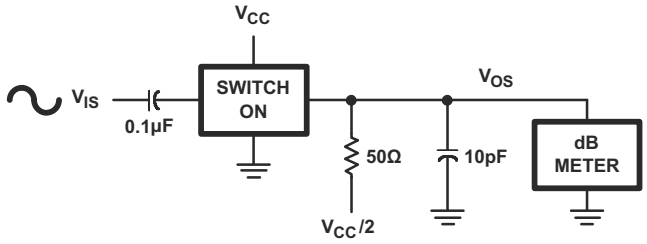
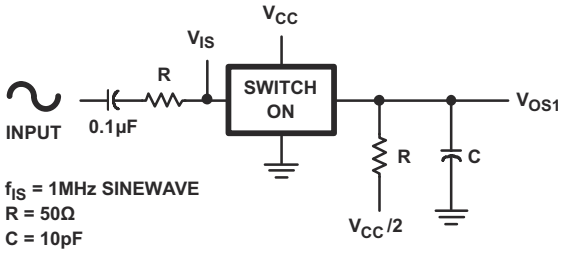


图 6-3. Frequency Response Test Circuit



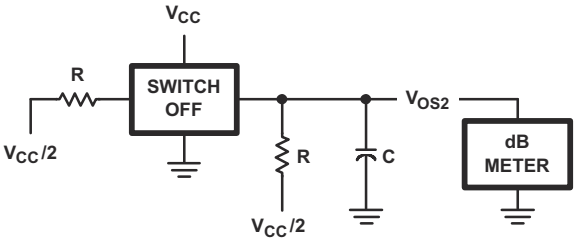


图 6-4. Crosstalk Between Two Switches Test Circuit

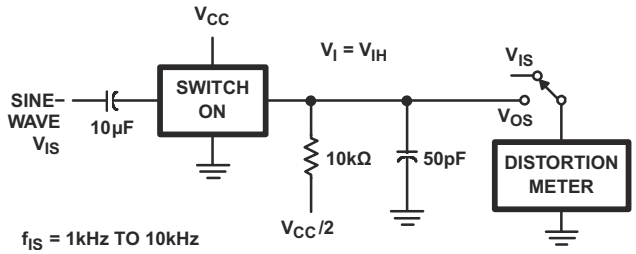


图 6-5. ¼Sine-Wave Distortion Test Circuit

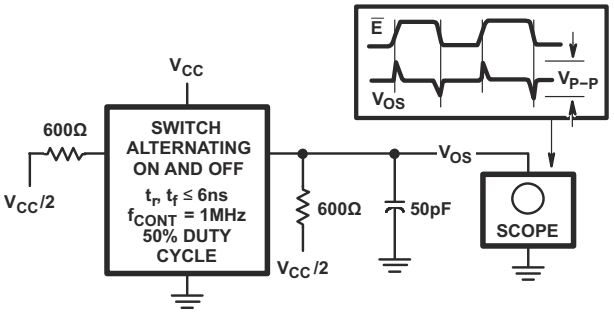


图 6-6. Control to Switch Feedthrough Noise Test Circuit

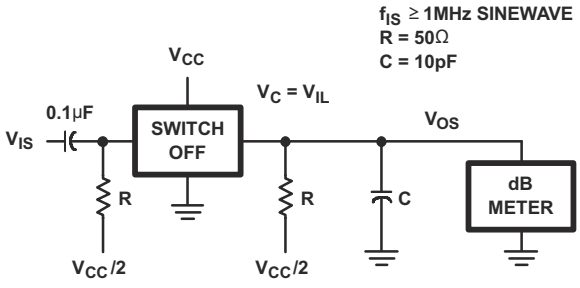


图 6-7. Switch OFF Signal Feedthrough

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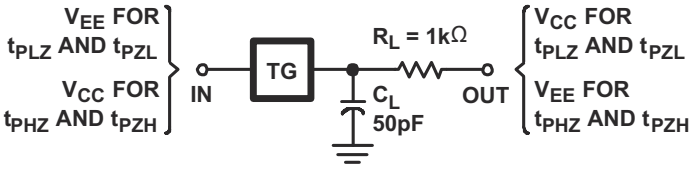

图 6-8. Switch ON/OFF Propagation Delay Test Circuit

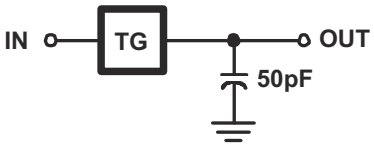

图 6-9. Switch In to Switch Out Propagation Delay Test Circuit

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7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

7.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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7.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2008) to Revision C (April 2024)	Page
• Changed HCT ICC at 25°C single/dual supply	5
• Changed t_{en} ADDRESS SEL or $\overline{E}$ to OUT	5
• Changed t_{dis} ADDRESS SEL or $\overline{E}$ to OUT	5

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4051QM96Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4051Q	Samples
D24051QM96G4Q1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	HCT4051Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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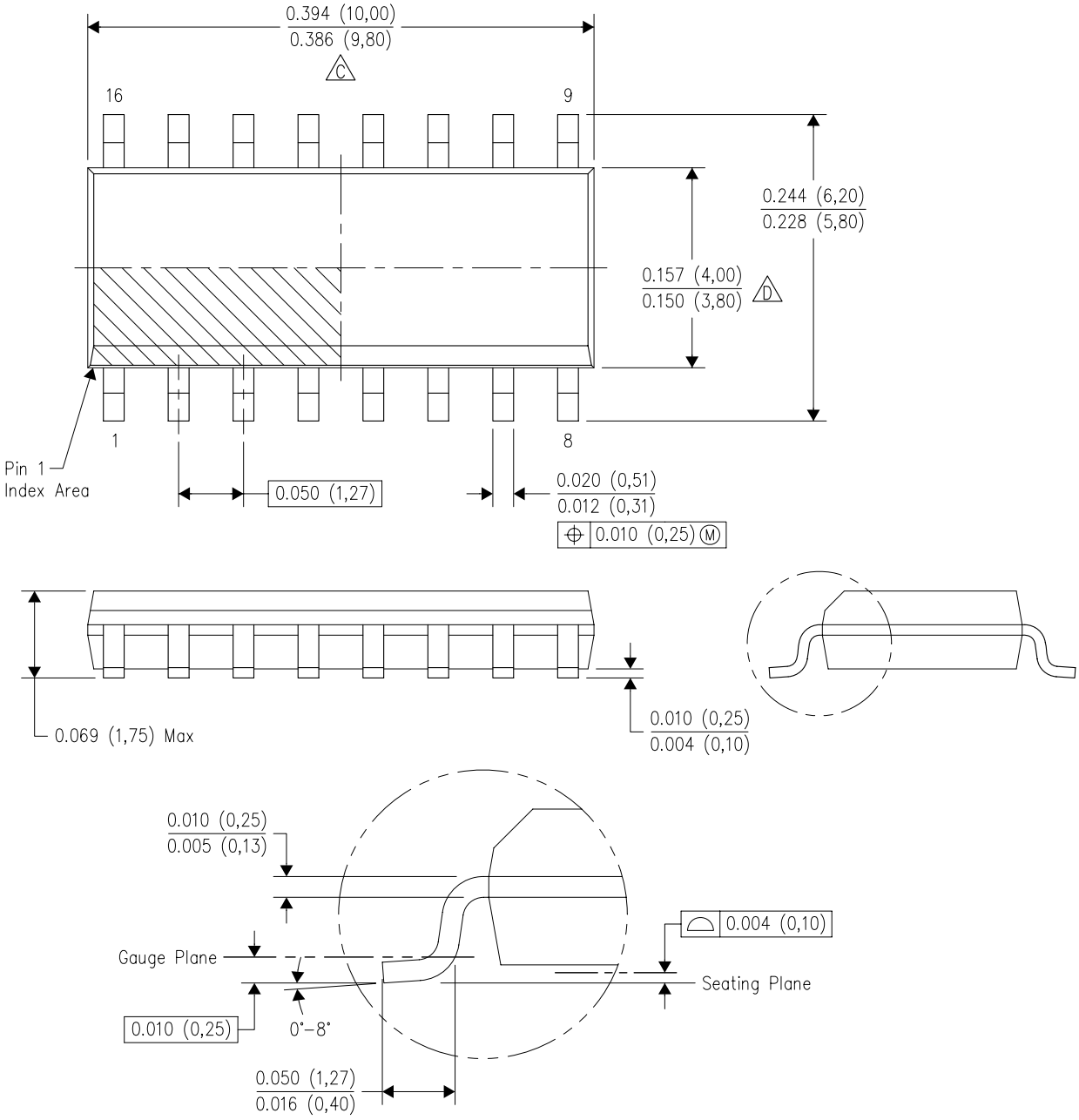
OTHER QUALIFIED VERSIONS OF CD74HCT4051-Q1 :

- Catalog : CD74HCT4051
- Military : CD54HCT4051

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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