CSD16321Q5 25V N 沟道 NexFET™ 功率 MOSFET

1 特性

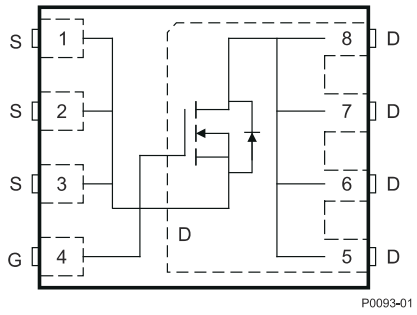
- 针对 5V 栅极驱动器进行了优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 5mm × 6mm SON 塑料封装

2 应用

- 用于网络互联，电信和计算系统的负载点同步降压转换器
- 已针对同步场效应晶体管 (FET) 应用进行优化

3 说明

这款 25V、1.9mΩ、5mm × 6mm SON NexFET™ 功率 MOSFET 旨在更大限度减小功率转换应用中的损耗，并针对 5V 栅极驱动应用进行了优化。



顶视图

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源极电压	25		V
Q_g	栅极电荷总量 (4.5V)	14		nC
Q_{gd}	栅极电荷（栅极到漏极）	2.5		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS}=3V	2.8	mΩ
		V_{GS} = 4.5V	2.1	
		V_{GS} = 8V	1.9	
$V_{GS(th)}$	阈值电压	1.1		V

器件信息(1)

器件	介质	数量	封装	出货
CSD16321Q5	13 英寸卷带	2500	SON 5.00mm × 6.00mm 塑料封装	卷带包装
CSD16321Q5T	7 英寸卷带	250		

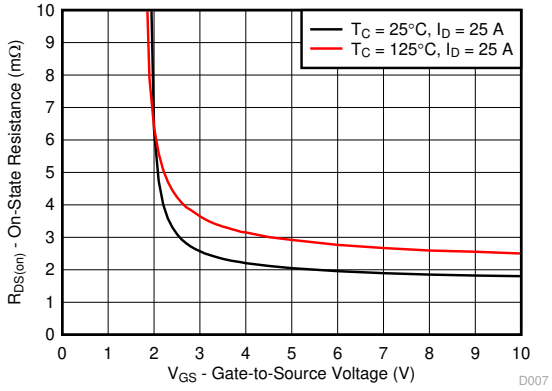
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

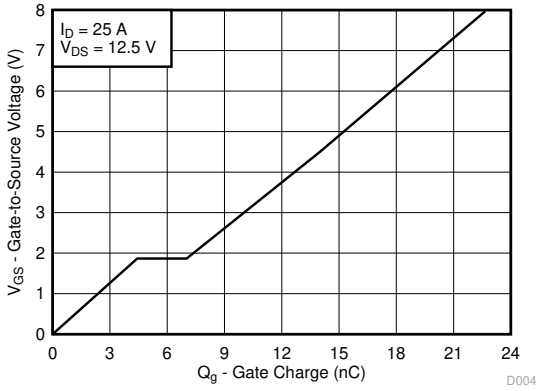
T_A = 25°C		值	单位
V_{DS}	漏源极电压	25	V
V_{GS}	栅源电压	+10 / –8	V
I_D	持续漏极电流（受封装限制）	100	A)
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	177	
	持续漏极电流(1)	29	
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功率耗散(1)	3.1	W
	功率耗散，T_C = 25°C	113	
T_J、T_{stg}	工作结温、贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 66A，L = 0.1mH，R_G = 25Ω	218	mJ

(1) $R_{\theta JA}$ = 40°C/W，这是在 0.06 英寸厚 FR4 PCB 上的 1 平方英寸、2oz 铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 1.1°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。



$R_{DS(ON)}$与 V_{GS} 间的关系



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

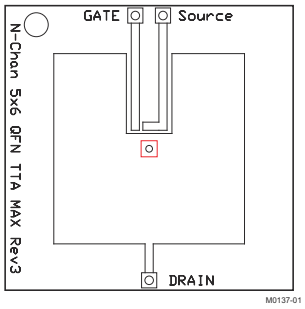
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3 V, I_D = 25 A		2.8	3.8	mΩ
		V_{GS} = 4.5 V, I_D = 25 A		2.1	2.6	
		V_{GS} = 8 V, I_D = 25 A		1.9	2.4	
g_{fs}	Transconductance	V_{DS} = 12.5 V, I_D = 25 A		150		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		2360	3100	pF
C_{oss}	Output capacitance			1700	2200	pF
C_{rss}	Reverse transfer capacitance			115	150	pF
R_G	Series gate resistance			1.5	3	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 25 A		14	19	nC
Q_{gd}	Gate charge gate-to-drain			2.5		nC
Q_{gs}	Gate charge gate-to-source			4		nC
$Q_{g(th)}$	Gate charge at V_{th}			2.1		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		36		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 25 A, R_G = 2 Ω		9		ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			17		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13 V, I_F = 25 A, di/dt = 300 A/μs		33		nC
t_{rr}	Reverse recovery time	V_{DD} = 13 V, I_F = 25 A, di/dt = 300 A/μs		32		ns

4.2 Thermal Information

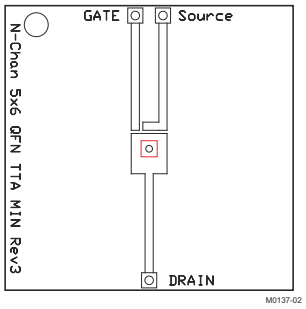
T_A = 25°C (unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			1.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2, 2-oz Cu pad on a 1.5-in × 1.5-in, 0.06-in thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 in^2 of 2-oz Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 of 2-oz Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

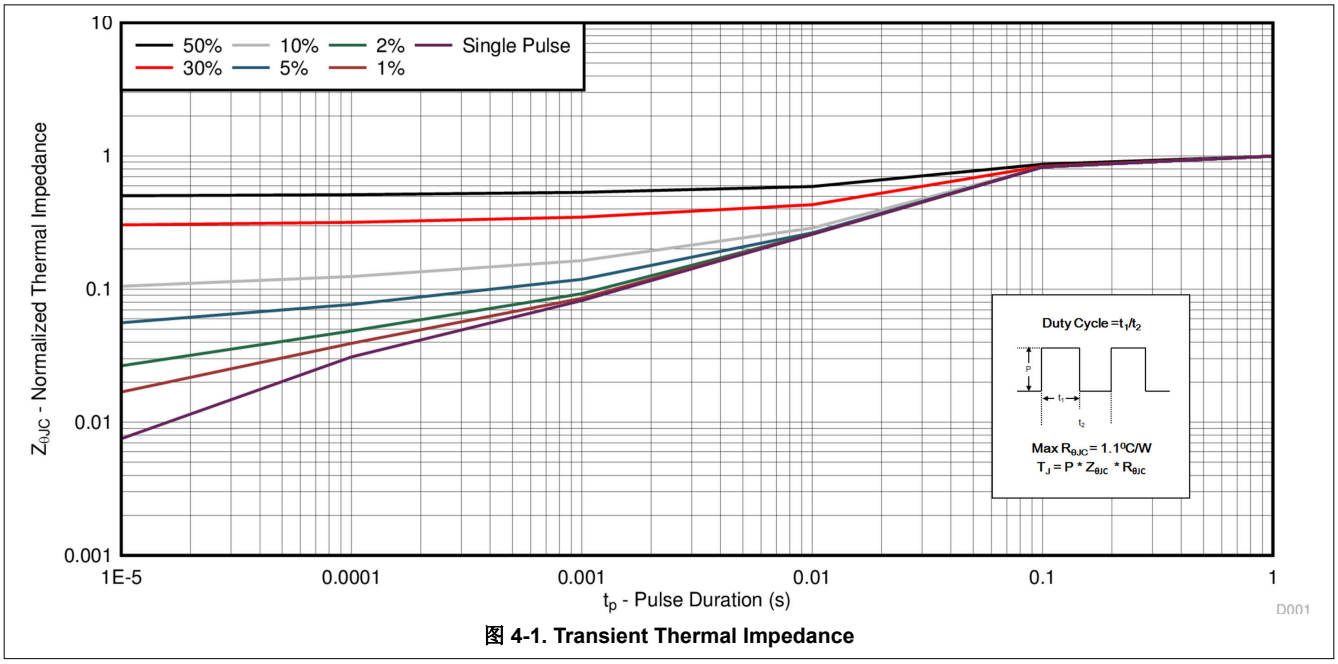


图 4-1. Transient Thermal Impedance

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

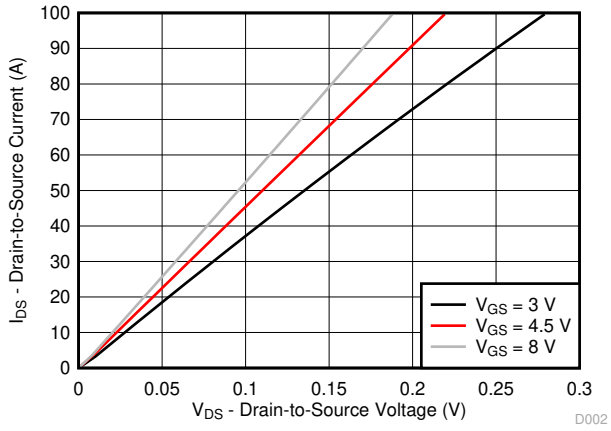
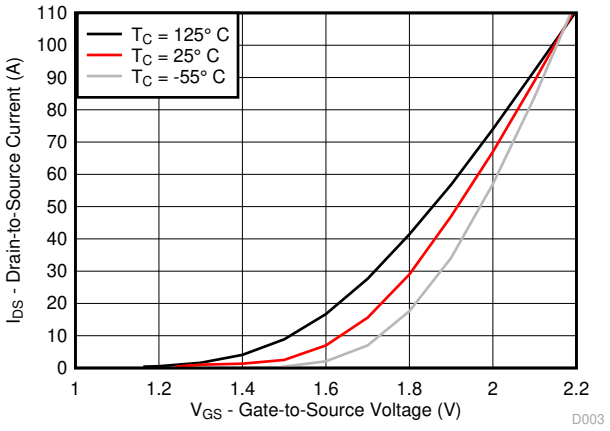
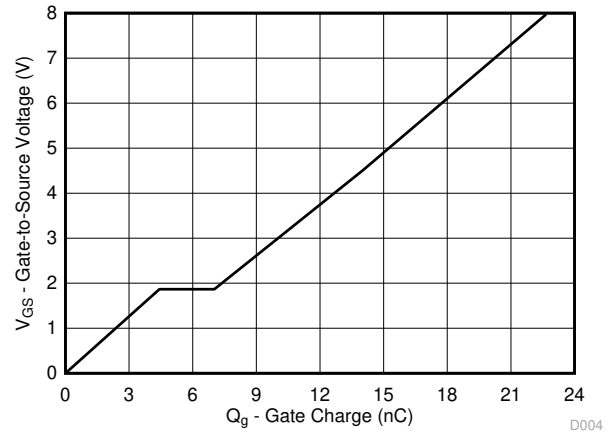


图 4-2. Saturation Characteristics



V_{DS} = 5 V

图 4-3. Transfer Characteristics



V_{DS} = 12.5 V I_D = 25 A

图 4-4. Gate Charge

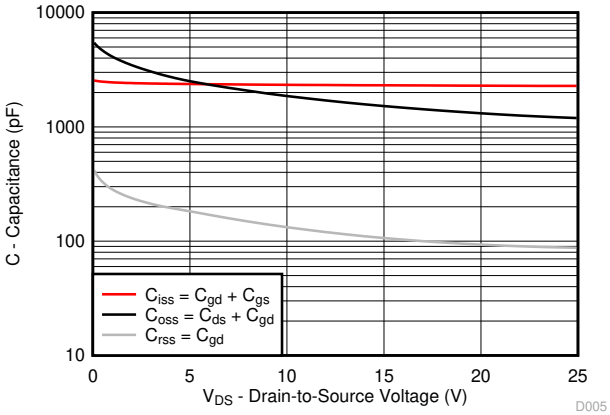
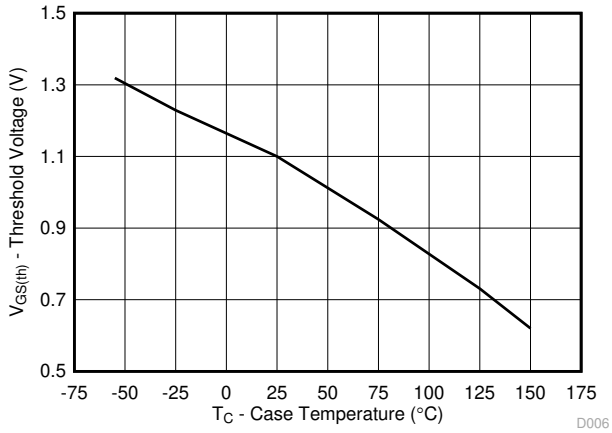


图 4-5. Capacitance



I_D = 250 µA

图 4-6. Threshold Voltage vs Temperature

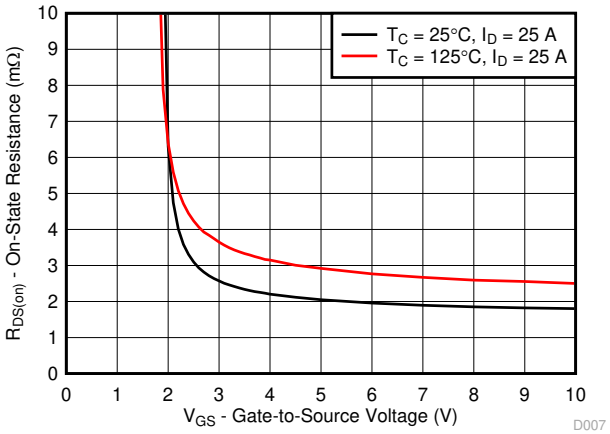
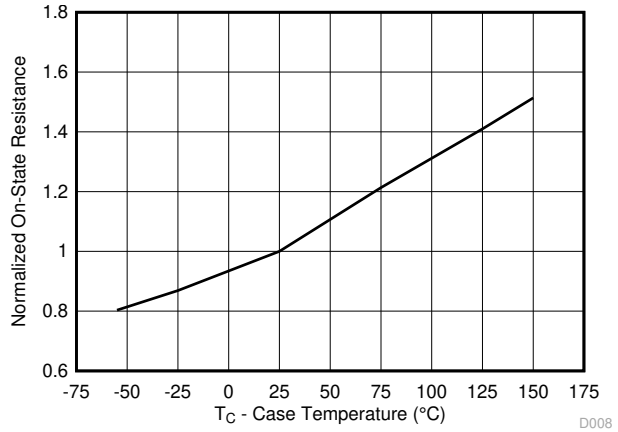


图 4-7. On Resistance vs Gate Voltage

4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = 25 A V_{GS} = 8 V

图 4-8. On Resistance vs Temperature

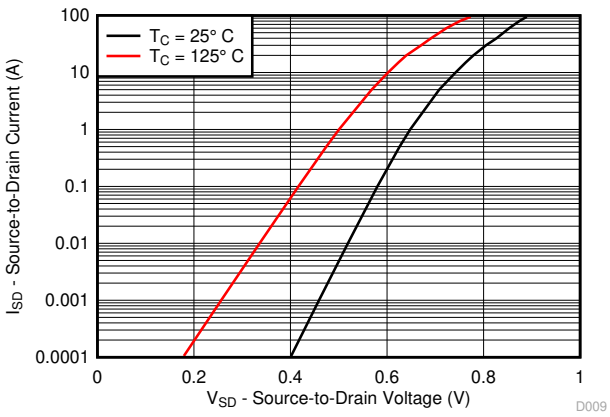
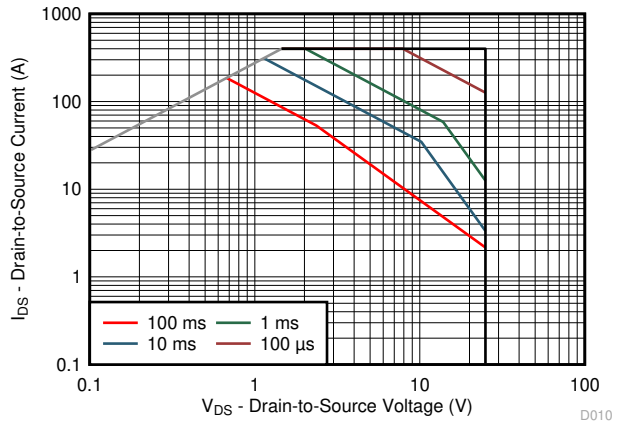


图 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 1.1°C/W

图 4-10. Maximum Safe Operating Area

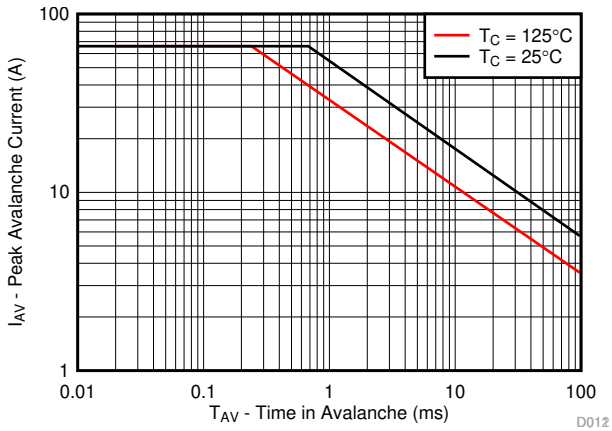


图 4-11. Single Pulse Unclamped Inductive Switching

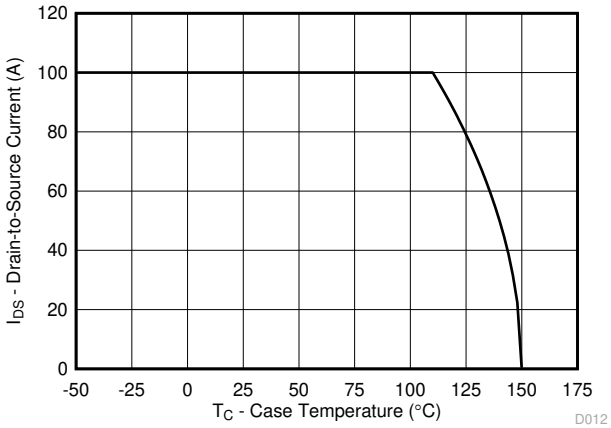


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.3 Trademarks

NexFET™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

5.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (May 2017) to Revision E (December 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision C (December 2016) to Revision D (May 2017)	Page
• 更改了 3V、4.5V、8V 时的 $R_{DS(ON)}$ 值以及*说明*，以匹配*电气特性* 表中的值	1

Changes from Revision B (May 2010) to Revision C (December 2016)	Page
• 更改了*说明* 文本	1
• 向*绝对最大额定值* 表中添加了受器件限制的持续漏极电流	1
• 向*绝对最大额定值* 表中添加了 T_C = 25°C 时的最大功率耗散	1
• 更改了*绝对最大额定值* 表中的注释 2	1
• Changed $R_{\theta JA}$ max from 48°C/W : to 50°C/W	3
• Changed the SOA in 图 4-10 to reflect measured data	4
• Changed *MECHANICAL DATA* section to *Mechanical, Packaging, and Orderable Information* section	9

Changes from Revision A (January 2010) to Revision B (May 2010)	Page
• Changed $R_{DS(on)}$ - V_{GS} = 3 V, I_D = 25 A MAX value From: 3.5 To: 3.8	3

Changes from Revision * (August 2009) to Revision A (January 2010)	Page
• 更改了顶视图引脚排列图上的标签	1
• 将*绝对最大额定值* 的注释 1 从“$R_{\theta JA}$ = 39°C/W”更改为“典型 $R_{\theta JA}$ = 39°C/W”	1
• Changed 图 4-1 text From: $R_{\theta JA}$ = 92°C/W To: Typical $R_{\theta JA}$ = 93°C/W	4

- Changed 图 4-10 text From: $R_{\theta JA}$ = 92°C/W To: Typical $R_{\theta JA}$ = 93°C/W 4
- Changed 图 4-11 X-axis values 4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Option Addendum

Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
CSD16321Q5	ACTIVE (1)	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

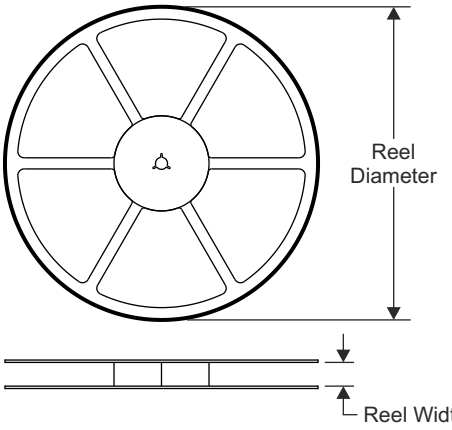
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

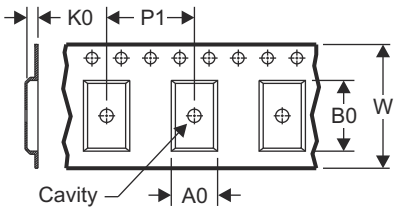
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

7.2 Tape and Reel Information

REEL DIMENSIONS

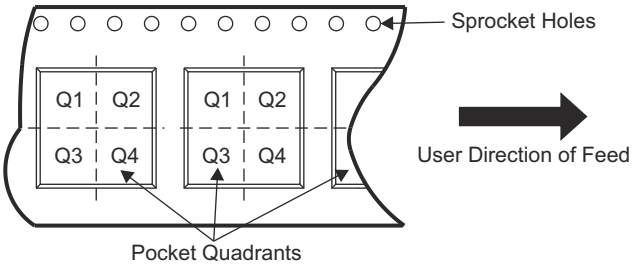


TAPE DIMENSIONS



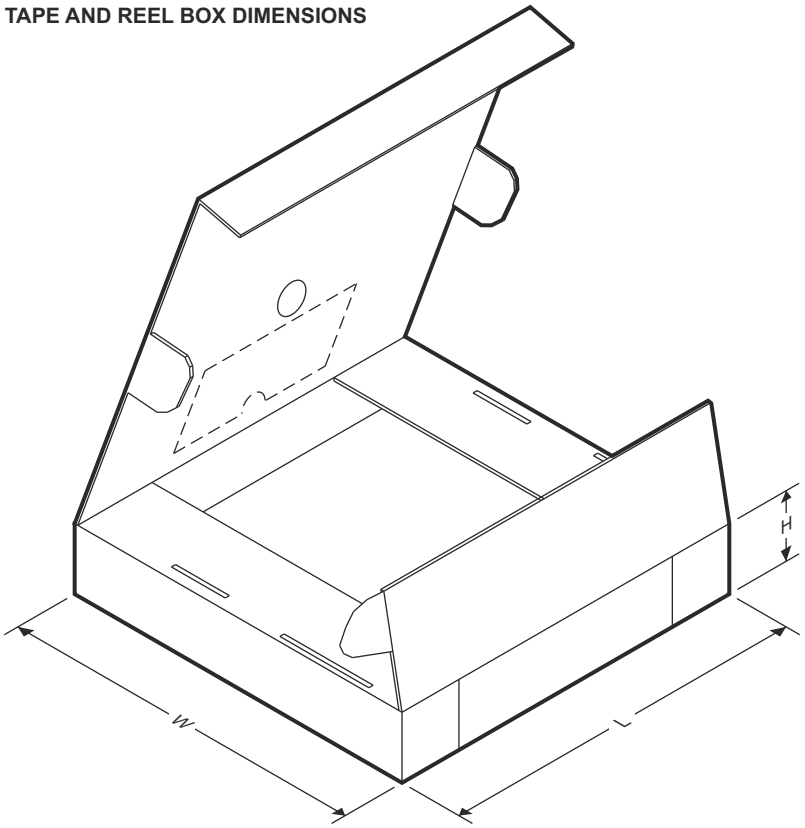
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

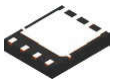
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

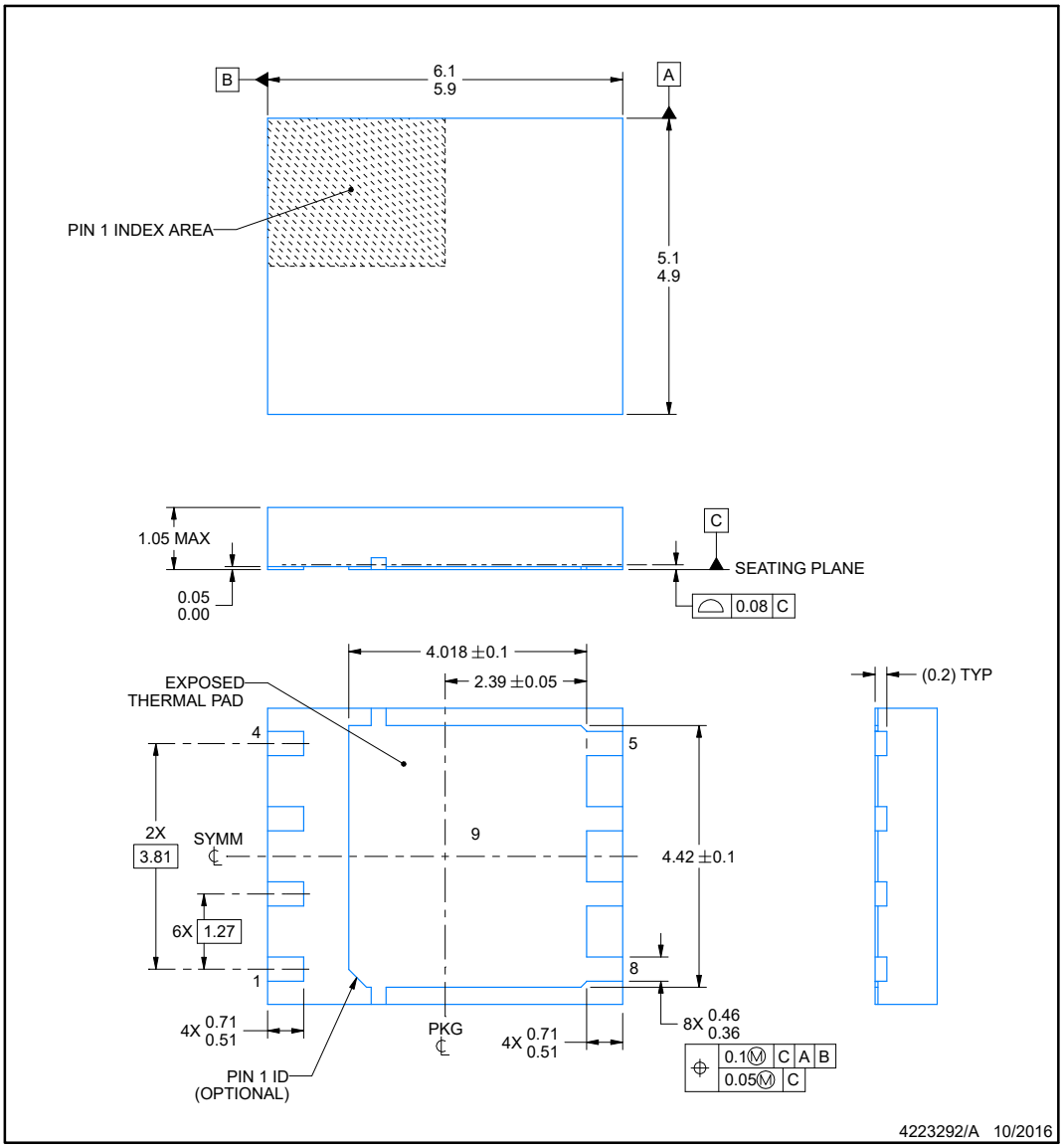
PACKAGE OUTLINE

DQH0008A



VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



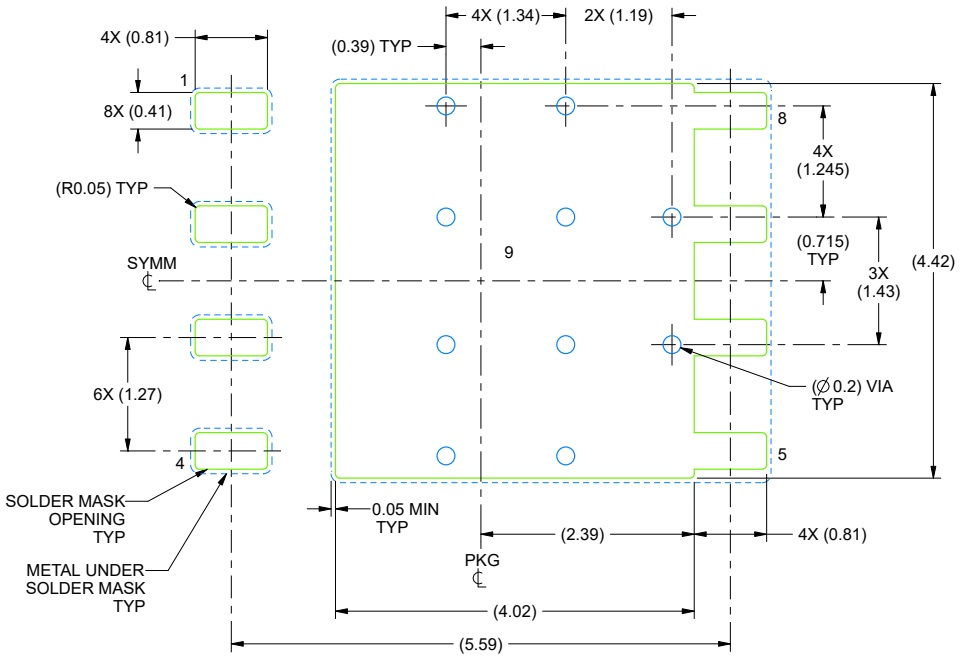
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DQH0008A — **VSON-CLIP - 1.05 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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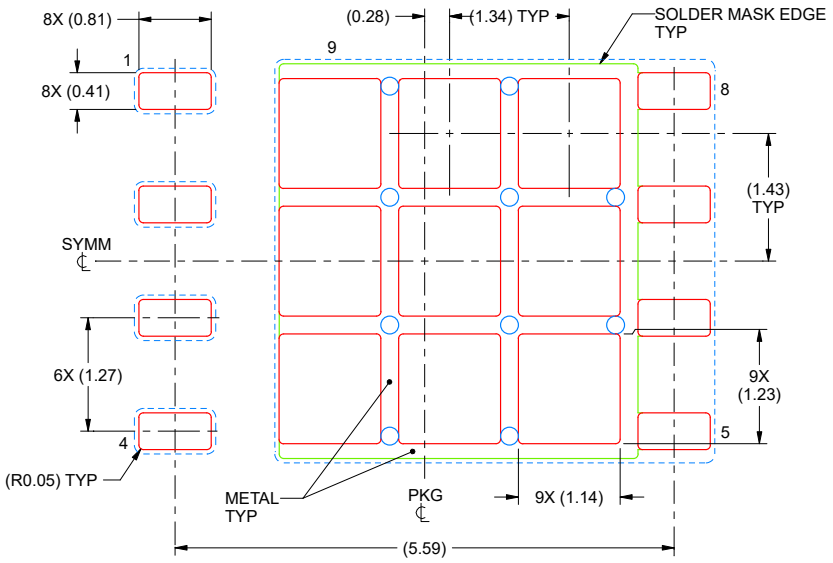
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQH0008A — **VSON-CLIP - 1.05 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16321Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321	Samples
CSD16321Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

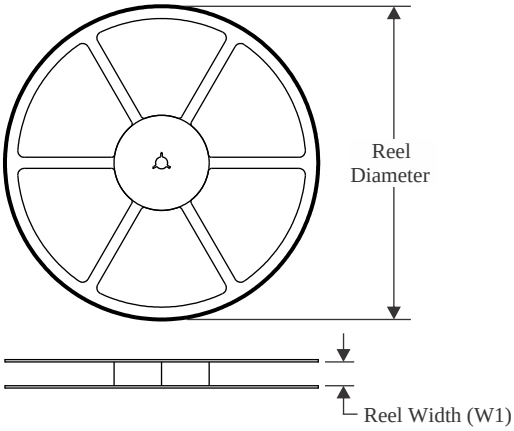
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

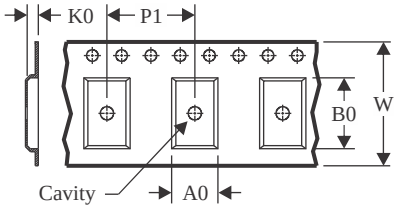
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

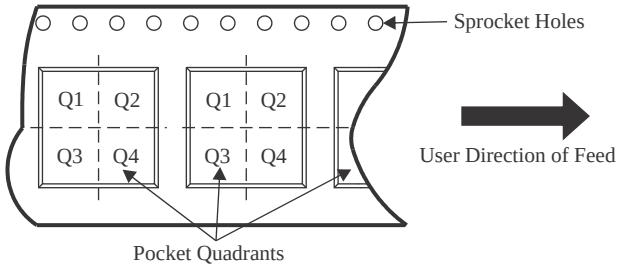


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

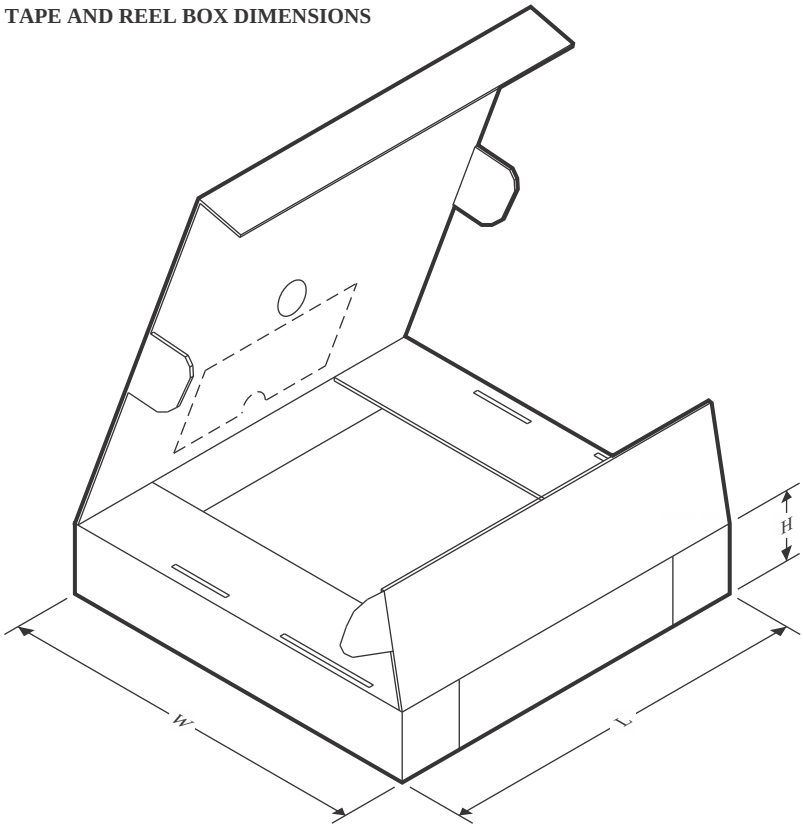
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

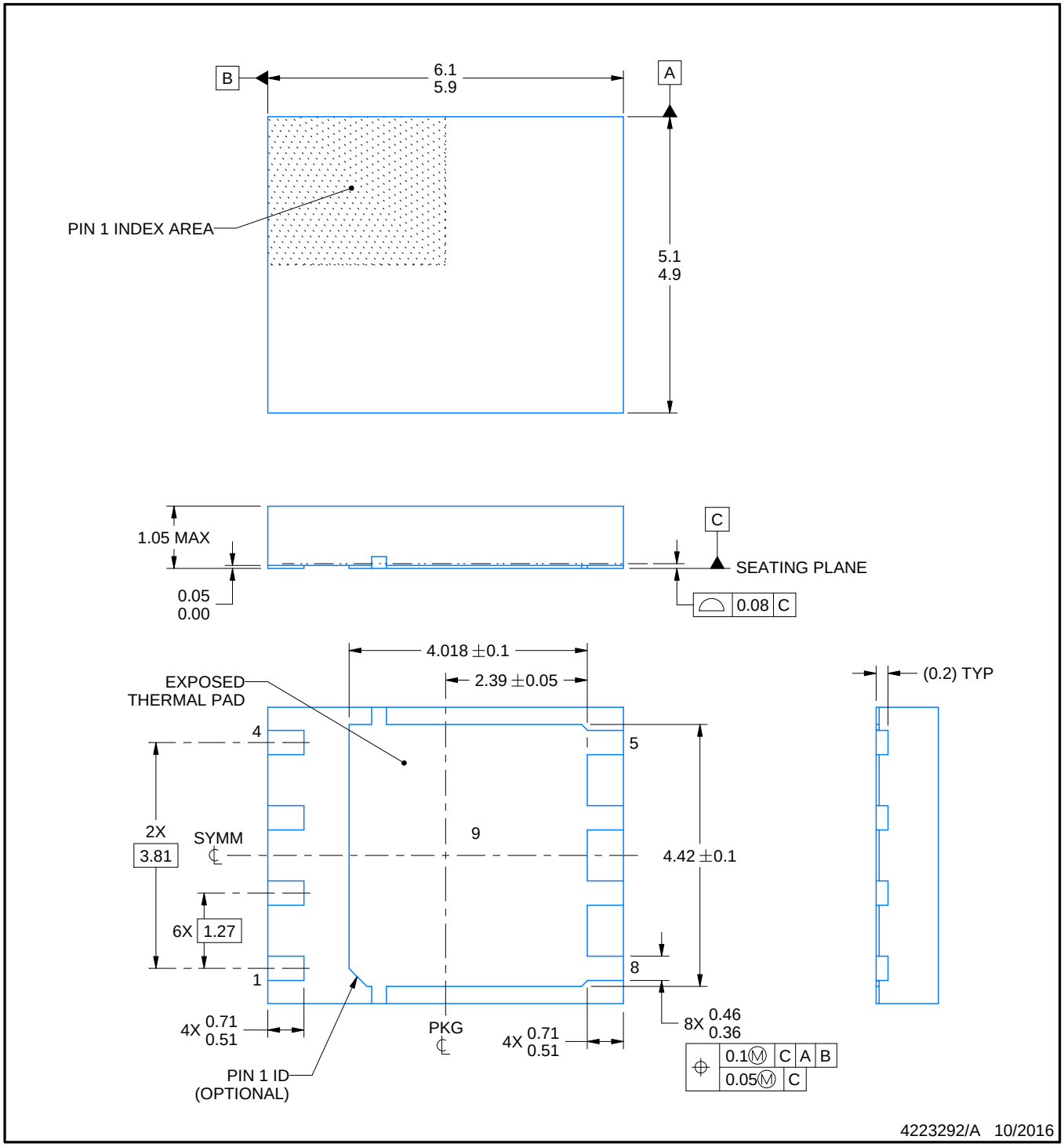
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

PACKAGE OUTLINE

DQH0008A

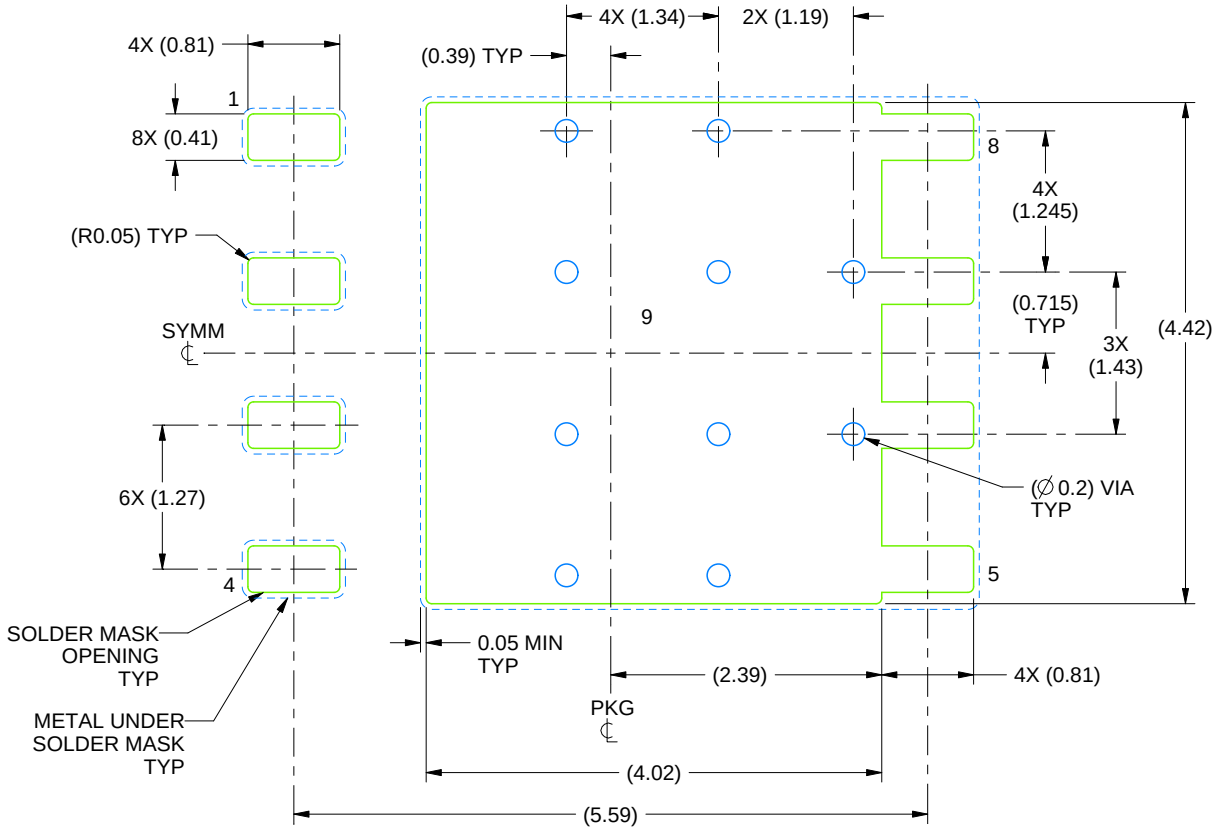
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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NOTES: (continued)

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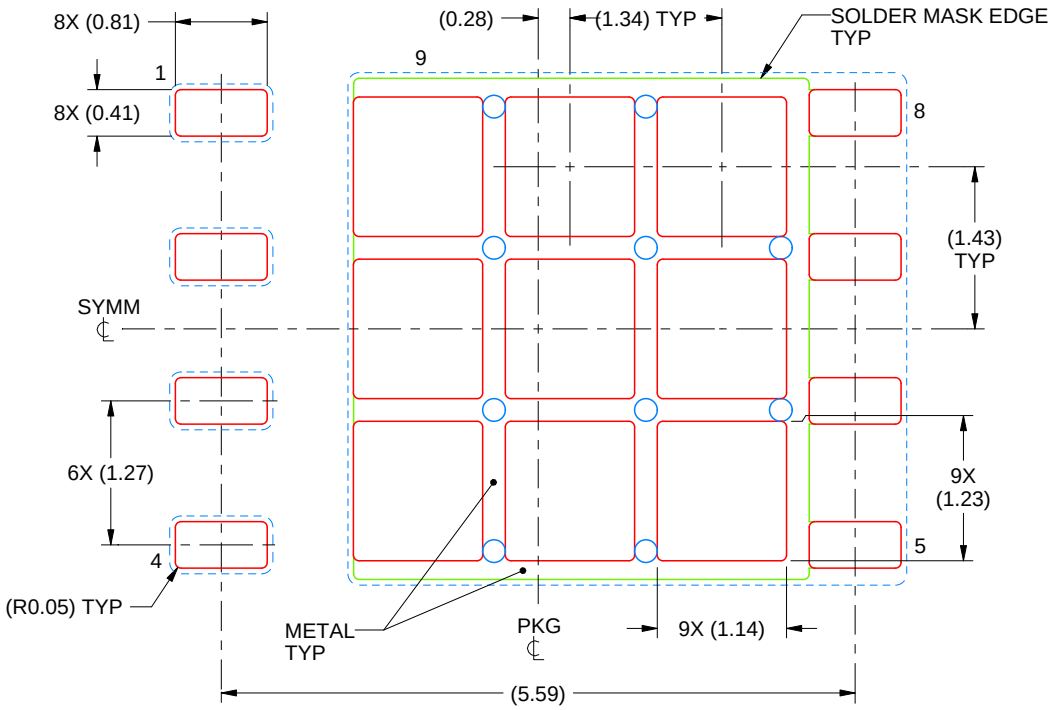

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

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