

CSD16401Q5 25V N 沟道 NexFET™ 功率 MOSFET

1 特性

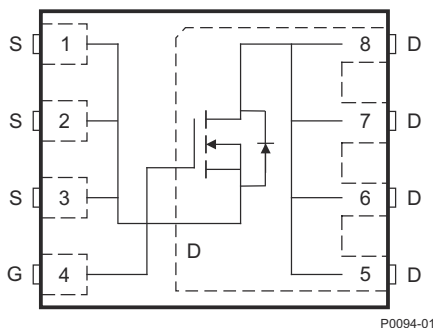
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- SON 5mm × 6mm 塑料封装

2 应用

- 网络、电信和计算系统应用中的负载点同步降压转换器
- 针对同步 FET 应用进行了优化

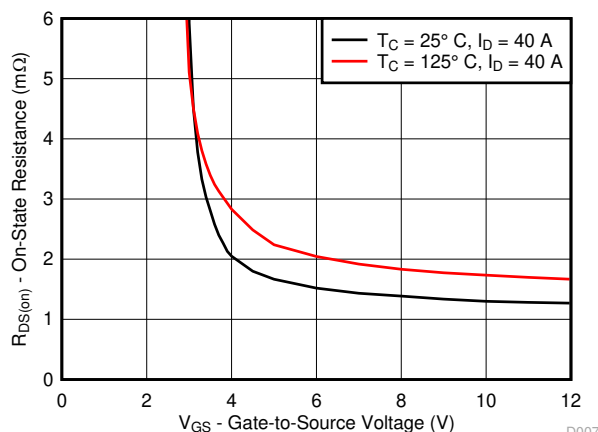
3 说明

这款 25V、1.3mΩ、5mm × 6mm SON NexFET™ 功率 MOSFET 旨在更大限度减小功率转换应用中的损耗。



P0094-01

顶视图



D007

$R_{DS(ON)}$ 与 V_{GS} 间的关系

产品概要

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源极电压	25	V
Q_g	总栅极电荷 (4.5V)	21	nC
Q_{gd}	栅极电荷 (栅漏极)	5.2	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	1.8
		$V_{GS} = 10\text{V}$	1.3
$V_{GS(th)}$	阈值电压	1.5	V

器件信息(1)

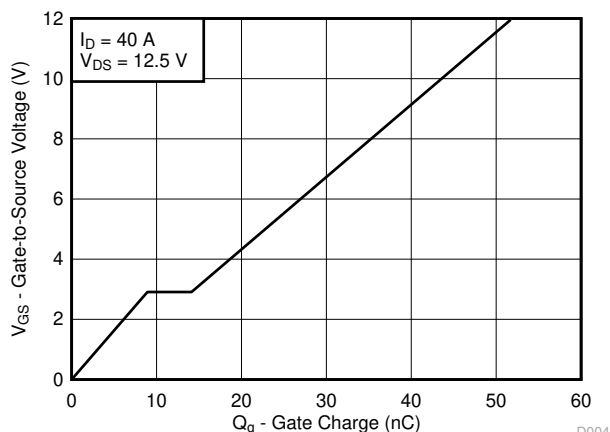
器件	介质	数量	封装	出货
CSD16401Q5	13 英寸卷带	2500	SON 5.00mm × 6.00mm 塑料封装	卷带包装

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源极电压	25	V
V_{GS}	栅源电压	-12 至 16	V
I_D	持续漏极电流 (受封装限制)	100	A)
	持续漏极电流 (受器件限制), $T_C = 25^\circ\text{C}$	261	
	持续漏极电流 ⁽¹⁾	38	
I_{DM}	脉冲漏极电流, $T_A = 25^\circ\text{C}$ ⁽²⁾	240	A
P_D	功率耗散 ⁽¹⁾	3.1	W
	功率耗散, $T_C = 25^\circ\text{C}$	156	
T_J , T_{stg}	工作结温, 贮存温度	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D = 100\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	500	mJ

- (1) $R_{\theta JA} = 40^\circ\text{C/W}$ (在 0.06in (1.52mm) 厚的 FR4 PCB 上安装 1in² (6.45cm²)、2oz (0.071mm) 厚的铜焊盘时)。
- (2) 最大 $R_{\theta JC} = 0.8^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。



D004

栅极电荷



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (January 2018) to Revision D (October 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

Changes from Revision B (August 2015) to Revision C (January 2018)	Page
• Added $V_{DS} = 5\text{ V}$ to 图 5-3	4

Changes from Revision A (September 2010) to Revision B (August 2015)	Page
• 向标题添加了器件型号.....	1
• 在 说明 部分进行了详述.....	1
• 添加了 器件和文档支持 部分以及 机械、封装和可订购信息 部分.....	1
• 更新了脉冲电流.....	1
• Updated 图 5-1 to a normalized $R_{\theta JC}$ curve.....	4
• Updated the SOA in 图 5-10	4

Changes from Revision * (August 2009) to Revision A (September 2010)	Page
• 删除了“特性”列表中的环境要点.....	1

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

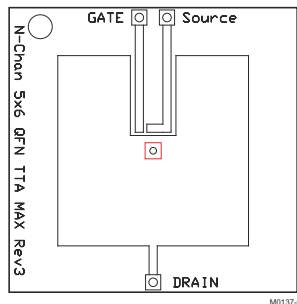
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	25			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = −12 V to 16 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.2	1.5	1.9	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5 V, I _D = 40 A		1.8	2.3	mΩ
		V _{GS} = 10 V, I _D = 40 A		1.3	1.6	
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 40 A		168		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input capacitance	V _{GS} = 0 V, V _{DS} = 12.5 V, f = 1 MHz		3150	4100	pF
C _{OSS}	Output capacitance			2530	3300	pF
C _{RSS}	Reverse transfer capacitance			175	230	pF
R _g	Series gate resistance	V _{DS} = 12.5 V, I _D = 40 A		1.2	2.4	Ω
Q _g	Gate charge total (4.5 V)			21	29	nC
Q _{gd}	Gate charge, gate-to-drain			5.2		nC
Q _{gs}	Gate charge, gate-to-source			8.3		nC
Q _{g(th)}	Gate charge at V _{th}			4.8		nC
Q _{OSS}	Output charge	V _{DS} = 15 V, V _{GS} = 0 V		55		nC
t _{d(on)}	Turnon delay time	V _{DS} = 12.5 V, V _{GS} = 4.5 V, I _D = 40 A R _G = 2 Ω		16.6		ns
t _r	Rise time			30		ns
t _{d(off)}	Turnoff delay time			20		ns
t _f	Fall time			12.7		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _S = 40 A, V _{GS} = 0 V		0.85	1	V
Q _{rr}	Reverse recovery charge	V _{DD} = 15 V, I _F = 40 A, di/dt = 300 A/μs		72		nC
t _{rr}	Reverse recovery time	V _{DD} = 15 V, I _F = 40 A, di/dt = 300 A/μs		45		ns

5.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

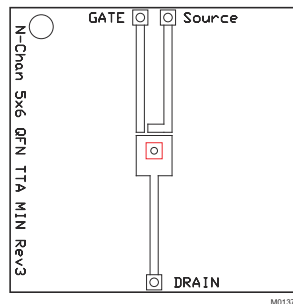
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case ⁽¹⁾			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ^{(1) (2)}			50	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-in (2.54-cm) square, 2-oz (0.071-mm) thick Cu pad on a 1.5-in $\times$ 1.5-in (3.81-cm $\times$ 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 in² (6.45 cm²) of 2-oz (0.071-mm) thick Cu.



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$ when mounted on 1 in² (6.45 cm²) of 2-oz (0.071-mm) thick Cu.

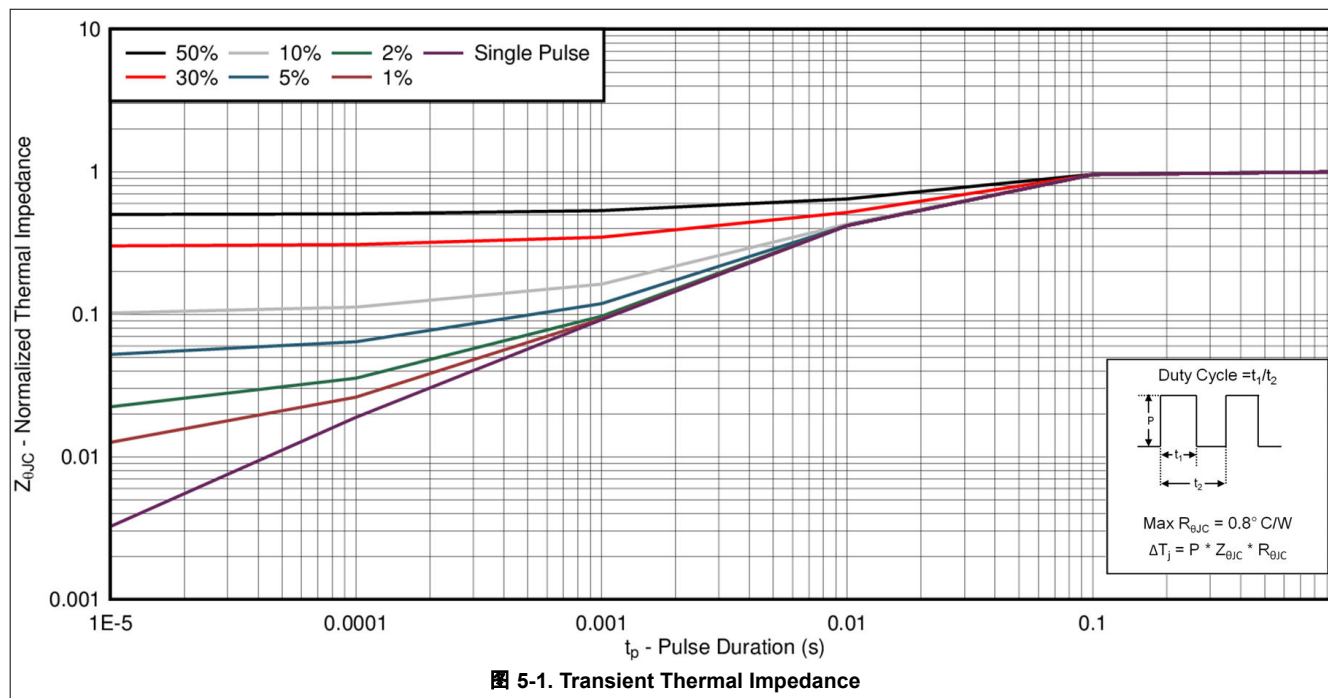


M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$ when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise noted)



5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

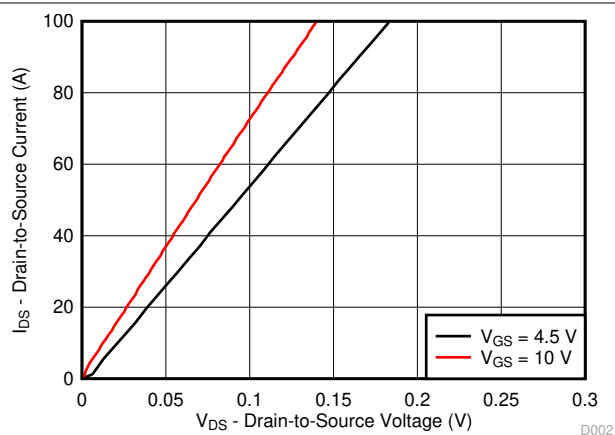


图 5-2. Saturation Characteristics

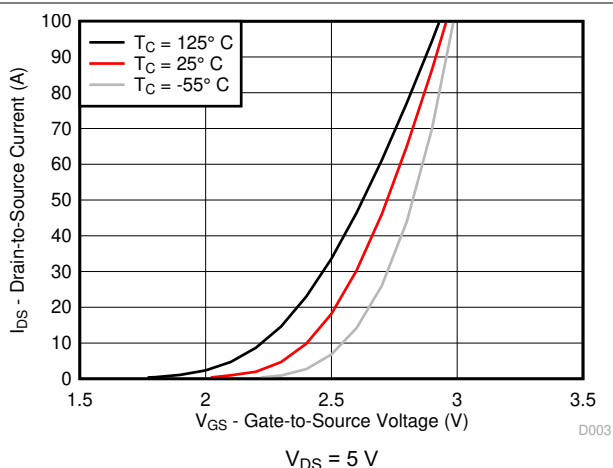


图 5-3. Transfer Characteristics

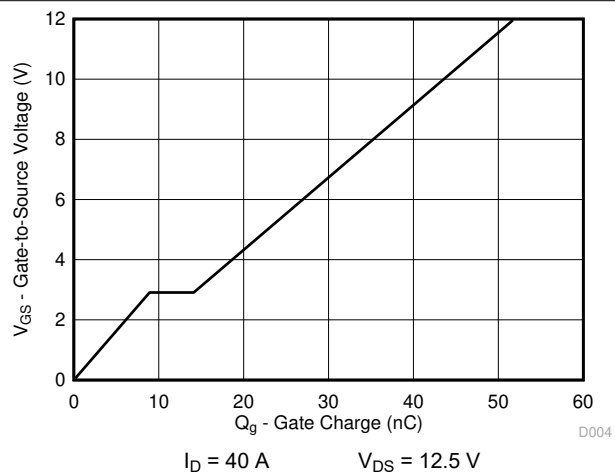


图 5-4. Gate Charge

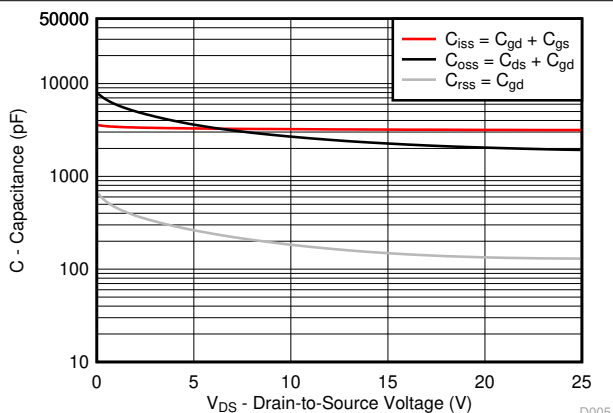


图 5-5. Capacitance

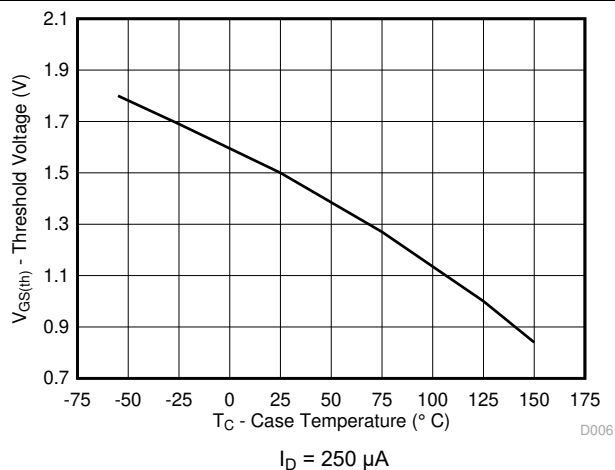


图 5-6. Threshold Voltage vs Temperature

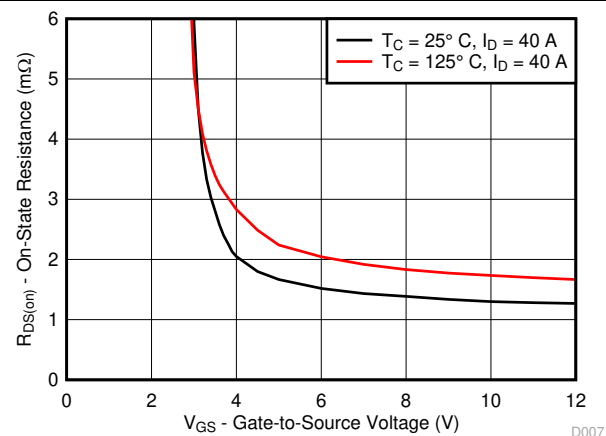


图 5-7. On-Resistance vs Gate Voltage

5.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

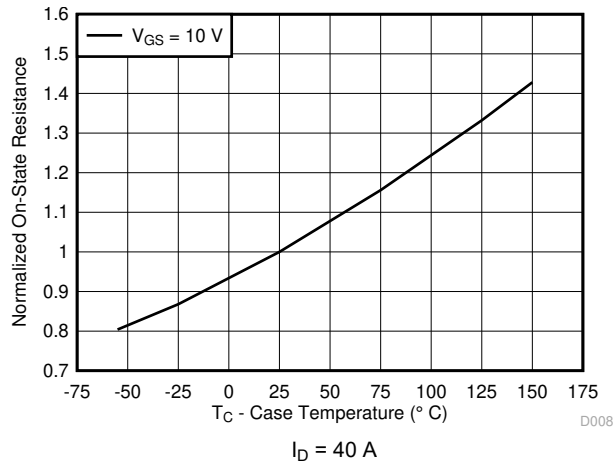


图 5-8. On-Resistance vs Temperature

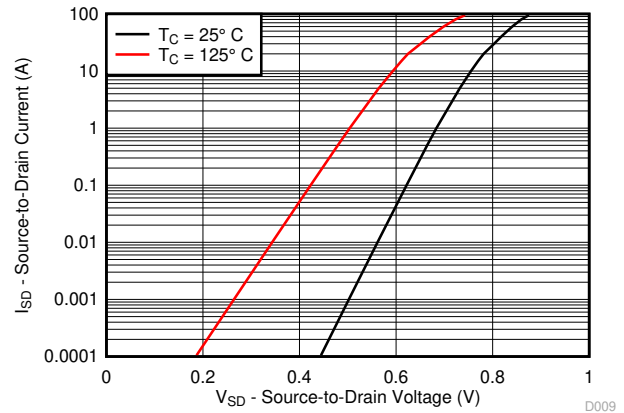


图 5-9. Typical Diode Forward Voltage

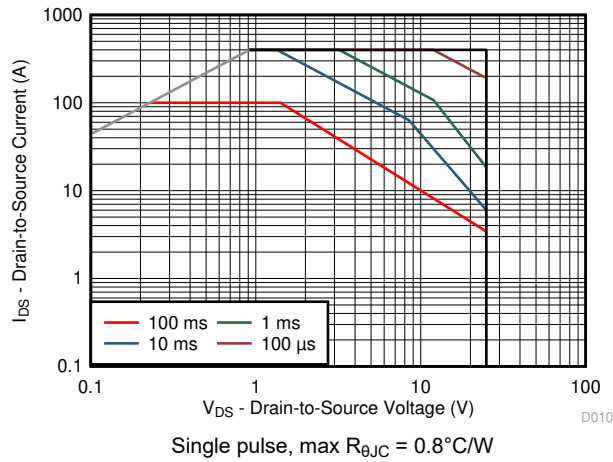


图 5-10. Maximum Safe Operating Area

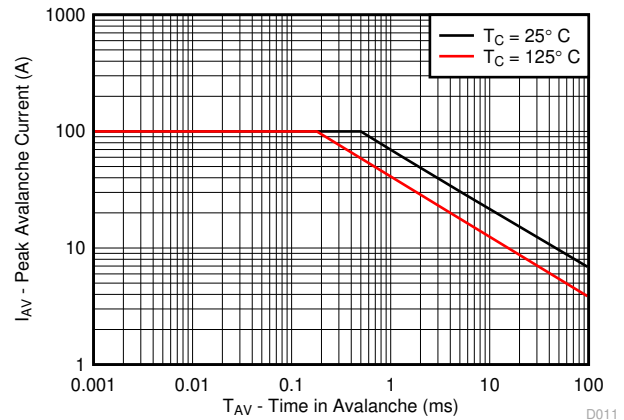


图 5-11. Single-Pulse Unclamped Inductive Switching

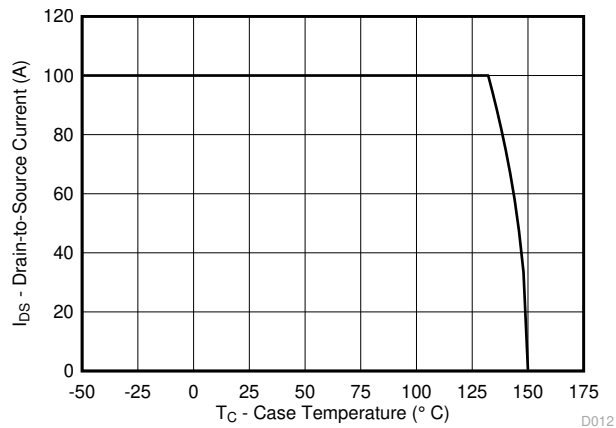


图 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

6.3 Trademarks

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6.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.5 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16401Q5	Active	Production	VSON-CLIP (DQH) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401
CSD16401Q5.B	Active	Production	VSON-CLIP (DQH) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401
CSD16401Q5T	Active	Production	VSON-CLIP (DQH) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401
CSD16401Q5T.B	Active	Production	VSON-CLIP (DQH) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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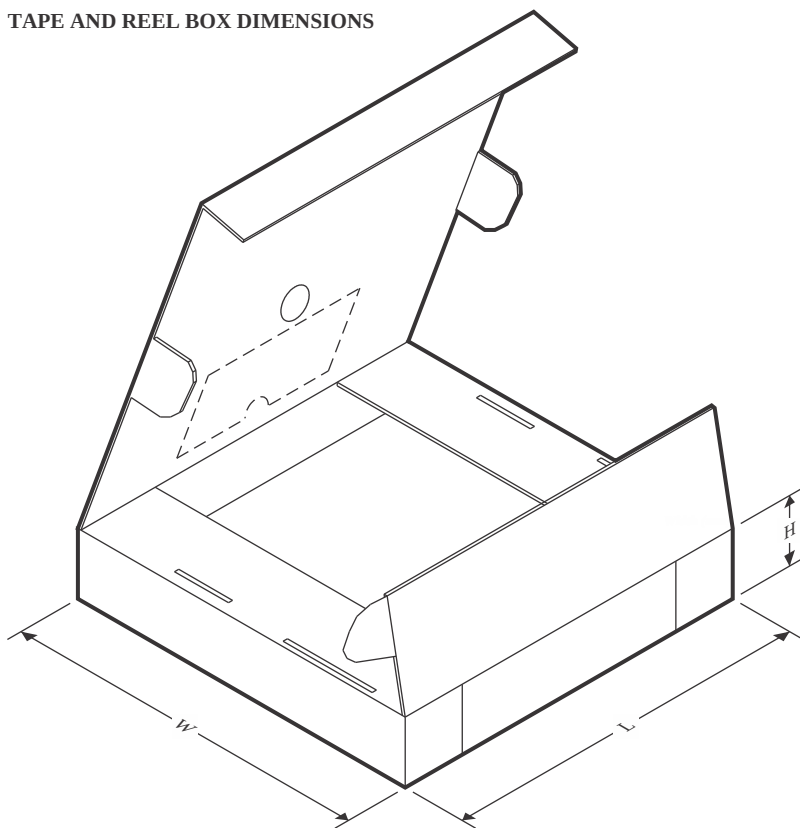
TAPE AND REEL INFORMATION



*All dimensions are nominal

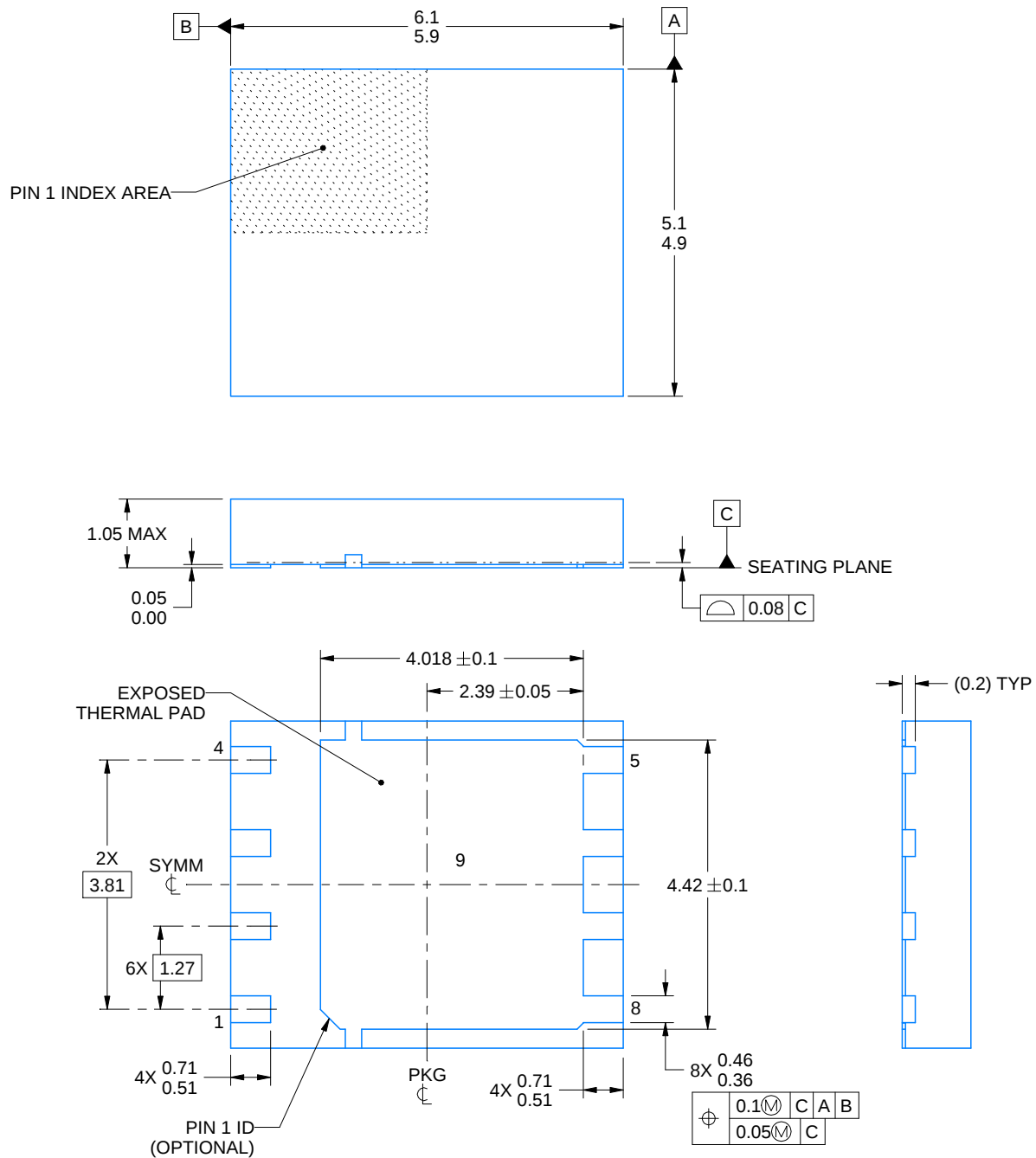
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16401Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16401Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0



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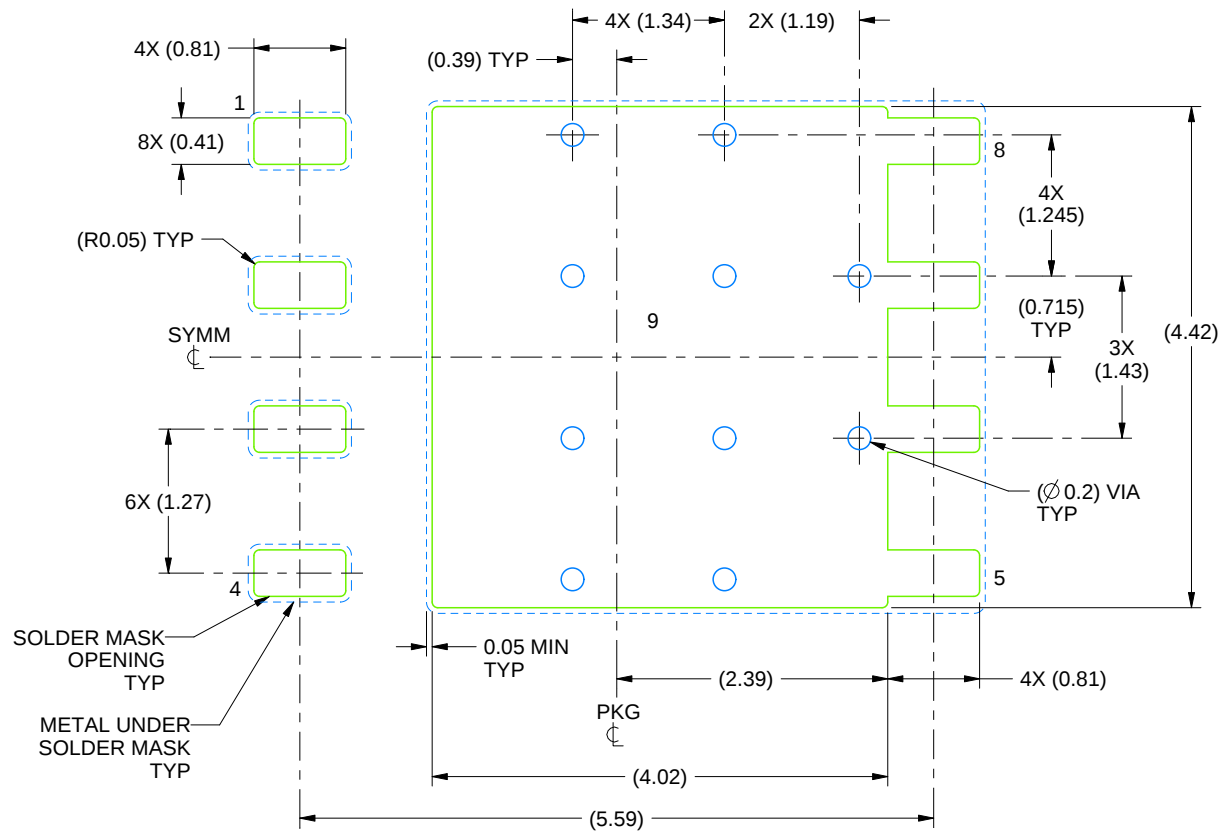
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

DQH0008A

VSON-CLIP - 1.05 mm max height

8X (0.81)

1

8X (0.41)

SYMM

6X (1.27)

4

(R0.05) TYP

9

(0.28)

(1.34) TYP

SOLDER MASK EDGE TYP

8

(1.43) TYP

9X (1.23)

5

9X (1.14)

PKG

METAL TYP

(5.59)

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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最后更新日期：2025 年 10 月