

N 沟道 NexFET™ 功率 MOSFET

1 特性

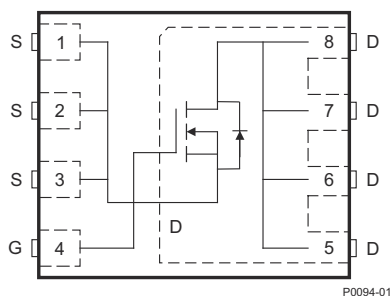
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- SON 5mm × 6mm 塑料封装

2 应用

- 网络、电信和计算系统中的负载点同步降压转换器
- 针对控制 FET 应用进行了优化

3 说明

NexFET™ 功率 MOSFET 旨在更大幅度地降低功率转换应用中的损耗。



顶视图

产品概要

V_{DS}	漏源极电压	25	V
Q_g	栅极电荷, 总数(4.5V)	6.7	nC
Q_{gd}	栅极电荷 (栅漏极)	1.9	nC
$r_{DS(接通)}$	漏源导通电阻	$V_{GS} = 4.5V$	5.4
		$V_{GS} = 10V$	3.6
$V_{GS(th)}$	阈值电压	1.8	V

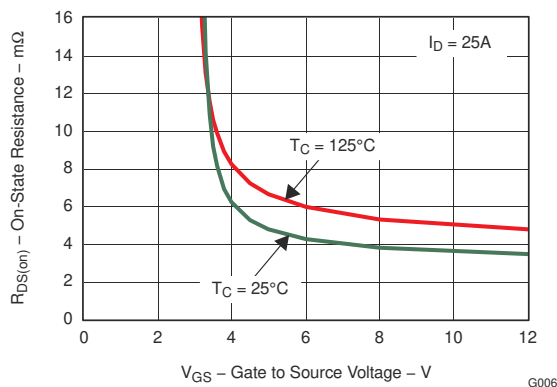
订购信息

器件	封装	介质	数量	出货
CSD16408Q5	SON 5mm × 6mm 塑料封装	13 英寸 (33cm) 卷带	2500	卷带

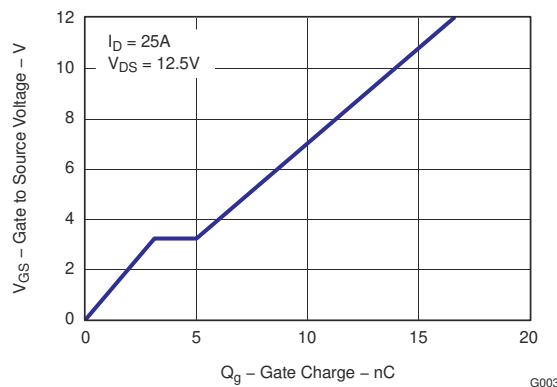
绝对最大额定值

$T_A = 25^\circ\text{C}$ 时测得, 除非另外注明		值	单位
V_{DS}	漏源极电压	25	V
V_{GS}	栅源电压	-12 至 16	V
I_D	持续漏极电流, $T_C = 25^\circ\text{C}$	113	A
	持续漏极电流 ⁽¹⁾	22	A
I_{DM}	脉冲漏极电流, $T_A = 25^\circ\text{C}$ ⁽²⁾	141	A
P_D	功率耗散 ⁽¹⁾	3.1	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲 $I_D = 23A, L = 0.1mH, R_G = 25\Omega$	126	mJ

- (1) 典型 $R_{\theta JA} = 41^\circ\text{C/W}$ (在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm²)、2oz、0.071mm 厚的铜焊盘时)。
- (2) 脉冲持续时间 $\leq 300\mu\text{s}$, 占空比 $\leq 2\%$



$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



Table of Contents

1 特性	1	5 Electrical Characteristics	3
2 应用	1	6 Thermal Characteristics	3
3 说明	1	7 Typical MOSFET Characteristics	4
4 Revision History	2	8 Mechanical, Packaging, and Orderable Information	7

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (September 2010) to Revision B (October 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

Changes from Revision * (October 2009) to Revision A (September 2010)	Page
• 删除了特性列表中的环境要点.....	1

5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise stated

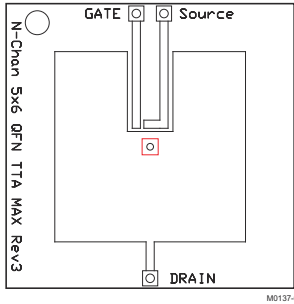
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
I_{DSS}	Drain-to-source leakage	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage	$V_{DS} = 0\text{ V}, V_{GS} = -12\text{ V to }16\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.4	1.8	2.1	V
$r_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		5.4	6.8	m Ω
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		3.6	4.5	m Ω
g_{fs}	Transconductance	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		60		S
Dynamic Characteristics						
C_{ISS}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 12.5\text{ V}, f = 1\text{ MHz}$		990	1300	pF
C_{OSS}	Output capacitance			760	1000	pF
C_{RSS}	Reverse transfer capacitance			75	100	pF
R_g	Series gate resistance			0.8	1.6	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 12.5\text{ V}, I_D = 25\text{ A}$		6.7	8.9	nC
Q_{gd}	Gate charge, gate-to-drain			1.9		nC
Q_{gs}	Gate charge, gate-to-source			3.1		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.8		nC
Q_{OSS}	Output charge	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}$		15.7		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}, R_G = 2\ \Omega$		11.3		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turnoff delay time			11		ns
t_f	Fall time			10.8		ns
Diode Characteristics						
V_{SD}	Diode forward voltage	$I_S = 25\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse recovery charge	$V_{DD} = 13\text{ V}, I_F = 2.5\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		17		nC
t_{rr}	Reverse recovery time	$V_{DD} = 13\text{ V}, I_F = 25\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		21		ns

6 Thermal Characteristics

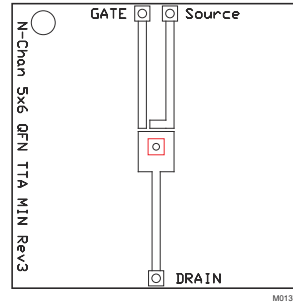
 $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			51	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



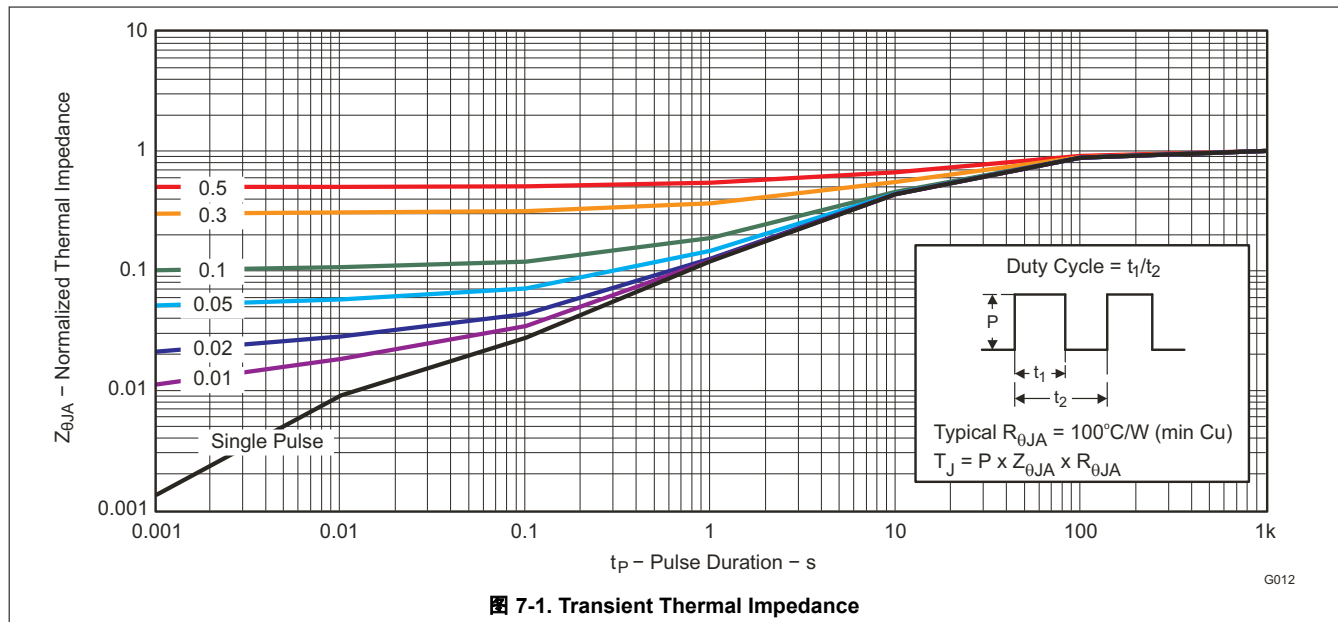
Max $R_{\theta JA}$ = 51°C/W
when mounted on 1 inch²
(6.45 cm²) of 2-oz. (0.071-
mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when
mounted on minimum pad
area of 2-oz. (0.071-mm
thick) Cu.

7 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated



7 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated

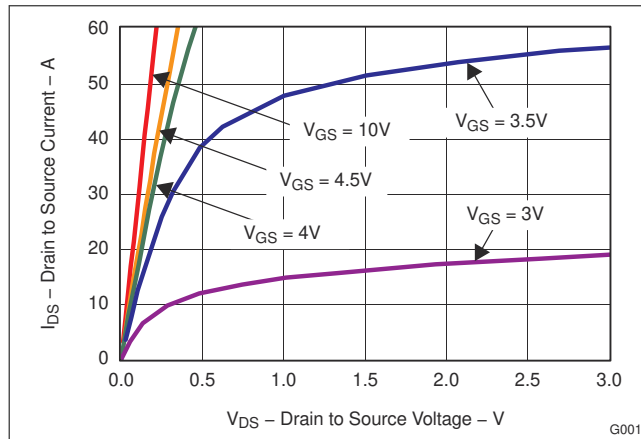


图 7-2. Saturation Characteristics

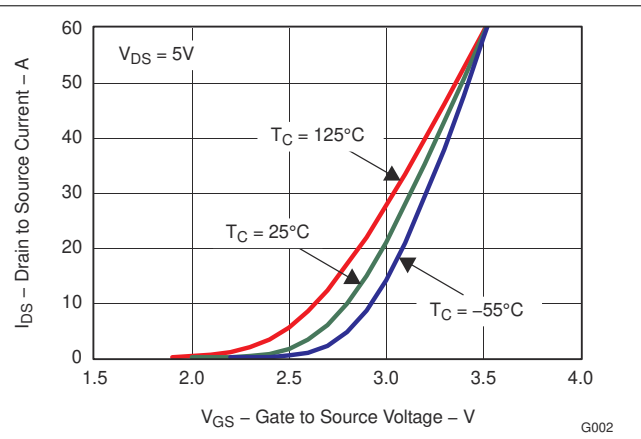


图 7-3. Transfer Characteristics

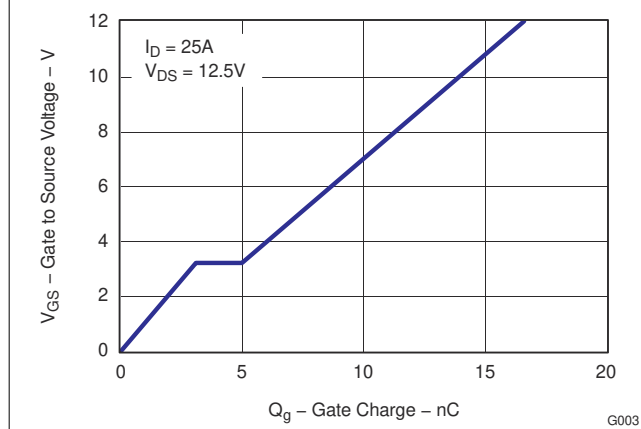


图 7-4. Gate Charge

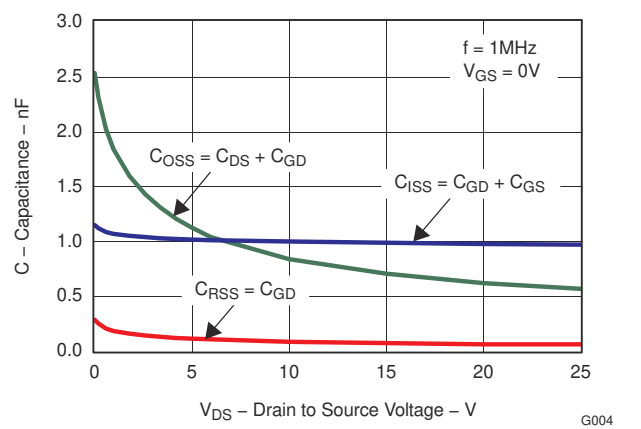


图 7-5. Capacitance

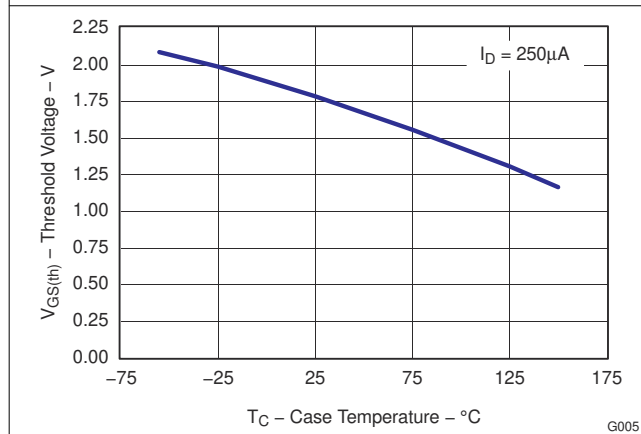


图 7-6. Threshold Voltage vs. Temperature

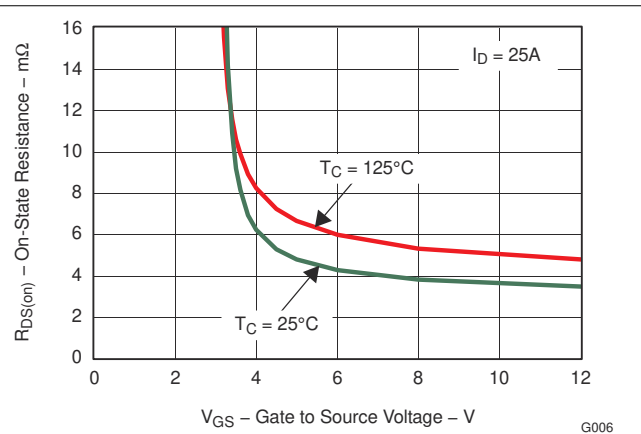


图 7-7. On-State Resistance vs. Gate-to-Source Voltage

7 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise stated

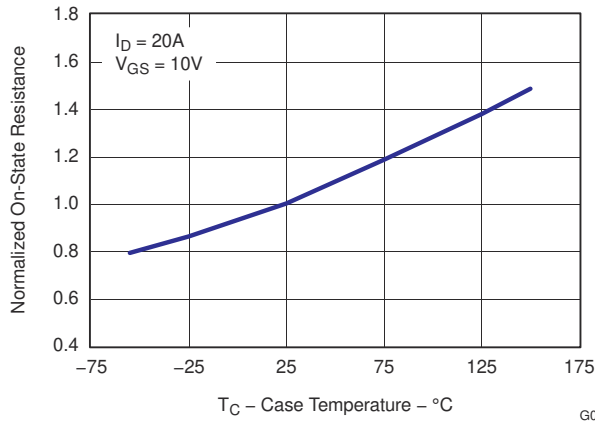


图 7-8. Normalized On-State Resistance vs. Temperature

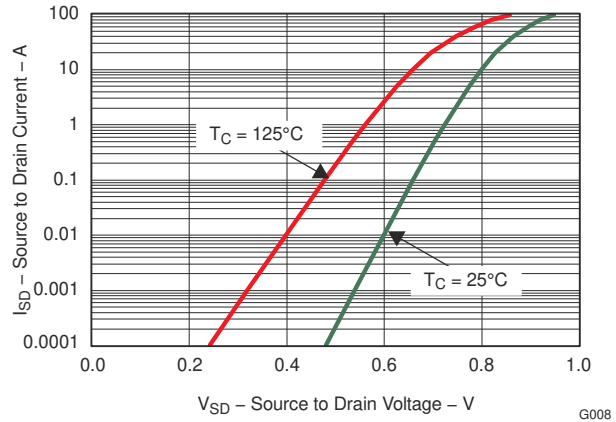


图 7-9. Typical Diode Forward Voltage

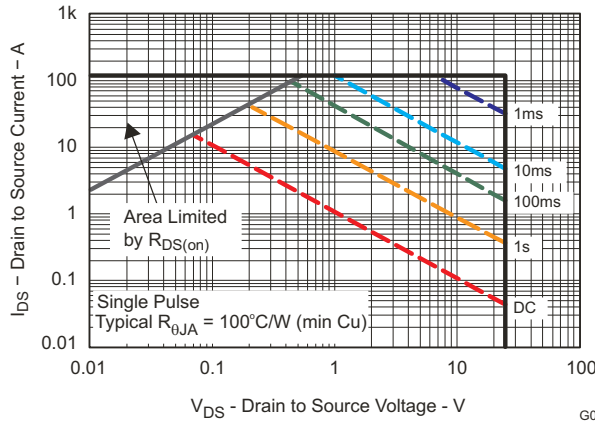


图 7-10. Maximum Safe Operating Area

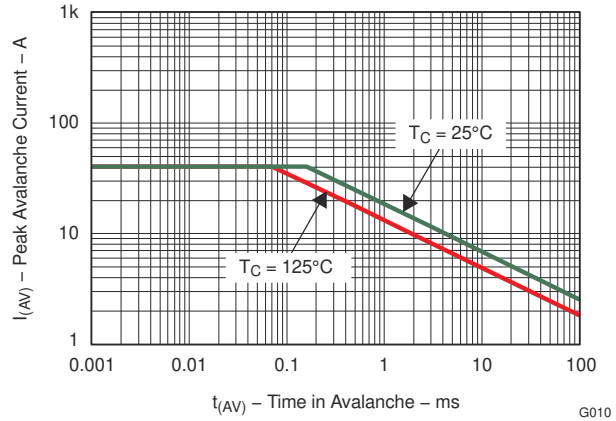


图 7-11. Single-Pulse Unclamped Inductive Switching

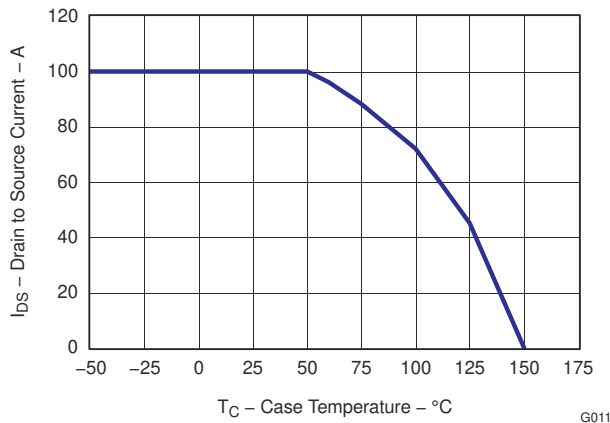


图 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16408Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16408	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司