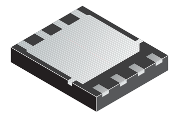


N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管(MOSFET)

查询样品: **CSD16415Q5**

特性

- 超低栅极电荷**(Qg)**和栅漏电荷**(Qgd)**
- 极低接通电阻
- 低热阻性
- 额定雪崩能量
- 无铅端子电镀
- 符合 **RoHS** 标准
- 无卤素

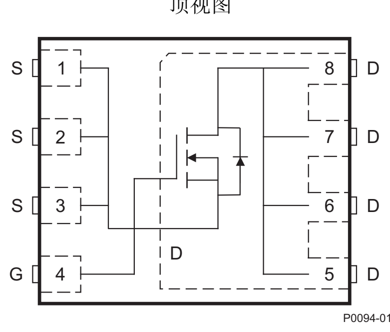
应用范围

- 负载点同步降压转换器用于网络，电信和计算系统
- 为同步场效应晶体管**(FET)**应用进行了优化

说明

此 NexFET™ 功率MOSFET已被设计成在功率转换应用中大大降低功率损失。

顶视图



产品概述

V_{DS}	漏源极电压	25		V
Q_g	栅极电荷，总数(4.5V)	21		nC
Q_{gd}	栅极电荷，栅漏	5.2		nC
$r_{DS(接通)}$	漏源极接通电阻	V_{GS} = 4.5 V	1.5	mΩ
		V_{GS} = 10 V	0.99	mΩ
$V_{GS(th)}$	阀值电压	1.5		V

订购信息

器件	封装	介质	数量	出货
CSD16415Q5	无引线小外形尺寸(SON)5mm x 6mm塑料封装	13英寸(33cm)卷带	2500	卷带

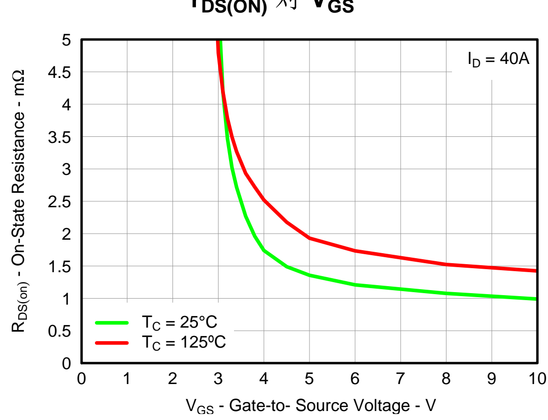
最大绝对额定值

除非另外说明，否则T_A = 25°C		数值	单位
V_{DS}	漏源极电压	25	V
V_{GS}	栅源极电压	+16/-12	V
I_D	持续漏极电流，T_C = 25°C	100	A
	持续漏极电流[(1)]	38	A
I_{DM}	脉冲漏极电流，T_A = 25°C[(2)]	200	A
P_D	功率耗散[(1)]	3.2	W
T_J，T_{STG}	运行结温和存储温度范围	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 100A，L = 0.1mH，R_G = 25 Ω	500	mJ

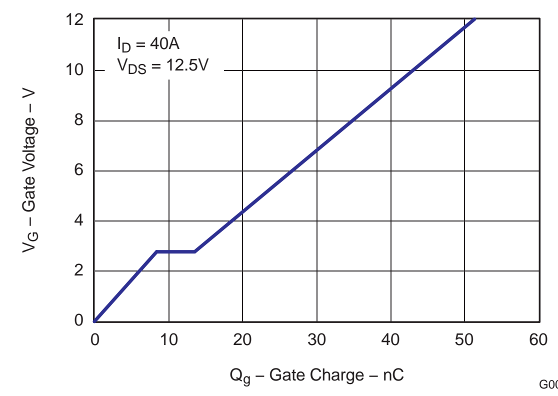
(1) $R_{\theta JA}$ = 40°C/W，此条件是在1in^2 (6.45cm^2) Cu [2 oz.（厚度为0.071mm）] 的0.060英寸厚度为 (1.52mm) FR4 印刷电路板(PCB)上。

(2) 脉冲持续时间≤300 μs，占空比 ≤2%

$r_{DS(ON)}$ 对 V_{GS}



栅极电荷



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: SLPS259

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V to 16 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.2	1.5	1.9	V
$r_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 40 A		1.5	1.8	mΩ
		V_{GS} = 10 V, I_D = 40 A		0.99	1.15	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 40 A		168		S
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		3150	4100	pF
C_{OSS}	Output capacitance			2530	3300	pF
C_{RSS}	Reverse transfer capacitance			175	230	pF
R_g	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, ID = 40 A		21	29	nC
Q_{gd}	Gate charge, gate-to-drain			5.2		nC
Q_{gs}	Gate charge, gate-to-source			8.3		nC
Qg(th)	Gate charge at Vth			4.8		nC
Q_{OSS}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		55		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 40 A R_G = 2 Ω		16.6		ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			12.7		ns
Diode Characteristics						
V_{SD}	Diode forward voltage	I_S = 40 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/μs		72		nC
t_{rr}	Reverse recovery time	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/μs		45		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case(1)			1.1	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch (2.54-cm) square, 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.060-inch (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.

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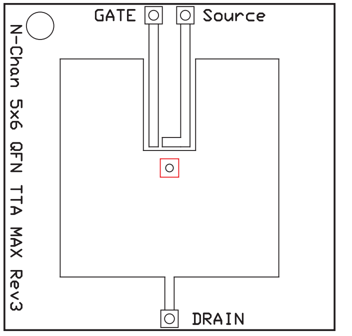
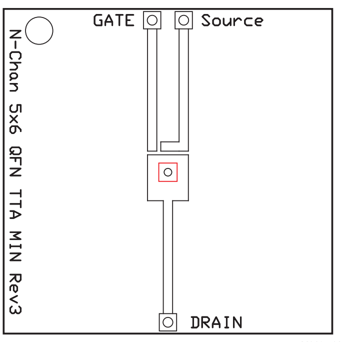


Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 121°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

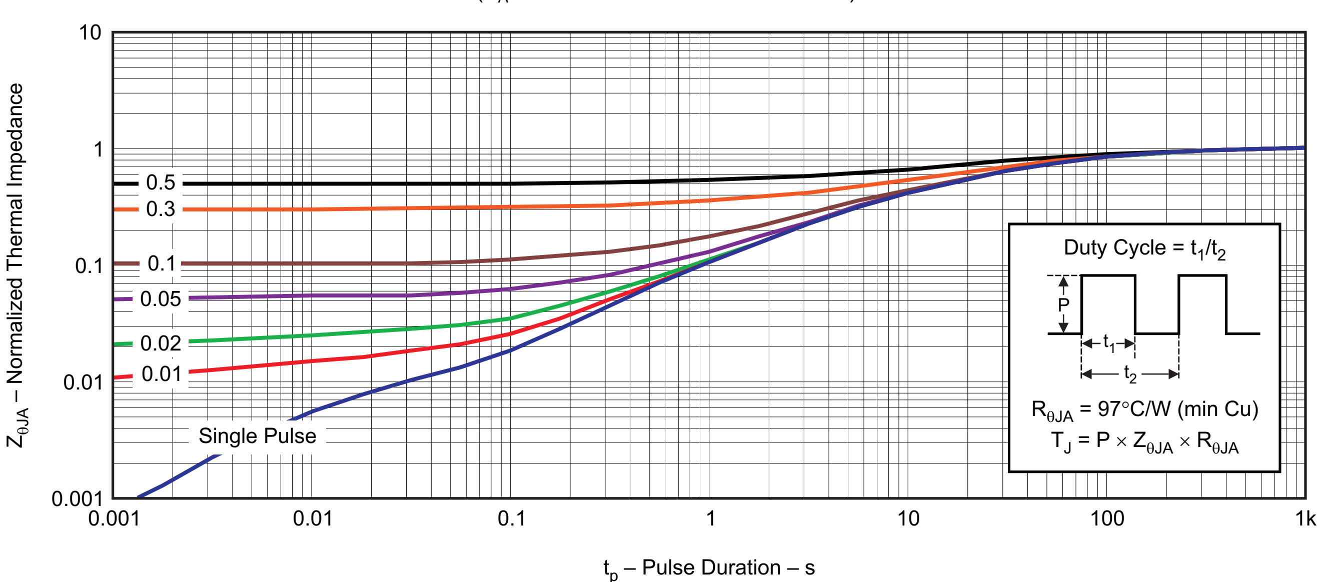


Figure 1. Transient Thermal Impedance

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

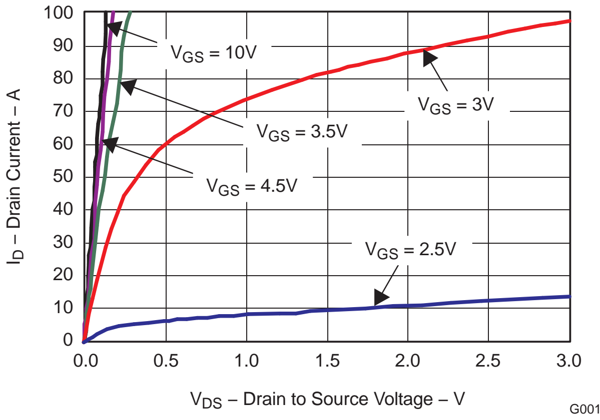

Figure 2. Saturation Characteristics

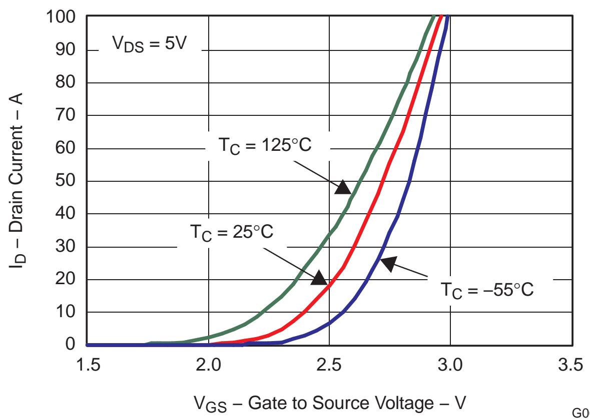

Figure 3. Transfer Characteristics

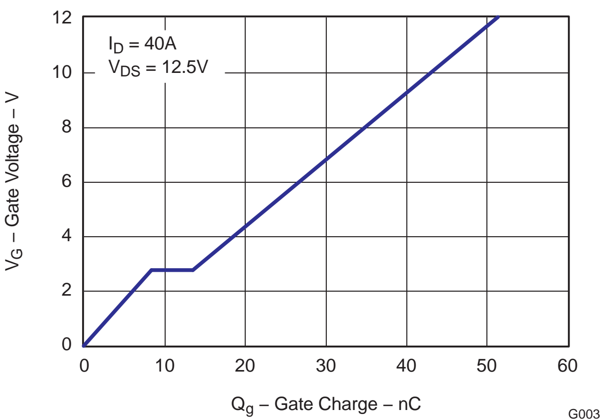

Figure 4. Gate Charge

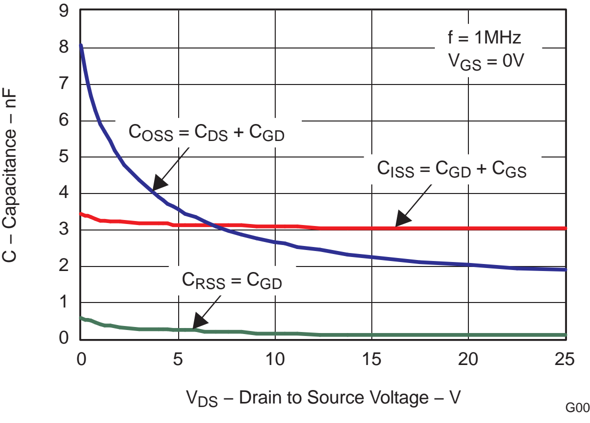

Figure 5. Capacitance

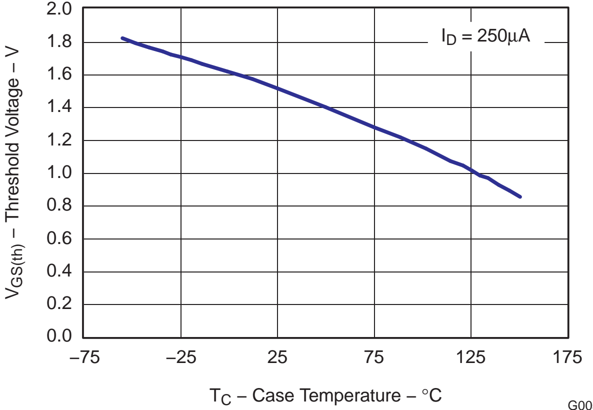

Figure 6. Threshold Voltage vs. Temperature

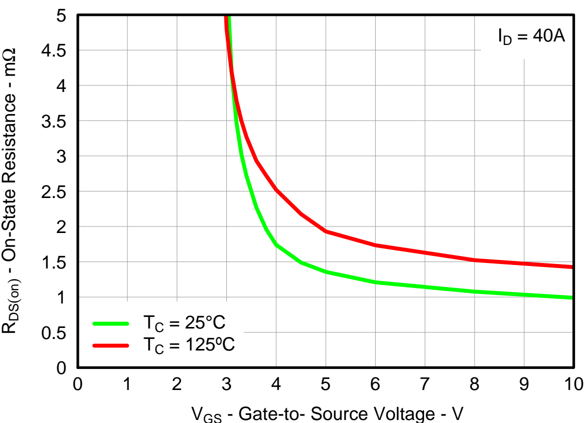

Figure 7. On-Resistance vs. Gate Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

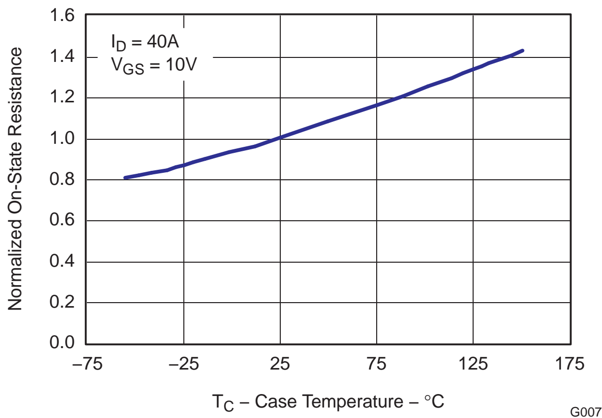

Figure 8. On-Resistance vs. Temperature

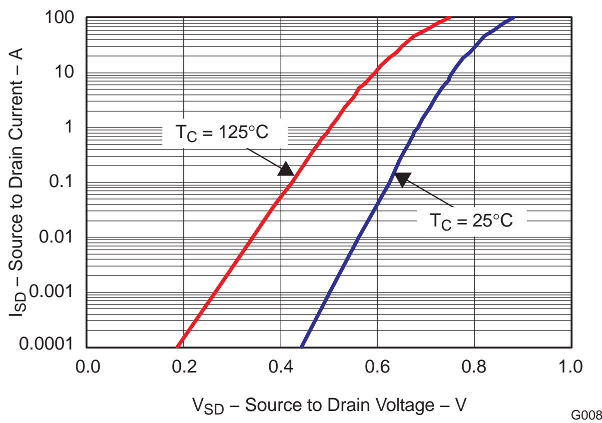

Figure 9. Typical Diode Forward Voltage

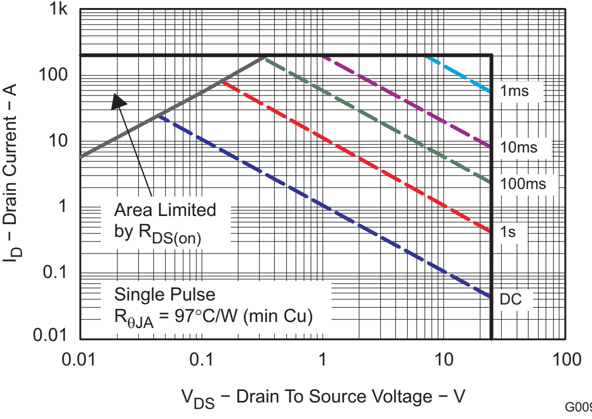

Figure 10. Maximum Safe Operating Area

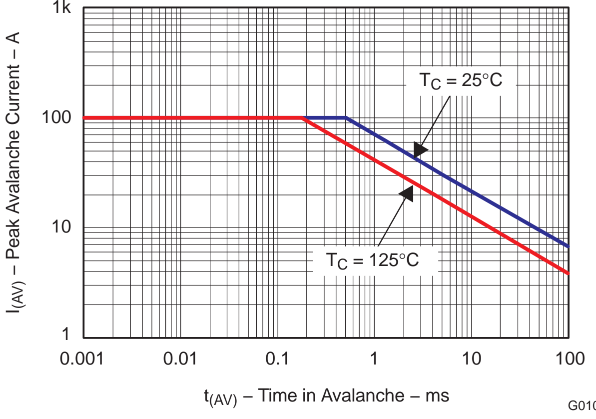

Figure 11. Single-Pulse Unclamped Inductive Switching

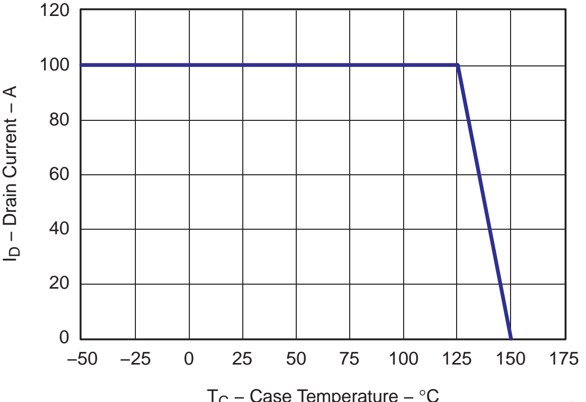

Figure 12. Maximum Drain Current vs. Temperature

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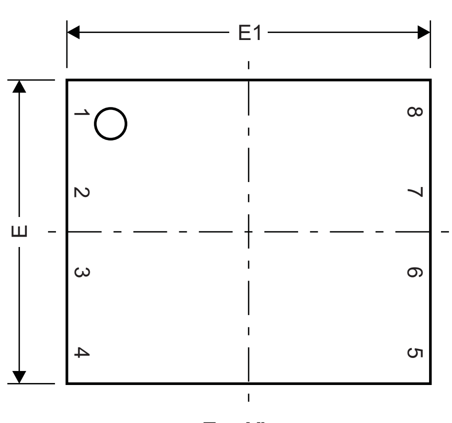
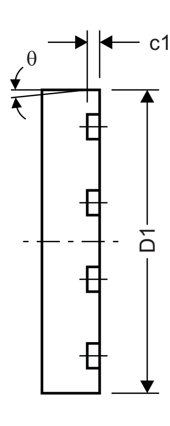
MECHANICAL DATA

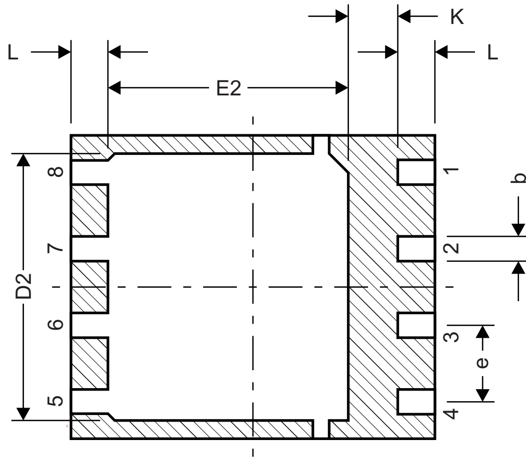
Q5 Package Dimensions



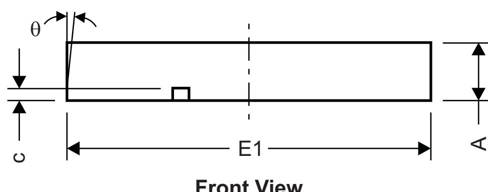
Top View



Side View



Bottom View



Front View

M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00			

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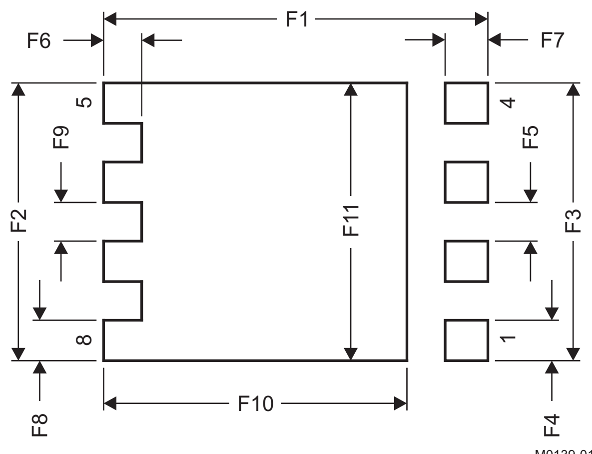
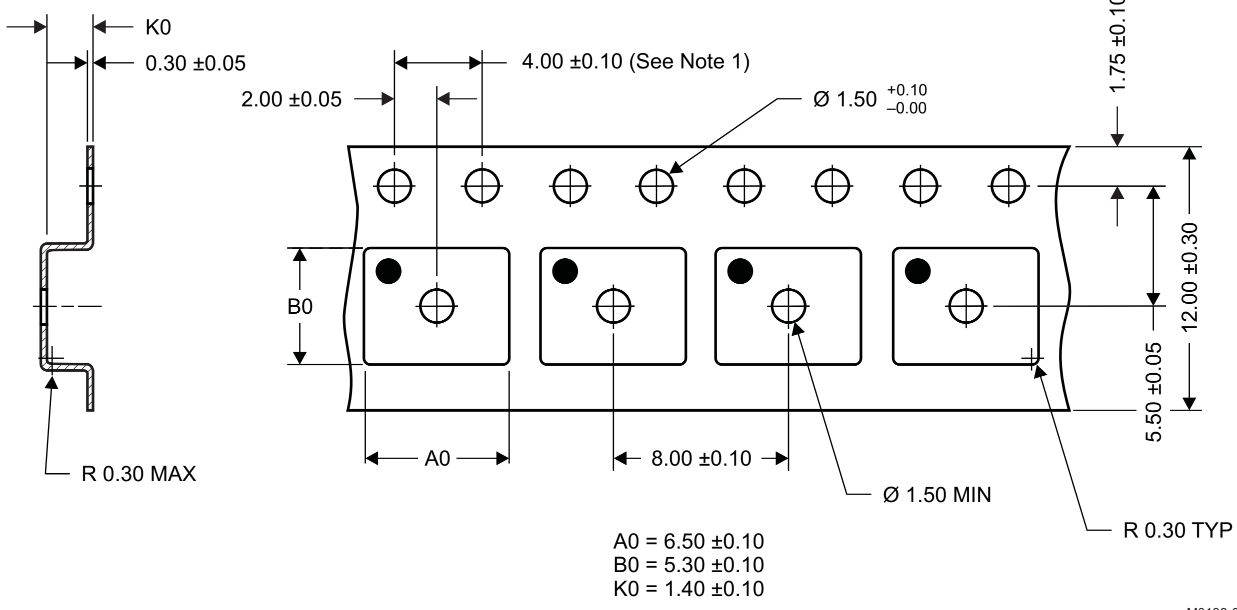
Figure 13. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16415Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16415	Samples
CSD16415Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16415	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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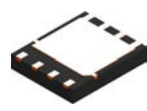

PACKAGE OUTLINE

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

B
6.1
5.9
A
PIN 1 INDEX AREA
5.1
4.9

1.05 MAX
C
SEATING PLANE
0.05
0.00
0.08 C

4.018 ±0.1
2.39 ±0.05
EXPOSED
THERMAL PAD
(0.2) TYP
4
5
2X
3.81
SYMM
9
4.42 ±0.1
6X 1.27
8
1
4X 0.71
0.51
PKG
4X 0.71
0.51
8X 0.46
0.36
0.1Ⓜ C A B
0.05Ⓜ C
PIN 1 ID
(OPTIONAL)

4223292/A 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

4X (0.81)
4X (1.34)
2X (1.19)
(0.39) TYP
1
8X (0.41)
8
4X (1.245)
(R0.05) TYP
(0.715) TYP
9
SYMM
3X (1.43)
(4.42)
6X (1.27)
(∅0.2) VIA TYP
4
5
SOLDER MASK OPENING TYP
0.05 MIN TYP
(2.39)
4X (0.81)
PKG
METAL UNDER SOLDER MASK TYP
(4.02)
(5.59)

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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