

CSD17581Q3A 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 低 Q_g 和 Q_{gd}
- 低 $R_{DS(on)}$
- 低热阻抗
- 雪崩级
- 无铅
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

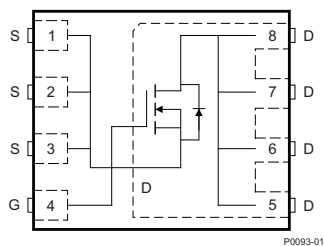
2 应用范围

- 用于网络互联、电信和计算系统的负载点同步降压转换器
- 电机控制应用
- 针对控制场效应晶体管 (FET) 应用进行了优化

3 说明

这款采用 3.3mm × 3.3mm SON 封装的 30V、3.2mΩ、NexFET™ 功率 MOSFET 被设计成在功率转换应用中大大降低损耗。

俯视图



P0093-01

产品概要

$T_A=25^\circ\text{C}$		典型值		单位
V_{DS}	漏源极电压	30		V
Q_g	栅极电荷总量 (4.5V)	20		nC
Q_{gd}	栅极电荷 (栅极到漏极)	4		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	3.9	mΩ
		$V_{GS} = 10\text{V}$	3.2	mΩ
$V_{GS(th)}$	阈值电压	1.3		V

器件信息(1)

器件	包装介质	数量	封装	运输
CSD17581Q3A	13 英寸卷带	2500	小外形尺寸无引线 (SON) 3.30mm × 3.30mm 塑料封装	卷带式
CSD17581Q3AT	7 英寸卷带	250		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

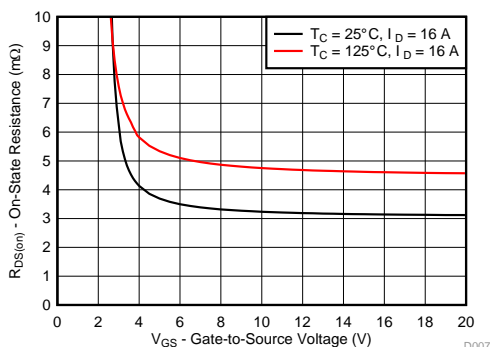
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源极电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流 (受封装限制)	60	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	101	
	持续漏极电流(1)	21	
I_{DM}	脉冲漏极电流(2)	154	A
P_D	功率耗散(1)	2.8	W
	功率耗散, $T_C = 25^\circ\text{C}$	63	
T_J, T_{stg}	工作结温, 储存温度	-55 至 150	°C
E_{AS}	雪崩能量, 单一脉冲 $I_D = 39\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	76	mJ

(1) $R_{\theta JA} = 45^\circ\text{C}/\text{W}$ 。这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸², 2 盎司铜焊盘上测得的典型值。

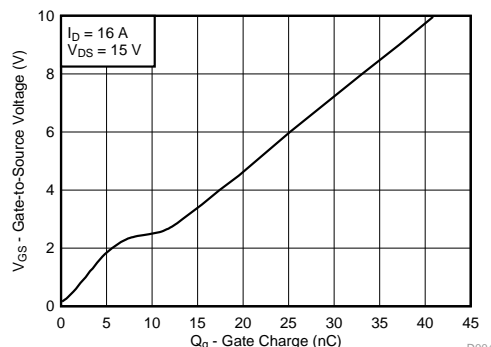
(2) 最大 $R_{\theta JC} = 2^\circ\text{C}/\text{W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。

$R_{DS(on)}$ 与 V_{GS} 间的关系



D007

栅极电荷



D004



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4 修订历史记录

日期	修订版本	注释
2016 年 10 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	1.3	1.7	V
$R_{DS(on)}$	Drain-to-source On-resistance	$V_{GS} = 4.5\text{ V}, I_D = 16\text{ A}$		3.9	4.7	m Ω
		$V_{GS} = 10\text{ V}, I_D = 16\text{ A}$		3.2	3.8	
g_{fs}	Transconductance	$V_{DS} = 3\text{ V}, I_D = 16\text{ A}$		78		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		2800	3640	pF
C_{oss}	Output capacitance			342	445	pF
C_{rss}	Reverse transfer capacitance			150	195	pF
R_G	Series gate resistance			1.8	3.6	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 15\text{ V}, I_D = 16\text{ A}$		20	25	nC
Q_g	Gate charge total (10 V)			41	54	nC
Q_{gd}	Gate charge gate-to-drain			4.0		nC
Q_{gs}	Gate charge gate-to-source			6.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			3.6		nC
Q_{oss}	Output charge		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		11.7	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 16\text{ A}, R_G = 0\ \Omega$		12		ns
t_r	Rise time			23		ns
$t_{d(off)}$	Turnoff delay time			23		ns
t_f	Fall time			10		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 16\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 15\text{ V}, I_F = 16\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		10.2		nC
t_{rr}	Reverse recovery time			9.8		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

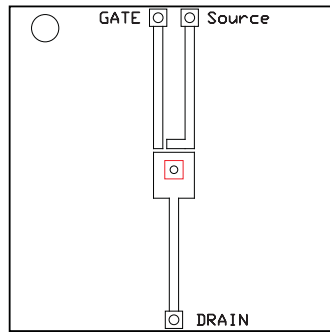
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			55	

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.



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Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on 1-in²
(6.45-cm²) of
2-oz (0.071-mm) thick
Cu.

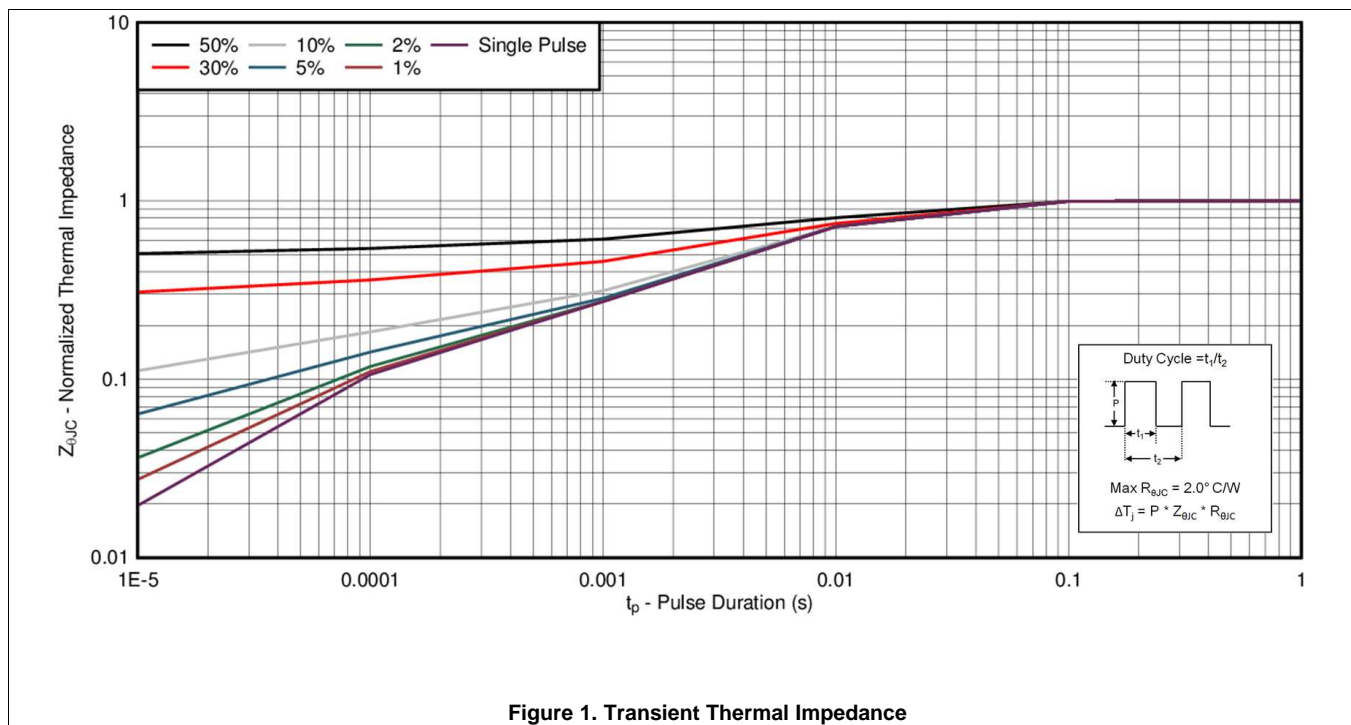


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Max $R_{\theta JA} = 160^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz (0.071-mm) thick
Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

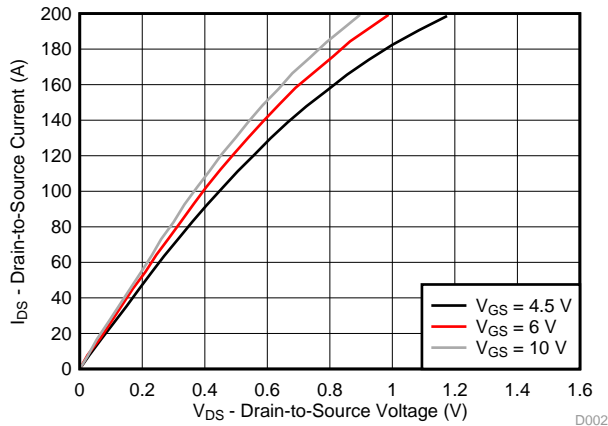


Figure 2. Saturation Characteristics

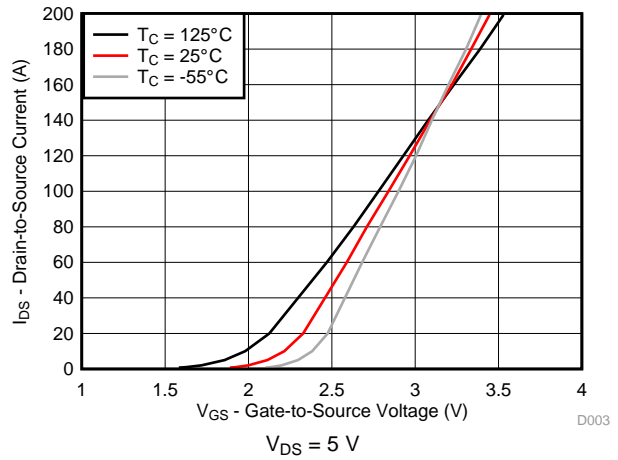


Figure 3. Transfer Characteristics

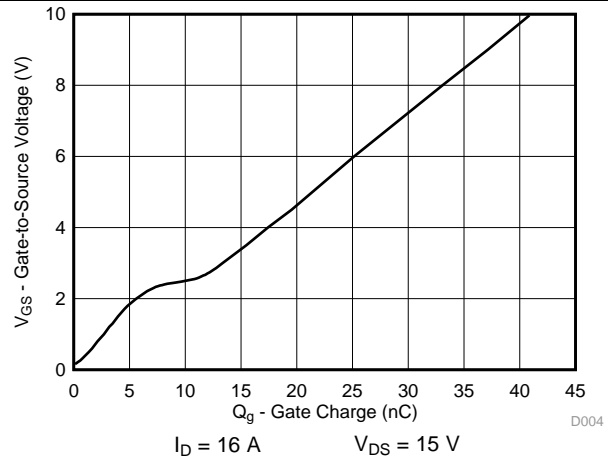


Figure 4. Gate Charge

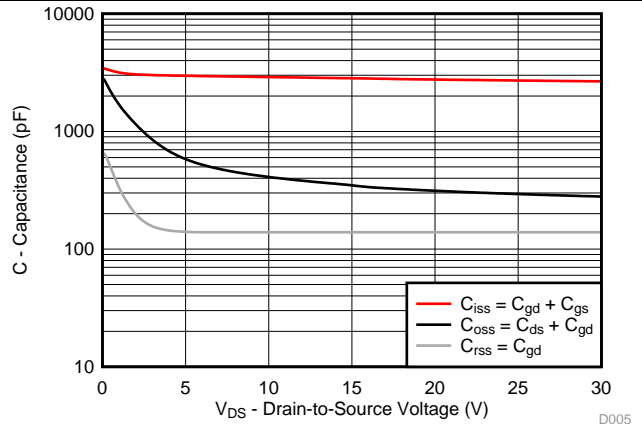


Figure 5. Capacitance

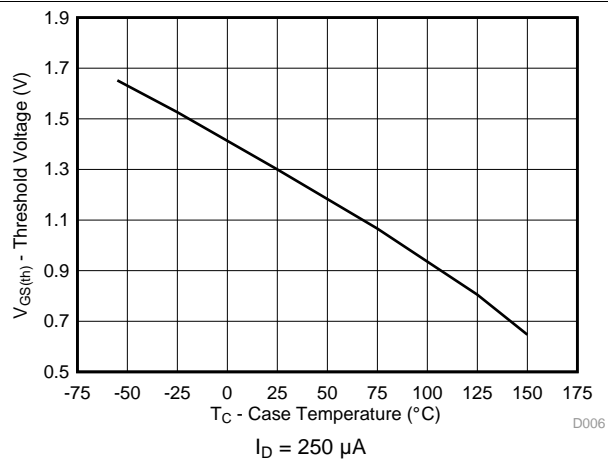


Figure 6. Threshold Voltage vs Temperature

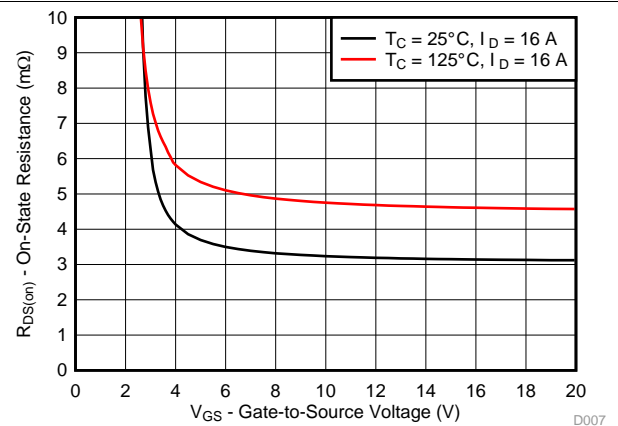


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

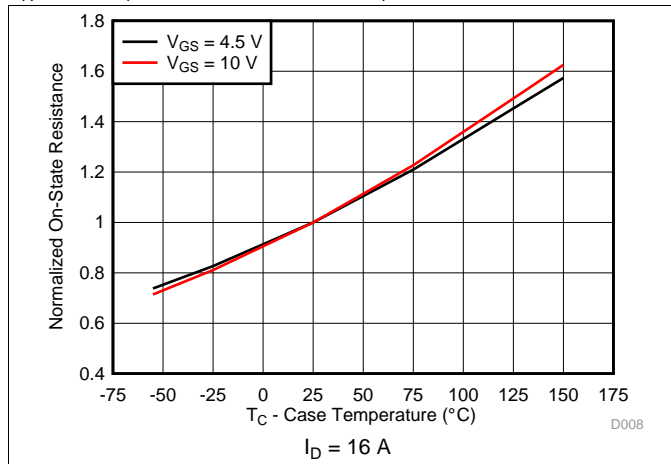


Figure 8. Normalized On-State Resistance vs Temperature

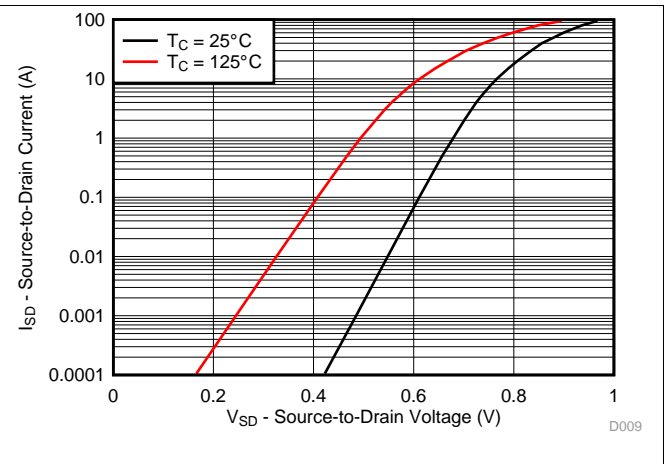


Figure 9. Typical Diode Forward Voltage

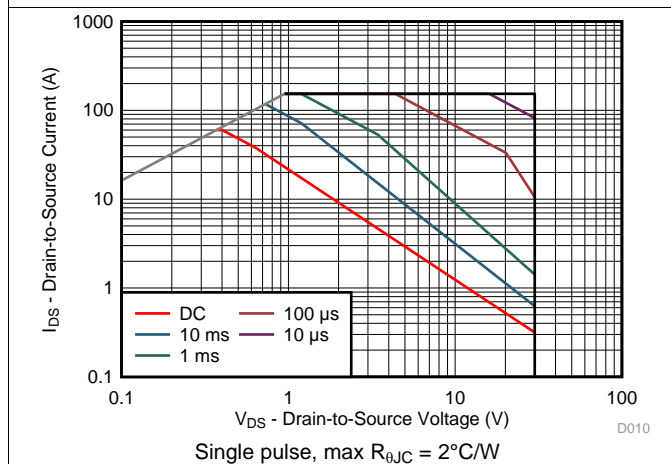


Figure 10. Maximum Safe Operating Area (SOA)

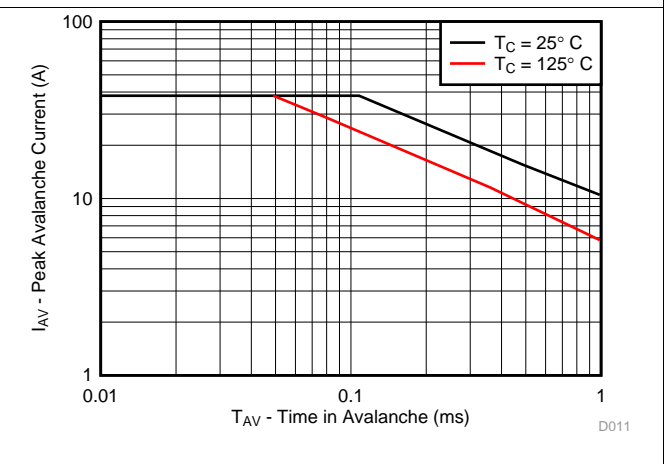


Figure 11. Single Pulse Unclamped Inductive Switching

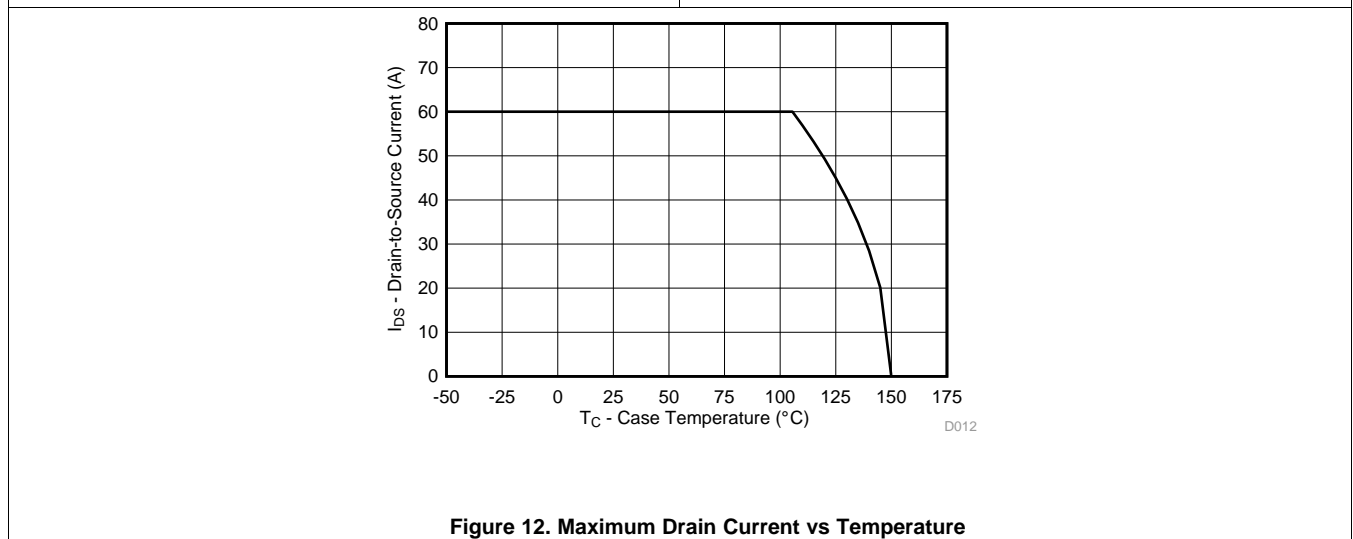


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

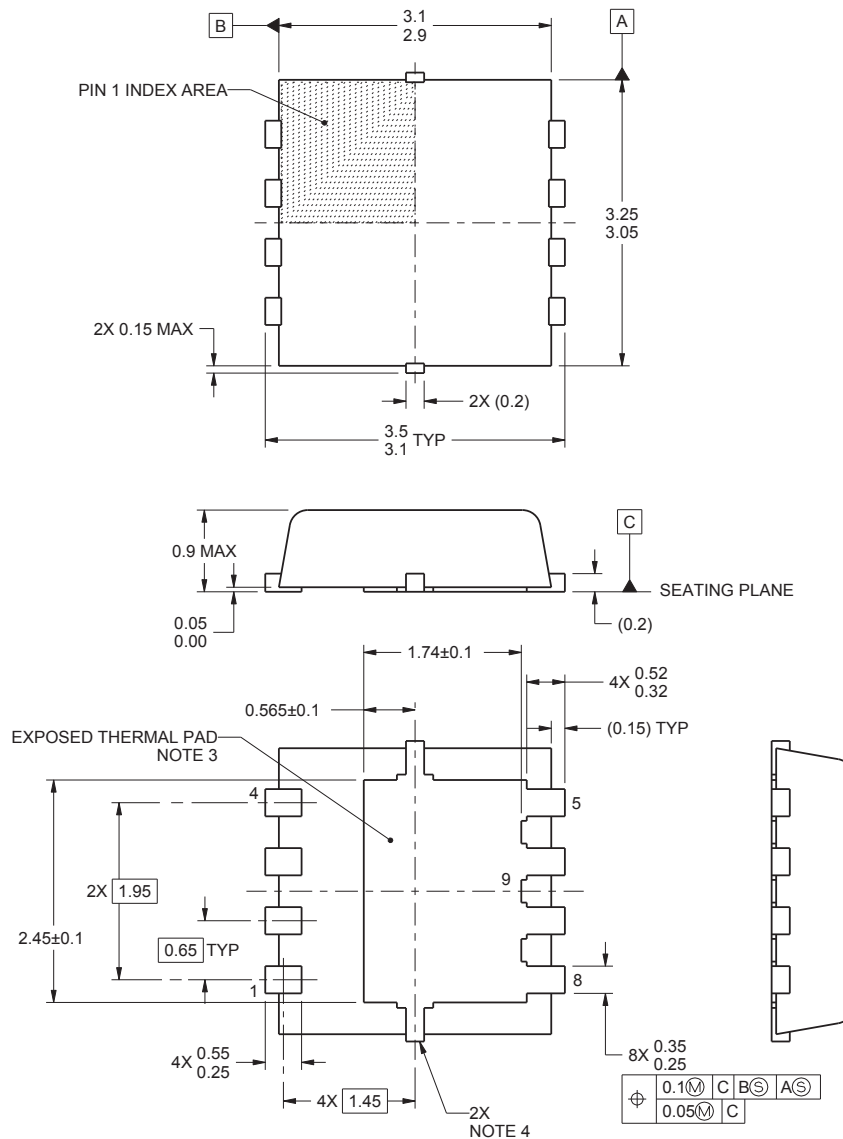
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

7.1 Q3A 封装尺寸



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和容限值遵循 ASME Y14.5M。
2. 本图纸如有变更，恕不通知。
3. 必须在印刷电路板上焊接封装散热焊盘，以获得良好的散热和机械性能。
4. 金属化特性为供应商选配特性，因此封装上可能不具备。
5. 所有尺寸不包括模具毛边或突出部分。

7.4 Q3A 卷带信息


M0144-01

- Notes:
1. 10 个链齿孔的累积容差为 ± 0.2 。
 2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
 3. 材料：黑色抗静电聚苯乙烯。
 4. 全部尺寸单位为 mm，除非另外注明。
 5. 厚度： 0.30 ± 0.05 mm。
 6. MSL1 260°C（红外 (IR) 和传导）PbF 回流焊兼容。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17581Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	17581	Samples
CSD17581Q3AT	ACTIVE	VSONP	DNH	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	17581	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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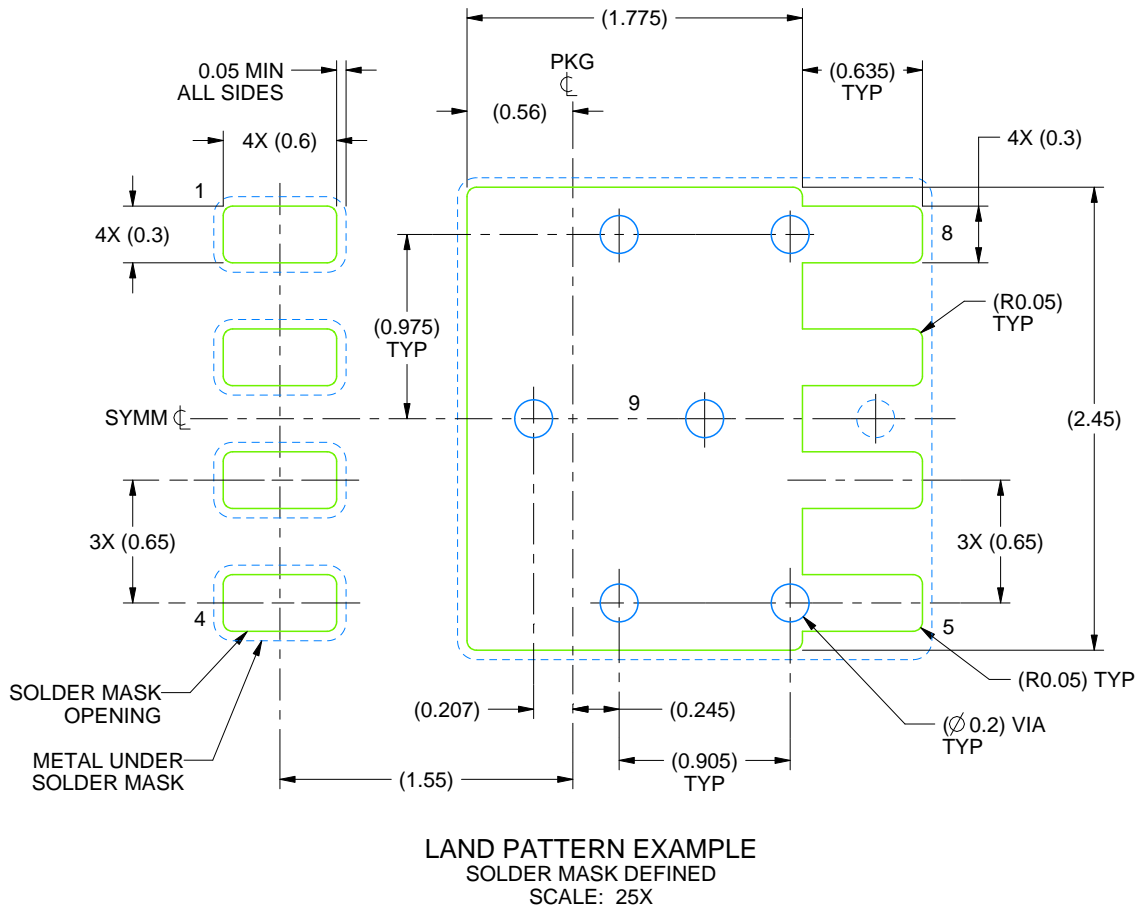
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EXAMPLE BOARD LAYOUT

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES: (continued)

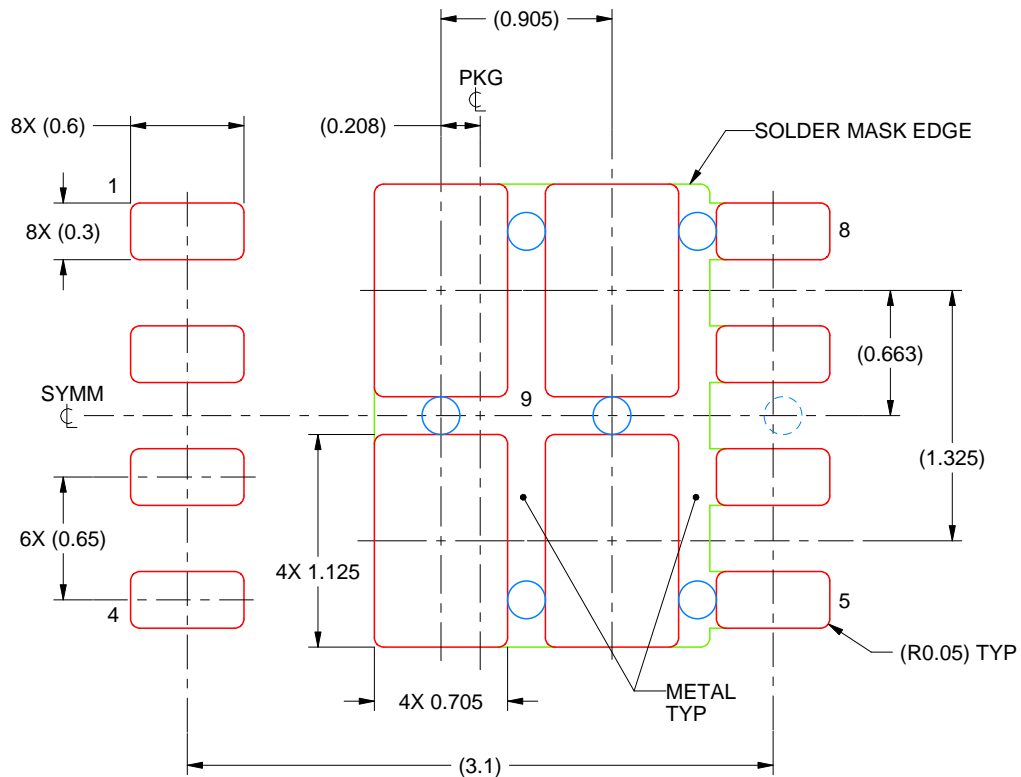
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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