CSD18501Q5A 40V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

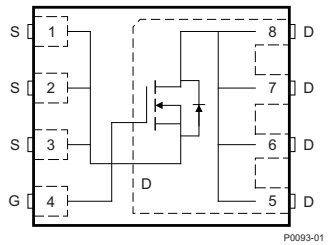
2 应用范围

- 直流 - 直流转换
- 次级侧同步整流
- 电池电机控制

3 说明

这款 40V，2.5mΩ，SON 5mm × 6mm NexFET™ 功率 MOSFET 被设计成在功率转换应用中最大限度地降低功率损耗。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (4.5V)	20		nC
Q_{gd}	栅极电荷（栅极到漏极）	5.9		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	3.3	mΩ
		V_{GS} = 10V	2.5	mΩ
$V_{GS(th)}$	阈值电压	1.8		V

订购信息(1)

器件	数量	介质	封装	出货
CSD18501Q5A	2500	13 英寸卷带	SON 5mm × 6mm 塑料封装	卷带封装
CSD18501Q5AT	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

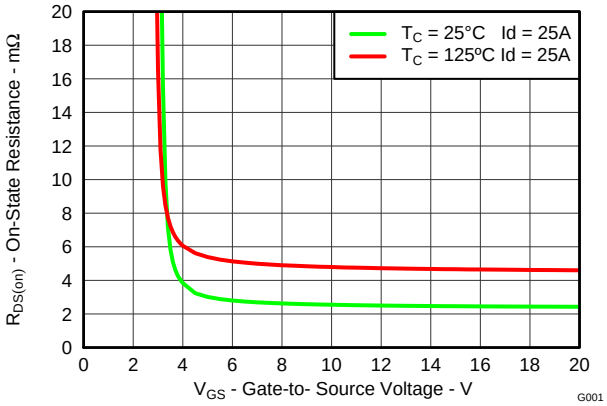
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	161	
	持续漏极电流 (1)	22	A
I_{DM}	脉冲漏极电流 (2)	400	A
P_D	功率耗散(1)	3.1	W
	功耗，T_C = 25°C	150	
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D=68A，L=0.1mH，R_G=25Ω	231	mJ

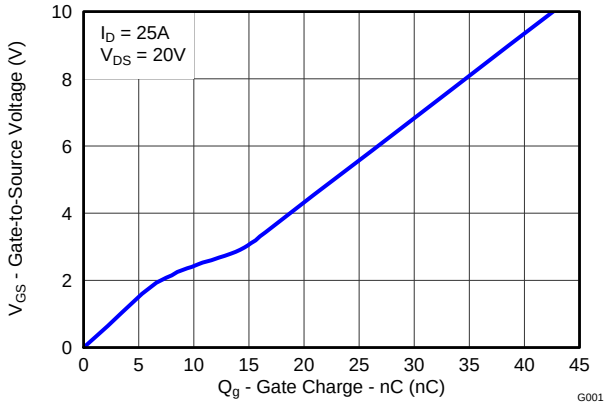
(1) $R_{\theta JA}$ = 40°C/W，这是在一个厚度 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司 的铜过渡垫片上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 1.0°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2012) to Revision C — **Page**

- 已添加器件编号至标题 ... 1
- 在订购信息表中添加了 7 英寸卷带 ... 1
- 已将受芯片限制的持续漏极电流增加至 161A ... 1
- 已将脉冲漏极电流增加至 400A ... 1
- 已添加外壳温度保持在 25°C 时的最大功耗一行 ... 1
- 已更新脉冲电流条件 ... 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve ... 4
- Updated the SOA in Figure 9 ... 6
- 已添加建议模板开口 ... 9

Changes from Revision A (June 2012) to Revision B — **Page**

- Changed the Transconductance TYP value From: 142 S To: 118 S. ... 3
- Changed the Turn On and Turn Off Delay Time, Rise and Fall Time Test Conditions From: I_{DS} = 25 A, R_G = 2 Ω To: I_{DS} = 25 A, R_G = 0 Ω ... 3
- Changed the Q_{rr} Reverse Recovery Charge TYP value From: 21 nC To: 70 nC ... 3

Changes from Original (June 2012) to Revision A — **Page**

- 已添加“T_A = 25°C”至产品概要表 ... 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

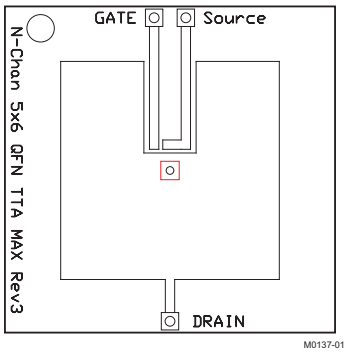
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 32 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.4	1.8	2.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 25 A		3.3	4.3	mΩ
		V_{GS} = 10 V, I_D = 25 A		2.5	3.2	mΩ
g_{fs}	Transconductance	V_{DS} = 20 V, I_D = 25 A		118		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		3200	3840	pF
C_{oss}	Output Capacitance			725	870	pF
C_{rss}	Reverse Transfer Capacitance			18	23	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 20 V, I_D = 25 A		20	24	nC
Q_g	Gate Charge Total (10 V)			42	50	
Q_{gd}	Gate Charge Gate-to-Drain			5.9		nC
Q_{gs}	Gate Charge Gate-to-Source			8.1		nC
$Q_{g(th)}$	Gate Charge at Vth			5.7		nC
Q_{oss}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		48		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 25 A, R_G = 0		4.7		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			3.4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 20 V, I_F = 25 A, di/dt = 300 A/µs		70		nC
t_{rr}	Reverse Recovery Time			40		ns

5.2 Thermal Information

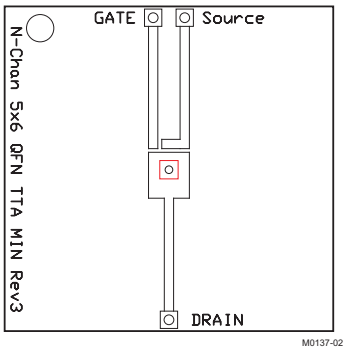
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45-cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

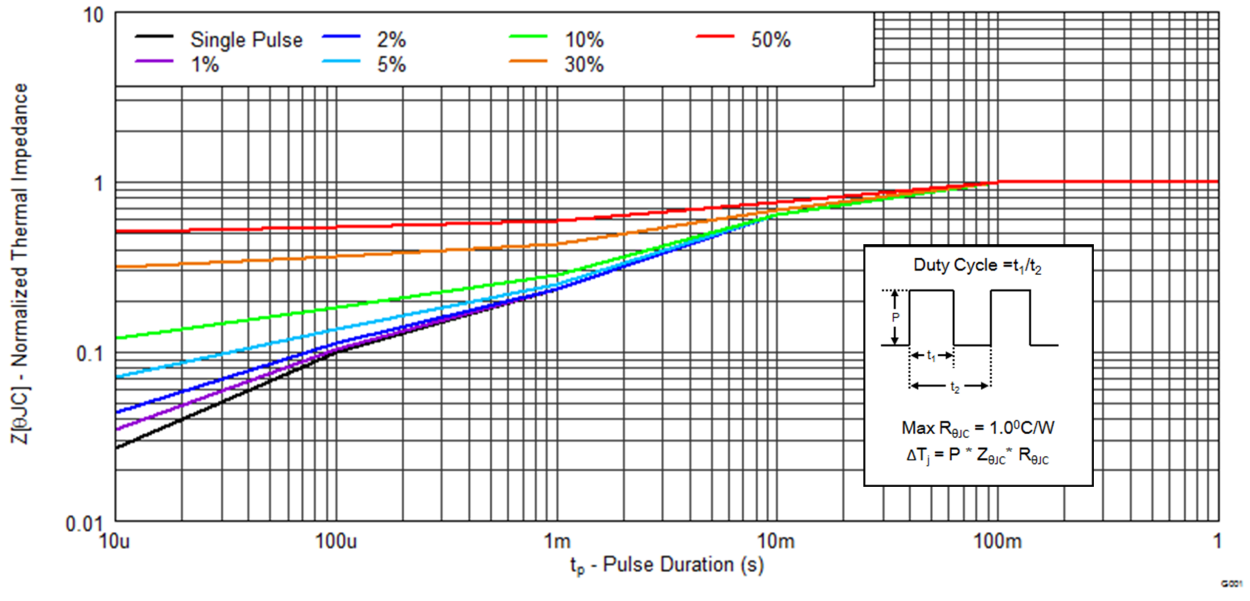


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

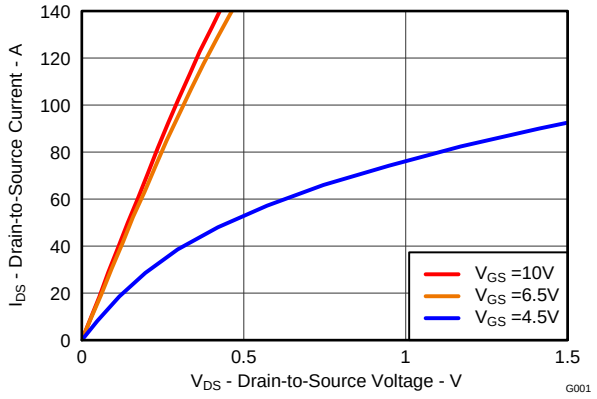


Figure 2. Saturation Characteristics

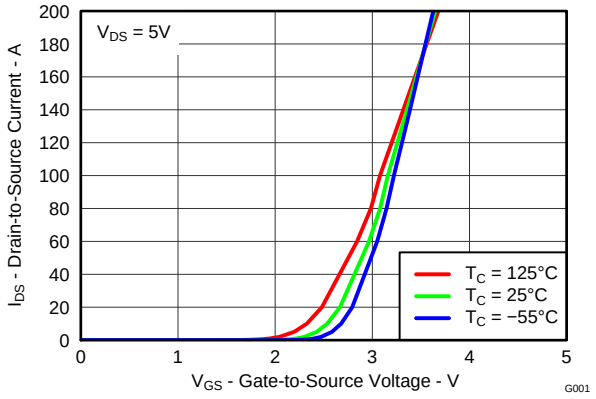


Figure 3. Transfer Characteristics

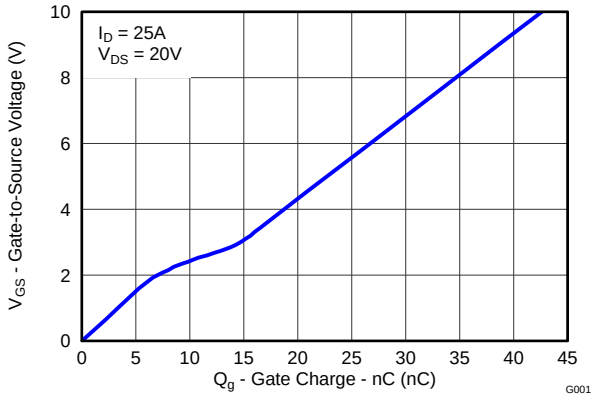


Figure 4. Gate Charge

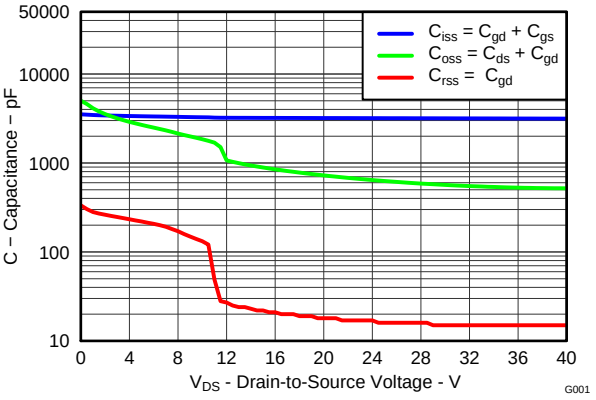


Figure 5. Capacitance

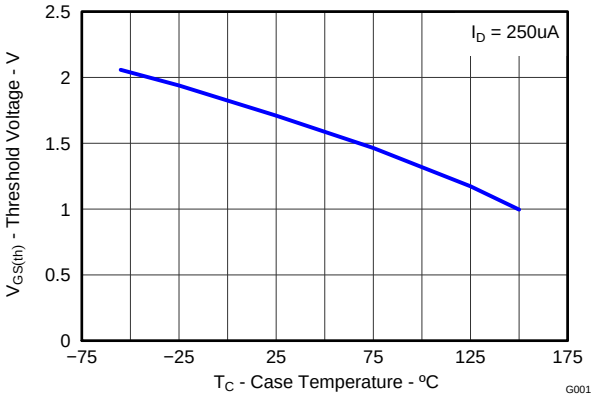


Figure 6. Threshold Voltage vs Temperature

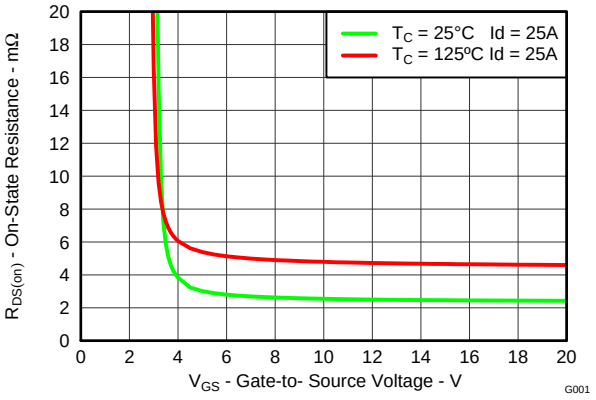


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

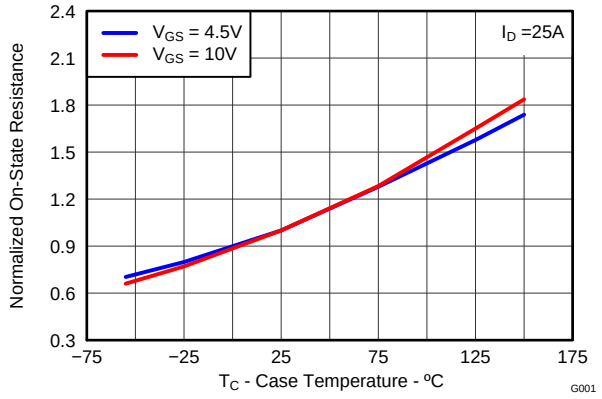


Figure 8. Normalized On-State Resistance vs Temperature

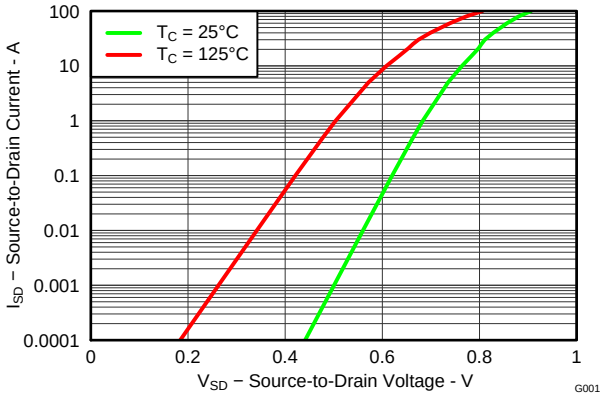


Figure 9. Typical Diode Forward Voltage

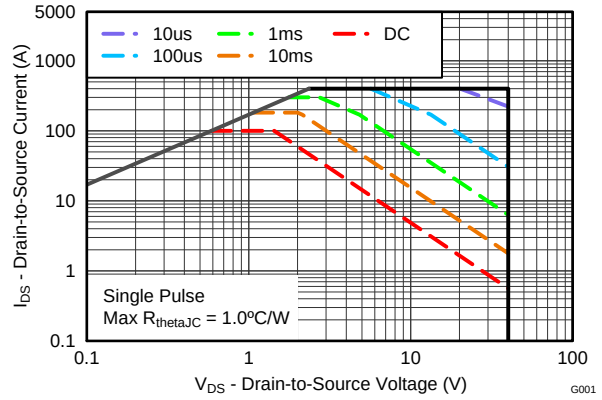


Figure 10. Maximum Safe Operating Area

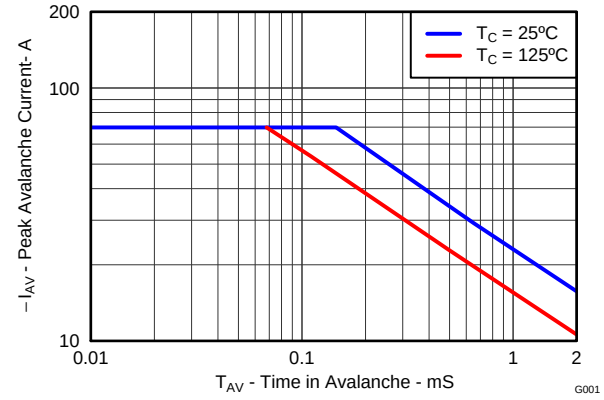


Figure 11. Single Pulse Unclamped Inductive Switching

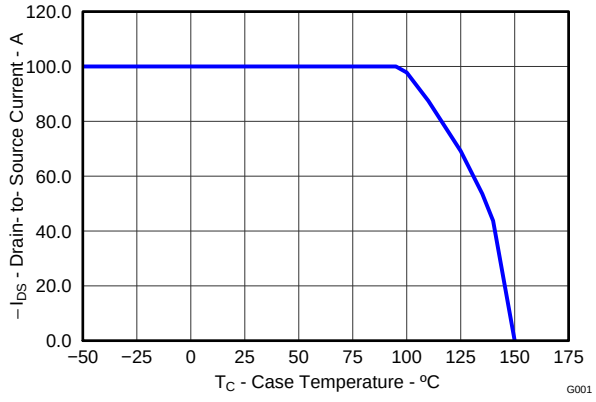


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

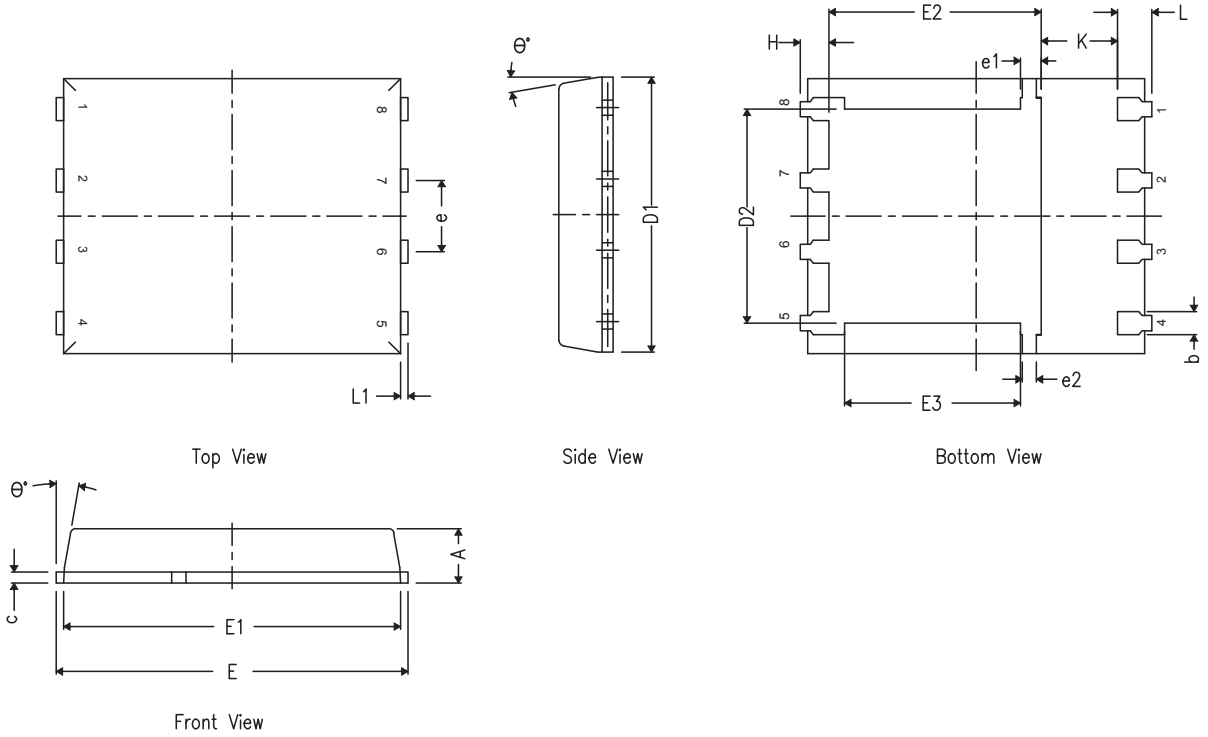
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械、封装和可订购信息

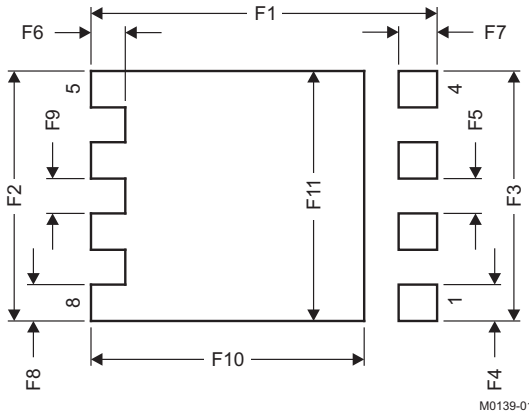
以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5A 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	-	12°

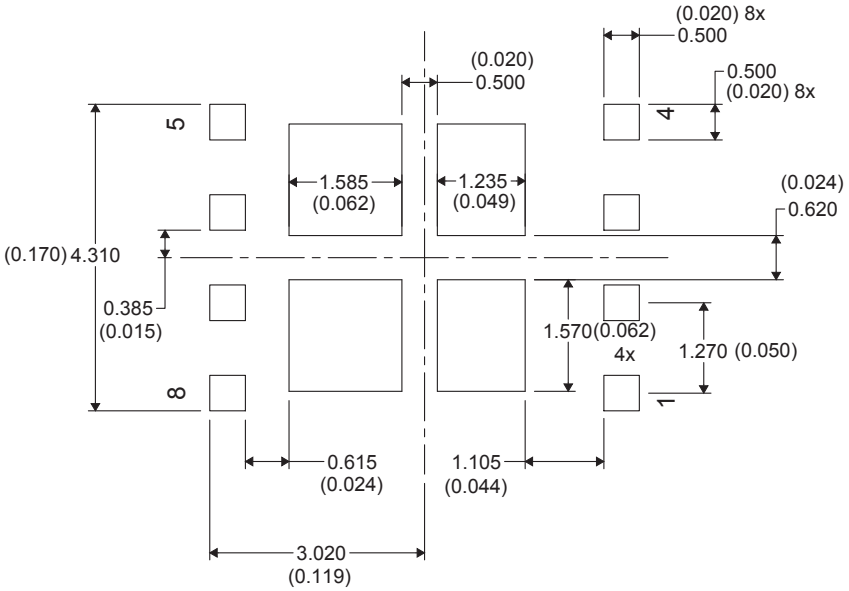
7.2 建议印刷电路板 (PCB) 布局



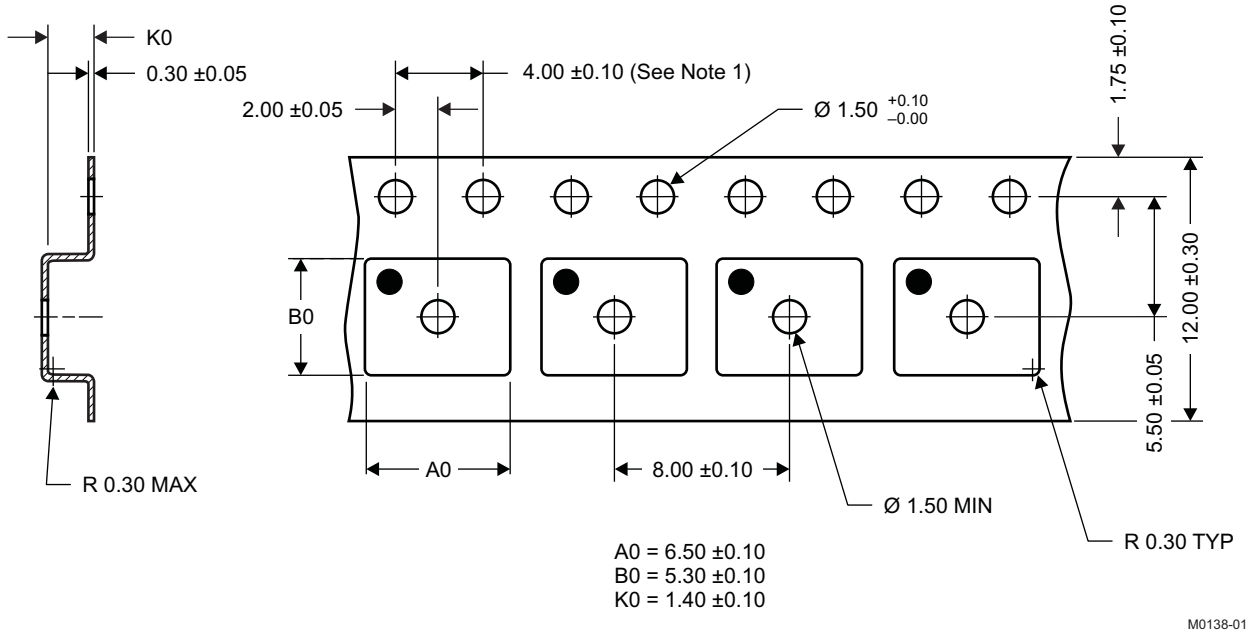
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板开口



7.4 Q5A 卷带信息



注：

1. 10 个链齿孔的累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18501Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

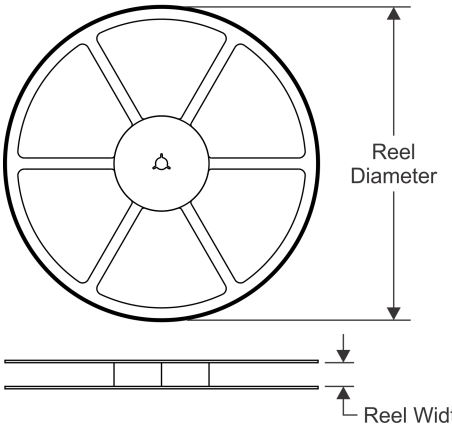
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

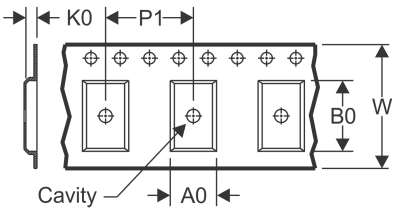
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

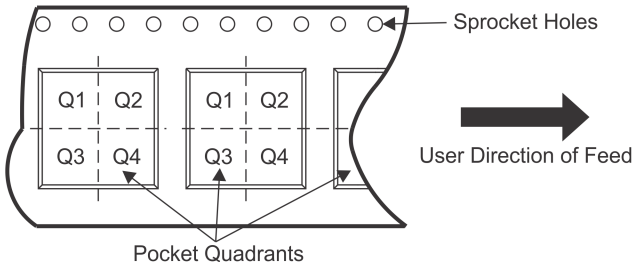


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

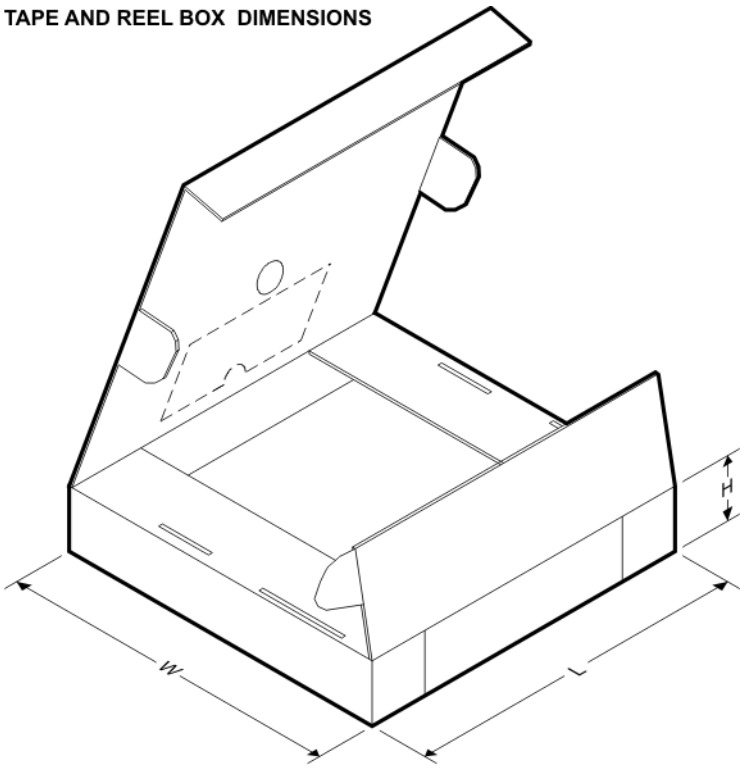
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

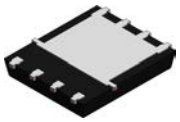
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18501Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18501Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

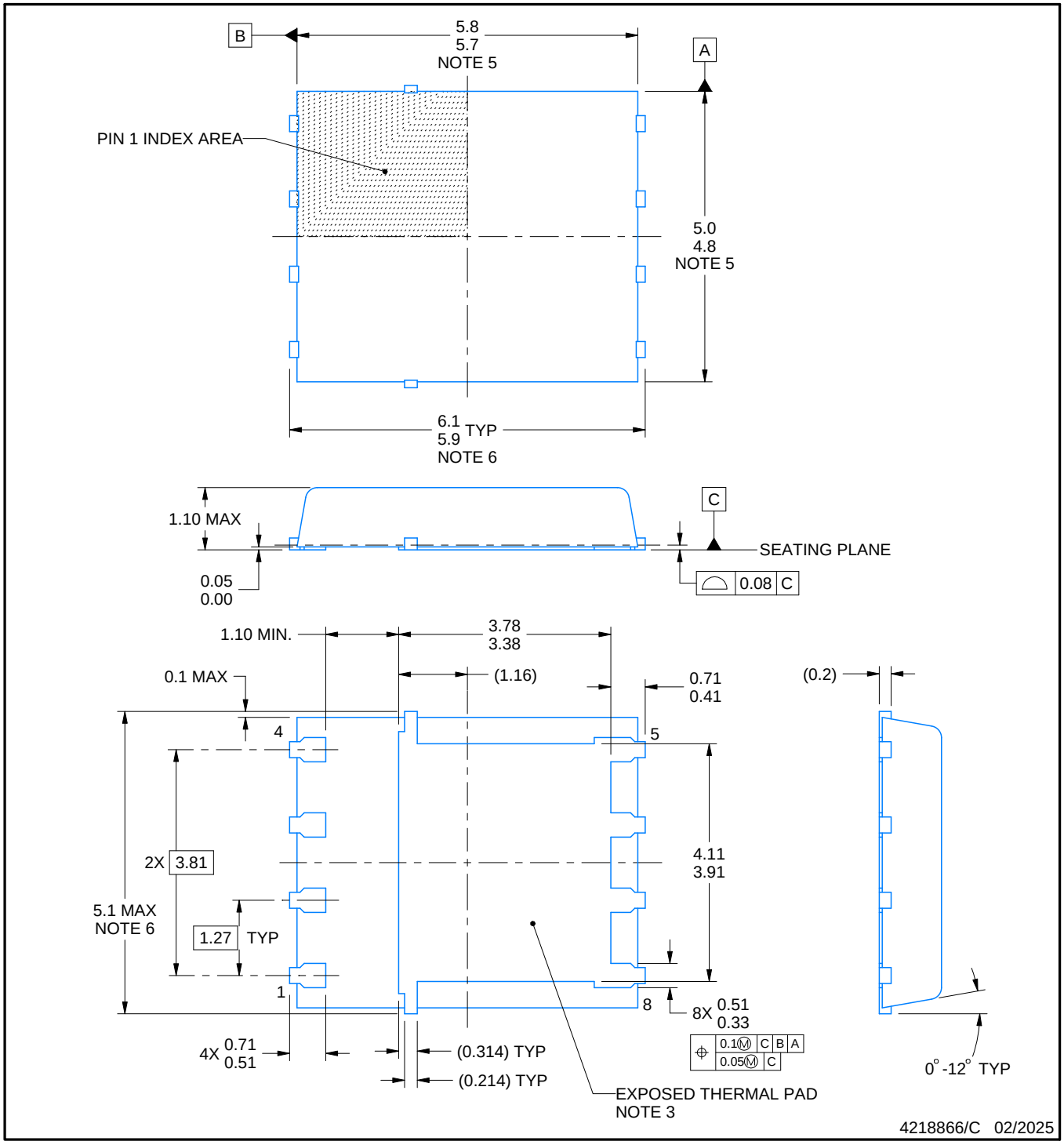


PACKAGE OUTLINE

DQJ0008A

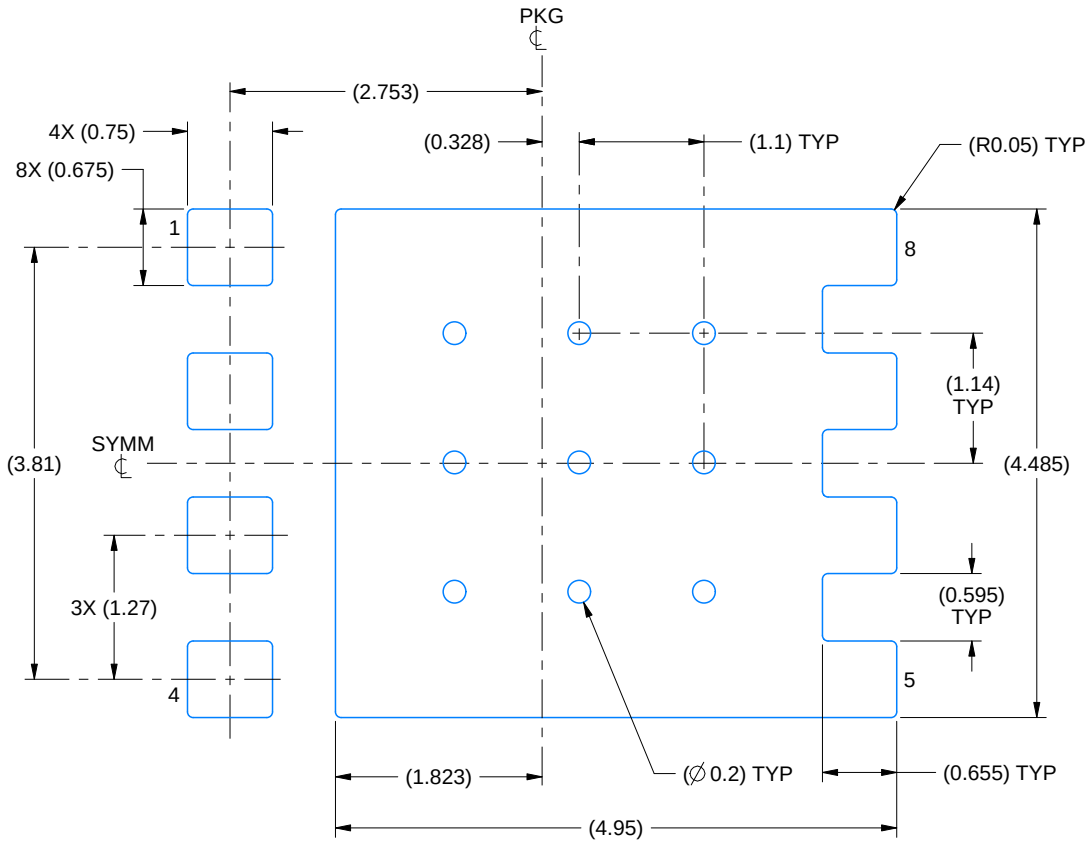
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

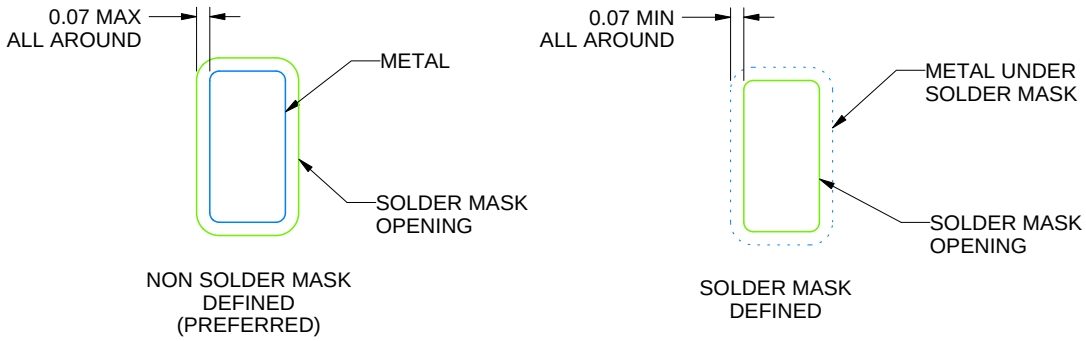


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X



SOLDER MASK DETAILS

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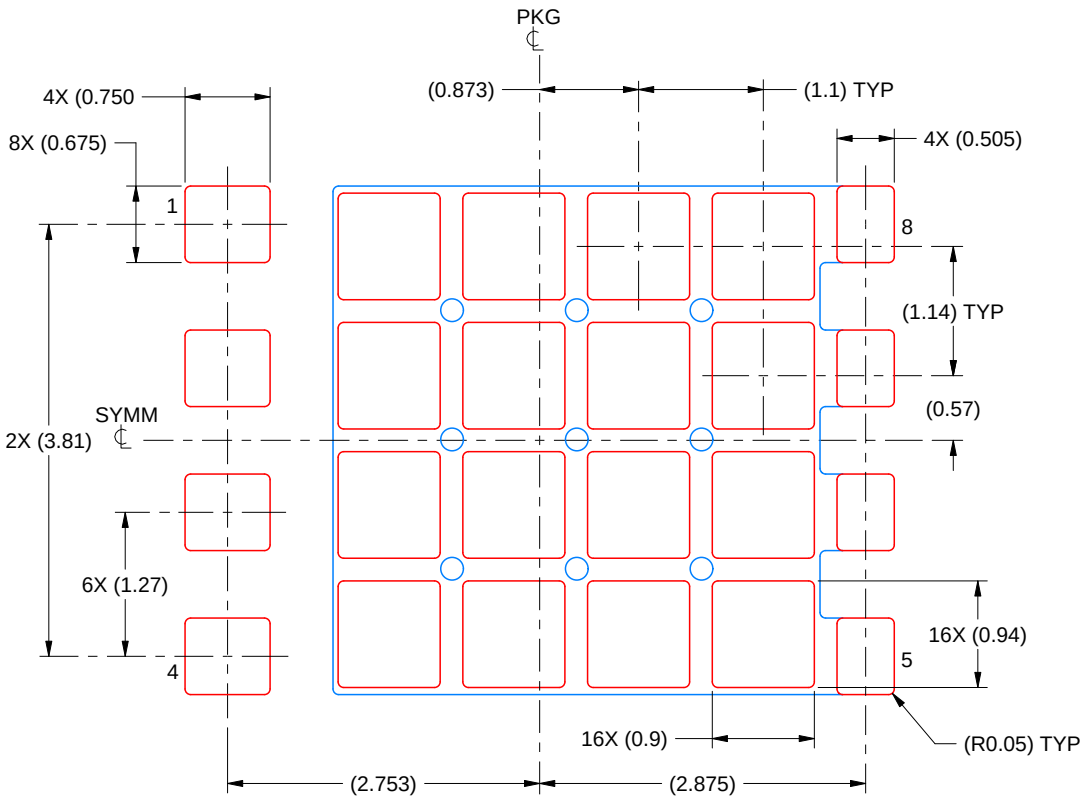
NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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