CSD18504Q5A 40V N 沟道 NexFET™ 功率 MOSFET

1 特性

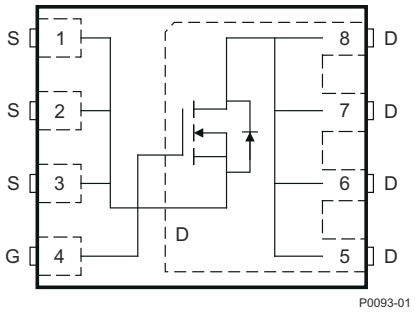
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS
- 无卤素
- SON 5mm × 6mm 塑料封装

2 应用

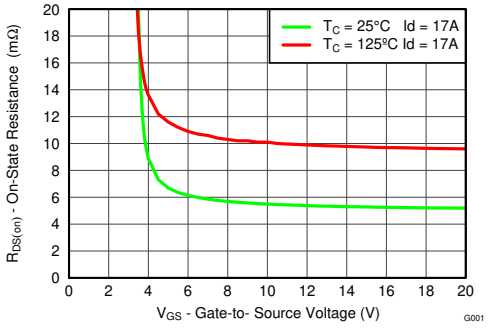
- 直流/直流转换
- 次级侧同步整流器
- 电池电机控制

3 说明

这款 5.3mΩ、SON 5mm × 6mm、40V NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



顶视图



$R_{DS(on)}$ 与 V_{GS} 之间的关系

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (4.5V)	7.7		nC
Q_{gd}	栅极电荷（栅极到漏极）	2.4		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	7.5	mΩ
		V_{GS} = 10V	5.3	mΩ
$V_{GS(th)}$	阈值电压	1.9		V

订购信息 (1)

器件	数量	介质	封装	运输
CSD18504Q5A	2500	13 英寸卷带	SON 5mm × 6mm 塑料封装	卷带包装
CSD18504Q5AT	250	7 英寸卷带		

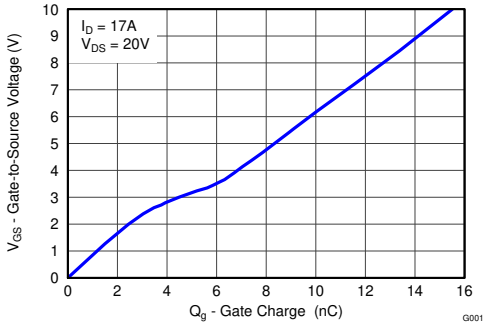
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	50	A
	持续漏极电流（受器件限制），T_C = 25°C 时测得	75	
	持续漏极电流(1)	15	
I_{DM}	脉冲漏极电流(2)	275	A
P_D	功率耗散(1)	3.1	W
	功率耗散，T_C = 25°C	77	
T_J、T_{stg}	工作结温和贮存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 43A，L = 0.1mH，R_G = 25Ω	92	mJ

(1) $R_{\theta JA}$ = 40°C/W，这是在 1 平方英寸的情况下，2 盎司铜焊盘安装在
0.06 英寸厚的 FR4 PCB 上时测得的典型值。

(2) 最大 $R_{\theta JC}$ = 2.0°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0V, I_D = 250 μA	40			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0V, V_{DS} = 32V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.5	1.9	2.4	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5V, I_D = 17A		7.5	9.8	mΩ
		V_{GS} = 10V, I_D = 17A		5.3	6.6	mΩ
g_{fs}	Transconductance	V_{DS} = 20V, I_D = 17A		71		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		1380	1656	pF
C_{oss}	Output Capacitance			310	372	pF
C_{rss}	Reverse Transfer Capacitance			8	9.6	pF
R_G	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 20V, I_D = 17A		7.7	9.2	nC
Q_g	Gate Charge Total (10V)			16	19	
Q_{gd}	Gate Charge Gate-to-Drain			2.4		nC
Q_{gs}	Gate Charge Gate-to-Source			3.2		nC
$Q_{g(th)}$	Gate Charge at V_{th}			2.2		nC
Q_{oss}	Output Charge	V_{DS} = 20V, V_{GS} = 0V		21		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 20V, V_{GS} = 10V, I_{DS} = 17A, R_G = 0 Ω		3.2		ns
t_r	Rise Time			6.8		ns
$t_{d(off)}$	Turn Off Delay Time			12		ns
t_f	Fall Time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 17A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 20V, I_F = 17A, di/dt = 300A/μs		39		nC
t_{rr}	Reverse Recovery Time			28		ns

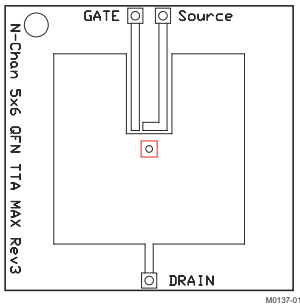
4.2 Thermal Information

(T_A = 25°C unless otherwise stated)

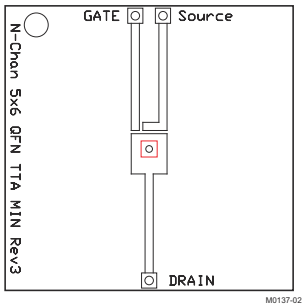
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			2.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1) (2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81cm × 3.81cm), 0.06-inch (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45cm^2) of 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2oz. (0.071mm thick) Cu.

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

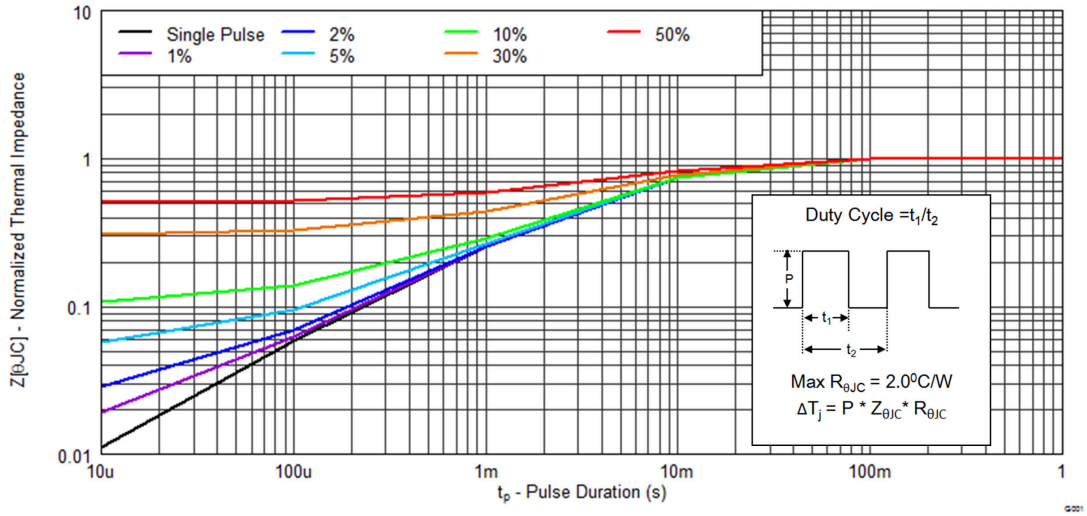


图 4-1. Transient Thermal Impedance

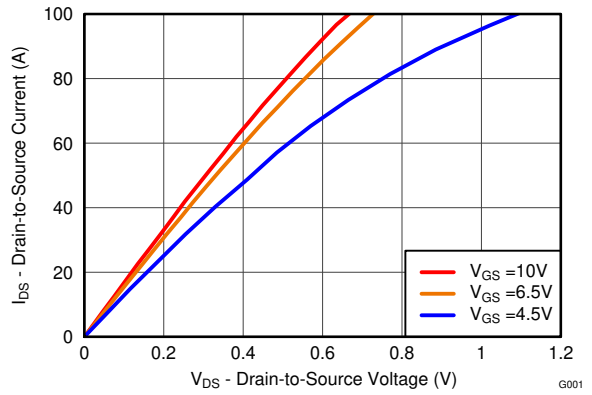


图 4-2. Saturation Characteristics

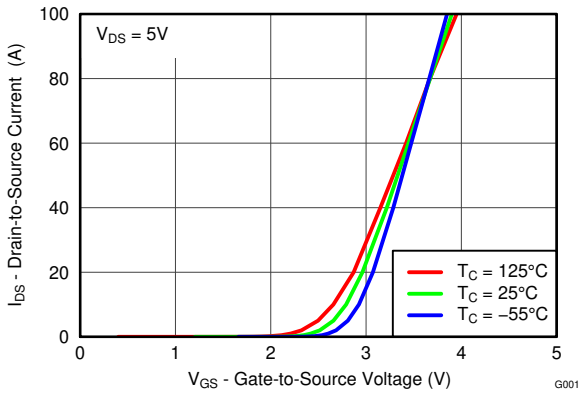


图 4-3. Transfer Characteristics

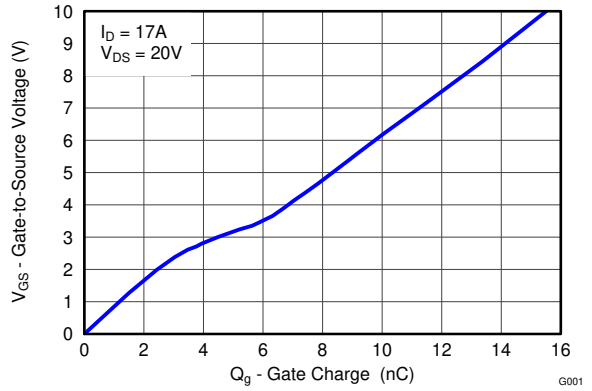


图 4-4. Gate Charge

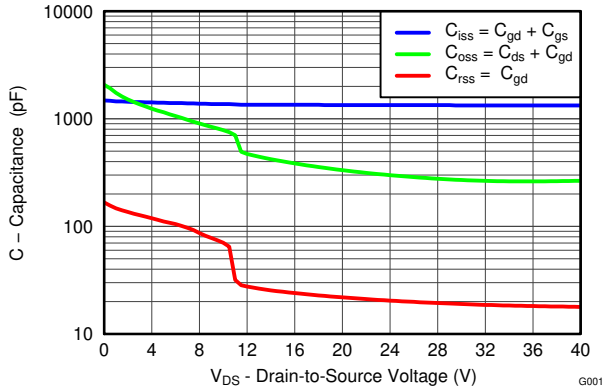


图 4-5. Capacitance

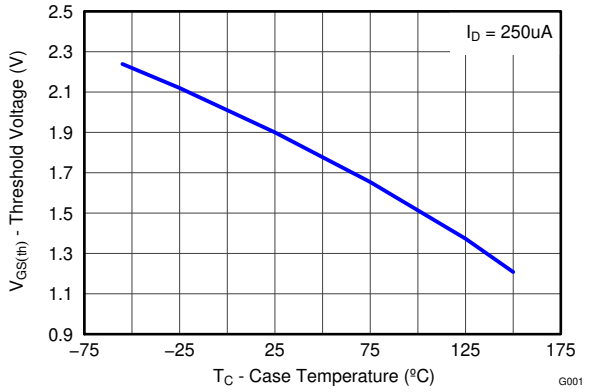


图 4-6. Threshold Voltage vs Temperature

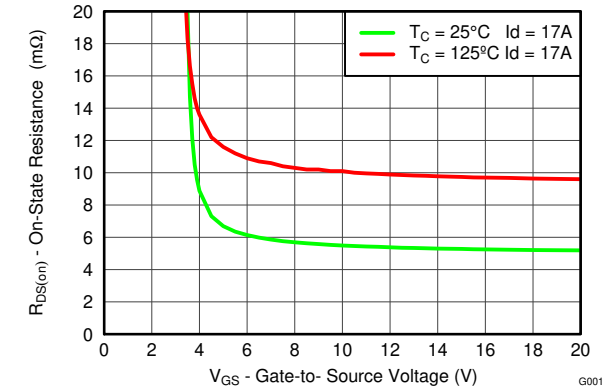


图 4-7. On-State Resistance vs Gate-to-Source Voltage

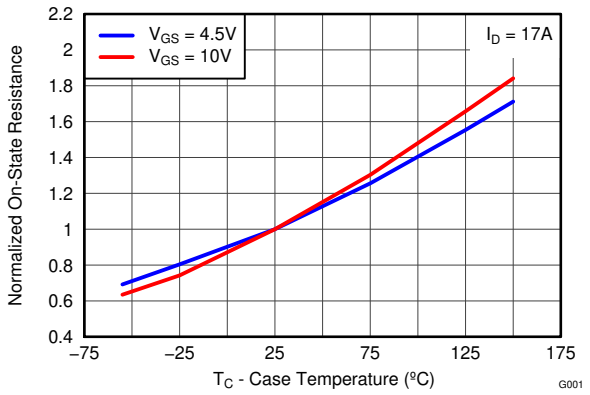


图 4-8. Normalized On-State Resistance vs Temperature

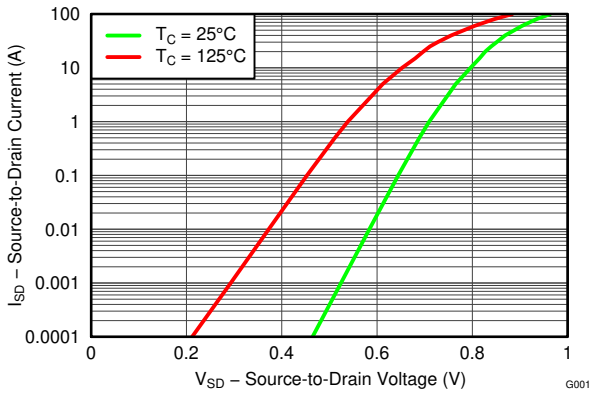


图 4-9. Typical Diode Forward Voltage

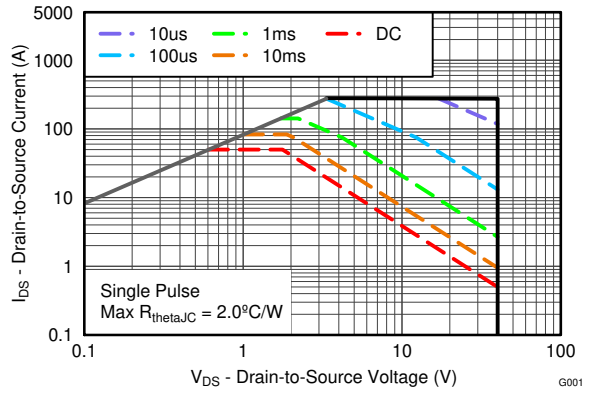


图 4-10. Maximum Safe Operating Area

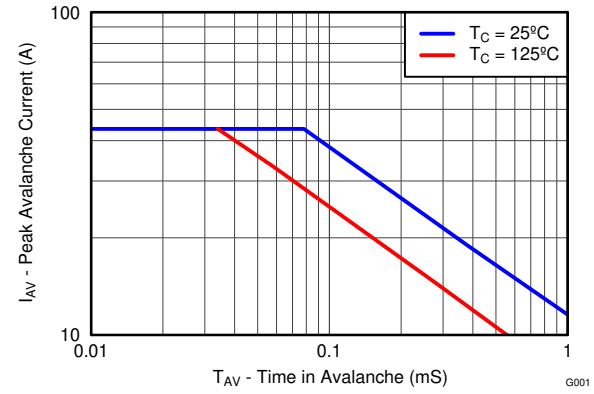


图 4-11. Single Pulse Unclamped Inductive Switching

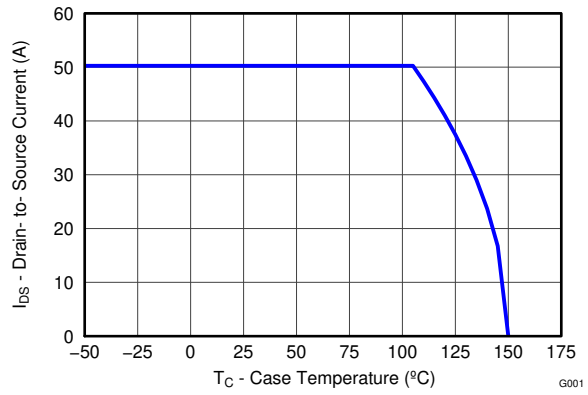


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

5.2 Documentation Support

5.2.1 Related Documentation

5.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.5 Trademarks

NexFET™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

5.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

Changes from Revision E (August 2014) to Revision F (January 2025) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1

Changes from Revision D (August 2014) to Revision E (August 2014) **Page**

- 已将脉冲电流增加到 275A.....1
- Updated the SOA in 图 4-10 4

Changes from Revision C (May 2013) to Revision D (August 2014) **Page**

- 向“订购信息”表中添加了 7 英寸卷带.....1
- 添加了管壳温度保持在 25°C 时的功率耗散参数.....1
- 更新了脉冲电流条件.....1
- Updated 图 4-1 to a normalized $R_{\theta JC}$ curve.....4

Changes from Revision B (November 2012) to Revision C (May 2013) **Page**

- Updated Mechanical stencil.....9

Changes from Revision A (October 2012) to Revision B (November 2012) **Page**

- 已更改 $R_{DS(on)}$ 与 V_{GS} 的关系曲线图以及栅极充电曲线图.....1
- Changed $R_{\theta JA}$ Max value From: 51 To: 50°C/W.....3
- Changed the Typical MOSFET Characteristics section.....4

Changes from Revision * (June 2012) to Revision A (October 2012) **Page**

- Changed the Transconductance TYP value From: 63S To: 71S.....3
- Changed the Turn On and Turn Off Delay Time, Rise and Fall Time Test Conditions From: I_{DS} = 17A, R_G = 2Ω To: I_{DS} = 17A, R_G = 0Ω.....3
- Changed the Q_{rr} Reverse Recovery Charge TYP value From: 18nC To: 39nC.....3

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18504Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18504	Samples
CSD18504Q5AT	ACTIVE	VSONP	DQJ	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18504	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

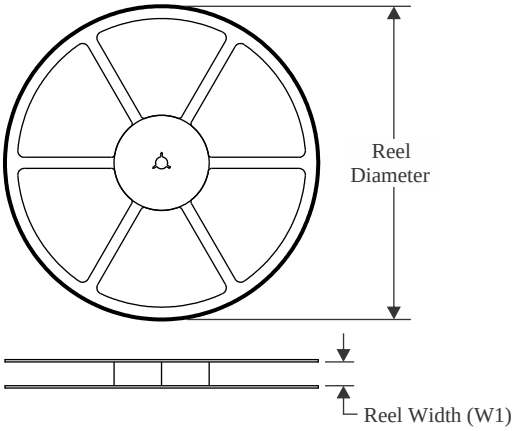
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

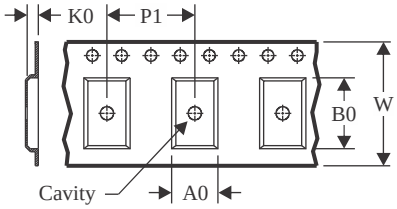
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

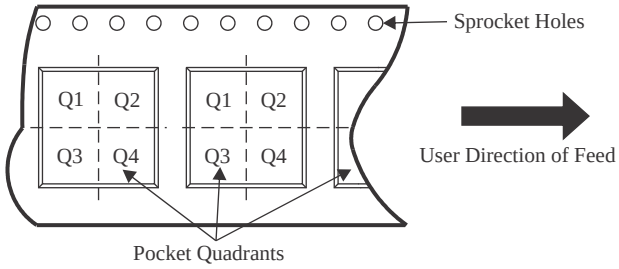


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

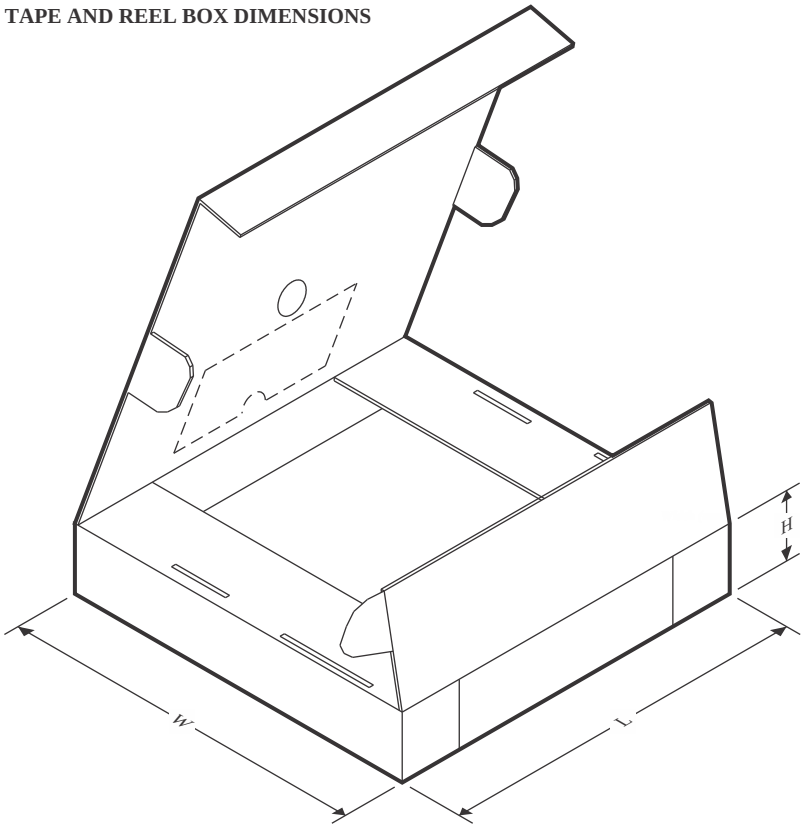
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

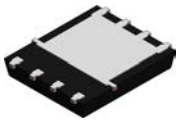
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18504Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18504Q5AT	VSONP	DQJ	8	250	180.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18504Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0
CSD18504Q5AT	VSONP	DQJ	8	250	190.0	190.0	30.0

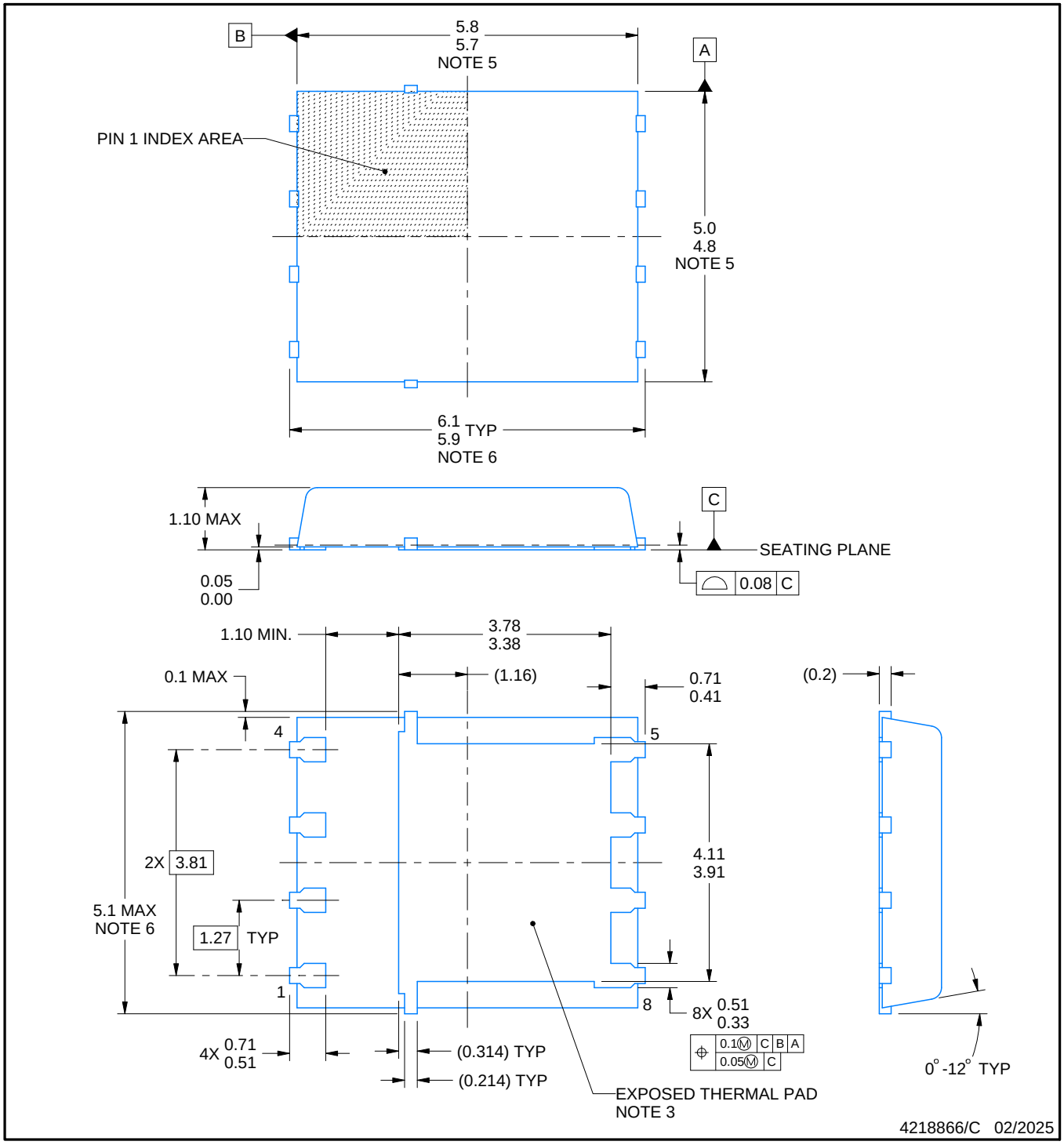


PACKAGE OUTLINE

DQJ0008A

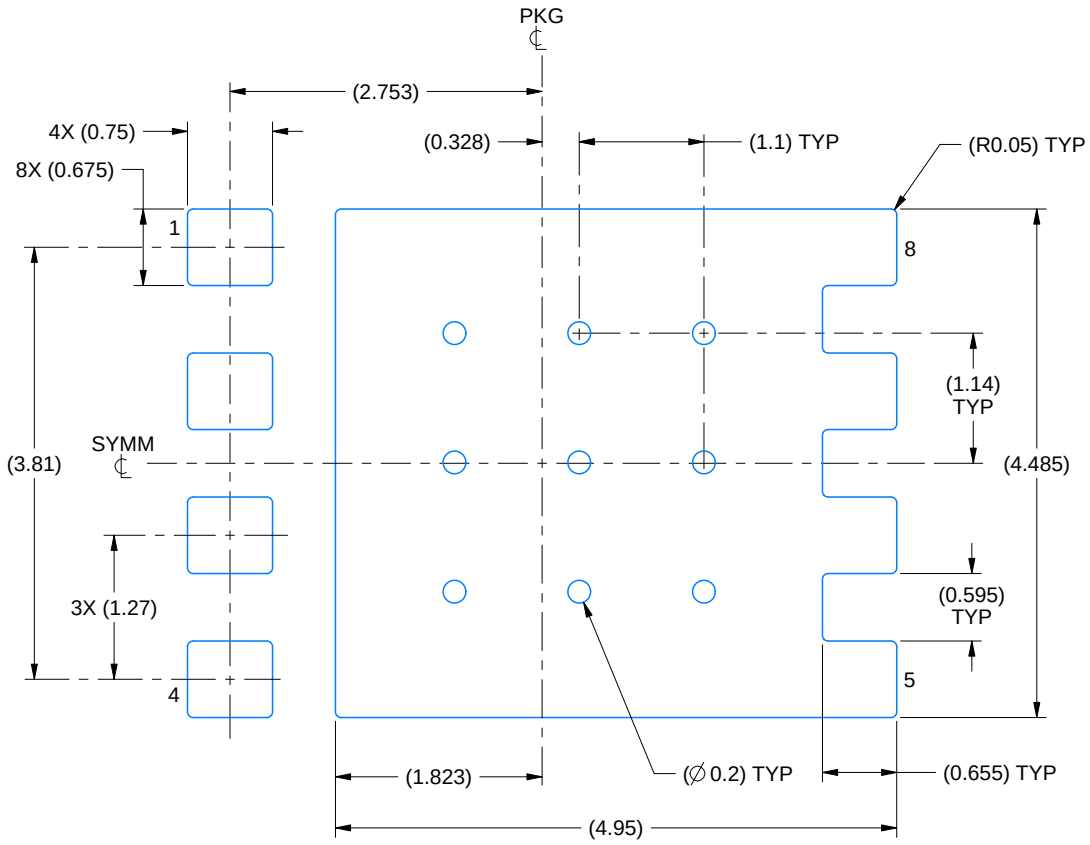
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

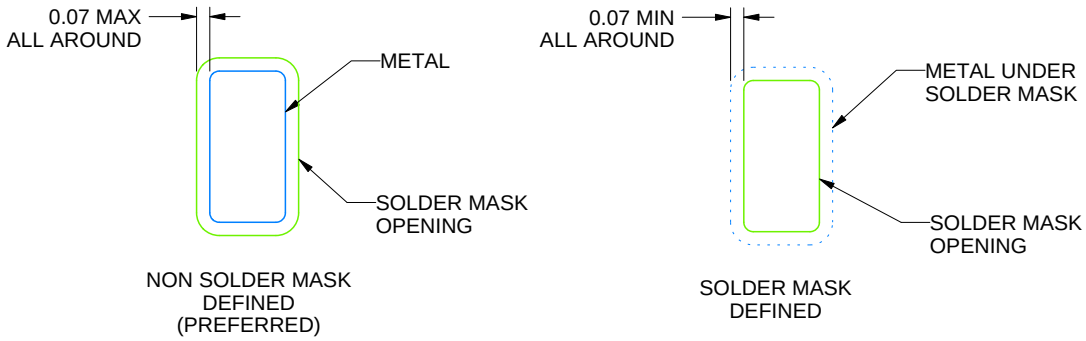


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X



SOLDER MASK DETAILS

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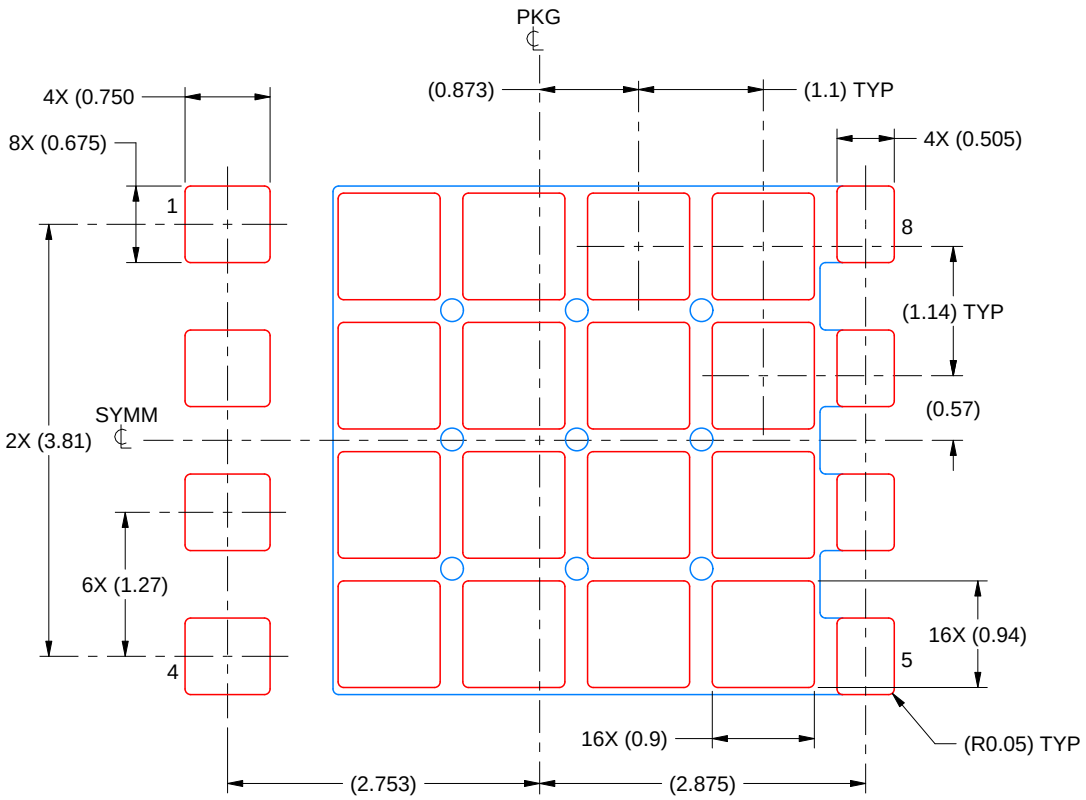
NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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