

# CSD18532KCS 60V N 沟道 NexFET™ 功率 MOSFET

## 1 特性

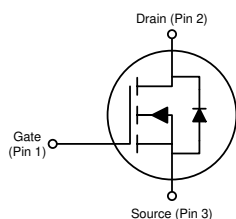
- 超低  $Q_g$  和  $Q_{gd}$
- 低热阻
- 雪崩级
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS
- 无卤素
- TO-220 塑料封装

## 2 应用

- 直流/直流转换
- 次级侧同步整流器
- 电机控制

## 说明

这款 60V、 $3.3m\Omega$ 、TO-220 NexFET™ 功率 MOSFET 旨在用于更最大限度地降低功率转换应用中的损耗。



### 产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
$V_{DS}$	漏源电压	60		V
$Q_g$	栅极电荷总量 (10V)	44		nC
$Q_{gd}$	栅极电荷 (栅极到漏极)	6.9		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	4.2	$m\Omega$
		$V_{GS} = 10\text{V}$	3.3	$m\Omega$
$V_{GS(th)}$	阈值电压	1.8		V

### 订购信息<sup>(1)</sup>

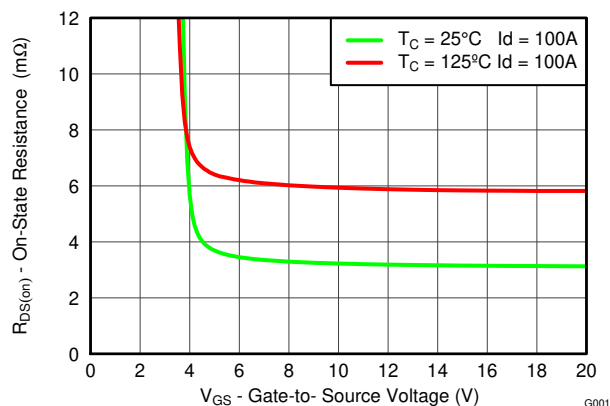
器件	封装	介质	数量	运输
CSD18532KCS	TO-220 塑料封装	管装	50	管装

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

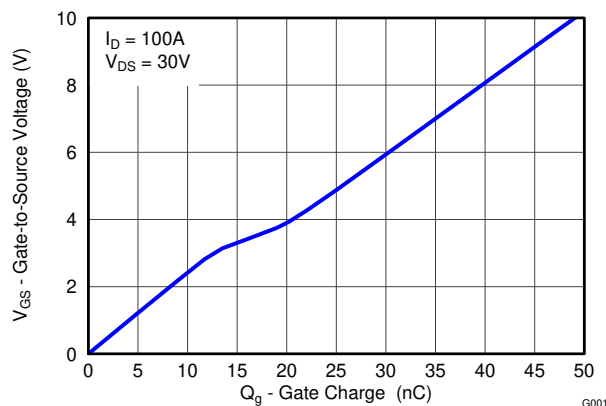
### 绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
$V_{DS}$	漏源电压	60	V
$V_{GS}$	栅源电压	$\pm 20$	V
$I_D$	持续漏极电流 (受封装限制), $T_C = 25^\circ\text{C}$ 时测得	100	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	169	
	持续漏极电流 (受芯片限制), $T_C = 100^\circ\text{C}$ 时测得	116	
$I_{DM}$	脉冲漏极电流 <sup>(1)</sup>	400	A
$P_D$	功率耗散	250	W
$T_J$ 、 $T_{stg}$	工作结温和贮存温度范围	-55 至 175	$^\circ\text{C}$
$E_{AS}$	雪崩能量, 单脉冲 $I_D = 75\text{A}$ , $L = 0.1\text{mH}$ , $R_G = 25\Omega$	281	mJ

(1) 脉冲持续时间  $\leq 300\mu\text{s}$ , 占空比  $\leq 2\%$



$R_{DS(on)}$  与  $V_{GS}$  之间的关系



栅极电荷



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## 3 Specifications

### 3.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-Source Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250 μA	60			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 48V			1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 20V			100	nA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	1.8	2.2	V
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 100A		4.2	5.3	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 100A		3.3	4.2	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 30V, I <sub>D</sub> = 100A		187		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 30V, f = 1MHz		3900	4680	pF
C <sub>oss</sub>	Output Capacitance			470	564	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			11	14	pF
R <sub>G</sub>	Series Gate Resistance			1.3	2.6	Ω
Q <sub>g</sub>	Gate Charge Total (4.5V)	V <sub>DS</sub> = 30V, I <sub>D</sub> = 100A		21	25	nC
Q <sub>g</sub>	Gate Charge Total (10V)			44	53	nC
Q <sub>gd</sub>	Gate Charge Gate-to-Drain			6.9		nC
Q <sub>gs</sub>	Gate Charge Gate-to-Source			10		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			7.3		nC
Q <sub>oss</sub>	Output Charge		V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V		52	
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 10V, I <sub>DS</sub> = 100A, R <sub>G</sub> = 0Ω		7.8		ns
t <sub>r</sub>	Rise Time			5.3		ns
t <sub>d(off)</sub>	Turn Off Delay Time			24.2		ns
t <sub>f</sub>	Fall Time			5.6		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = 100A, V <sub>GS</sub> = 0V		0.8	1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = 30V, I <sub>F</sub> = 100A,		127		nC
t <sub>rr</sub>	Reverse Recovery Time	di/dt = 300A/μs		57		ns

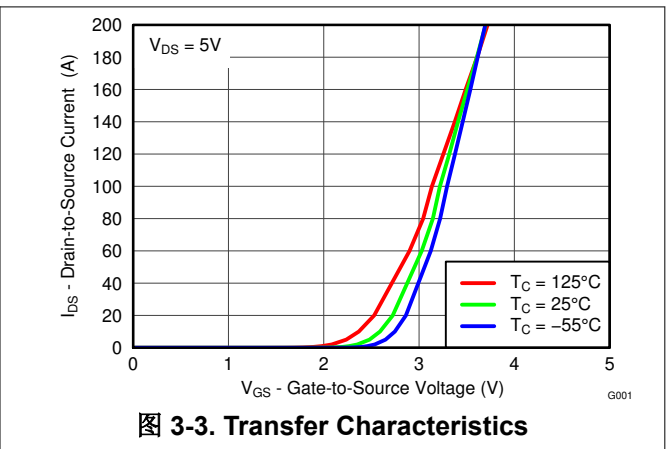
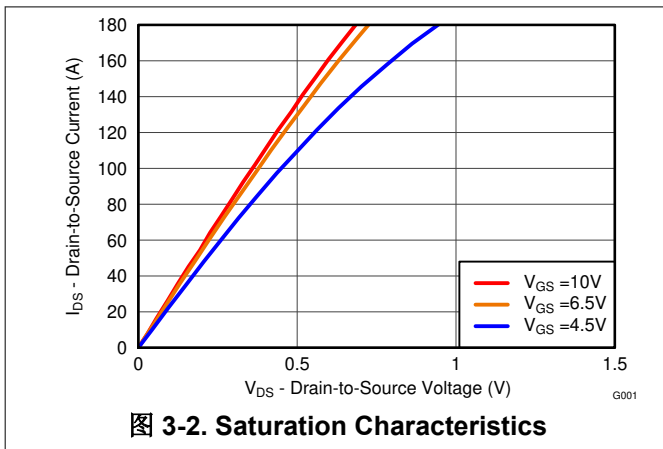
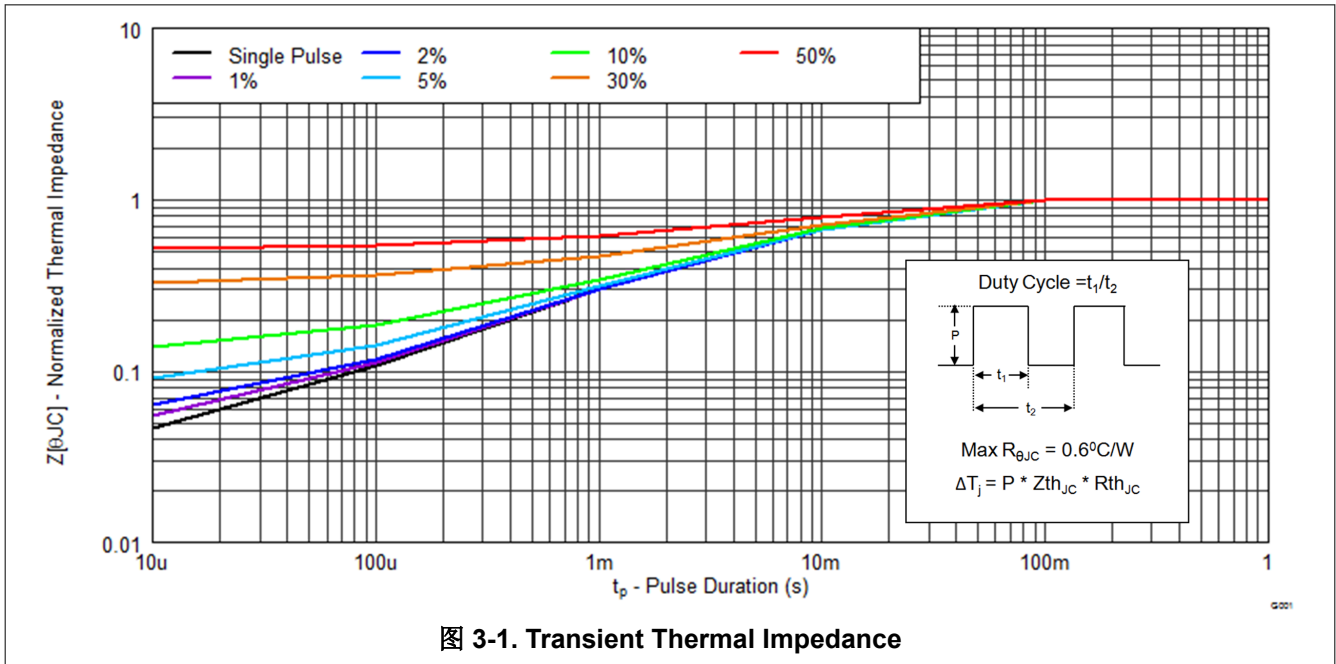
### 3.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-Case Thermal Resistance			0.6	°C/W
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance			62	

### 3.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



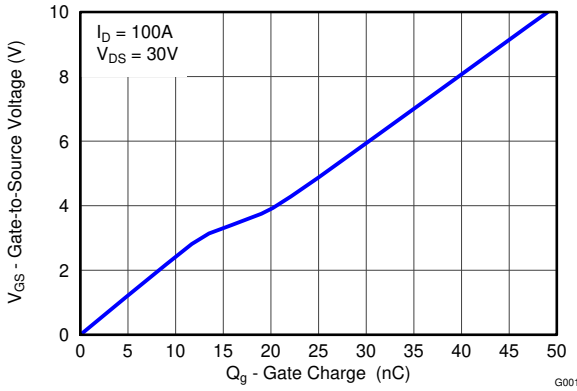


图 3-4. Gate Charge

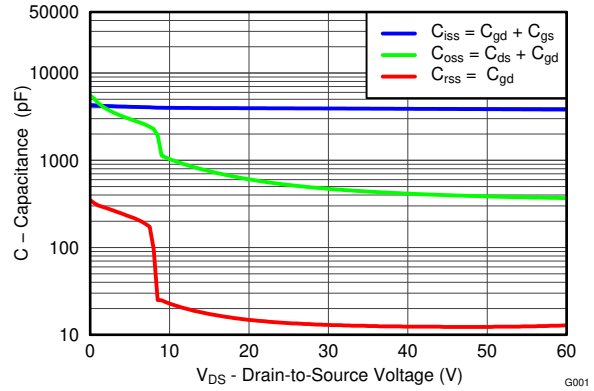


图 3-5. Capacitance

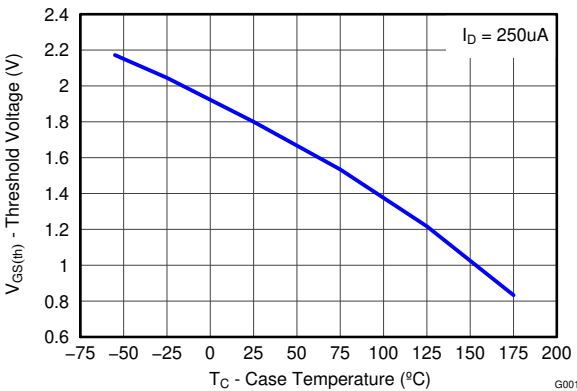


图 3-6. Threshold Voltage vs Temperature

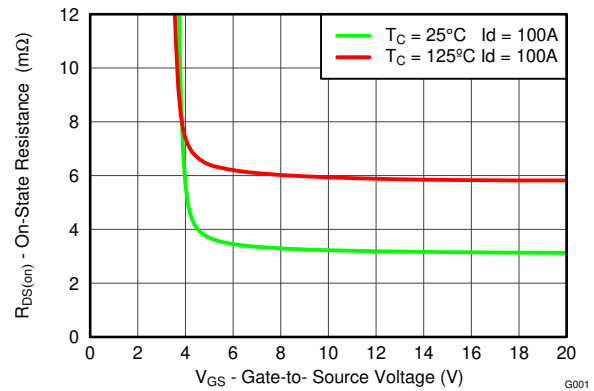


图 3-7. On-State Resistance vs Gate-to-Source Voltage

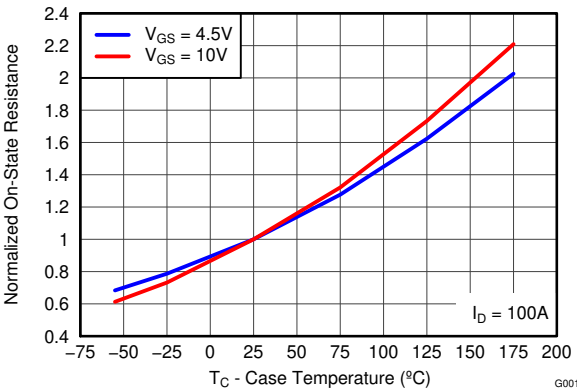


图 3-8. Normalized On-State Resistance vs Temperature

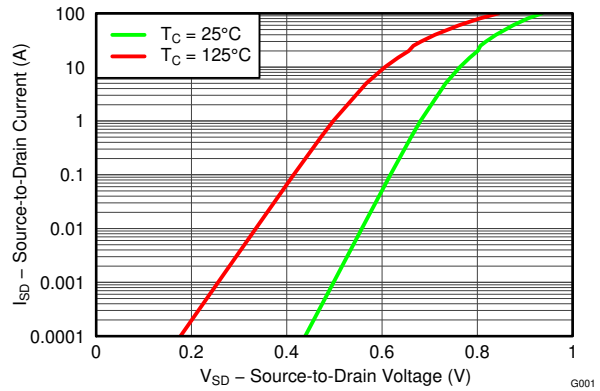


图 3-9. Typical Diode Forward Voltage

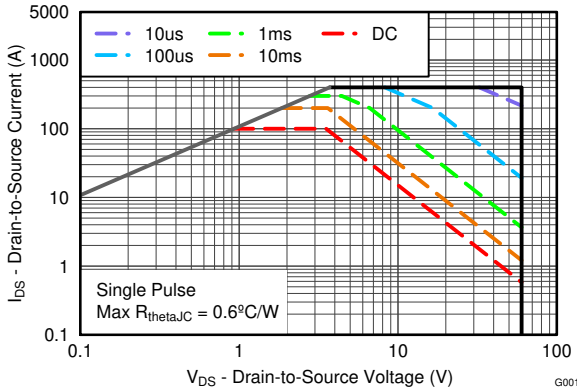


图 3-10. Maximum Safe Operating Area

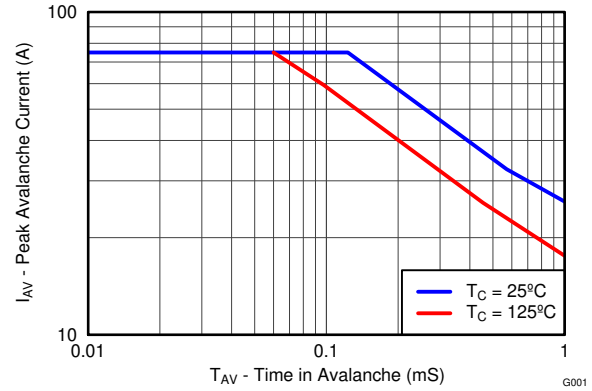


图 3-11. Single Pulse Unclamped Inductive Switching

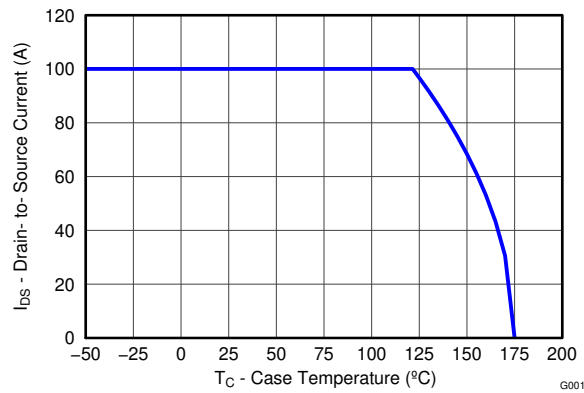


图 3-12. Maximum Drain Current vs Temperature

## 4 Device and Documentation Support

### 4.1 第三方产品免责声明

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### 4.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

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TI E2E™ is a trademark of Texas Instruments.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 4.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 5 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from Revision B (August 2012) to Revision C (March 2024) Page

- 更新了整个文档中的表格、图和交叉参考的编号格式..... 1

### Changes from Revision A (October 2012) to Revision B (July 2014) Page

- 将  $T_C = 100^\circ\text{C}$  时的  $I_D$  增加至 116A..... 1
- 将  $I_{DM}$  增加至 400A..... 1
- 将最大工作结温和贮存温度增加至  $175^\circ\text{C}$ ..... 1
- Updated [图 3-1](#) from a normalized  $R_{\theta JA}$  to an  $R_{\theta JC}$  curve..... 4
- Updated [图 3-6](#) to extend to  $175^\circ\text{C}$  ..... 4
- Updated [图 3-8](#) to extend to  $175^\circ\text{C}$  ..... 4
- Updated the SOA in [图 3-10](#) ..... 4
- Updated [图 3-12](#) to extend to  $175^\circ\text{C}$  ..... 4

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**Changes from Revision \* (August 2012) to Revision A (October 2012)**

**Page**

- Changed the Transconductance TYP value From: 146S To: 187S.....3
  - Changed  $R_{\theta JA}$  From: MAX = 62°C/W To: MAX = 65°C/W.....3
  - Changed  3-2 .....4
-



## 6 Mechanical Data

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18532KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD18532KCS	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD18532KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD18532KCS	KCS	TO-220	3	50	532	34.1	700	9.6

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