

CSD18542KTT 60V N 沟道 NexFET™ 功率 MOSFET

1 特性

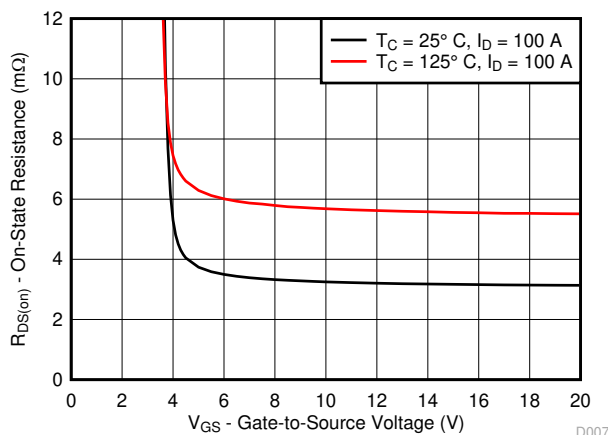
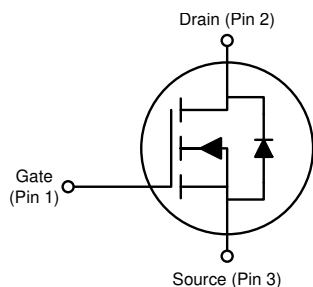
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 逻辑电平
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- D²PAK 塑料封装

2 应用

- 直流/直流转换
- 次级侧同步整流器
- 电机控制

3 说明

这款 60V、3.3mΩ、D²PAK (TO-263) NexFET™ 功率 MOSFET 旨在用于更大幅度地降低功率转换应用中的损耗。



$R_{DS(on)}$ 与 V_{GS} 之间的关系

产品概要

| $T_A = 25^\circ C$ | | 典型值 | | 单位 |
|--------------------|--------------|-----------------|-----|----|
| V_{DS} | 漏源电压 | 60 | | V |
| Q_g | 栅极电荷总量 (10V) | 44 | | nC |
| Q_{gd} | 栅极电荷 (栅极到漏极) | 6.9 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS} = 4.5V$ | 4.0 | mΩ |
| | | $V_{GS} = 10V$ | 3.3 | |
| $V_{GS(th)}$ | 阈值电压 | 1.8 | | V |

器件信息 (1)

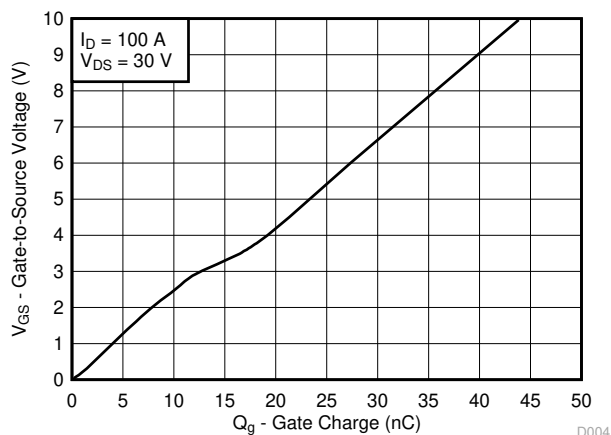
| 器件 | 数量 | 介质 | 封装 | 运输 |
|--------------|-----|---------|-------------------------|------|
| CSD18542KTT | 500 | 13 英寸卷带 | D ² PAK 塑料封装 | 卷带包装 |
| CSD18542KTTT | 50 | | | |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

绝对最大额定值

| $T_A = 25^\circ C$ | | 值 | 单位 |
|--------------------|---|-----------|----|
| V_{DS} | 漏源电压 | 60 | V |
| V_{GS} | 栅源电压 | ±20 | V |
| I_D | 持续漏极电流 (受封装限制) | 200 | A |
| | 持续漏极电流 (受器件限制), $T_C = 25^\circ C$ 时测得 | 170 | |
| | 持续漏极电流 (受器件限制), $T_C = 100^\circ C$ 时测得 | 120 | |
| I_{DM} | 脉冲漏极电流 ⁽¹⁾ | 400 | A |
| P_D | 功率耗散 | 250 | W |
| T_J , T_{stg} | 工作结温, 贮存温度 | -55 至 175 | °C |
| E_{AS} | 雪崩能量, 单脉冲 $I_D = 75A, L = 0.1mH, R_G = 25\Omega$ | 281 | mJ |

(1) 最大 $R_{\theta JC} = 0.6^\circ C/W$, 脉冲持续时间 $\leq 100 \mu s$, 占空比 $\leq 1\%$ 。



栅极电荷



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4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------------------|----------------------------------|---|-----------------------------|------|------|------------|----|
| STATIC CHARACTERISTICS | | | | | | | |
| BV_{DSS} | Drain-to-source voltage | $V_{GS} = 0V, I_D = 250 \mu A$ | 60 | | | V | |
| I_{DSS} | Drain-to-source leakage current | $V_{GS} = 0V, V_{DS} = 48V$ | | | 1 | μA | |
| I_{GSS} | Gate-to-source leakage current | $V_{DS} = 0V, V_{GS} = 20V$ | | | 100 | nA | |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS} = V_{GS}, I_D = 250 \mu A$ | 1.5 | 1.8 | 2.2 | V | |
| $R_{DS(on)}$ | Drain-to-source on resistance | $V_{GS} = 4.5V, I_D = 100A$ | | 4.0 | 5.1 | m Ω | |
| | | $V_{GS} = 10V, I_D = 100A$ | | 3.3 | 4.0 | | |
| g_{fs} | Transconductance | $V_{DS} = 6V, I_D = 100A$ | | 198 | | S | |
| DYNAMIC CHARACTERISTICS | | | | | | | |
| C_{iss} | Input capacitance | $V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$ | | 3900 | 5070 | pF | |
| C_{oss} | Output capacitance | | | 570 | 740 | pF | |
| C_{riss} | Reverse transfer capacitance | | | 11 | 14 | pF | |
| R_G | Series gate resistance | | | 1.3 | 2.6 | Ω | |
| Q_g | Gate charge total (4.5V) | $V_{DS} = 30V, I_D = 100A$ | | 21 | 27 | nC | |
| Q_g | Gate charge total (10V) | | | 44 | 57 | nC | |
| Q_{gd} | Gate charge gate-to-drain | | | 6.9 | | nC | |
| Q_{gs} | Gate charge gate-to-source | | | 10 | | nC | |
| $Q_{g(th)}$ | Gate charge at V_{th} | | | 7.3 | | nC | |
| Q_{oss} | Output charge | | $V_{DS} = 30V, V_{GS} = 0V$ | | 63 | | nC |
| $t_{d(on)}$ | Turnon delay time | | | | 6 | | ns |
| t_r | Rise time | $V_{DS} = 30V, V_{GS} = 10V,$ $I_{DS} = 100A, R_G = 0\Omega$ | | 5 | | ns | |
| $t_{d(off)}$ | Turnoff delay time | | | 18 | | ns | |
| t_f | Fall time | | | 21 | | ns | |
| DIODE CHARACTERISTICS | | | | | | | |
| V_{SD} | Diode forward voltage | $I_{SD} = 100A, V_{GS} = 0V$ | | 0.9 | 1.0 | V | |
| Q_{rr} | Reverse recovery charge | $V_{DS} = 30V, I_F = 100A,$ $di/dt = 300A/\mu s$ | | 148 | | nC | |
| t_{rr} | Reverse recovery time | | | 53 | | ns | |

4.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|-----------------|--|-----|-----|-----|--------------------|
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 0.6 | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | | 62 | $^\circ\text{C/W}$ |

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

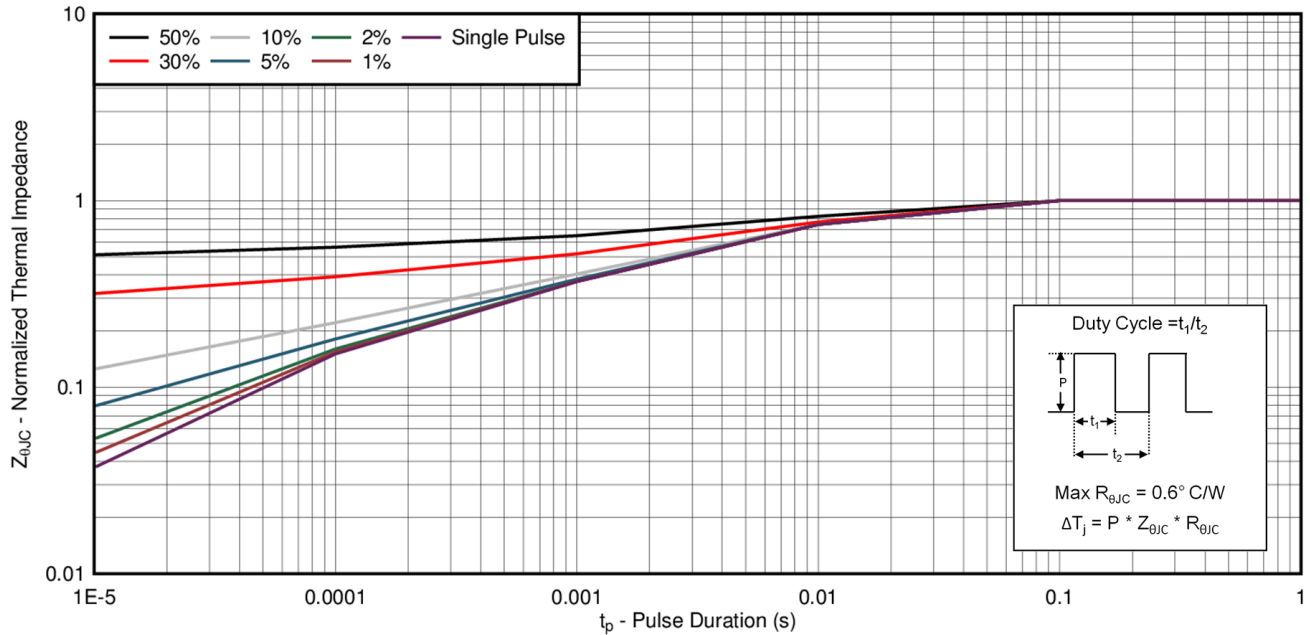


图 4-1. Transient Thermal Impedance

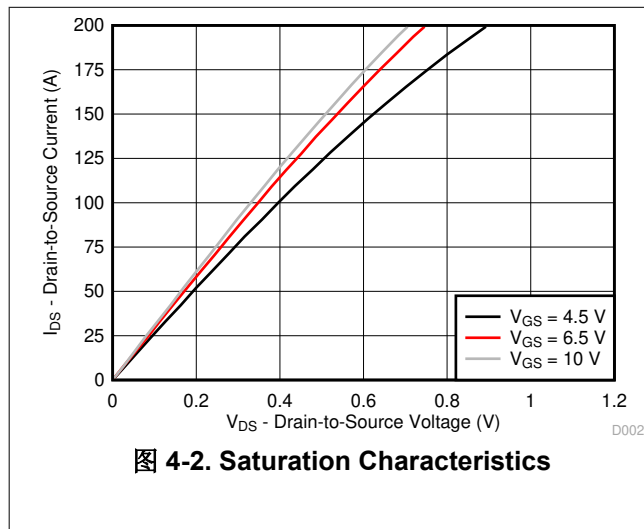


图 4-2. Saturation Characteristics

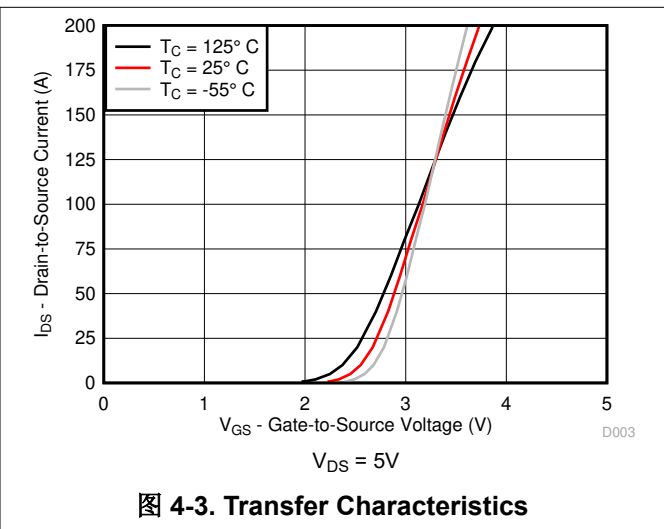


图 4-3. Transfer Characteristics

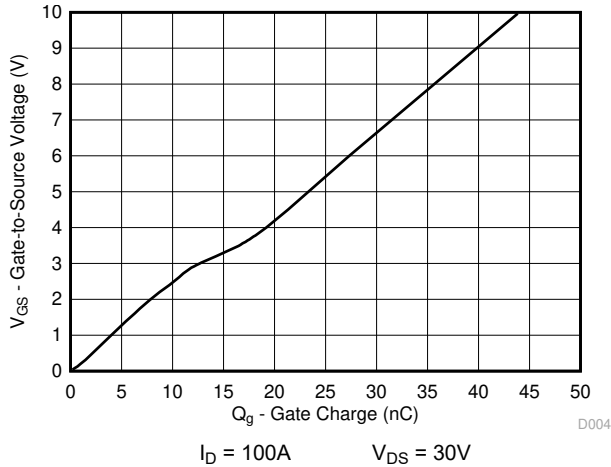


图 4-4. Gate Charge

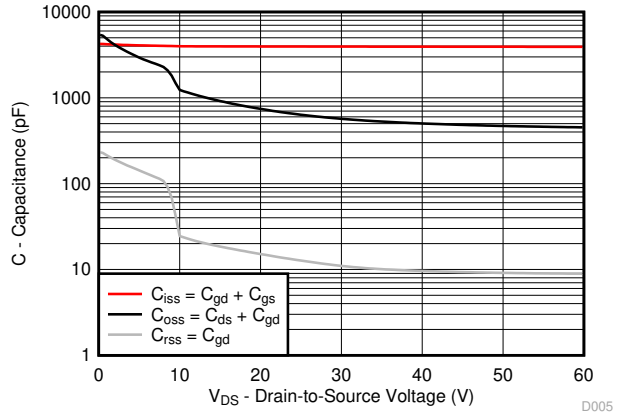


图 4-5. Capacitance

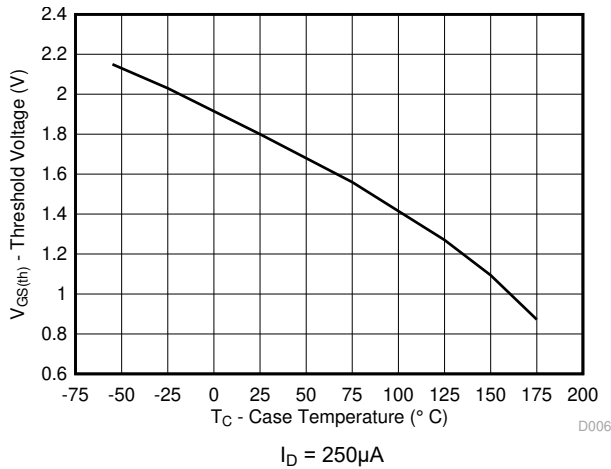


图 4-6. Threshold Voltage vs Temperature

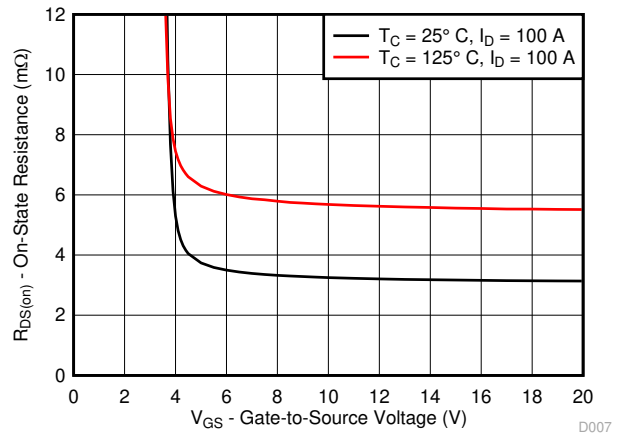


图 4-7. On-State Resistance vs Gate-to-Source Voltage

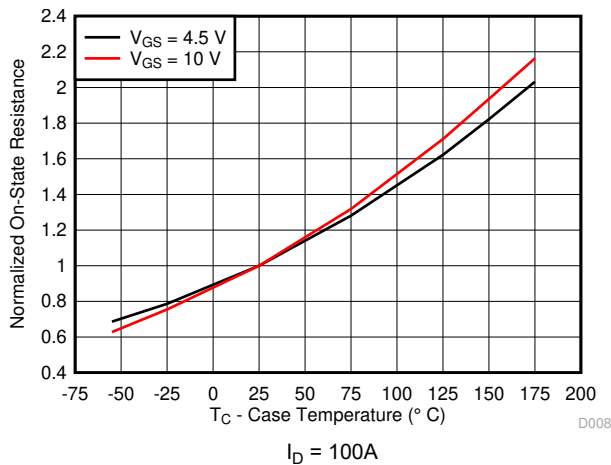


图 4-8. Normalized On-State Resistance vs Temperature

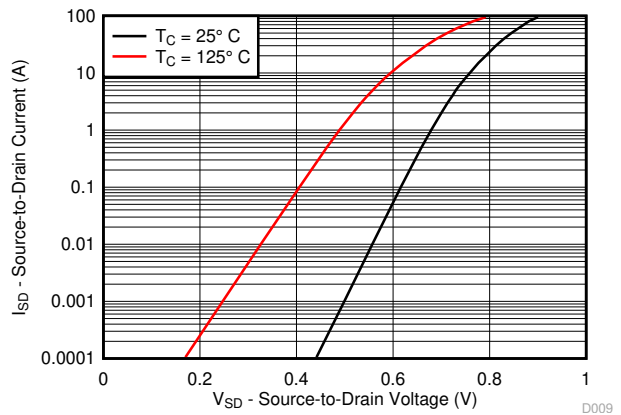


图 4-9. Typical Diode Forward Voltage

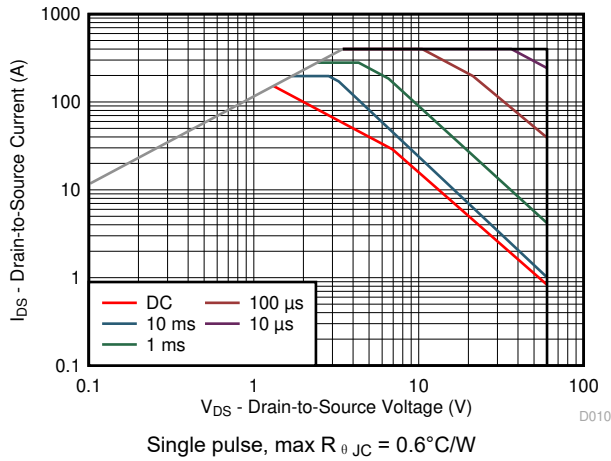


图 4-10. Maximum Safe Operating Area

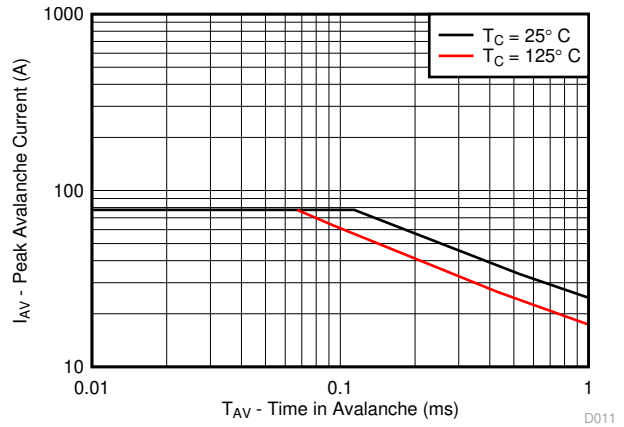


图 4-11. Single Pulse Unclamped Inductive Switching

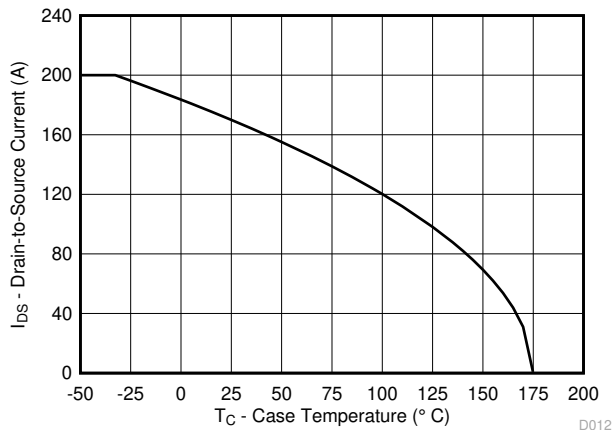


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

5.3 Trademarks

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5.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

Changes from Revision A (March 2017) to Revision B (June 2024) Page

- 更新了整个文档中的表格、图和交叉参考的编号格式..... **1**

Changes from Revision * (March 2016) to Revision A (March 2017) Page

- Changed the values for C_{OSS} , Q_{gs} , t_r , $t_{d(off)}$, t_f , Q_{rr} , and t_{rr} in the *Electrical Characteristics* table..... **3**

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|------------------|-----------------|------|-------------|------------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CSD18542KTT | ACTIVE | DDPAK/ TO-263 | KTT | 2 | 500 | RoHS-Exempt & Green | SN | Level-2-260C-1 YEAR | -55 to 175 | CSD18542KTT | Samples |
| CSD18542KTTT | ACTIVE | DDPAK/ TO-263 | KTT | 2 | 50 | RoHS-Exempt & Green | SN | Level-2-260C-1 YEAR | -55 to 175 | CSD18542KTT | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

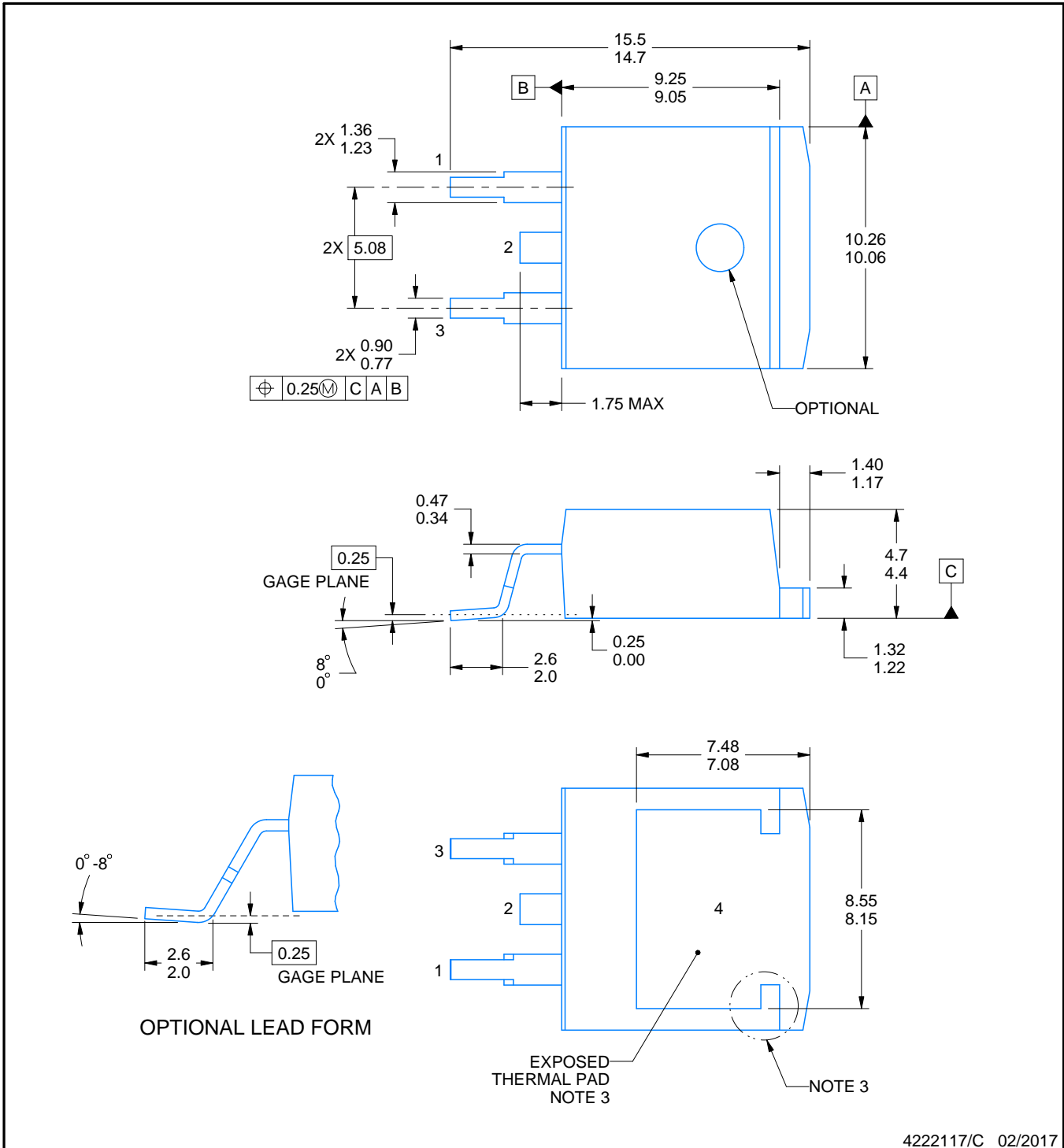

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD18542KTT | DDPAK/TO-263 | KTT | 2 | 500 | 330.0 | 24.4 | 10.8 | 16.3 | 5.11 | 16.0 | 24.0 | Q2 |
| CSD18542KTTT | DDPAK/TO-263 | KTT | 2 | 50 | 330.0 | 24.4 | 10.8 | 16.3 | 5.11 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CSD18542KTT | DDPAK/TO-263 | KTT | 2 | 500 | 340.0 | 340.0 | 38.0 |
| CSD18542KTTT | DDPAK/TO-263 | KTT | 2 | 50 | 340.0 | 340.0 | 38.0 |



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NOTES:

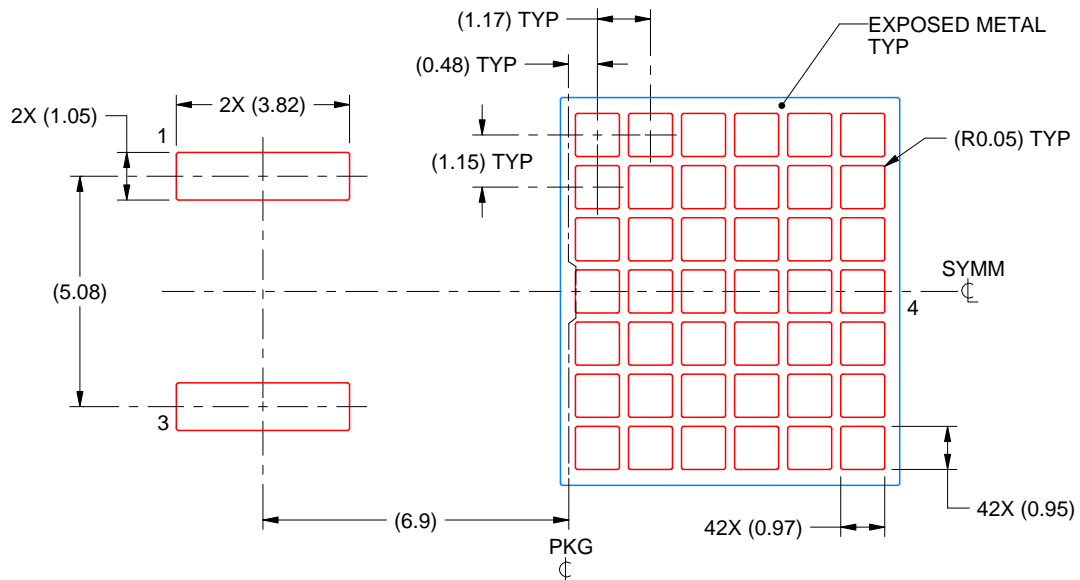
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263.

EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TO-263



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/C 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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