CSD19505KTT 80V N 沟道 NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

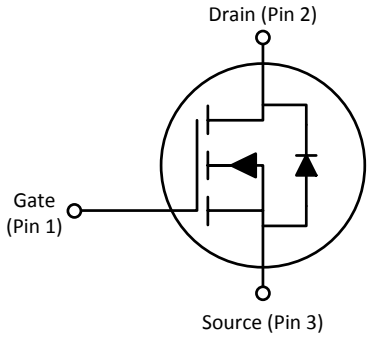
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- D^2PAK 塑料封装

2 应用

- 次级侧同步整流器
- 电机控制

3 说明

这款 80V、2.6mΩ、D^2PAK (TO-263) NexFET™功率 MOSFET 被设计成在功率转换应用中大大降低 损耗。



产品概要

T_A=25°C		典型值		单位
V_{DS}	漏源电压	80		V
Q_g	栅极电荷总量 (10V)	76		nC
Q_{gd}	栅极电荷 栅极到漏极	11		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	2.9	mΩ
		V_{GS} = 10V	2.6	mΩ
$V_{GS(th)}$	阈值电压	2.6		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD19505KTT	500	13 英寸卷带	D^2PAK 塑料封装	卷带封装
CSD19505KTTT	50			

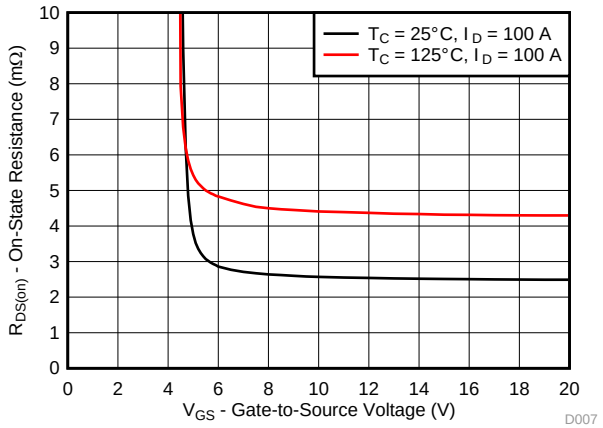
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

绝对最大额定值

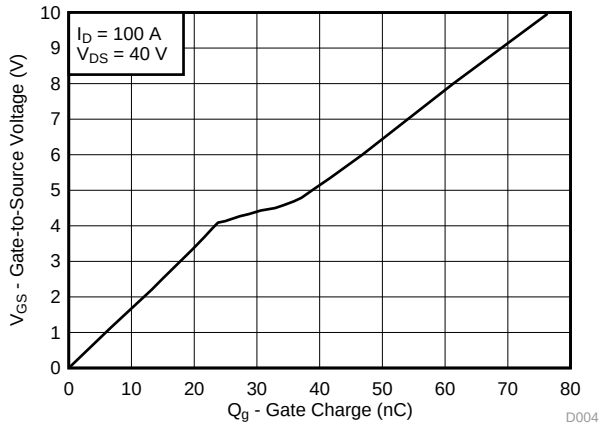
T_A = 25°C		值	单位
V_{DS}	漏源电压	80	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	200	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	212	A
	持续漏极电流（受芯片限制），T_C = 100°C 时测得	150	A
I_{DM}	脉冲漏极电流(1)	400	A
P_D	功率耗散	300	W
T_J, T_{stg}	工作结温，储存温度	-55 至 175	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 101A，L = 0.1mH，R_G = 25Ω	510	mJ

(1) 最大 $R_{\theta JC}$ = 0.5°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

日期	修订版本	注释
2016 年 3 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	80			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 64 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.2	2.6	3.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V, I_D = 100 A		2.9	3.8	mΩ
		V_{GS} = 10 V, I_D = 100 A		2.6	3.1	mΩ
g_{fs}	Transconductance	V_{DS} = 8 V, I_D = 100 A		262		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		6090	7920	pF
C_{oss}	Output capacitance			1600	2080	pF
C_{rss}	Reverse transfer capacitance			26	34	pF
R_G	Series gate resistance			1.4	2.8	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 40 V, I_D = 100 A		76		nC
Q_{gd}	Gate charge gate-to-drain			11		nC
Q_{gs}	Gate charge gate-to-source			25		nC
$Q_{g(th)}$	Gate charge at V_{th}			15		nC
Q_{oss}	Output charge	V_{DS} = 40 V, V_{GS} = 0 V		214		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 40 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		11		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turn off delay time			22		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 40 V, I_F = 100 A, di/dt = 300 A/µs		400		nC
t_{rr}	Reverse recovery time			88		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	°C/W

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

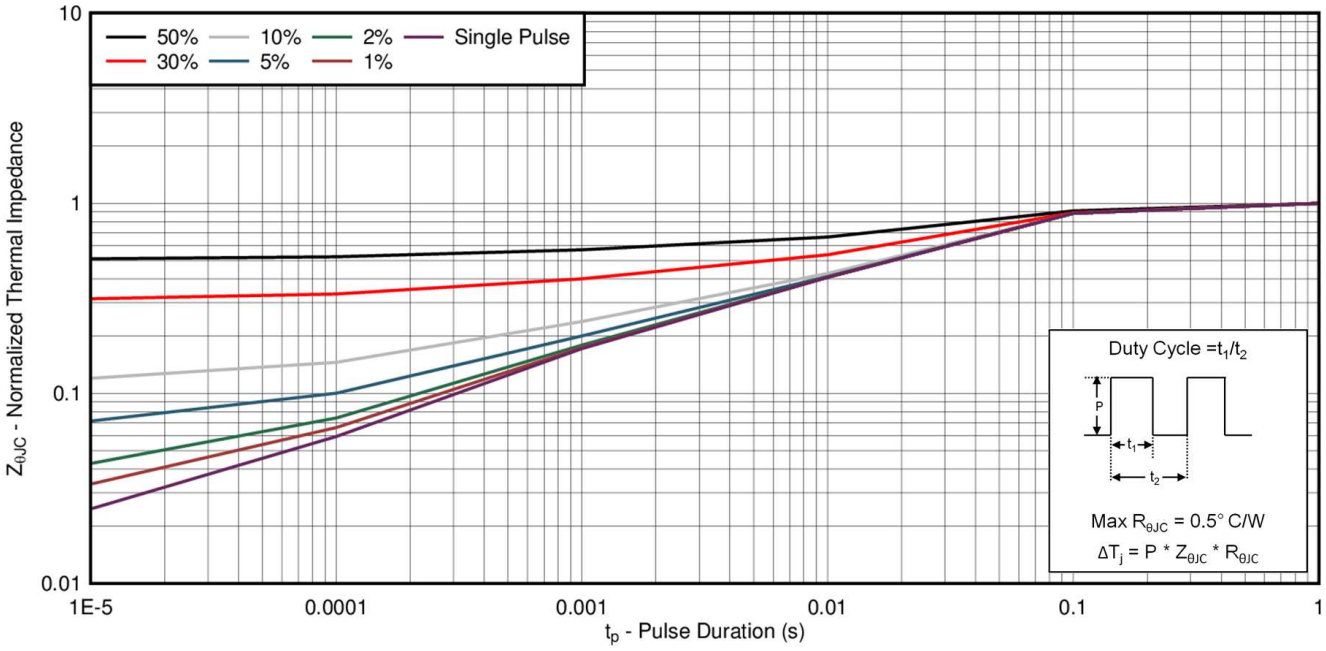


Figure 1. Transient Thermal Impedance

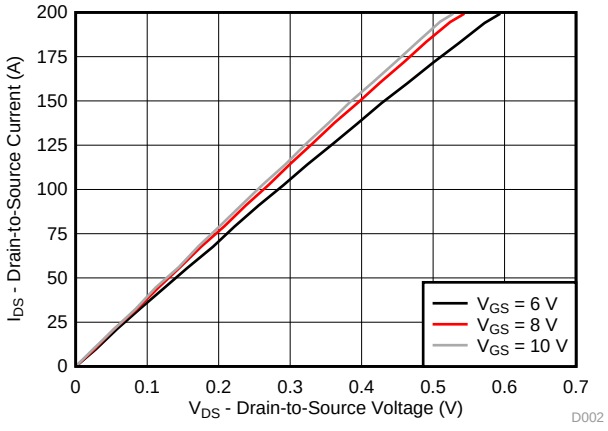


Figure 2. Saturation Characteristics

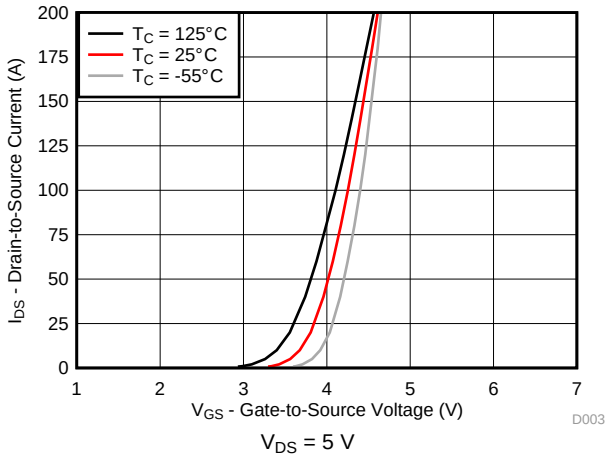


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

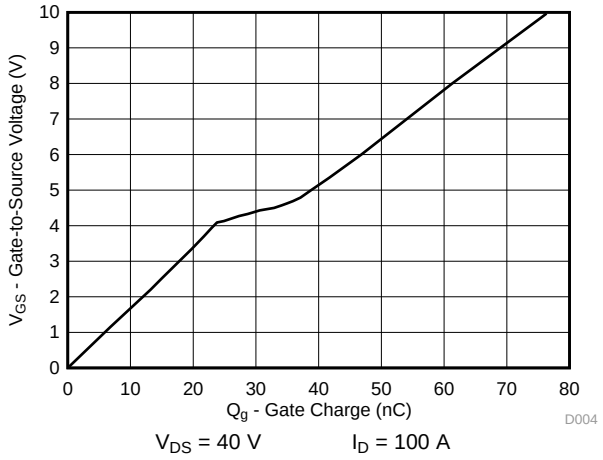


Figure 4. Gate Charge

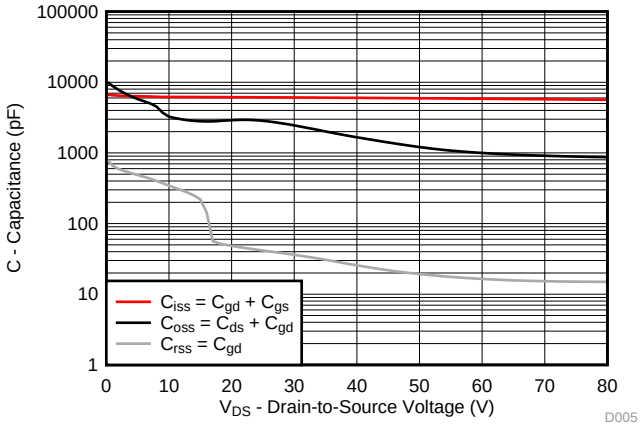


Figure 5. Capacitance

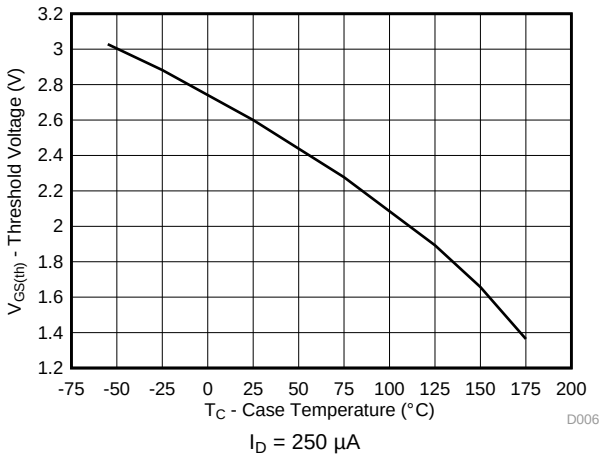


Figure 6. Threshold Voltage vs Temperature

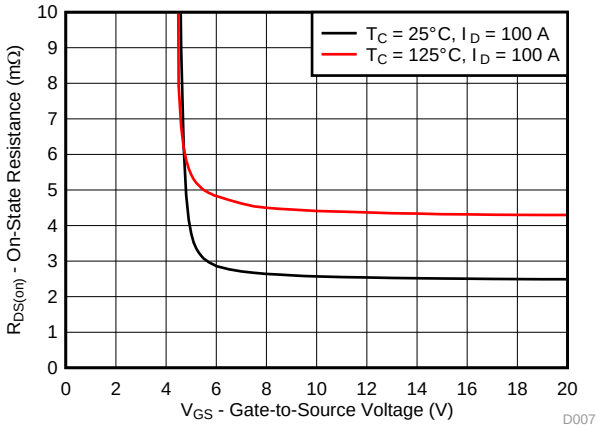


Figure 7. On-State Resistance vs Gate-to-Source Voltage

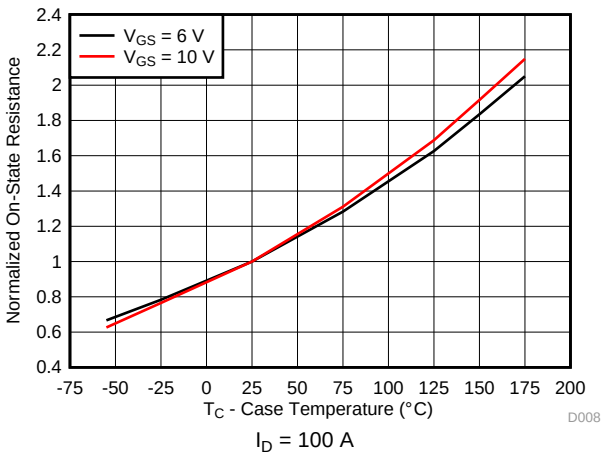


Figure 8. Normalized On-State Resistance vs Temperature

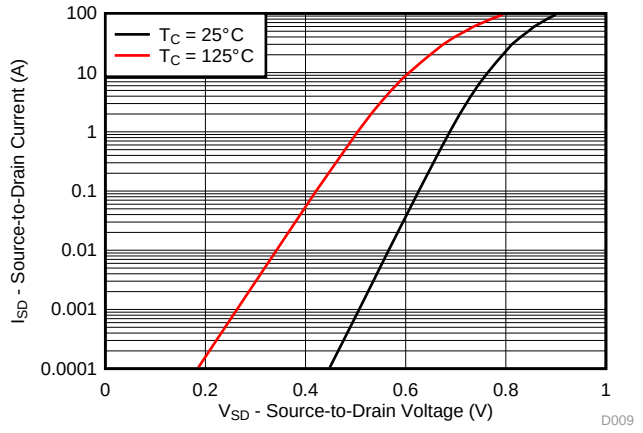


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

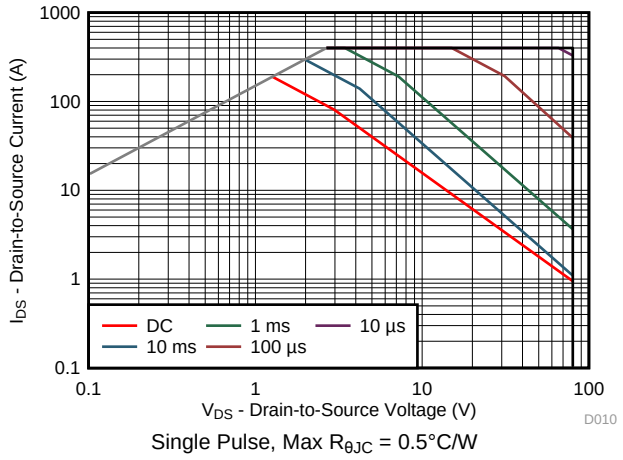


Figure 10. Maximum Safe Operating Area

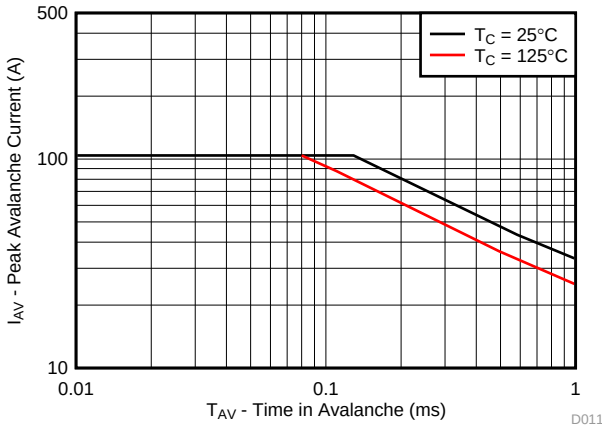


Figure 11. Single Pulse Unclamped Inductive Switching

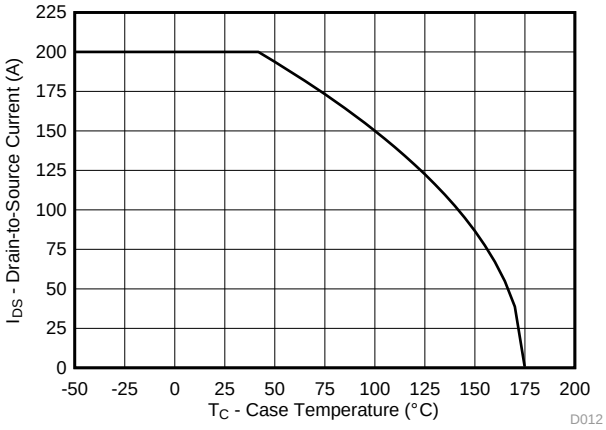


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 商标

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6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

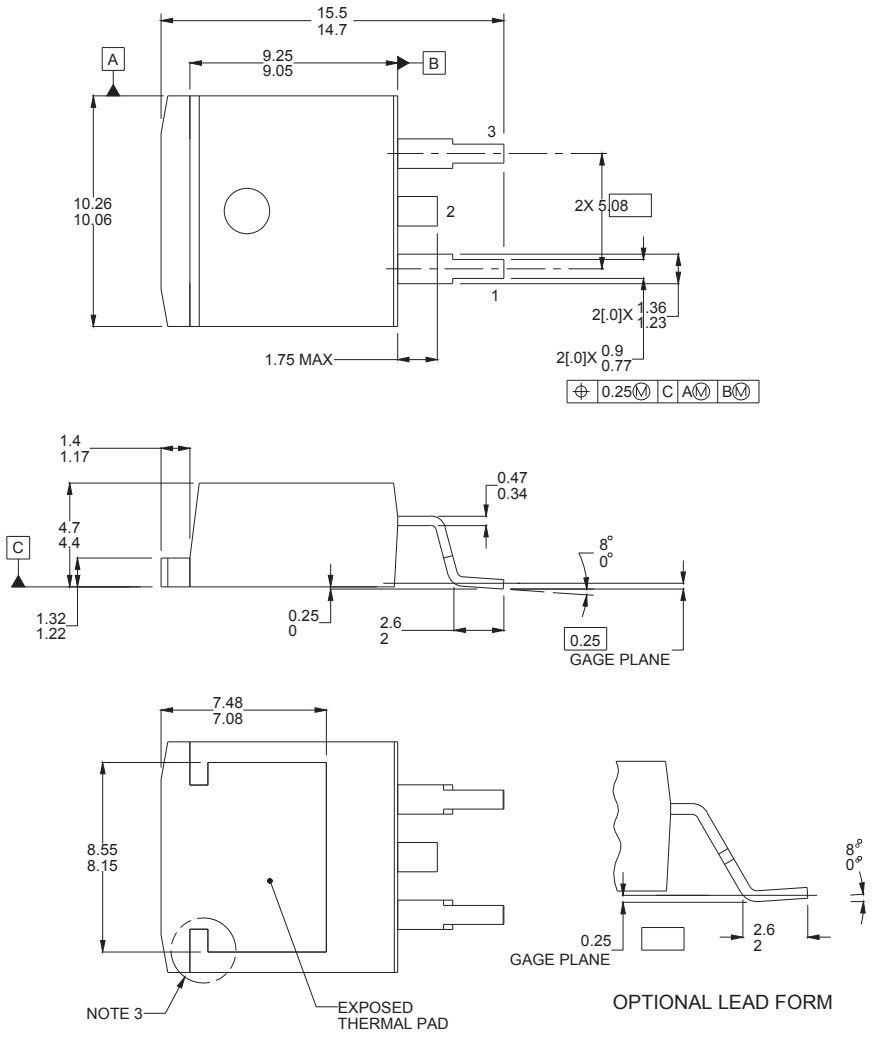
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 KTT 封装尺寸



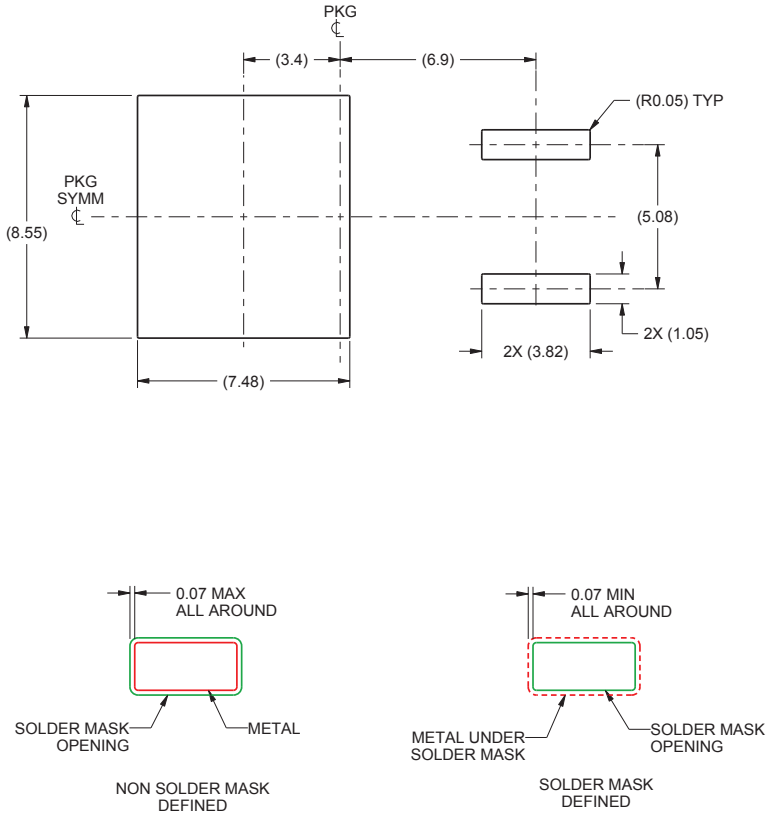
注：

1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和容限值遵循 ASME Y14.5M。
2. 本图纸如有变更，恕不通知。
3. 来自 不同装配现场的产品可能不具备某些特性，形状也可能有所不同。

引脚配置

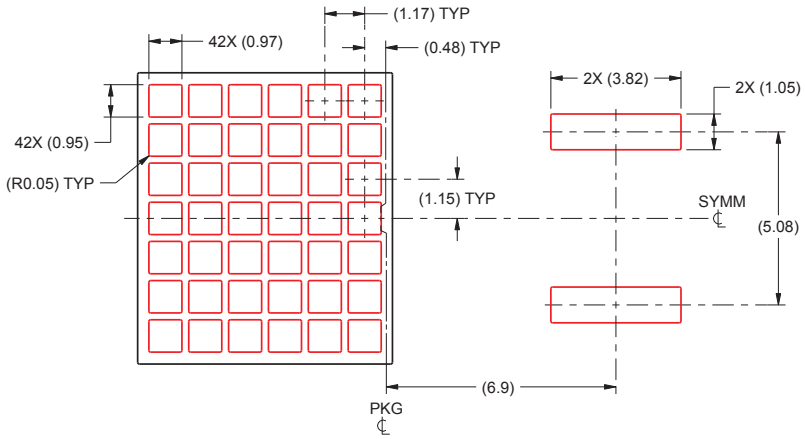
位置	名称
引脚 1	栅极
引脚 2 / 标签	漏极
引脚 3	源极

7.2 推荐的 PCB 布局



要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》文献编号：SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板开口（模板厚度为 0.125mm）



注：

1. 此封装设计用于焊接到电路板的散热焊盘上。更多信息，请参见应用手册，《*PowerPAD 耐热增强型封装*》（文献编号：SLMA002）和《*PowerPAD 速成*》（文献编号：SLMA004）。
2. 具有漏斗形壁和圆角的激光切割窗孔将提供更佳的焊锡膏脱离。IPC-7525 可能提供其他替代性设计建议。
3. 在电路板装配现场，对于模板设计可能有不同的建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19505KTT	ACTIVE	DDPAK/ TO-263	KTT	2	500	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19505KTT	Samples
CSD19505KTTT	ACTIVE	DDPAK/ TO-263	KTT	2	50	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19505KTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

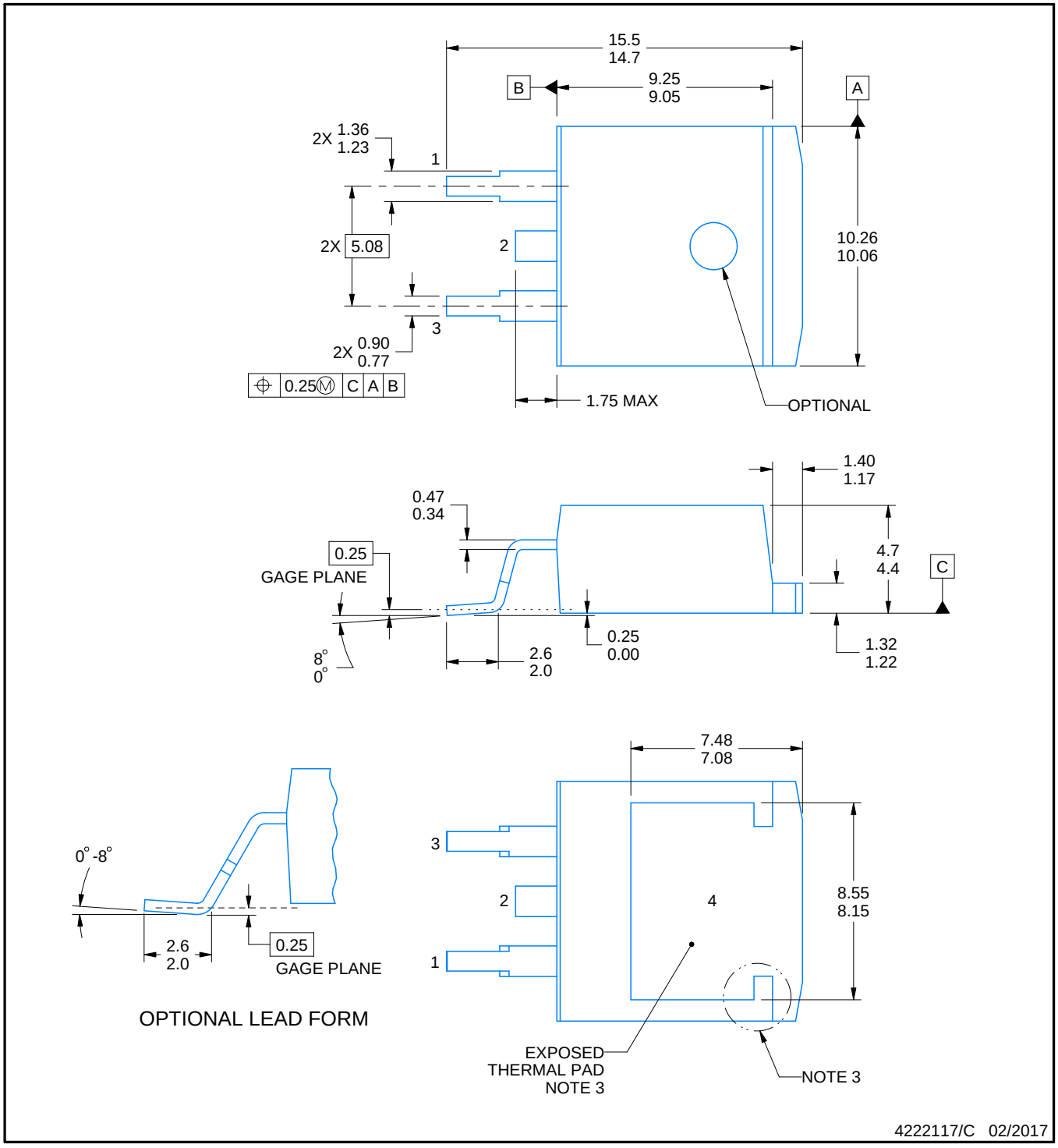
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

KTT0002A

PACKAGE OUTLINE

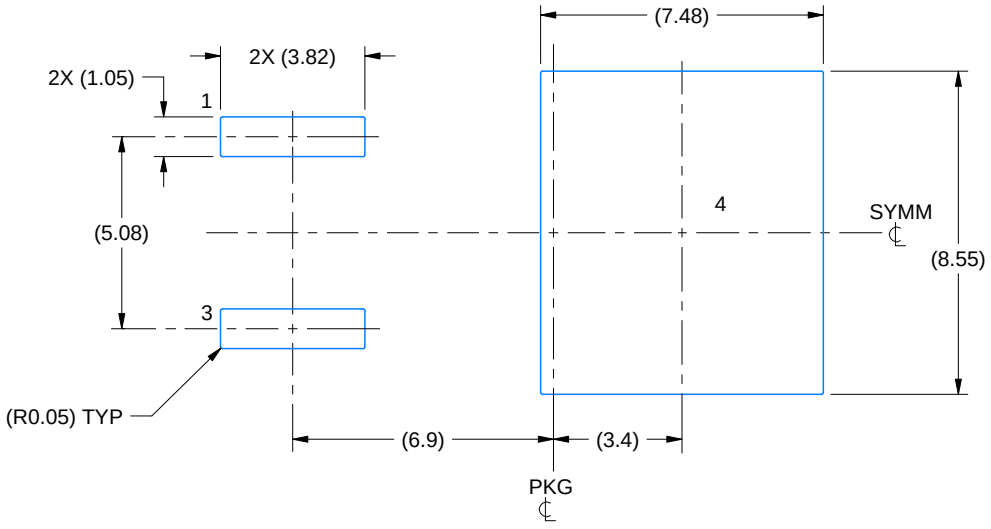
TO-263 - 4.7 mm max height

TO-263

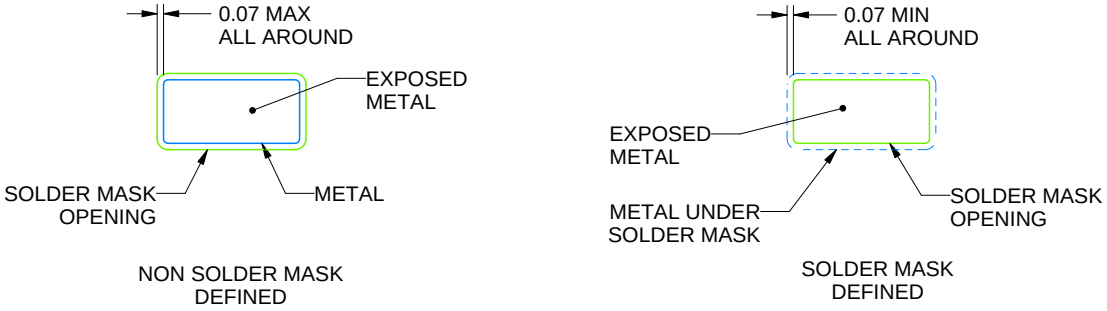


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

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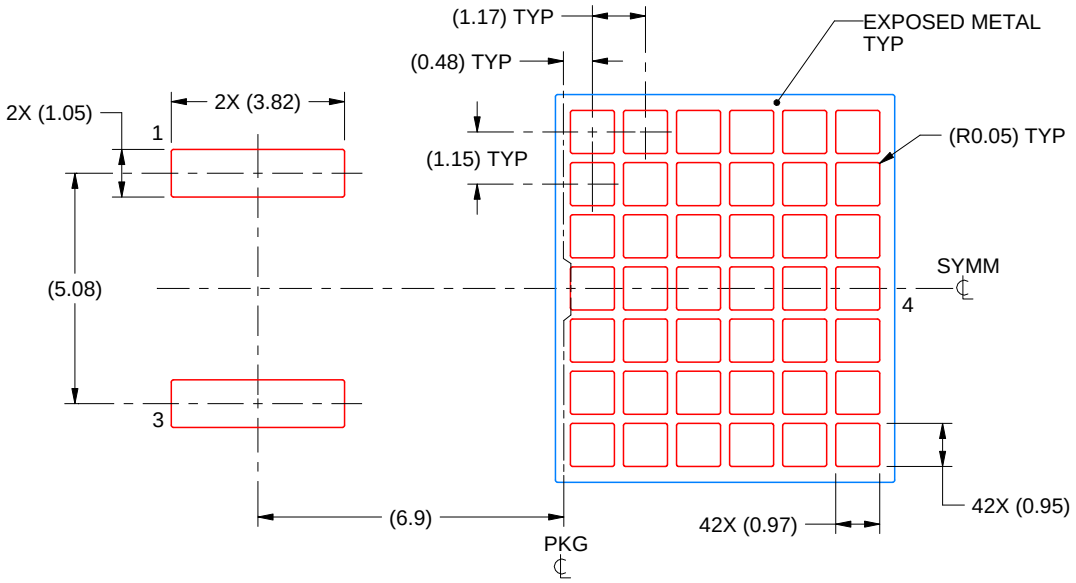
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/C 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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