

# CSD19534KCS 100V N 沟道 NexFET™ 功率 MOSFET

## 1 特性

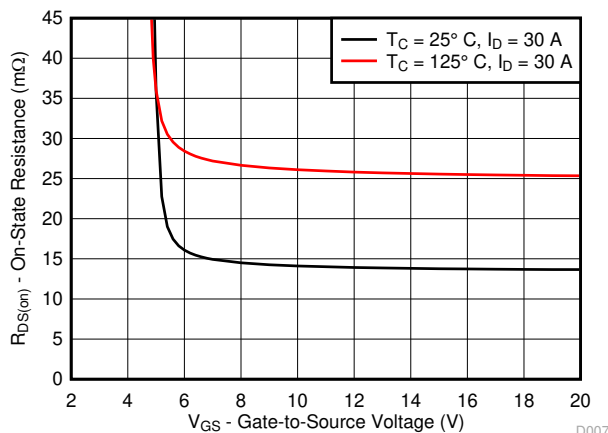
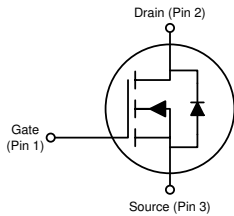
- 超低  $Q_g$  和  $Q_{gd}$
- 低热阻
- 具有雪崩能力
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- TO-220 塑料封装

## 2 应用

- 次级侧同步整流器
- 电机控制

## 3 说明

这款 100V、13.7mΩ、TO-220 NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



$R_{DS(on)}$  与  $V_{GS}$  之间的关系

## 产品概要

$T_A = 25^\circ C$		典型值		单位
$V_{DS}$	漏源电压	100		V
$Q_g$	栅极电荷总量 (10V)	16.4		nC
$Q_{gd}$	栅极电荷 (栅极到漏极)	3.3		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 6V$	16.3	mΩ
		$V_{GS} = 10V$	13.7	mΩ
$V_{GS(th)}$	阈值电压	2.8		V

## 订购信息 (1)

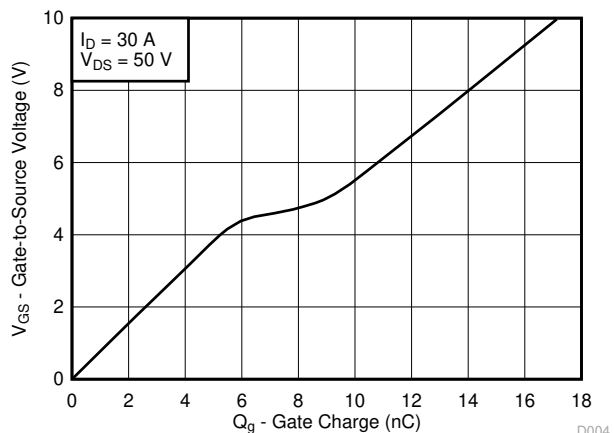
器件	封装	介质	数量	运输
CSD19534KCS	TO-220 塑料封装	管装	50	管装

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

## 绝对最大额定值

$T_A = 25^\circ C$		值	单位
$V_{DS}$	漏源电压	100	V
$V_{GS}$	栅源电压	±20	V
$I_D$	持续漏极电流 (受封装限制)	100	A
	持续漏极电流 (受器件限制), $T_C = 25^\circ C$ 时测得	54	
	持续漏极电流 (受器件限制), $T_C = 100^\circ C$ 时测得	38	
$I_{DM}$	脉冲漏极电流 (1)	138	A
$P_D$	功率耗散	118	W
$T_J$ 、 $T_{stg}$	工作结温和贮存温度范围	-55 至 175	$^\circ C$
$E_{AS}$	雪崩能量, 单脉冲 $I_D = 33A, L = 0.1mH, R_G = 25\Omega$	54	mJ

(1) 最大  $R_{\theta JC} = 1.3^\circ C/W$ , 脉冲持续时间  $\leq 100 \mu s$ , 占空比  $\leq 1\%$



栅极电荷



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## 4 Specifications

### 4.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	100			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 80V$			1	$\mu A$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.4	2.8	3.4	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6V, I_D = 30A$		16.3	20.0	m $\Omega$
		$V_{GS} = 10V, I_D = 30A$		13.7	16.5	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 10V, I_D = 30A$		80		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$		1290	1670	pF
$C_{oss}$	Output Capacitance			257	334	pF
$C_{riss}$	Reverse Transfer Capacitance			5.7	7.4	pF
$R_G$	Series Gate Resistance			1.1	2.2	$\Omega$
$Q_g$	Gate Charge Total (10V)	$V_{DS} = 50V, I_D = 30A$		17.1	22.2	nC
$Q_{gd}$	Gate Charge Gate-to-Drain			3.2		nC
$Q_{gs}$	Gate Charge Gate-to-Source			5.1		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			3.3		nC
$Q_{oss}$	Output Charge	$V_{DS} = 50V, V_{GS} = 0V$		44		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 50V, V_{GS} = 10V,$ $I_{DS} = 30A, R_G = 0\Omega$		6		ns
$t_r$	Rise Time			2		ns
$t_{d(off)}$	Turn Off Delay Time			9		ns
$t_f$	Fall Time			1		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 30A, V_{GS} = 0V$		0.9	1.1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 50V, I_F = 30A,$ $di/dt = 300A/\mu s$		195		nC
$t_{rr}$	Reverse Recovery Time			72		ns

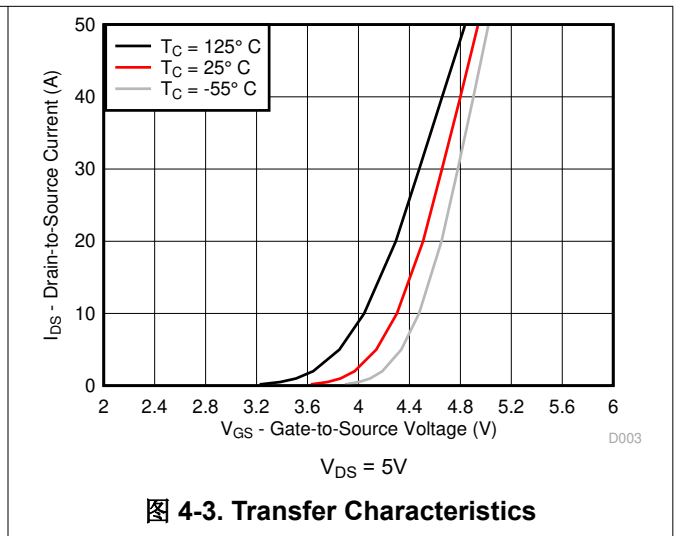
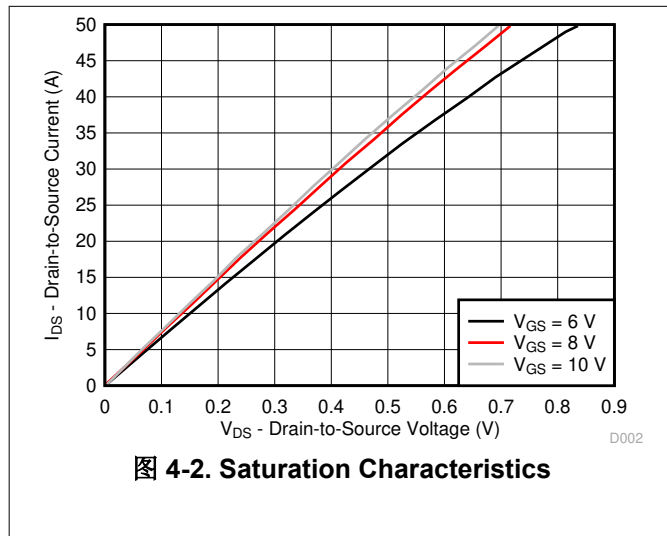
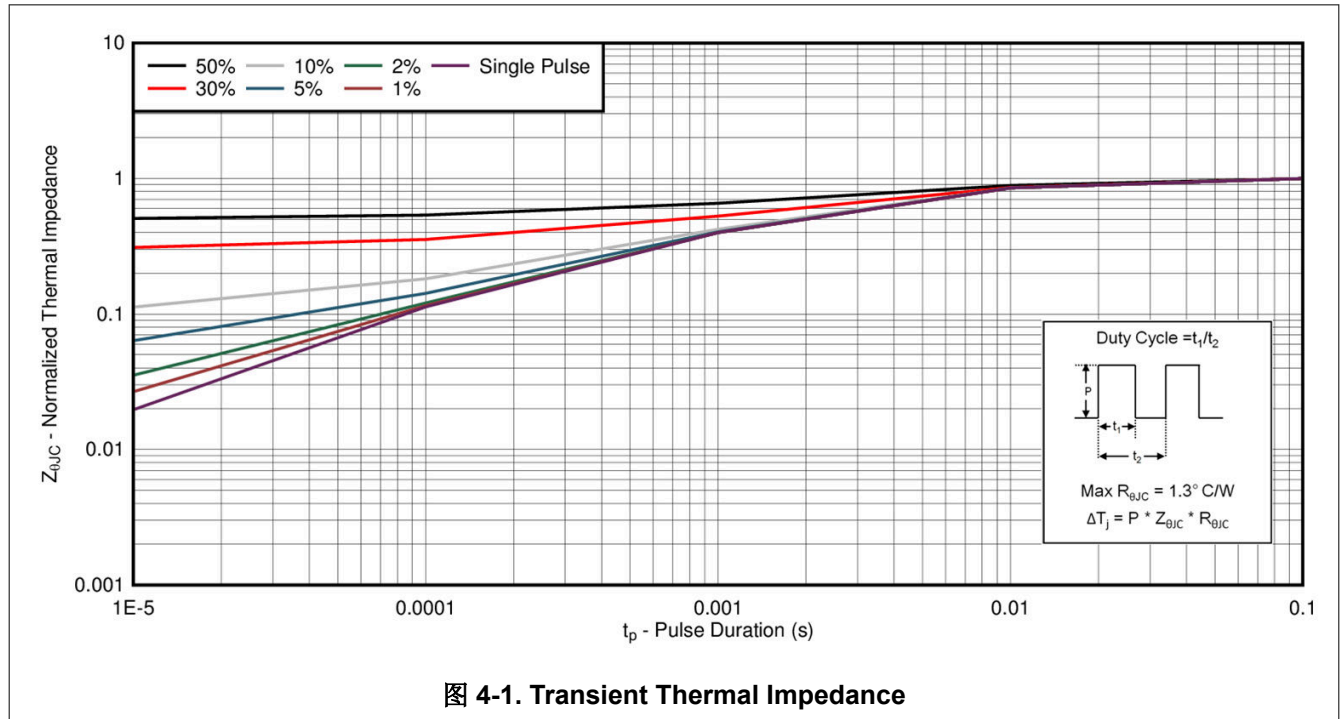
### 4.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			1.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

### 4.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



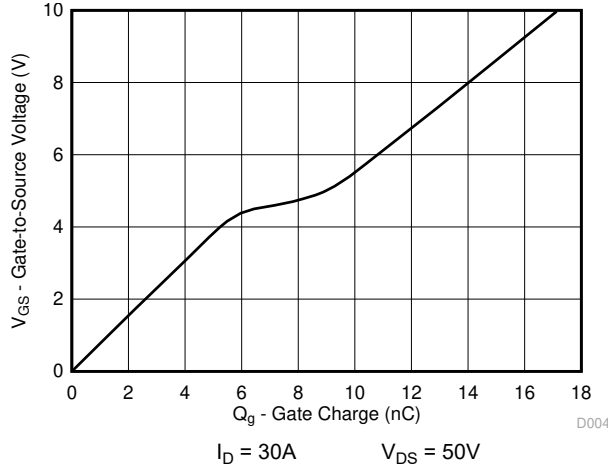


图 4-4. Gate Charge

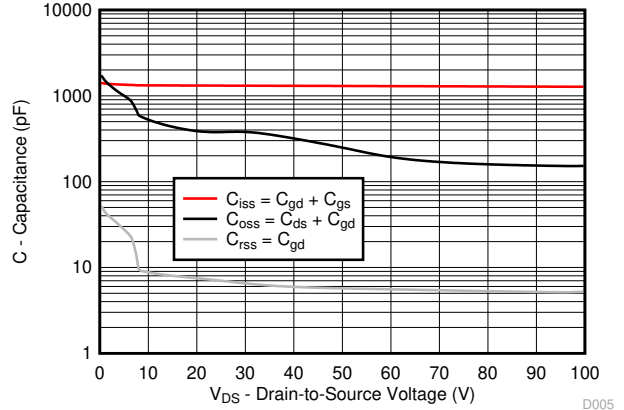


图 4-5. Capacitance

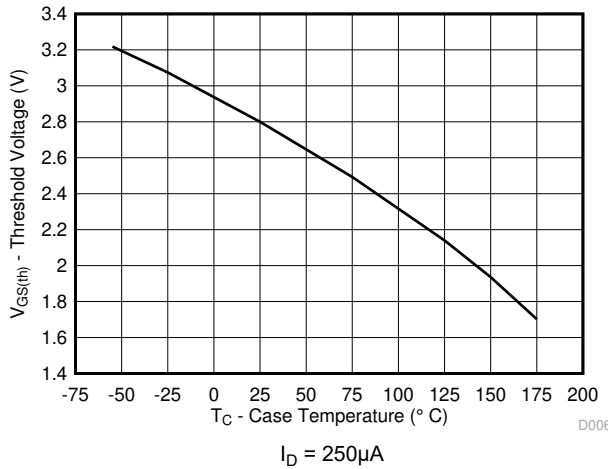


图 4-6. Threshold Voltage vs Temperature

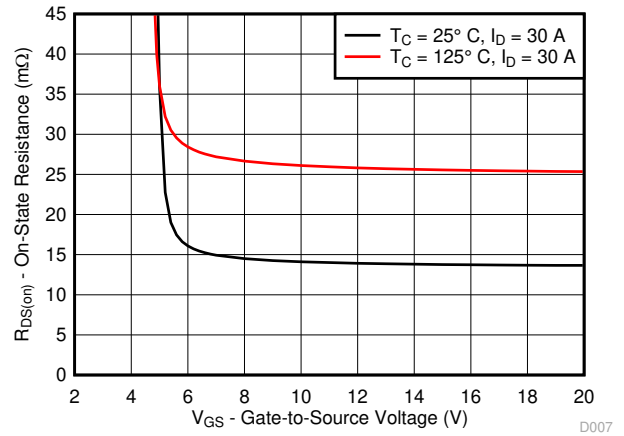


图 4-7. On-State Resistance vs Gate-to-Source Voltage

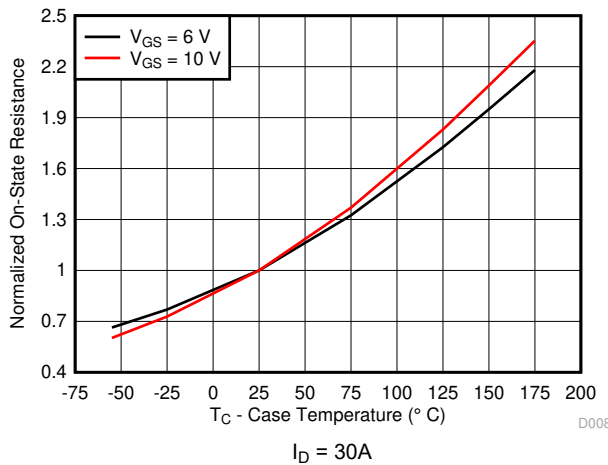


图 4-8. Normalized On-State Resistance vs Temperature

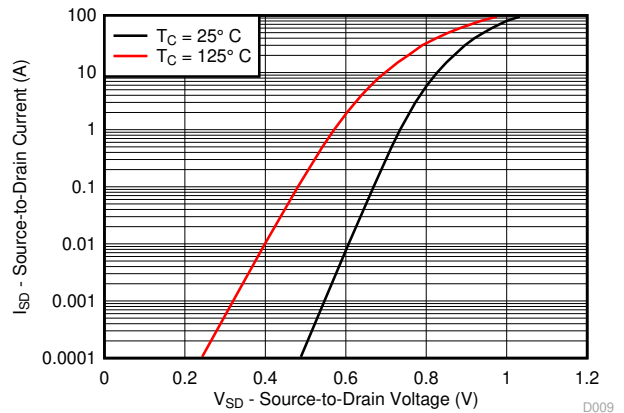


图 4-9. Typical Diode Forward Voltage

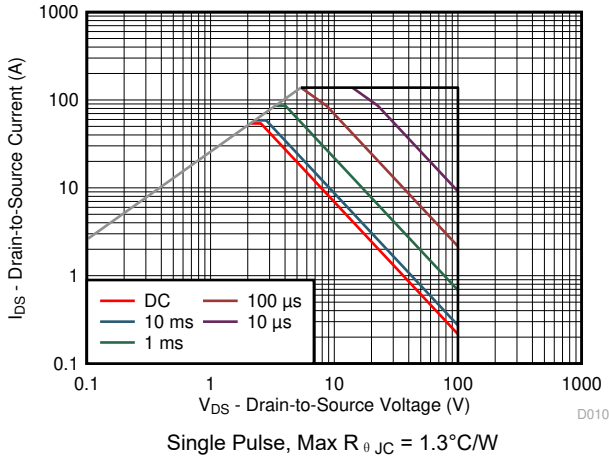


图 4-10. Maximum Safe Operating Area

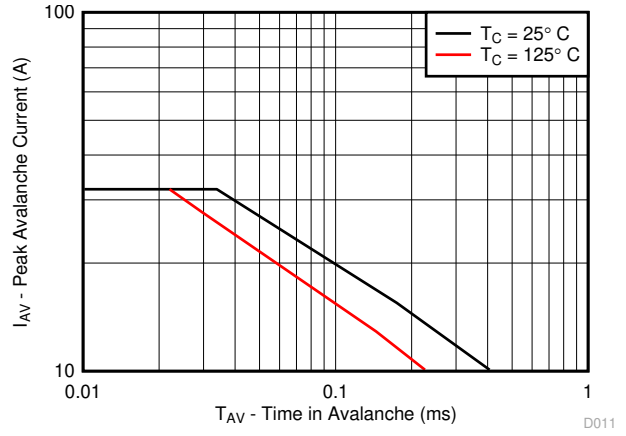


图 4-11. Single Pulse Unclamped Inductive Switching

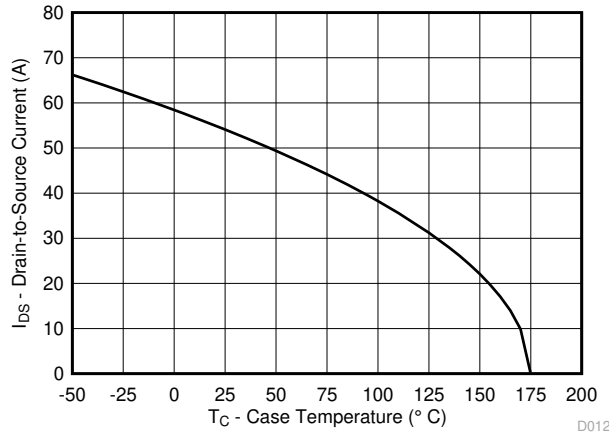


图 4-12. Maximum Drain Current vs Temperature

## 5 Device and Documentation Support

### 5.1 第三方产品免责声明

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### 5.2 Documentation Support

#### 5.2.1 Related Documentation

### 5.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 5.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 5.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 6 Revision History

### Changes from Revision \* (January 2015) to Revision A (December 2024)

**Page**

- |                                |   |
|--------------------------------|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式..... | 1 |
|--------------------------------|---|

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19534KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD19534KCS	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD19534KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD19534KCS	KCS	TO-220	3	50	532	34.1	700	9.6

# KCS0003B



# PACKAGE OUTLINE

TO-220 - 19.65 mm max height

TO-220



4222214/B 08/2018

### NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

# EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE:15X

4222214/B 08/2018

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