CSD22205L –8V P 沟道 NexFET™ 功率 MOSFET

1 特性

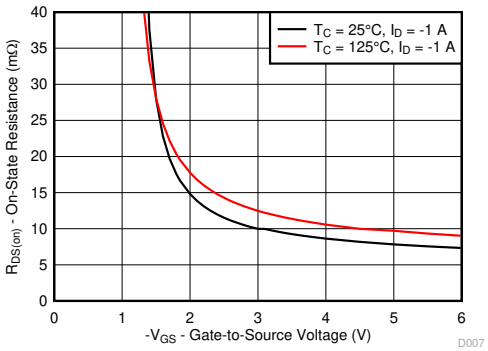
- 低电阻
- 1.2mm × 1.2mm 小尺寸封装
- 0.36mm 厚，超薄型
- 无铅
- 栅源电压钳位
- 栅极 ESD 保护
- 符合 RoHS
- 无卤素

2 应用

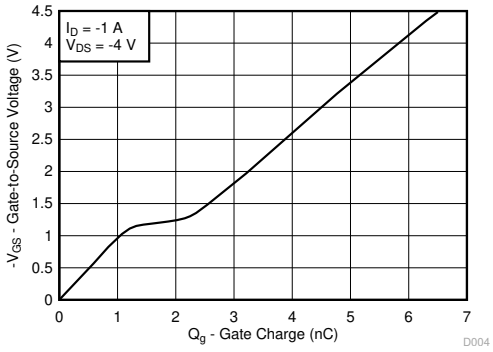
- 电池管理
- 负载开关
- 电池保护

3 说明

这款 -8V、8.2mΩ、1.2mm × 1.2mm 基板栅格阵列 (LGA) NexFET™ 器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内提供更低的导通电阻和栅极电荷。基板栅格阵列 (LGA) 封装是一种带有金属接触板（而非焊球）的器件芯片级封装。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



$R_{DS(on)}$ 与 V_{GS} 之间的关系

产品概要

T_A = 25°C		值		单位
V_{DS}	漏源电压	-8		V
Q_g	栅极电荷总量（-4.5V）	6.5		nC
Q_{gd}	栅极电荷（栅极到漏极）	1.0		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.5V	30	mΩ
		V_{GS} = -1.8V	20	
		V_{GS} = -2.5V	11.5	
		V_{GS} = -4.5V	8.2	
$V_{GS(th)}$	阈值电压	-0.7		V

器件信息(1)

器件	数量	介质	封装	配送
CSD22205L	3000	7 英寸卷带	1.20mm × 1.20mm 基板栅格阵列封装	卷带包装
CSD22205LT	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-8	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	-7.4	A
I_{DM}	脉冲漏极电流(2)	-71	A
P_D	功率耗散(1)	0.6	W
T_J、T_{stg}	工作结温，贮存温度	-55 至 150	°C

(1) $R_{\theta JA}$ = 225°C/W（覆铜面积最小时的值）。
(2) 脉宽 ≤ 100 μs，占空比 ≤ 1%。

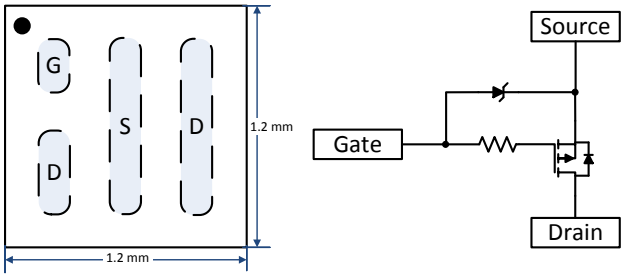


图 3-1. 顶视图和电路配置

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022)	Page
• 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm	1
• Changed CSD22205L Package Dimensions image height from 0.35 mm to 0.36 mm	8

Changes from Revision * (May 2017) to Revision A (August 2017)	Page
• Changed the units for timing parameters from µs : to ns (nanoseconds) in the 节 *5.1* table	3

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = –250 μA	–8			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –6.4 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.4	–0.7	–1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_D = –0.2 A		30		mΩ
		V_{GS} = –1.8 V, I_D = –1 A		20	40	
		V_{GS} = –2.5 V, I_D = –1 A		11.5	15.0	
		V_{GS} = –4.5 V, I_D = –1 A		8.2	9.9	
g_{fs}	Transconductance	V_{DS} = –0.8 V, I_D = –1 A		10.4		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = –4 V, f = 1 MHz		1070	1390	pF
C_{OSS}	Output capacitance			560	730	pF
C_{RSS}	Reverse transfer capacitance			190	250	pF
R_G	Series gate resistance			30		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –4 V, I_D = –1 A		6.5	8.5	nC
Q_{gd}	Gate charge gate-to-drain			1.0		nC
Q_{gs}	Gate charge gate-to-source			1.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.7		nC
Q_{OSS}	Output charge	V_{DS} = –4 V, V_{GS} = 0 V		4.1		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –4 V, V_{GS} = –4.5 V, I_D = –1 A , R_G = 0 Ω		30		ns
t_r	Rise time			14		ns
$t_{d(off)}$	Turnoff delay time			70		ns
t_f	Fall time			32		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = –1 A, V_{GS} = 0 V		–0.68	–1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= –4 V, I_F = –1 A, di/dt = 200 A/μs		16		nC
t_{rr}	Reverse recovery time			38		ns

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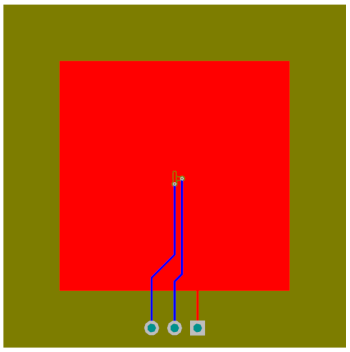
5.2 Thermal Information

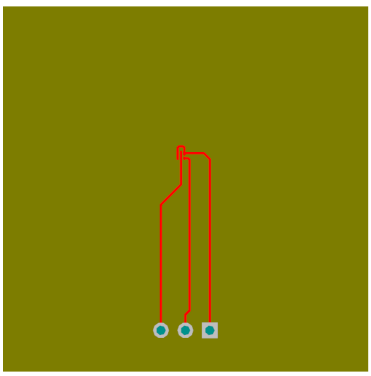
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)		75		°C/W
	Junction-to-ambient thermal resistance(1)		225		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Typ $R_{\theta JA}$ =75°C/W when mounted on 1 in^2 of 2-oz Cu.



Typ $R_{\theta JA}$ = 225°C/W when mounted on minimum pad area of 2-oz Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

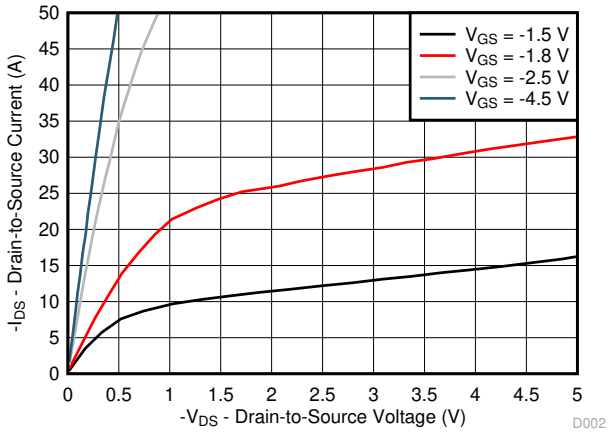
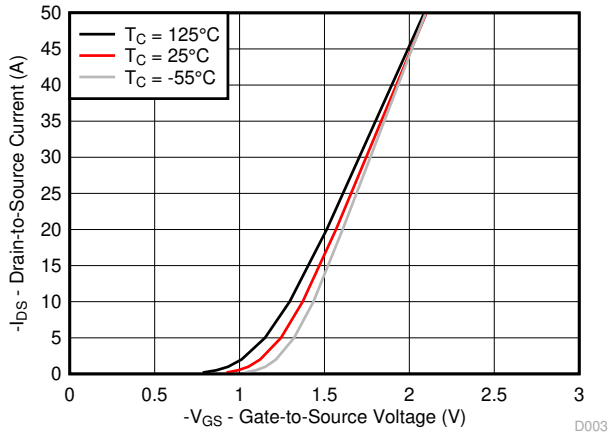


图 5-1. Saturation Characteristics



V_{DS} = – 5 V

图 5-2. Transfer Characteristics

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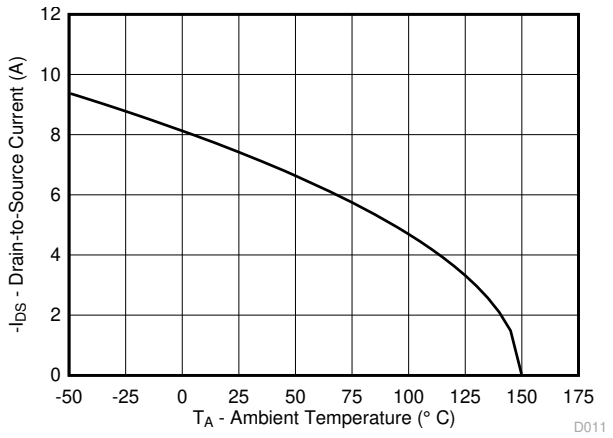
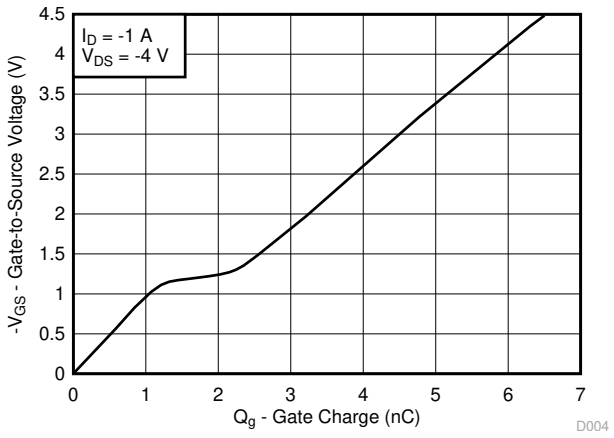


图 5-3. Maximum Drain Current vs Temperature



I_D = –1 A V_{DS} = –4 V

图 5-4. Gate Charge

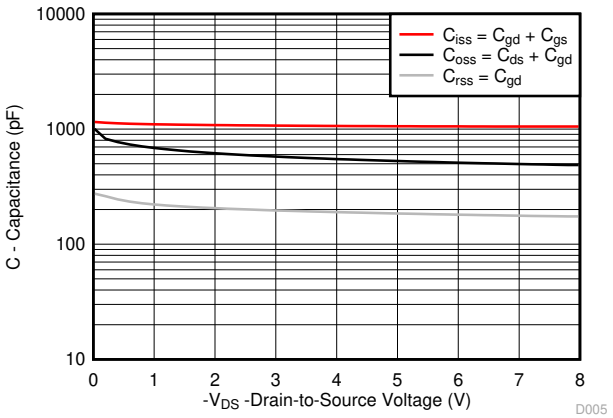
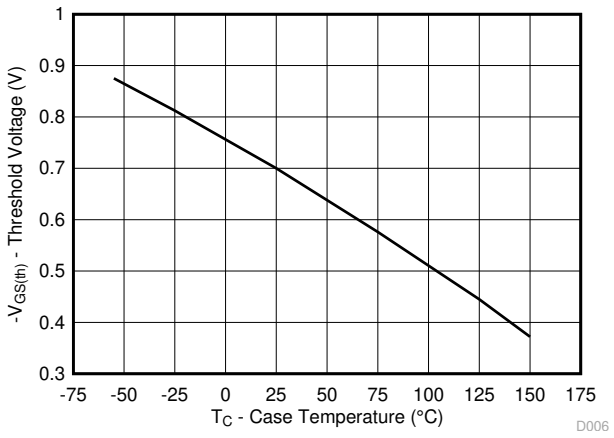


图 5-5. Capacitance



I_D = –250 µA

图 5-6. Threshold Voltage vs Temperature

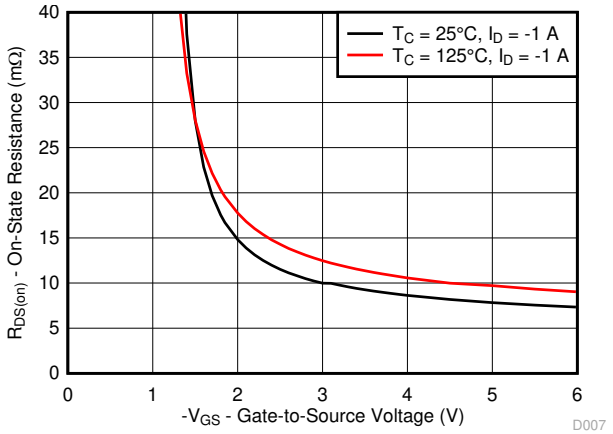
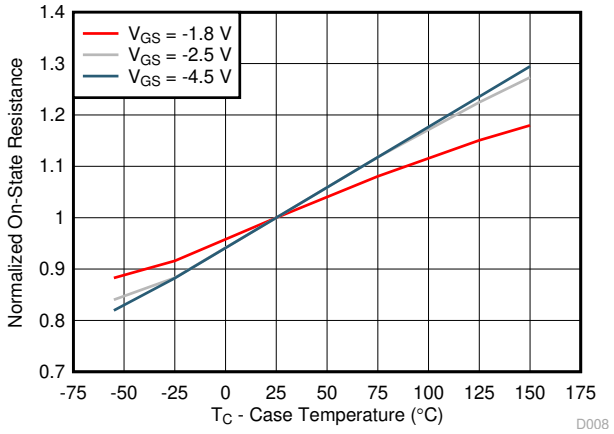


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –1 A

图 5-8. Normalized On-State Resistance vs Temperature

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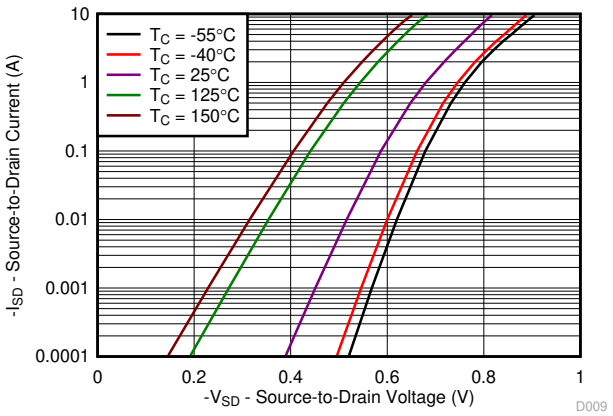
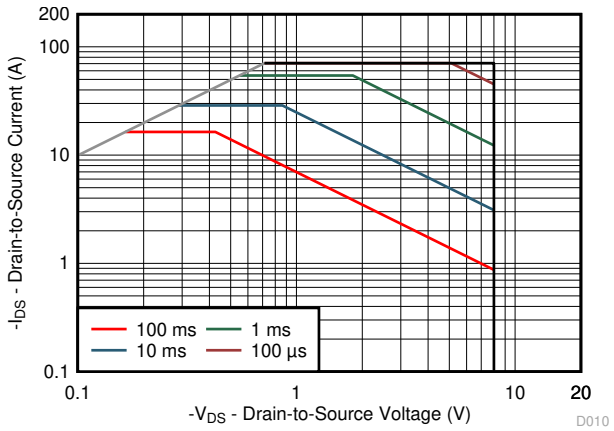


图 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 225°C/W

图 5-10. Maximum Safe Operating Area

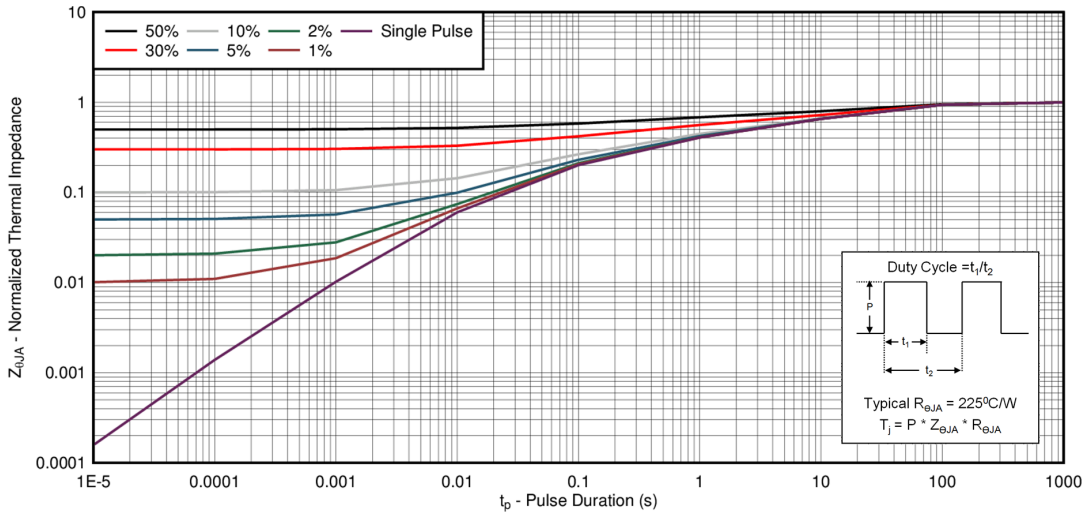


图 5-11. Transient Thermal Impedance

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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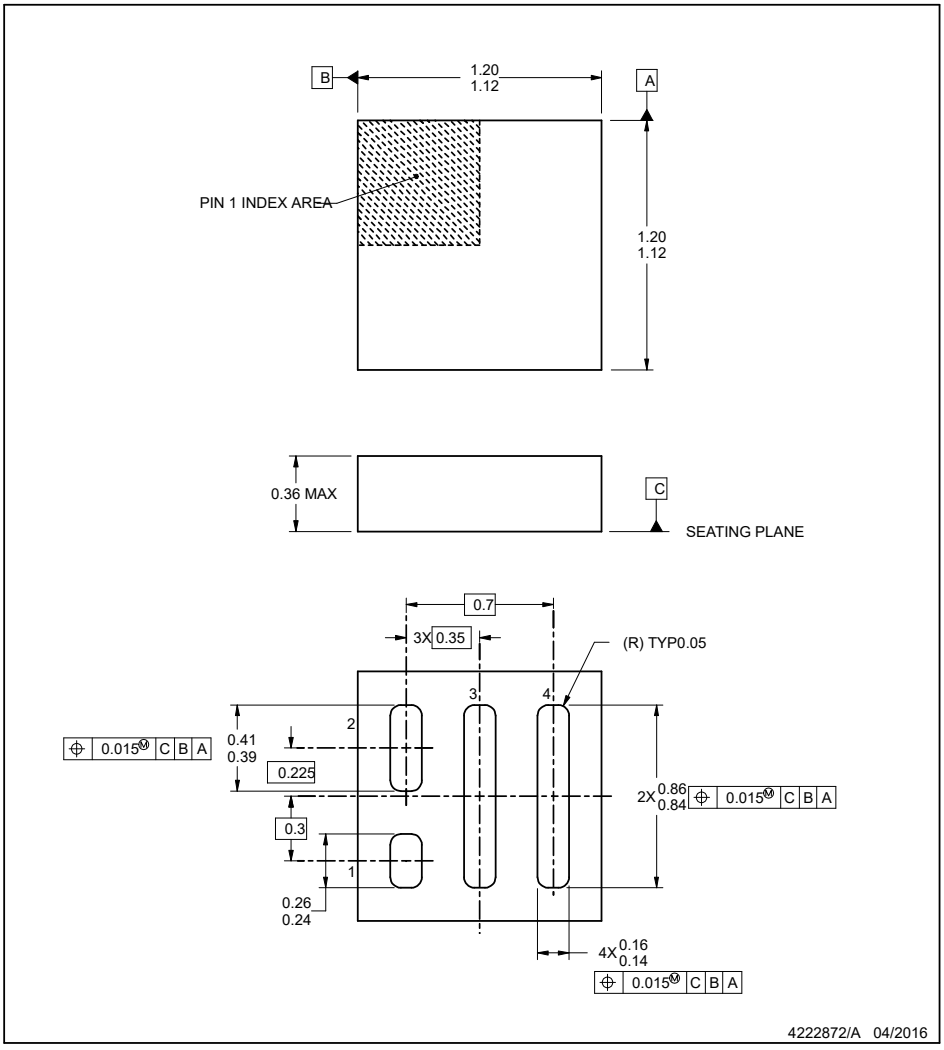
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD22205L Package Dimensions



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is a lead-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

表 7-1. Pin Configuration Table

POSITION	DESIGNATION
1	Gate
2	Drain
3	Source
4	Drain

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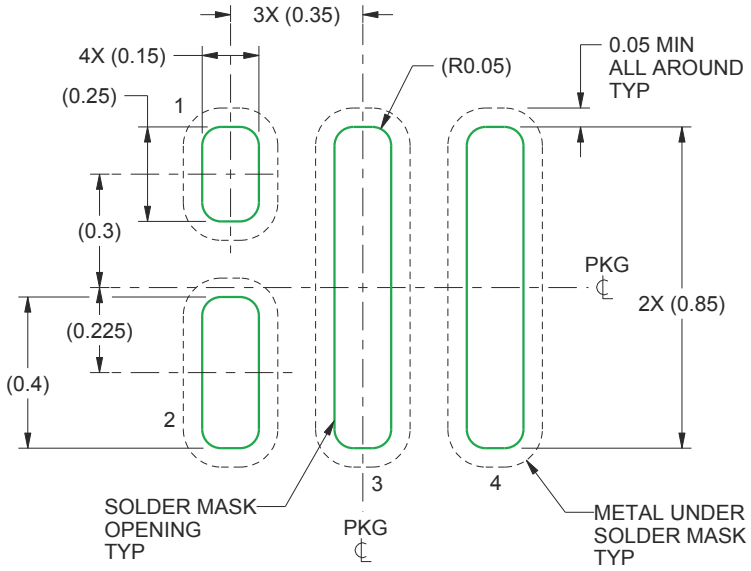
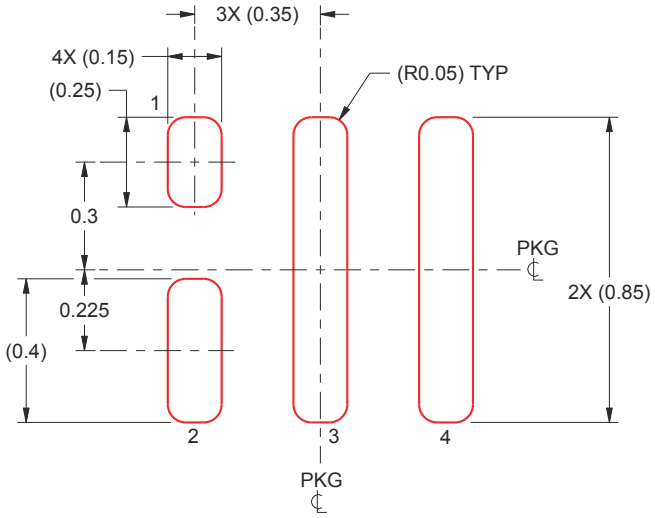
7.2 Land Pattern Recommendation



7.3 Stencil Recommendation



A. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22205L	ACTIVE	PICOSTAR	YMG	4	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	205	Samples
CSD22205LT	ACTIVE	PICOSTAR	YMG	4	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	205	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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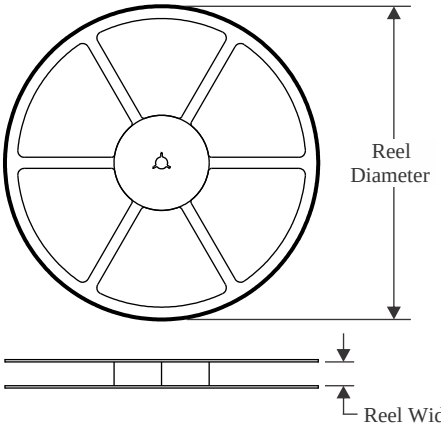
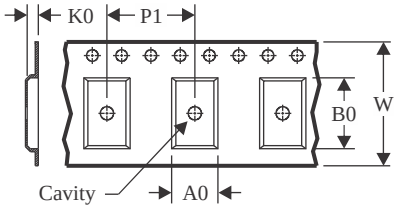
TAPE AND REEL INFORMATION

REEL DIMENSIONS

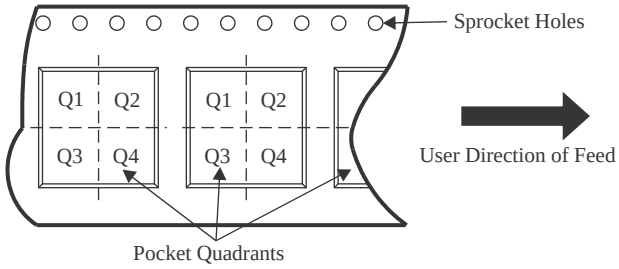


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

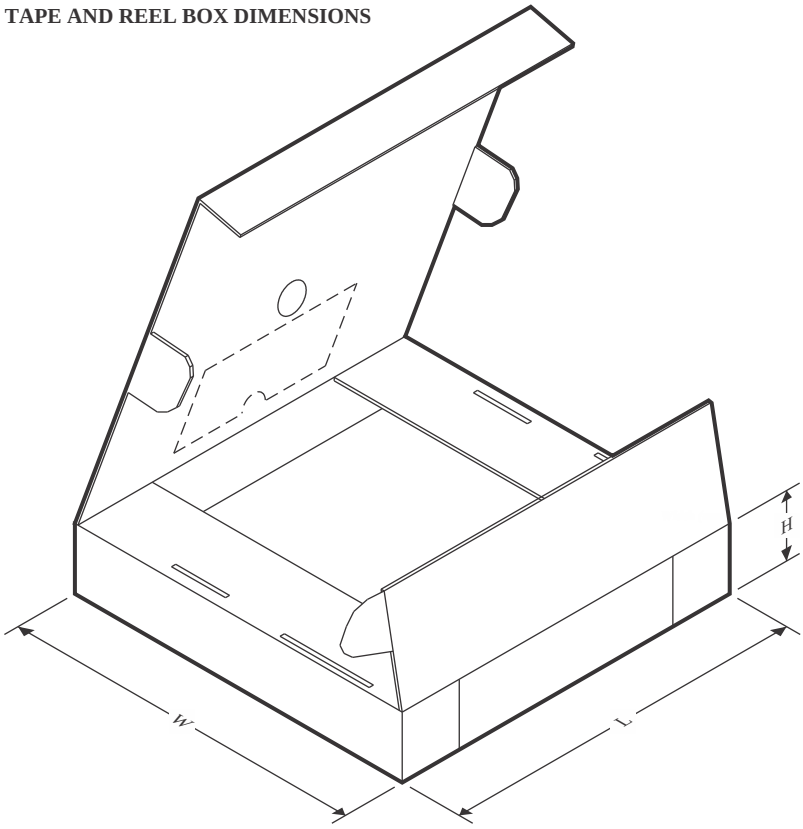
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22205L	PICOSTAR	YMG	4	3000	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1
CSD22205LT	PICOSTAR	YMG	4	250	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22205L	PICOSTAR	YMG	4	3000	182.0	182.0	20.0
CSD22205LT	PICOSTAR	YMG	4	250	182.0	182.0	20.0

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