CSD25202W15 20V P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

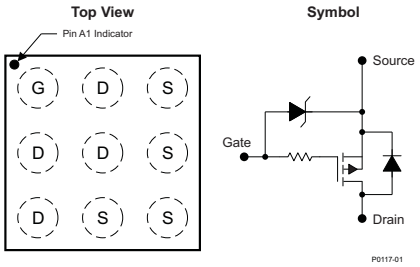
- 低电阻
- 小尺寸封装 1.5mm x 1.5mm
- 栅极静电放电 (ESD) 保护 - 3kV
- 无铅
- 符合 RoHS 环保标准
- 无卤素
- 栅 - 源电压钳位

2 应用范围

- 电池管理
- 电池保护

3 说明

这款 21mΩ，20V 器件设计用于在超薄且具有出色散热特性的 1.5mm × 1.5mm 小外形封装内提供最低的导通电阻和栅极电荷。 低导通电阻与小型封装尺寸和低高度结合在一起，使得此器件非常适合于电池供电运行的空间受限应用。



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	5.8		nC
Q_{gd}	栅漏栅极电荷	0.8		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.8V	40	mΩ
		V_{GS} = -2.5V	26	mΩ
		V_{GS} = -4.5V	21	mΩ
$V_{GS(th)}$	阀值电压	-0.75		V

订购信息(1)

器件	数量	介质	封装	出货
CSD25202W15	3000	7 英寸卷带	1.5mm x 1.5mm 晶圆级封装	卷带封装
CSD25202W15T	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

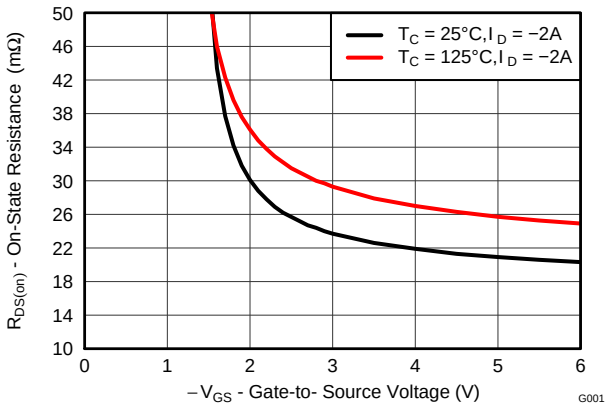
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	-4	A
	脉冲漏极电流(2)	-38	A
I_G	持续栅极电流(1)	-0.5	A
	脉冲栅极电流(2)	-7	A
P_D	功率耗散	0.5	W
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C

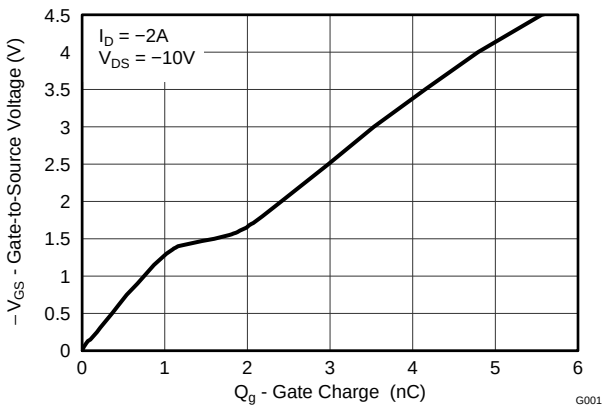
(1) 焊球受限

(2) $R_{\theta JA}$ = 220°C/W（典型值），脉冲持续时间 ≤100µs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

Changes from Original (June 2014) to Revision A **Page**

- “漏漏电压”已更正为“漏源电压” 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = –250 µA	–6		–7.2	V
I_{DDS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.45	–0.75	–1.05	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V, I_{DS} = –2 A		40	52	mΩ
		V_{GS} = –2.5 V, I_{DS} = –2 A		26	32	mΩ
		V_{GS} = –4.5 V, I_{DS} = –2 A		21	26	mΩ
g_{fs}	Transconductance	V_{DS} = –2 V, I_{DS} = –2 A		16		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		778	1010	pF
C_{OSS}	Output Capacitance			400	520	pF
C_{RSS}	Reverse Transfer Capacitance			21	27	pF
R_G	Series Gate Resistance(1)			31		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_D = –2 A		5.8	7.5	nC
Q_{gd}	Gate Charge - Gate-to-Drain			0.8		nC
Q_{gs}	Gate Charge - Gate-to-Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = –9.5 V, V_{GS} = 0 V		8.7		nC
$t_{d(on)}$	Turn On Delay Time(2)	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –2 A, R_G = 2 Ω		15		ns
t_r	Rise Time(2)			12		ns
$t_{d(off)}$	Turn Off Delay Time(2)			64		ns
t_f	Fall Time(2)			28		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –2 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{SD} = –10 V, I_F = –2 A, di/dt = 200 A/µs		19		nC
t_{rr}	Reverse Recovery Time			26		ns

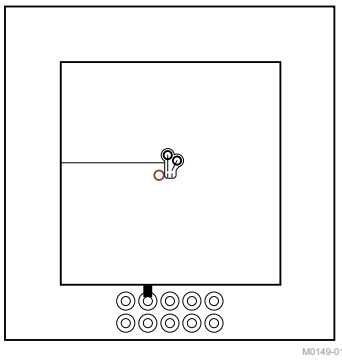
(1) Includes gate clamp resistor
(2) External R_G is in addition to the internal gate clamp resistor

5.2 Thermal Information

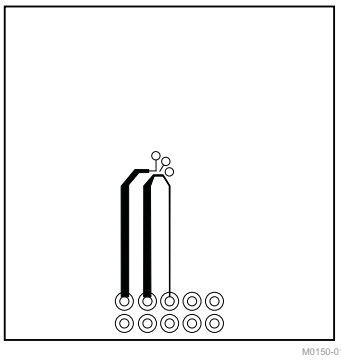
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		220		°C/W
	Junction-to-Ambient Thermal Resistance(2)		140		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 140°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 220°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

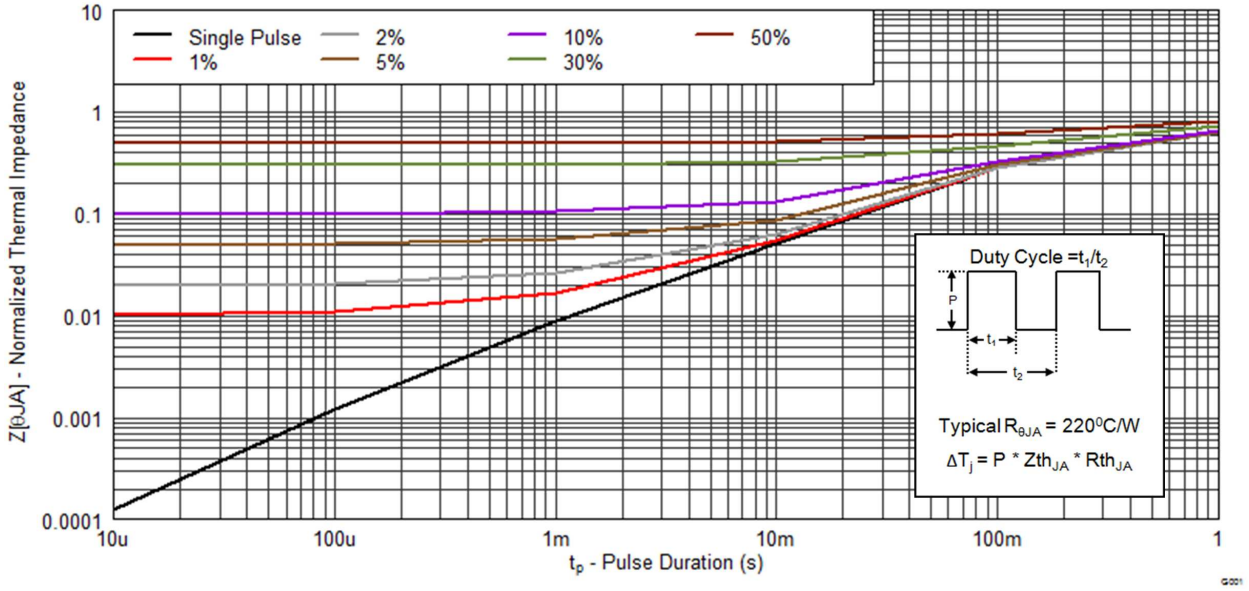


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

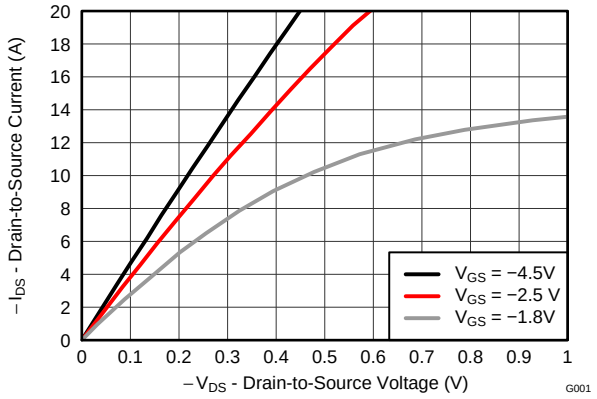


Figure 2. Saturation Characteristics

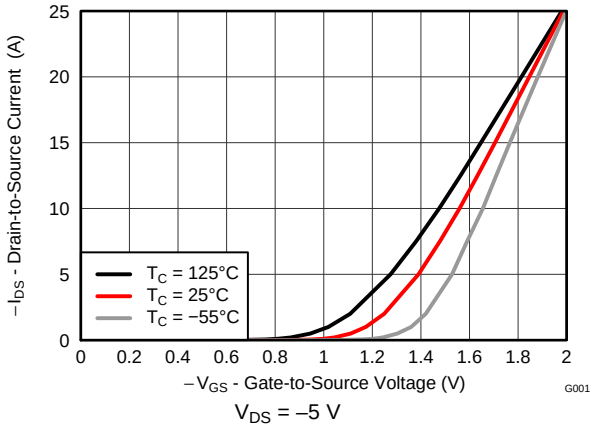


Figure 3. Transfer Characteristics

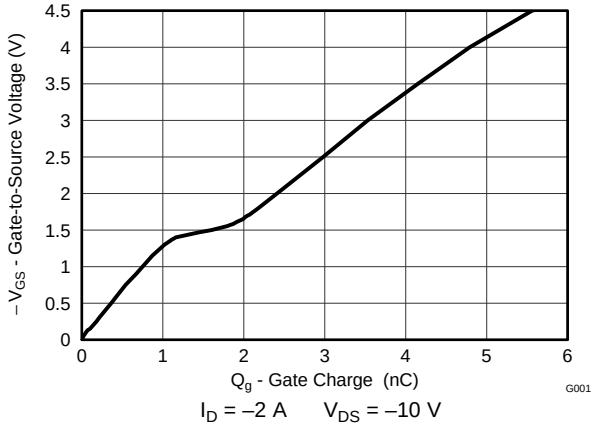


Figure 4. Gate Charge

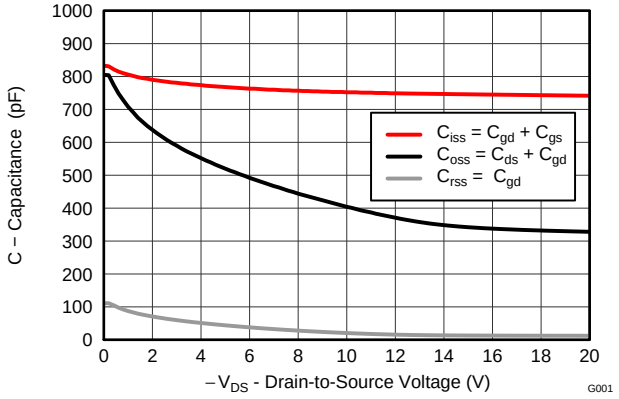


Figure 5. Capacitance

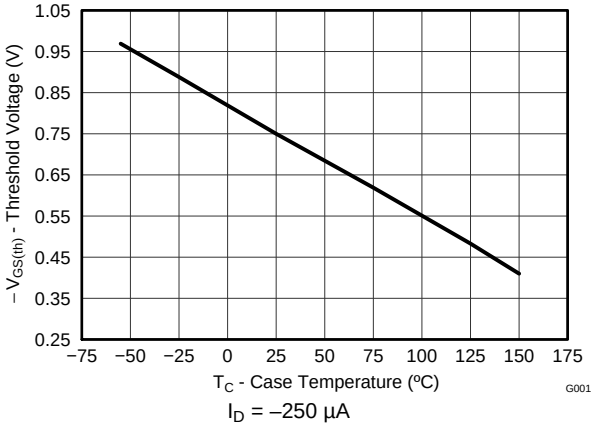


Figure 6. Threshold Voltage vs Temperature

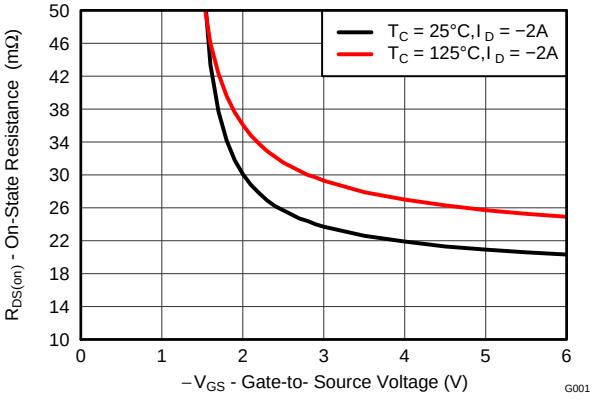


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

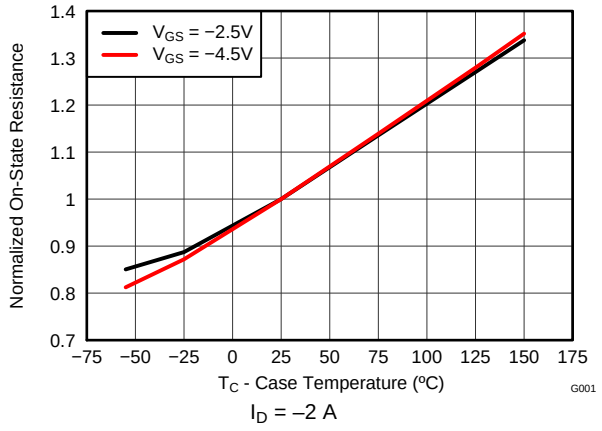


Figure 8. Normalized On-State Resistance vs Temperature

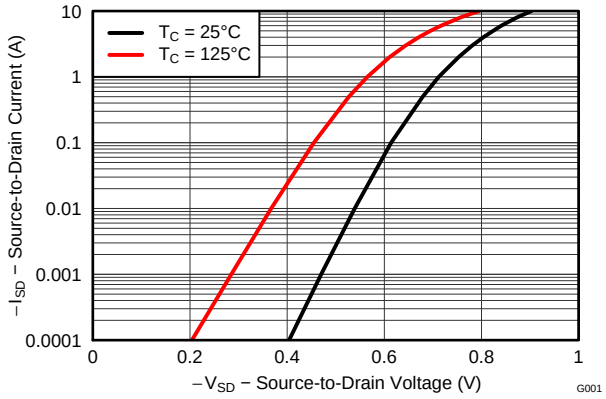


Figure 9. Typical Diode Forward Voltage

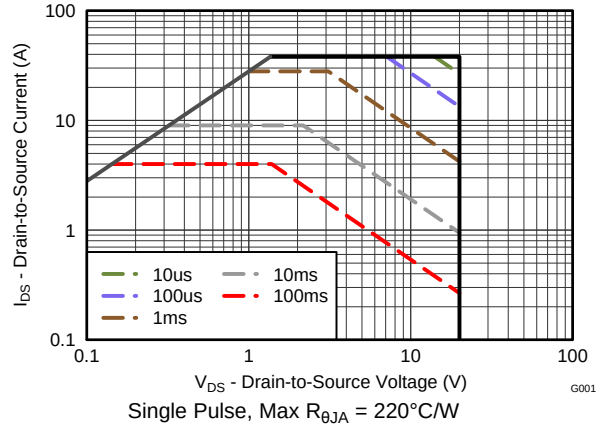


Figure 10. Maximum Safe Operating Area

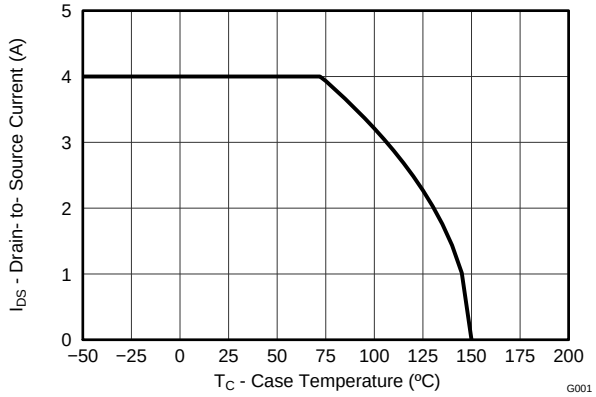


Figure 11. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

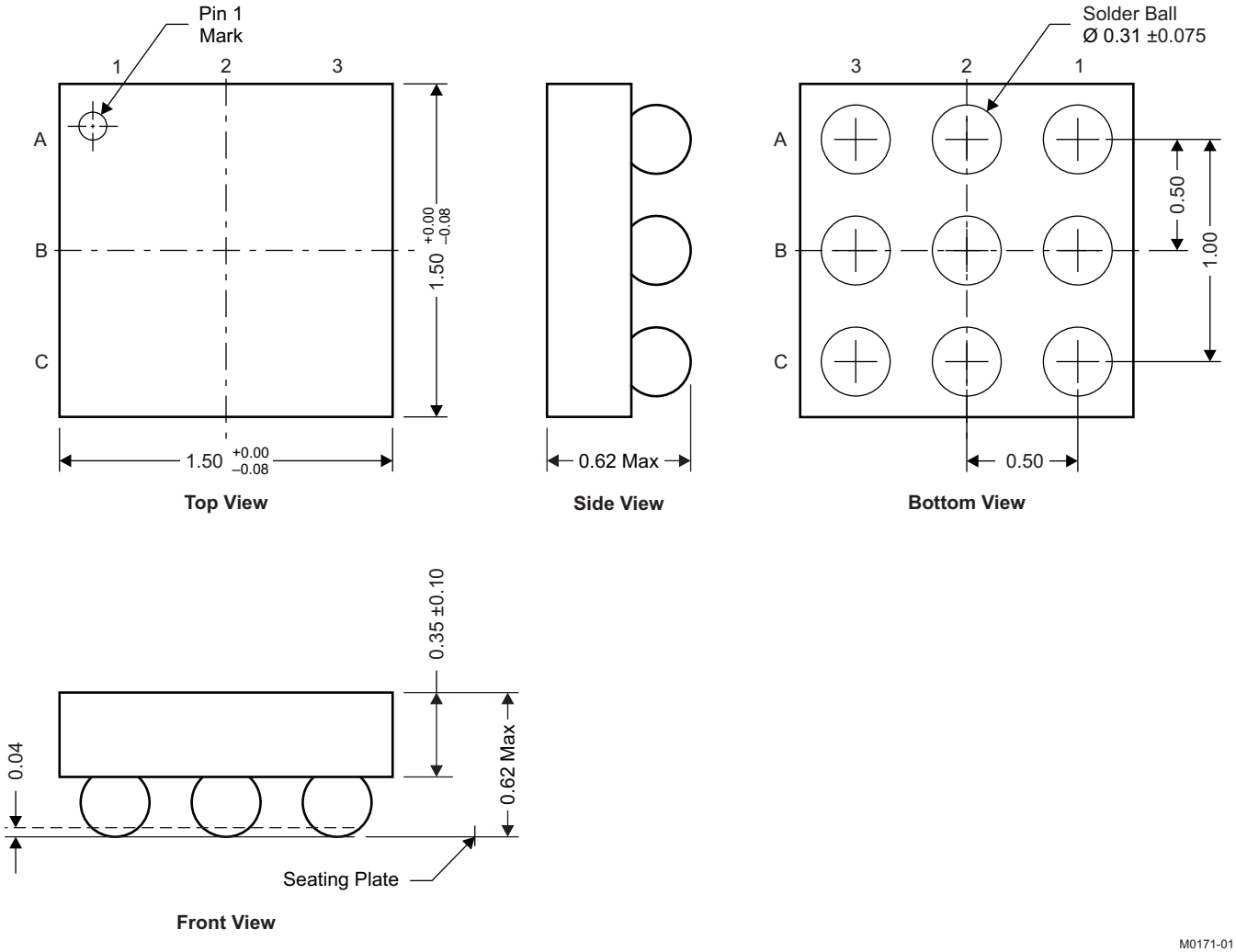
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD25202W15 封装尺寸

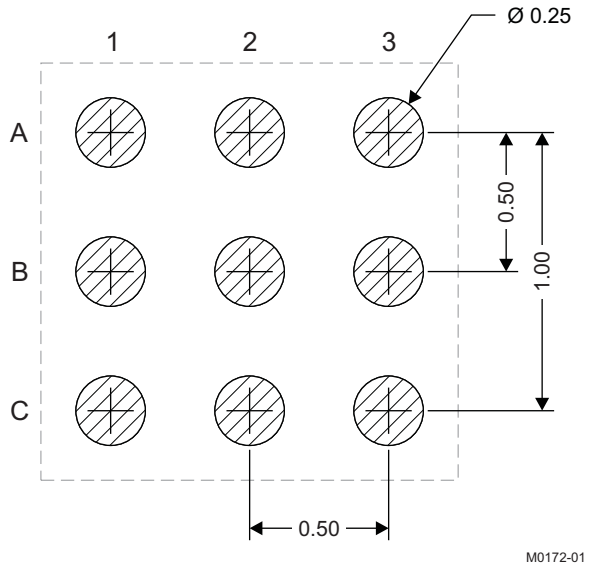


NOTE: 全部尺寸单位为 mm（除非另外注明）

引脚分配

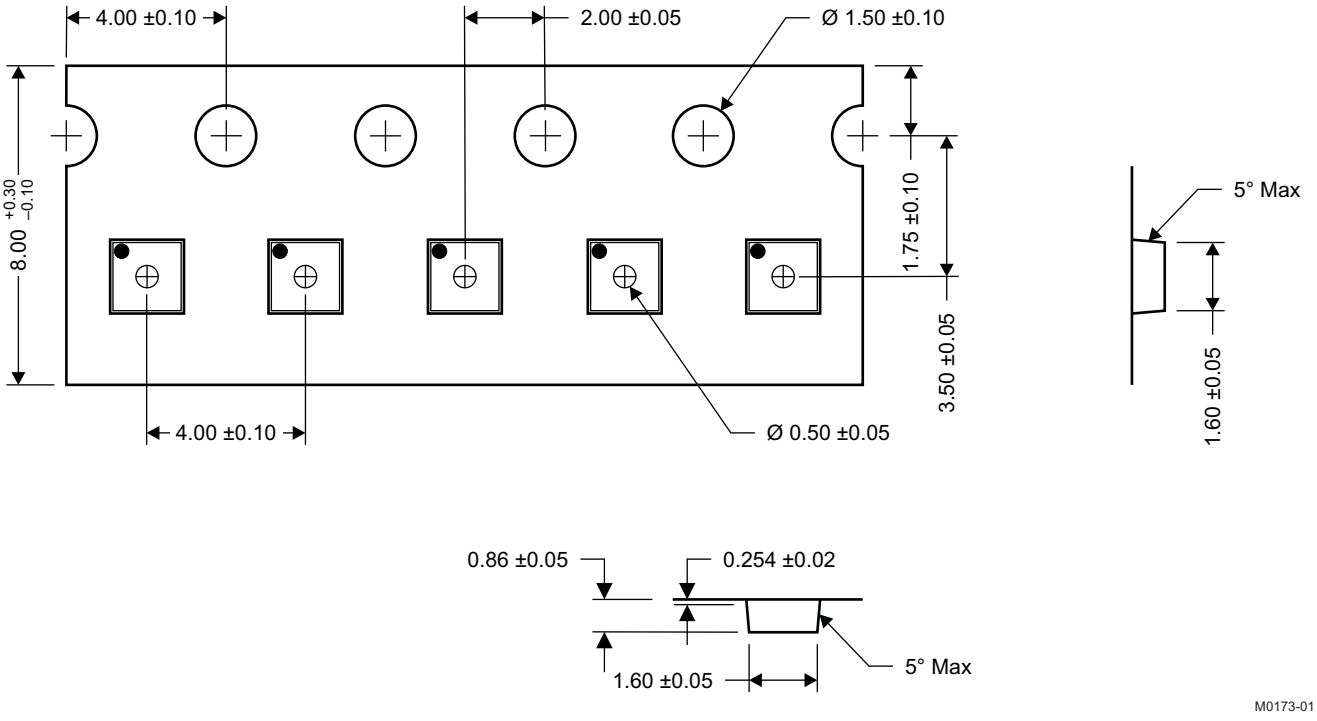
位置	名称
A1	栅极
A2，B1，B2，C1	漏
A3，B3，C2，C3	源

7.2 建议焊盘图案



NOTE: 全部尺寸单位为 mm（除非另外注明）

7.3 卷带信息



NOTES: 1. 10 个链齿孔的累积容差为 ±0.2

2. 每 100mm 长度的外倾角不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）
5. 厚度：0.30 ± 0.05mm
6. MSL1 260°C（红外 (IR) 和传导）PbF 回流焊兼容

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25202W15	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		25202	Samples
CSD25202W15T	ACTIVE	DSBGA	YZF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	25202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

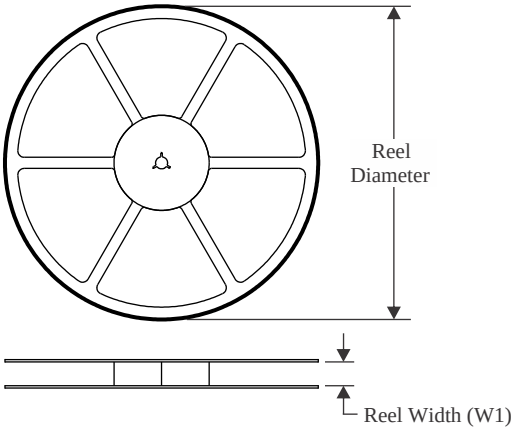
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

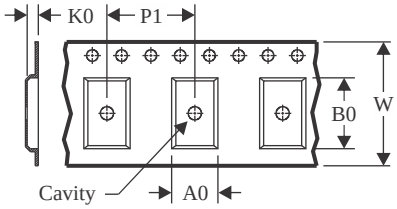
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

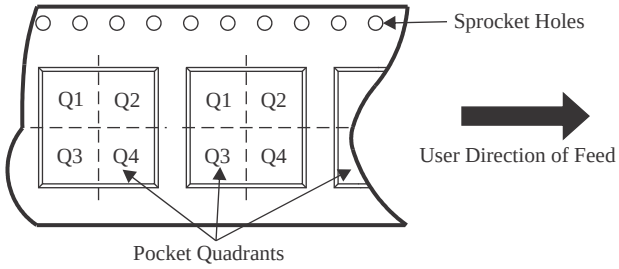


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

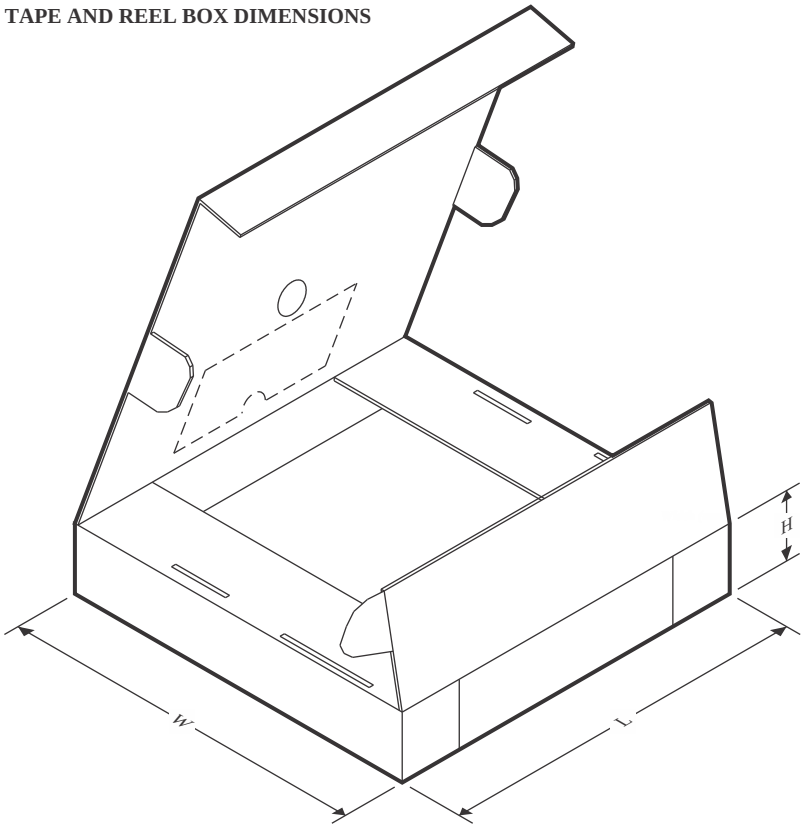
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25202W15	DSBGA	YZF	9	3000	180.0	9.0	1.69	1.69	0.69	4.0	8.0	Q1
CSD25202W15T	DSBGA	YZF	9	250	180.0	9.0	1.69	1.69	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

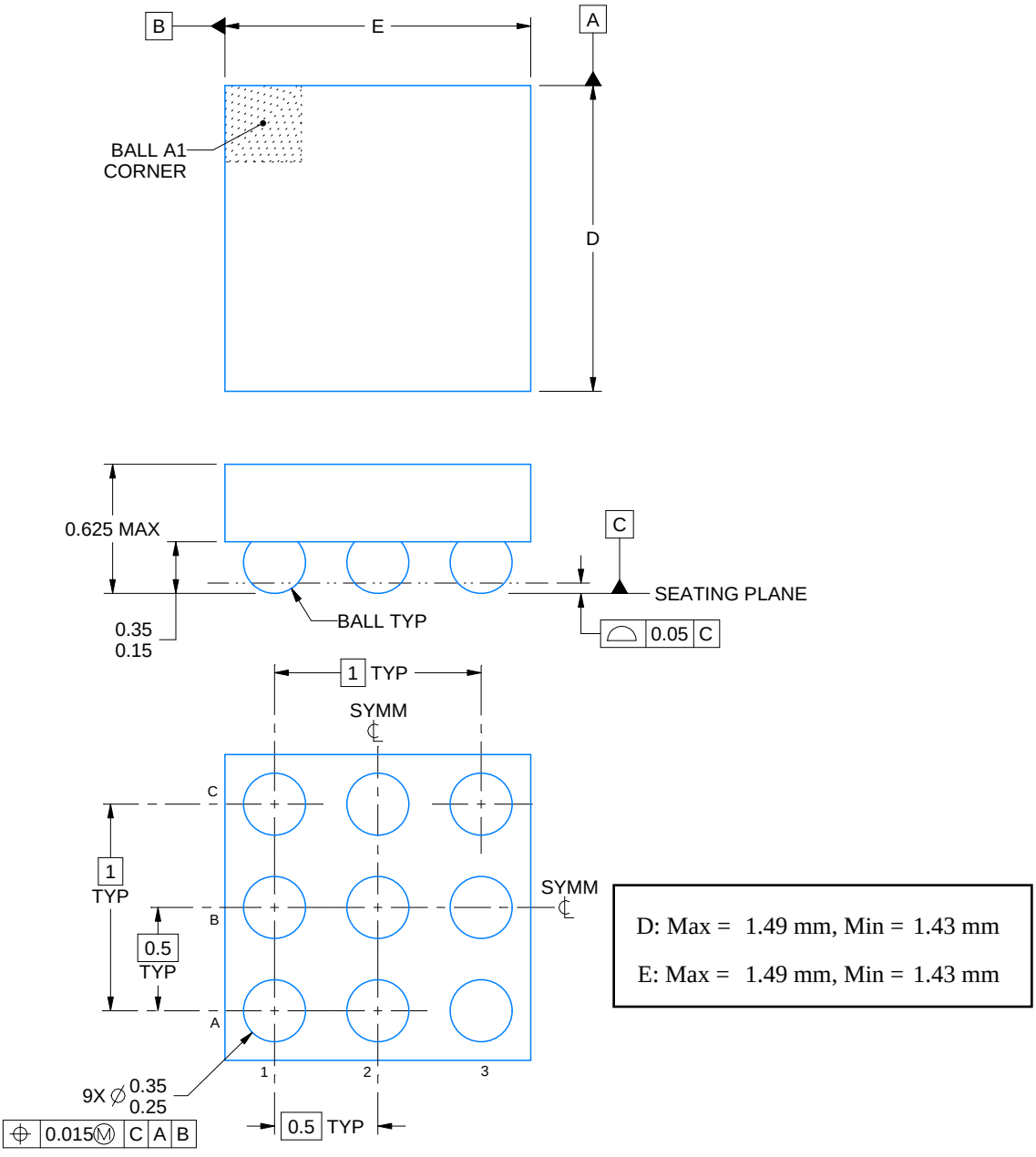
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25202W15	DSBGA	YZF	9	3000	195.0	210.0	39.0
CSD25202W15T	DSBGA	YZF	9	250	195.0	210.0	39.0

PACKAGE OUTLINE

YZF0009

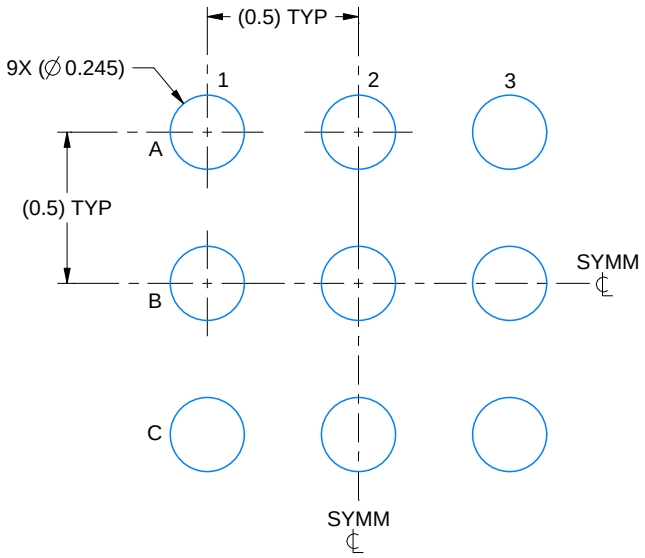
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

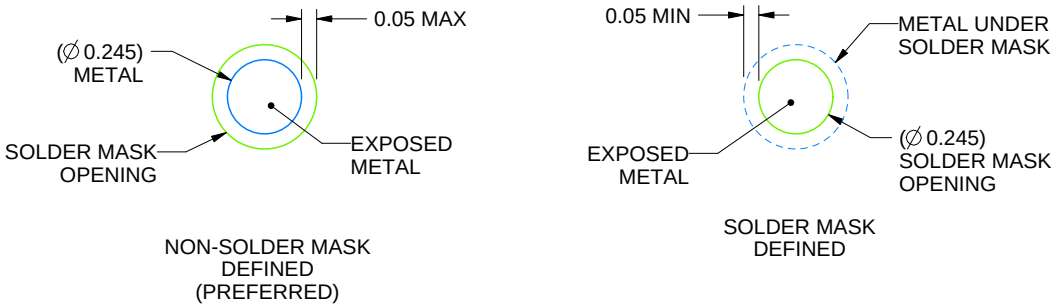


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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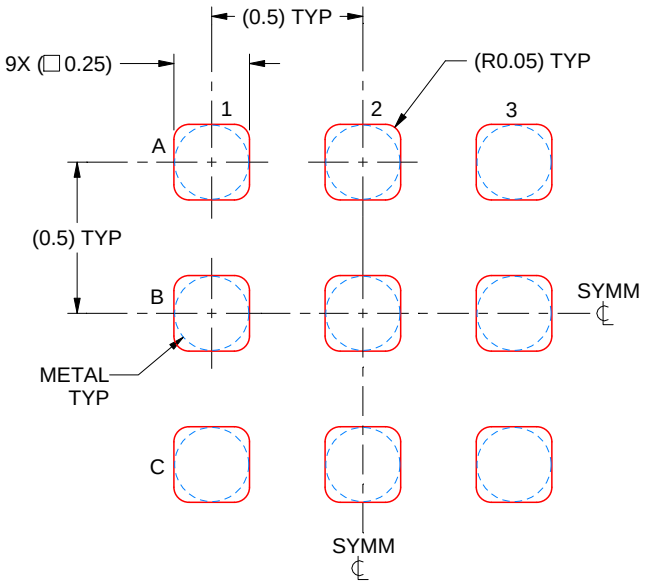
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4219558/A 10/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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