CSD75207W15 双路 P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

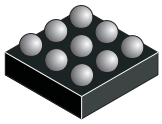
- 双路 P 通道 MOSFET
- 共源配置
- 小型封装尺寸 1.5mm x 1.5mm
- 栅极 - 源电压钳位
- 栅极静电放电 (ESD) 保护大于 4kV
  - 人体模型 (HBM) JEDEC 标准 JESD22-A114
- 无铅且无卤素
- 符合 RoHS 环保标准

2 应用范围

- 电池管理
- 电池保护
- 负载和输入开关

3 说明

CSD75207W15 器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内产生尽可能低的导通电阻和栅极电荷。 低导通电阻与小型封装尺寸和低高度结合在一起，使得此器件非常适合于电池供电运行的空间受限应用。 此器件也已经被授予美国专利 7952145，7420247，7235845 和 6600182。



产品概要

T_A = 25°C		典型值		单位
V_{D1D2}	漏极-漏极电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	2.9		nC
Q_{gd}	栅漏栅极电荷	0.4		nC
R_{D1D2}（导通）	漏极到漏极导通电阻	V_{GS} = –1.8V	119	mΩ
		V_{GS} = -2.5V	64	mΩ
		V_{GS} = -4.5V	45	mΩ
$V_{GS(th)}$	阀值电压	-0.8		V

订购信息(1)

器件	封装	介质	数量	出货
CSD75207W15	1.5mm x 1.5mm 晶圆级封装	7 英寸卷带	3000	卷带封装

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

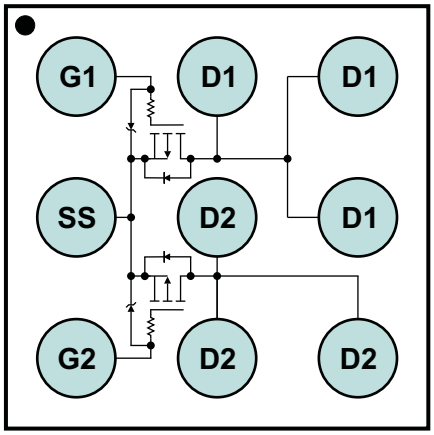
T_A = 25°C		值	单位
V_{D1D2}	漏极-漏极电压	-20	V
V_{GS}	栅源电压	-6.0	V
I_{D1D2}	持续漏极到漏极电流(1) (2)	–3.9	A
	脉冲漏极到漏极电流，T_C= 25°C(3)时测得	–24	A
I_S	持续源引脚电流	–1.2	A
	(3)脉冲源引脚电流	-15	A
I_G	持续栅极钳位电流	-0.5	A
	脉冲栅极钳位电流(3)	-7	A
P_D	功率耗散(1)	0.7	W
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C

(1) 每个器件两侧均导电

(2) 器件在 105ºC 温度下运行

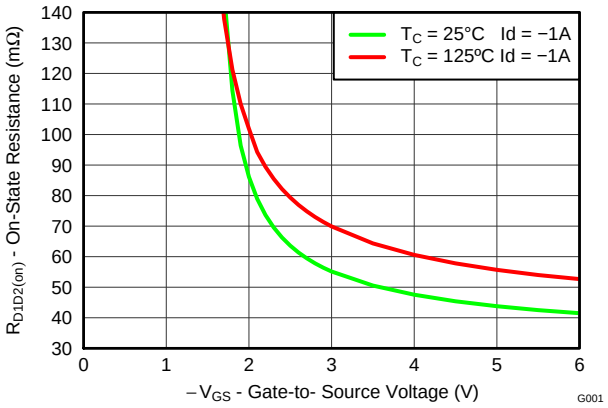
(3) 脉冲持续时间 10µs，占空比 ≤ 2%

顶视图



P0109-01

R_{D1D2}（导通）与 V_{GS}间的关系



目录

4 修订历史记录

Changes from Original (June 2013) to Revision A **Page**

- 持续漏极到漏极电流增加至 3.9A 1
- 更新了持续漏极到漏极电流条件，指定温度为 105ºC 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration.

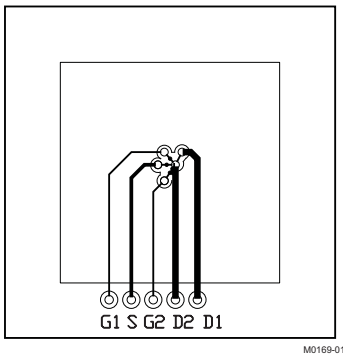
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{D1D2}	Drain-to-Drain Voltage	V_{GS} = 0 V, I_{D1D2} = –250 µA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{D1D2} = 0 V, I_G = -250 µA	–6			V
I_{DDS}	Drain-to-Drain Leakage Current	V_{GS} = 0 V, V_{D1D2} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{D1D2} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{D1D2} = V_{GS}, I_{DS} = –250 µA	–0.6	–0.8	–1.1	V
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V, I_{D1D2} = –1 A		119	162	mΩ
		V_{GS} = –2.5 V, I_{D1D2} = –1 A		64	77	mΩ
		V_{GS} = –4.5 V, I_{D1D2} = –1 A		45	54	mΩ
g_{fs}	Transconductance	V_{D1D2} = –10 V, I_{D1D2} = –1 A		6.2		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{D1D2} = –10 V, f = 1 MHz		458	595	pF
C_{OSS}	Output Capacitance			225	293	pF
C_{RSS}	Reverse Transfer Capacitance			10.4	13.5	pF
R_g	Series Gate Resistance			27		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{D1D2} = –10 V, I_{D1D2} = –1 A		2.9	3.7	nC
Q_{gd}	Gate Charge – Gate to Drain			0.4		nC
Q_{gs}	Gate Charge – Gate to Source			0.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.4		nC
Q_{OSS}	Output Charge	V_{D1D2} = –9.5 V, V_{GS} = 0 V		3.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{D1D2} = –10 V, V_{GS} = –4.5 V, I_{D1D2} = –1 A, R_G = 30 Ω		12.8		ns
t_r	Rise Time			8.6		ns
$t_{d(off)}$	Turn Off Delay Time			32.1		ns
t_f	Fall Time			16.0		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{D1D2} = –1 A, V_{GS} = 0 V		–0.8	–1	V
Q_{rr}	Reverse Recovery Charge	V_{dd} = –10 V, I_F = –1 A, di/dt = 200 A/µs		10.5		nC
t_{rr}	Reverse Recovery Time	V_{dd} = –10 V, I_F = –1 A, di/dt = 200 A/µs		23		ns

5.2 Thermal Information

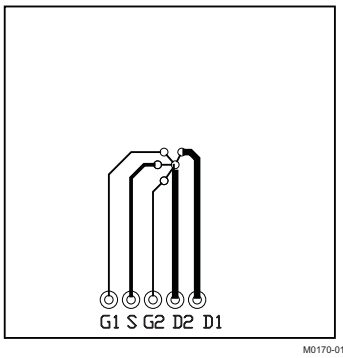
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUE	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1) (2)	70	°C/W
	Junction-to-Ambient Thermal Resistance (3) (2)	165	

(1) Device mounted on FR4 material with Minimum Cu mounting area.
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch^2 of Cu (2 oz).



Typ $R_{\theta JA}$ = 70°C/W when mounted on 1-inch^2 of 2 oz. Cu.



Typ $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2-oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

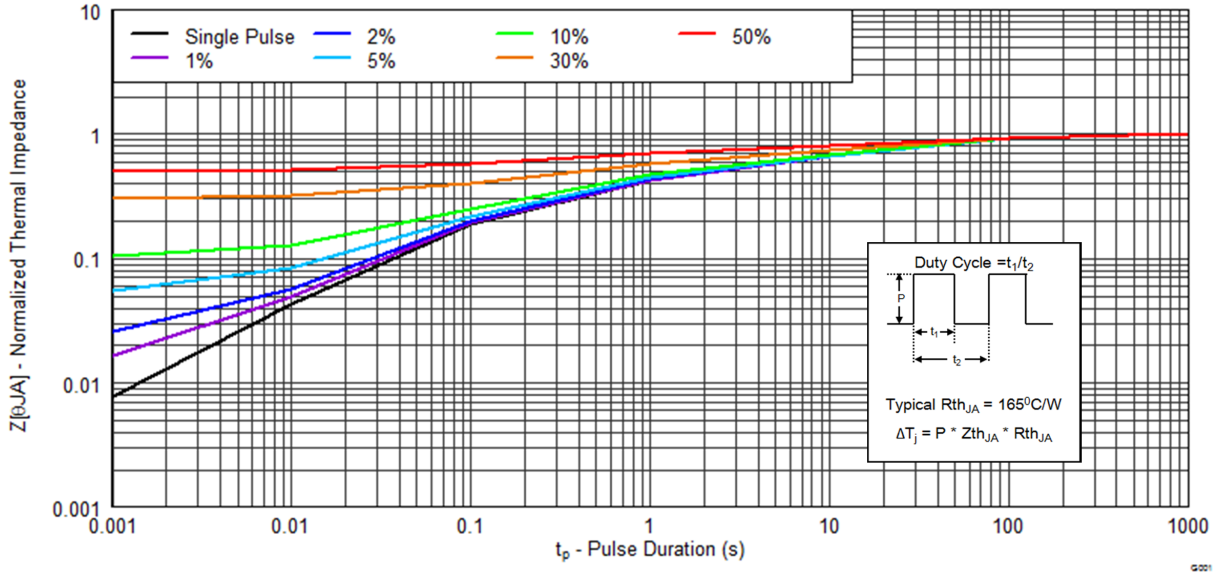


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

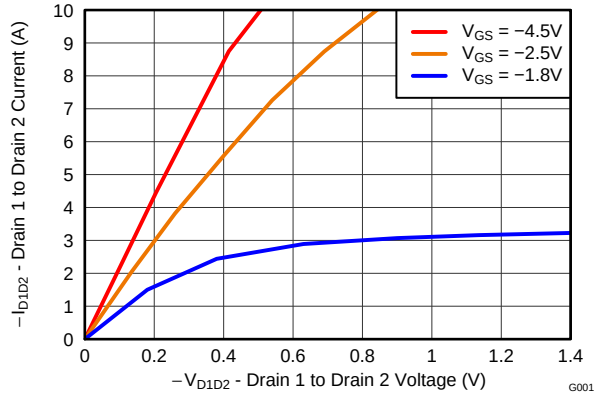


Figure 2. Saturation Characteristics

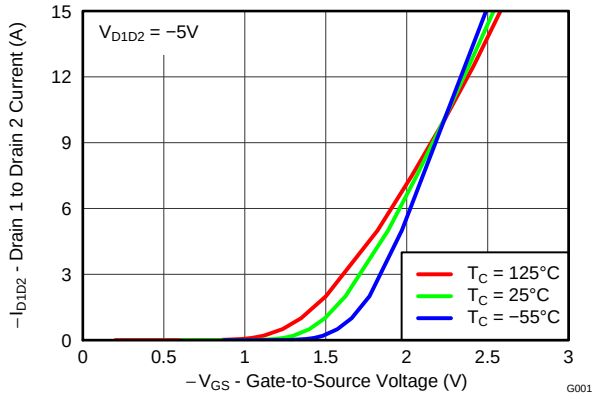


Figure 3. Transfer Characteristics

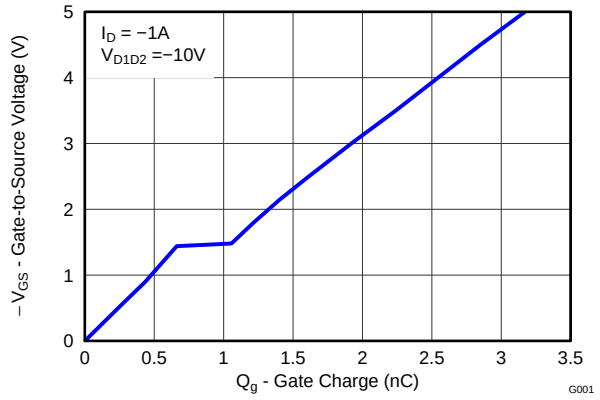


Figure 4. Gate Charge

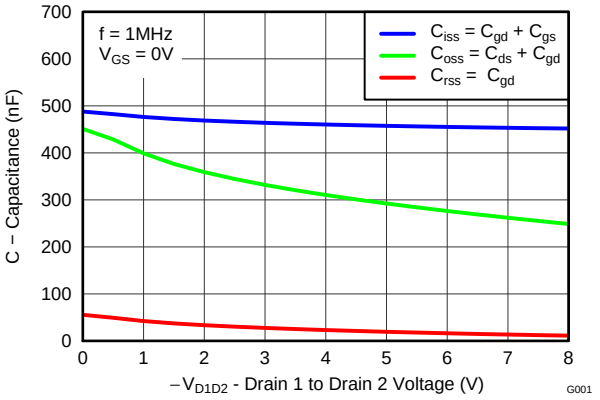


Figure 5. Capacitance

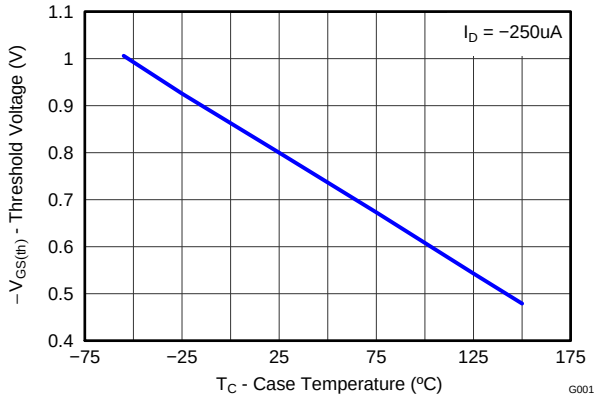


Figure 6. Threshold Voltage vs Temperature

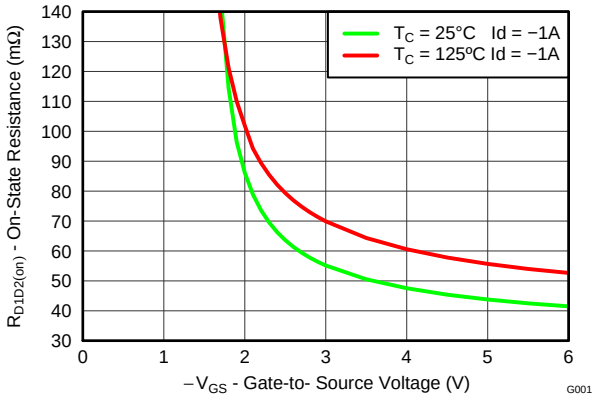


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

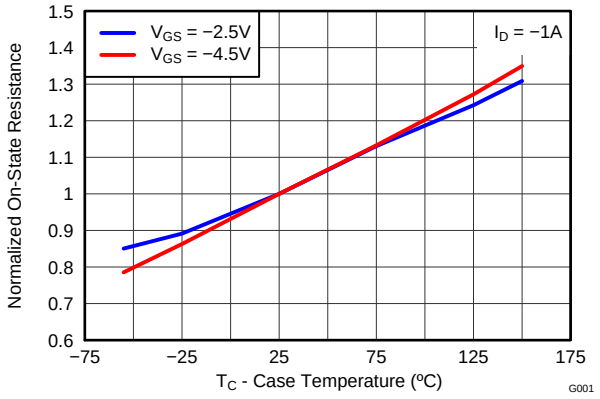


Figure 8. Normalized On-State Resistance vs Temperature

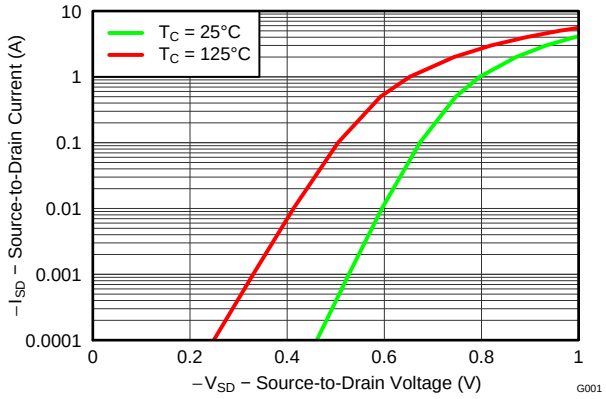


Figure 9. Typical Diode Forward Voltage

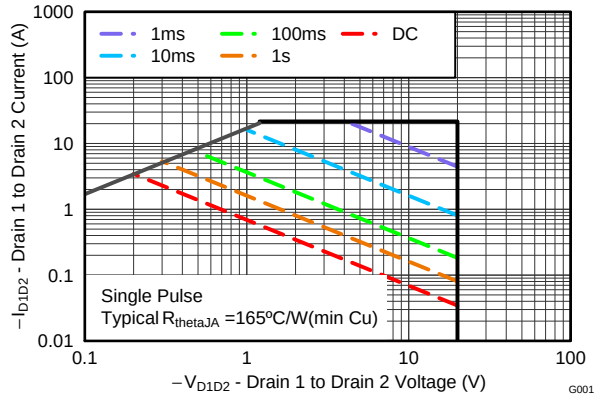


Figure 10. Maximum Safe Operating Area

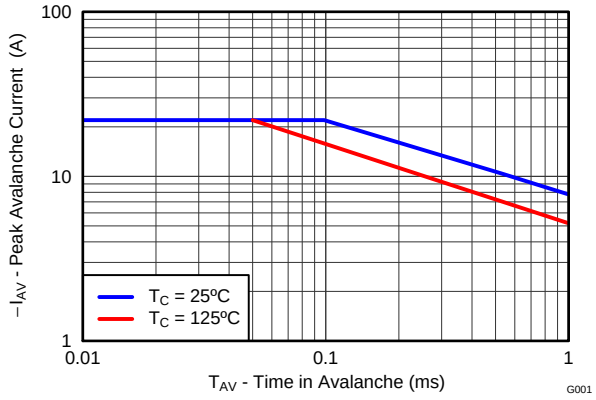


Figure 11. Single Pulse Unclamped Inductive Switching

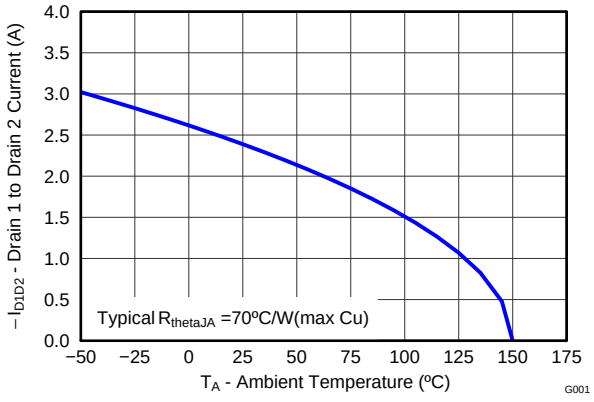


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

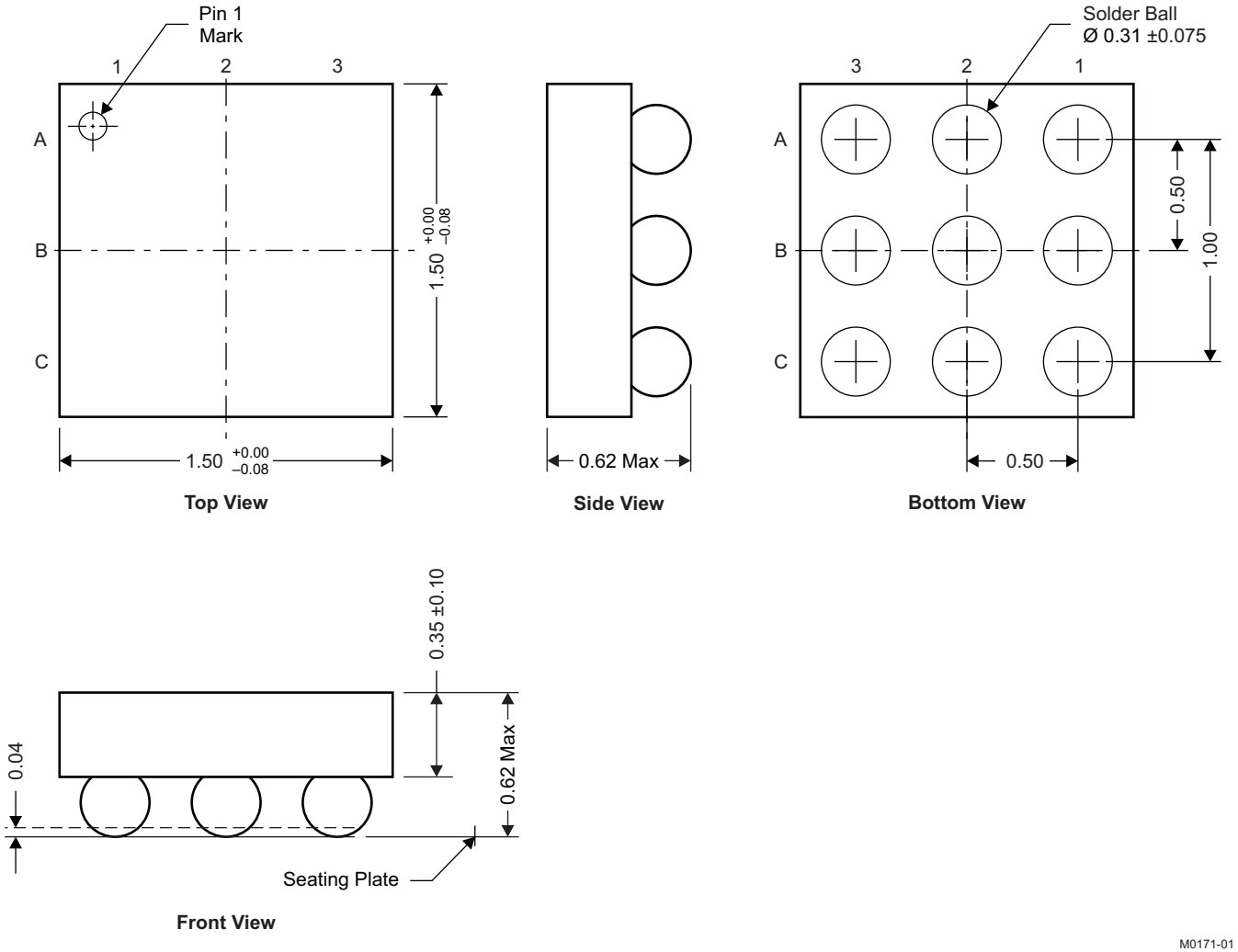
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD75207W15 封装尺寸

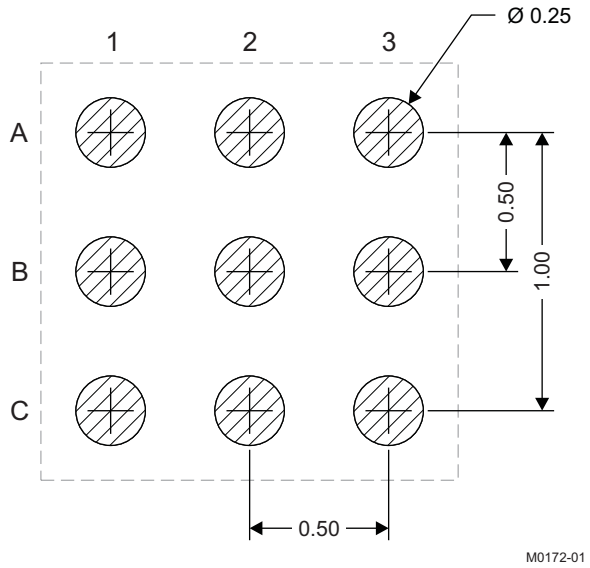


NOTE: 全部尺寸单位为 mm（除非另外注明）

引脚分配

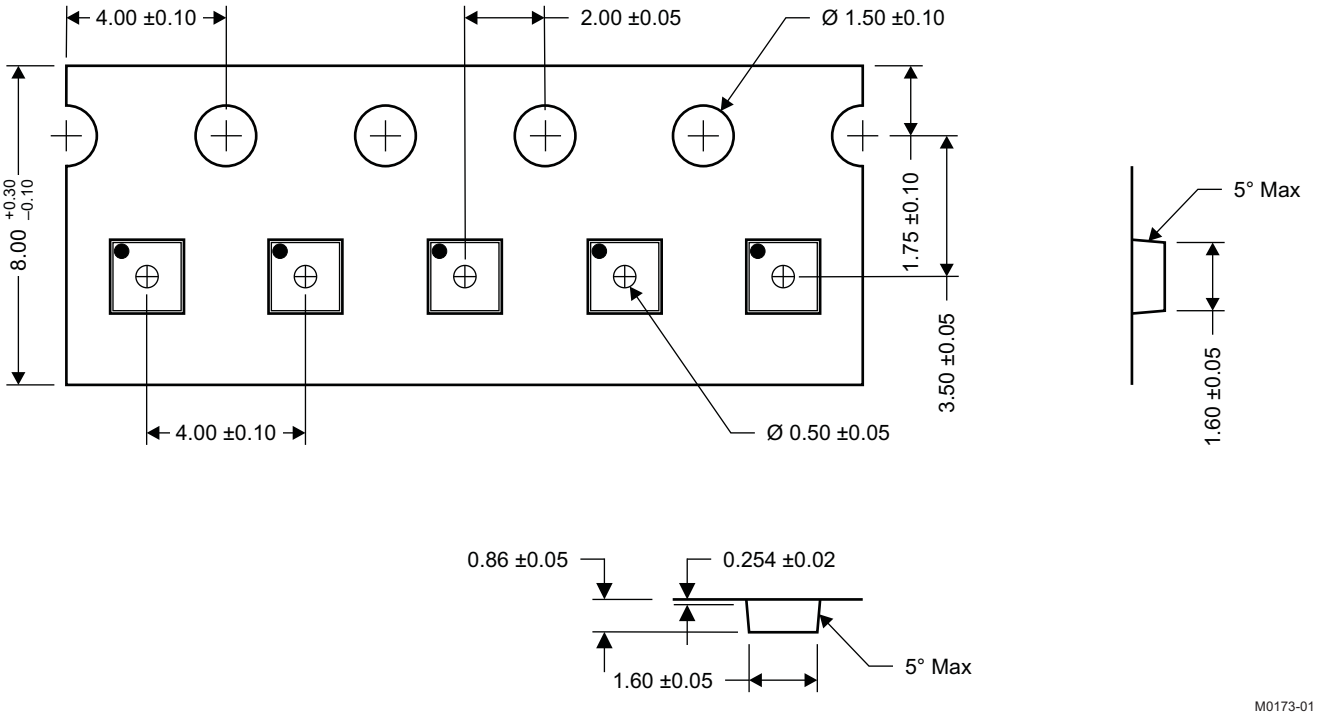
位置	名称
A1	栅极1
A2、A3 和 B3	Drain1
C1	Gate2
C2、C3 和 B2	Drain2
B1	源极检测

7.2 建议印刷电路板 (PCB) 焊盘图案



NOTE: 全部尺寸单位为 mm（除非另外注明）。

7.3 卷带封装信息



NOTE: 全部尺寸单位为 mm（除非另外注明）。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75207W15	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75207	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

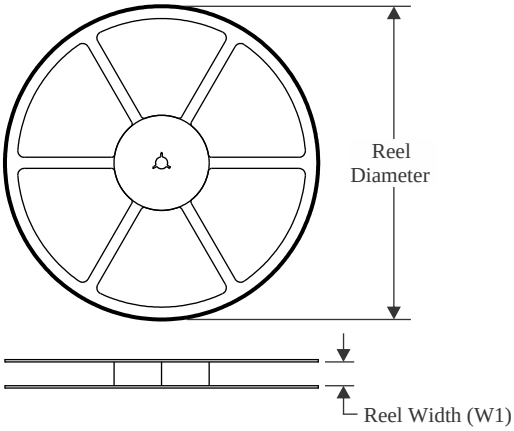
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

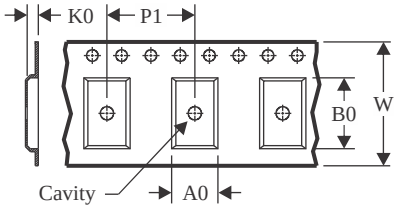
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

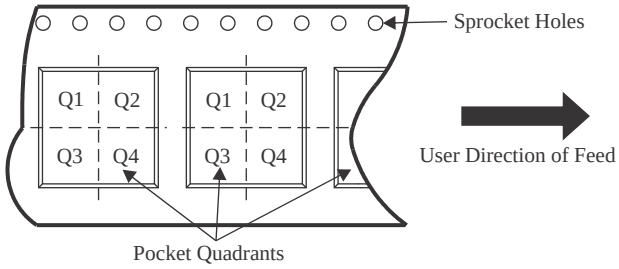


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

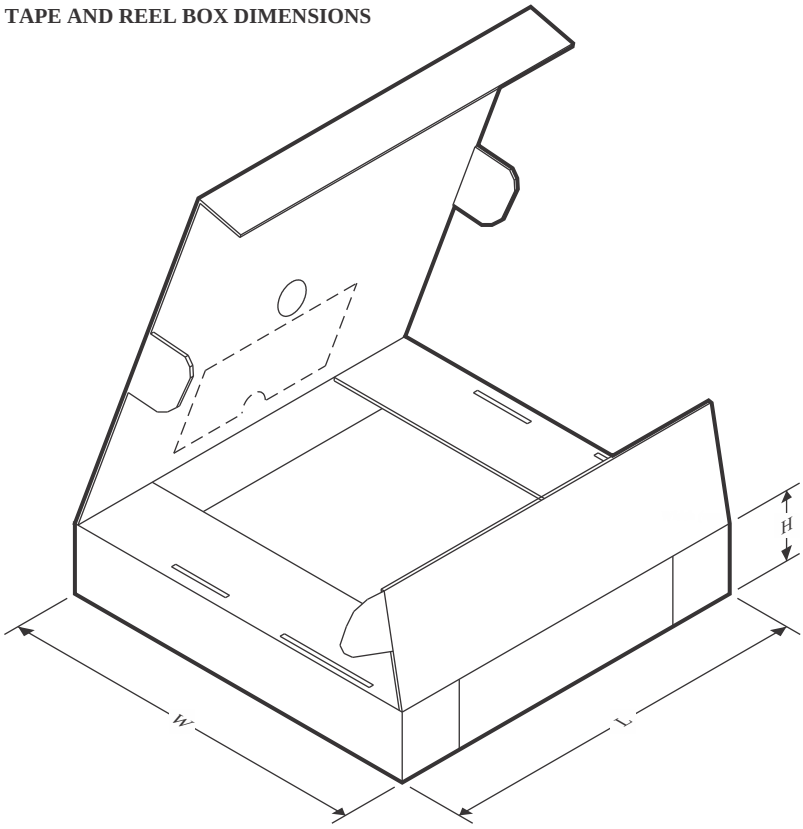
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

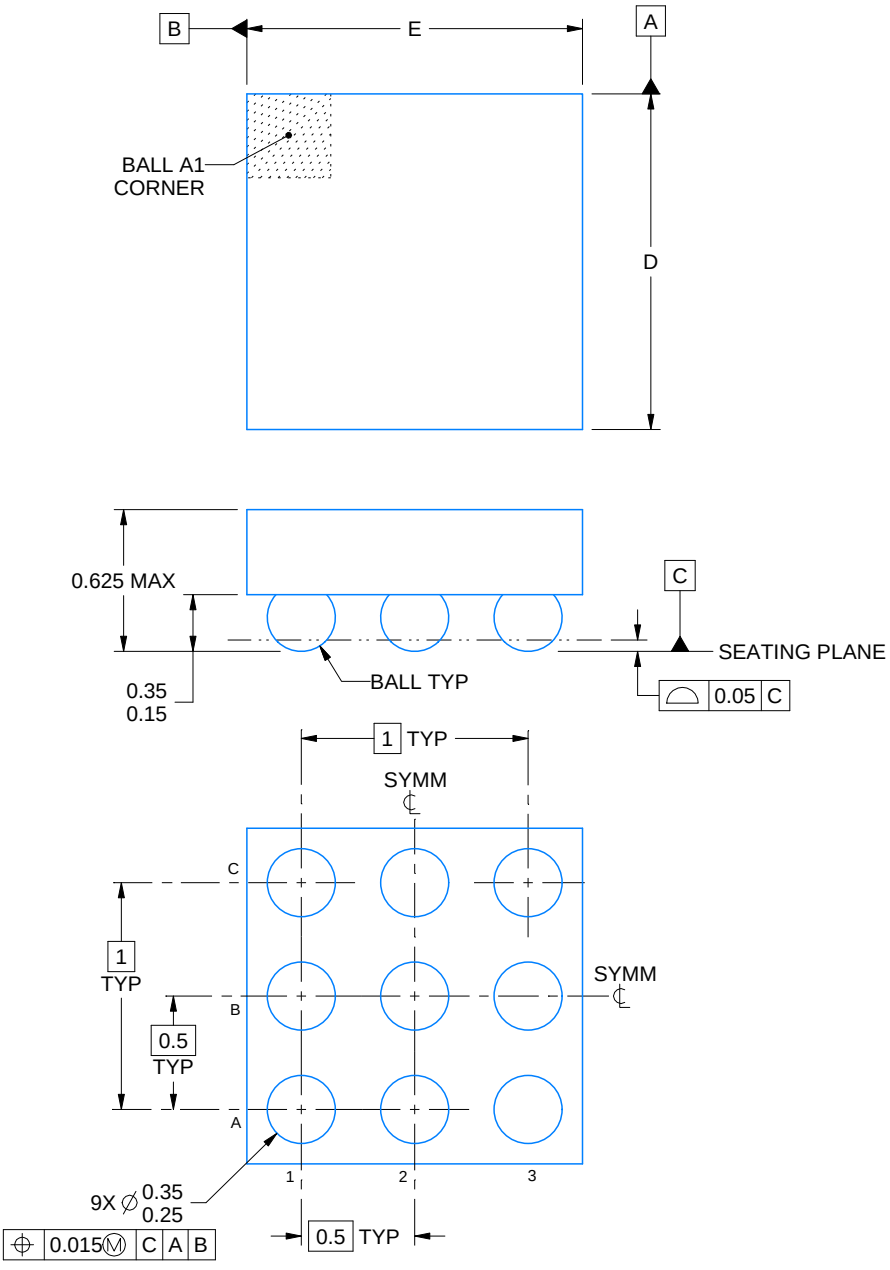
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD75207W15	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

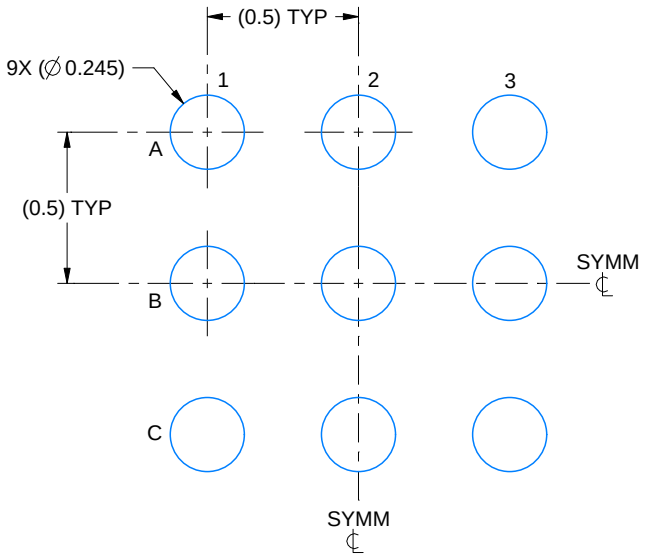
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD75207W15	DSBGA	YZF	9	3000	182.0	182.0	20.0



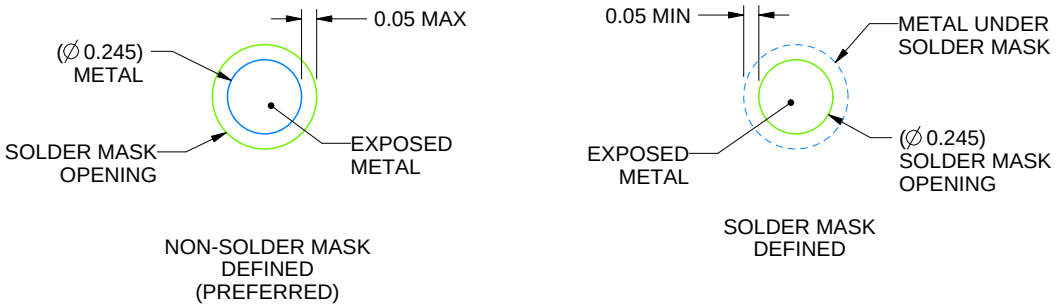
4219558/A 10/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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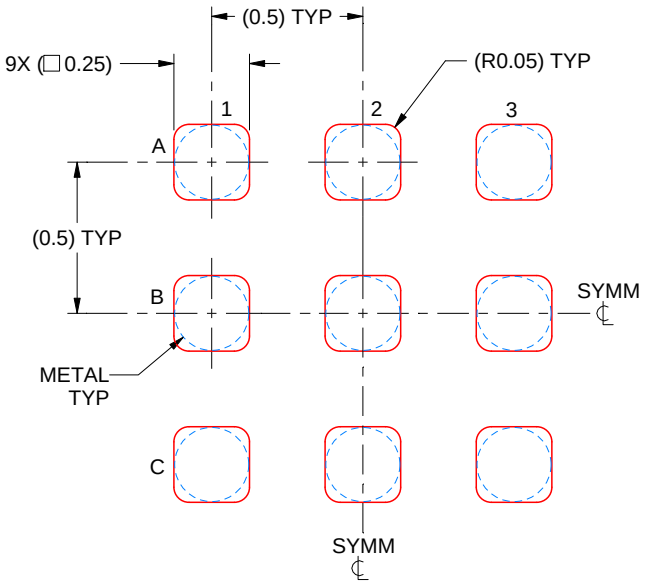
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4219558/A 10/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

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