CSD83325L 12V 双路 N 通道 NexFET™ 功率 MOSFET

1 特性

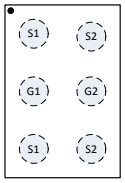
- 共漏极配置
- 低导通电阻
- 2.2mm x 1.15mm 的小尺寸
- 无铅
- 符合 RoHS
- 无卤素
- 栅极 ESD 保护

2 应用

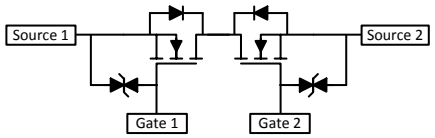
- 电池管理
- 电池保护

3 说明

这款 12V、9.9mΩ、2.2mm x 1.15mm LGA 双路 NexFET™ 功率 MOSFET 旨在以小巧封装更大程度地降低电阻和栅极电荷。该器件尺寸小巧并采用共漏极配置，非常适合小型手持设备的电池包应用。



顶视图



配置

产品概要

T_A = 25°C		典型值		单位
V_{S1S2}	源源电压	12		V
Q_g	栅极电荷总量 (4.5V)	8.4		nC
Q_{gd}	栅极电荷（栅极到漏极）	1.9		nC
$R_{S1S2(on)}$	源极至源极导通电阻	V_{GS} = 2.5V	17.5	mΩ
		V_{GS} = 3.8V	10.9	mΩ
		V_{GS} = 4.5V	9.9	mΩ
$V_{GS(th)}$	阈值电压	1.0		V

器件信息(1)

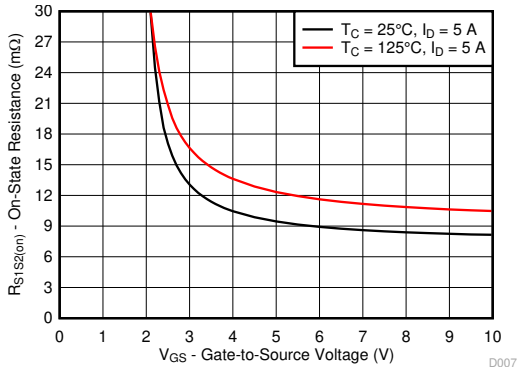
器件	数量	介质	封装	出货
CSD83325L	3000	7 英寸卷带	2.20mm x 1.15mm Land Grid Array (LGA) 封装	卷带包装
CSD83325LT	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

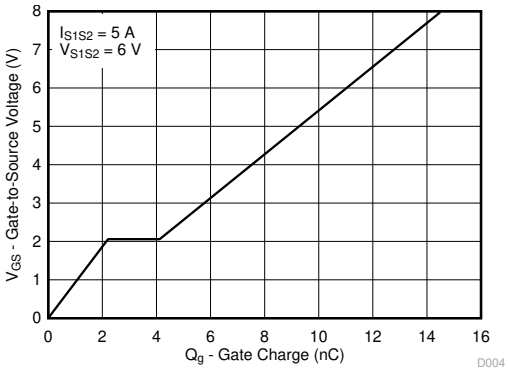
绝对最大额定值

T_A = 25°C		值	单位
V_{S1S2}	源源电压	12	V
V_{GS}	栅源电压	±10	V
I_S	持续源极电流(1)	8	A
I_{SM}	脉冲源极电流(2)	52	A
P_D	功率耗散	2.3	W
$V_{(ESD)}$	人体放电模型 (HBM)	2000	V
T_J、T_{stg}	工作结温，贮存温度	-55 至 150	°C

(1) 器件在 105ºC 温度下运行.
(2) $R_{\theta JA}$ = 150°C/W（覆铜面积最小时的典型值），脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-source voltage	V_{GS} = 0 V, I_S = 250 µA	12			V
I_{S1S2}	Source-to-source leakage current	V_{GS} = 0 V, V_{S1S2} = 9.6 V			1.0	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 10 V			10	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_S = 250 µA	0.7	1.0	1.4	V
$R_{S1S2(on)}$	Source-to-source on resistance	V_{GS} = 2.5 V, I_S = 5 A	12.0	17.5	23.0	mΩ
		V_{GS} = 3.8 V, I_S = 5 A	8.8	10.9	13.0	mΩ
		V_{GS} = 4.5 V, I_S = 5 A	7.9	9.9	11.9	mΩ
g_{fs}	Transconductance	V_{S1S2} = 1.2 V, I_S = 5 A		36		S
DYNAMIC CHARACTERISTICS(1)						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 6 V, f = 1 MHz		902	1170	pF
C_{oss}	Output capacitance			187	243	pF
C_{rss}	Reverse transfer capacitance			111	144	pF
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 6 V, I_S = 5 A		8.4	10.9	nC
Q_{gd}	Gate charge gate-to-drain			1.9		nC
Q_{gs}	Gate charge gate-to-source			2.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.6		nC
Q_{oss}	Output charge	V_{S1S2} = 6 V, V_{GS} = 0 V		2.9		nC
$t_{d(on)}$	Turnon delay time	V_{S1S2} = 6 V, V_{GS} = 4.5 V, I_{S1S2} = 5 A, R_G = 0 Ω		205		ns
t_r	Rise time			353		ns
$t_{d(off)}$	Turnoff delay time			711		ns
t_f	Fall time			589		ns
DIODE CHARACTERISTICS						
$V_{F(S-S)}$	Source-to-source diode forward voltage	I_{SS} = 5 A, V_{G1S1} = 0 V, V_{G2S2} = 4.5 V		0.79	1.0	V

(1) Dynamic characteristics values specified are per single FET.

4.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		150		°C/W
	Junction-to-ambient thermal resistance(2)		55		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

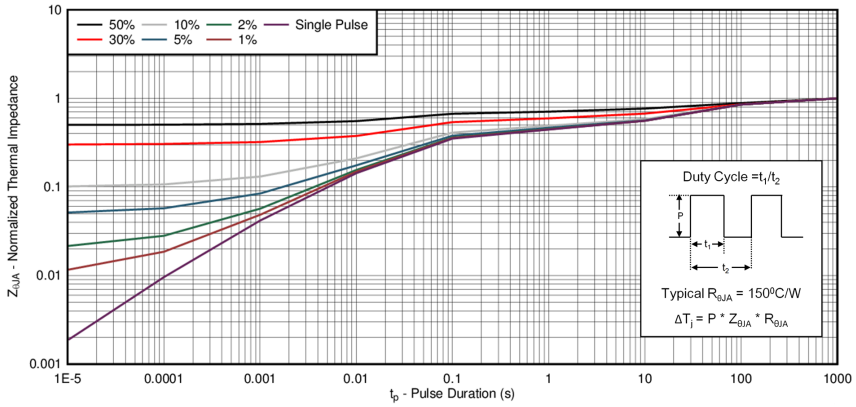


图 4-1. Transient Thermal Impedance

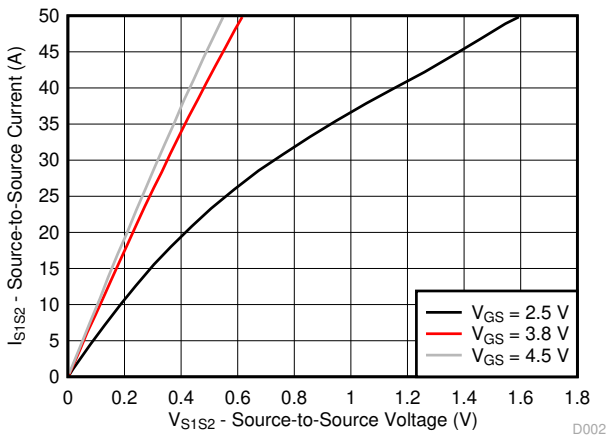
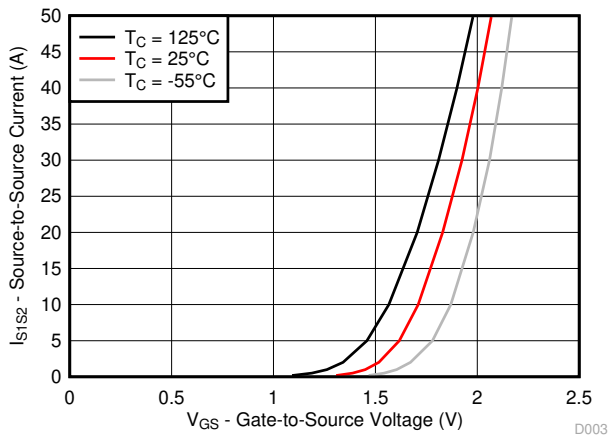
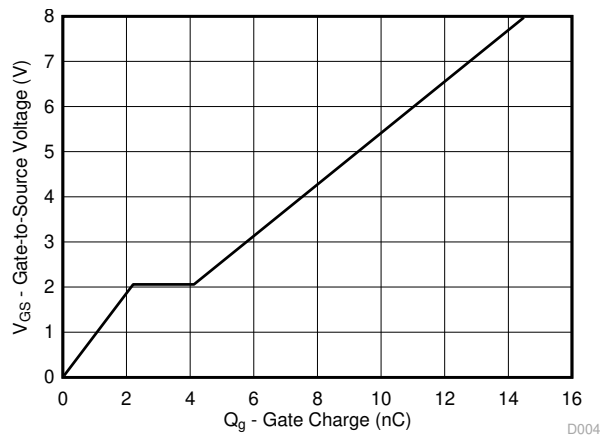


图 4-2. Saturation Characteristics



V_{S1S2} = 5 V

图 4-3. Transfer Characteristics



I_S = 5 A V_{S1S2} = 6 V

图 4-4. Gate Charge

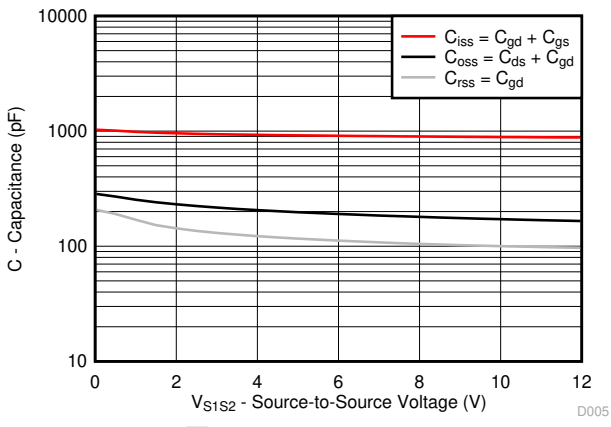
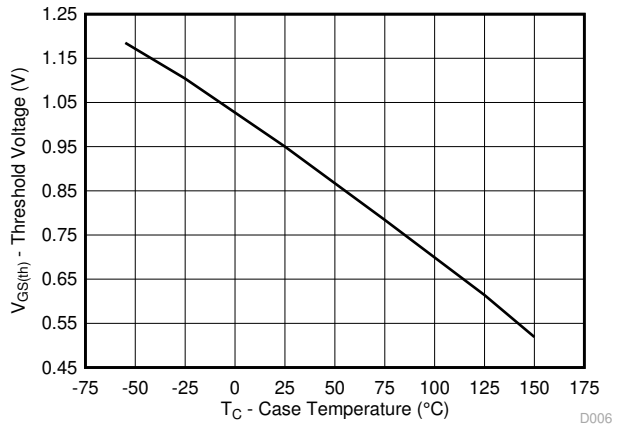


图 4-5. Capacitance



I_S = 250 µA

图 4-6. Threshold Voltage vs Temperature

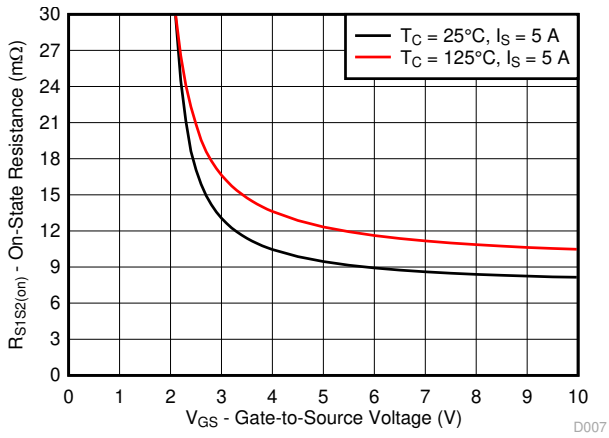
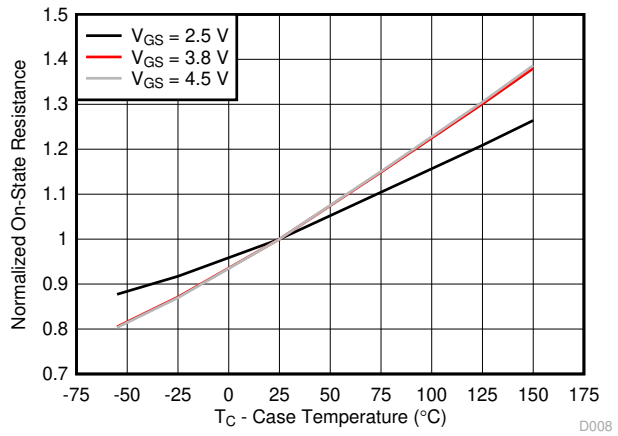


图 4-7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage



I_S = 5 A

图 4-8. Normalized On-State Resistance vs Temperature

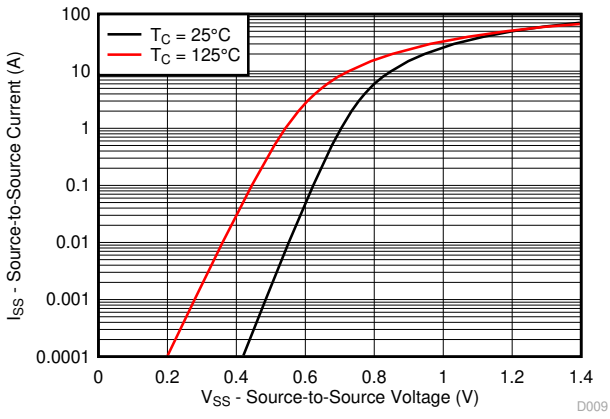
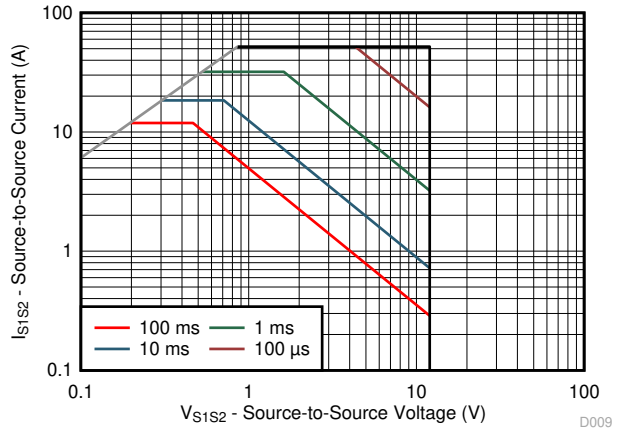


图 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JA}$ = 150°C/W

图 4-10. Maximum Safe Operating Area

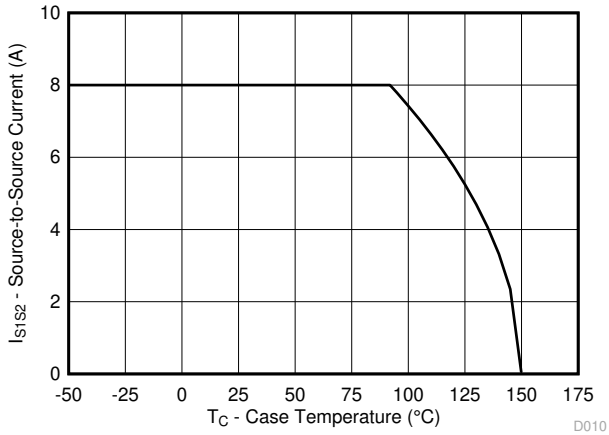


图 4-11. Maximum Source Current vs Temperature

5 Device and Documentation Support

5.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

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要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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5.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (February 2017) to Revision C (November 2023)	Page
• 将阈值电压 GS(th) 从 0.95V 更新为 1.0V	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated Source-to-source on resistance VGS = 2.5 V from 14 mΩ to 12 mΩ	3
• Updated Gate-to-source threshold voltage from 0.75 V min, 0.95 V typ, 1.25 V max to 0.7 V min, 1.0 V typ, 1.4 V max	3

Changes from Revision A (January 2016) to Revision B (February 2017)	Page
• Added Diode Characteristics ($V_{F(S-S)}$) in the *Electrical Characteristics* table	3
• Added 图 4-9 to *Typical MOSFET Characteristics* section	4

Changes from Revision * (November 2014) to Revision A (January 2016)	Page
• Improved graph setup for readability	4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD83325L	ACTIVE	PICOSTAR	YJE	6	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM		83325L	Samples
CSD83325LT	ACTIVE	PICOSTAR	YJE	6	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	83325L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

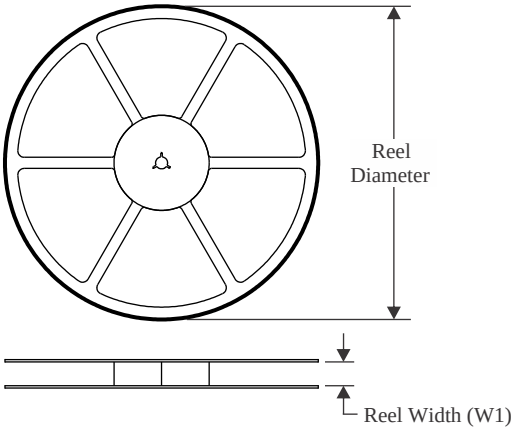
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

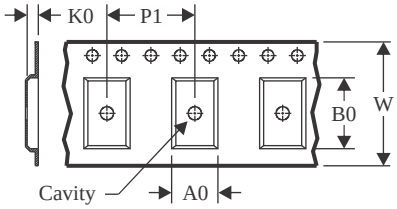
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

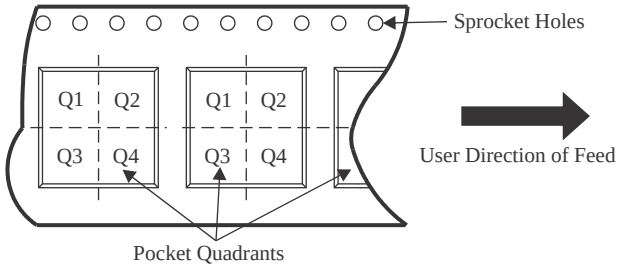


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

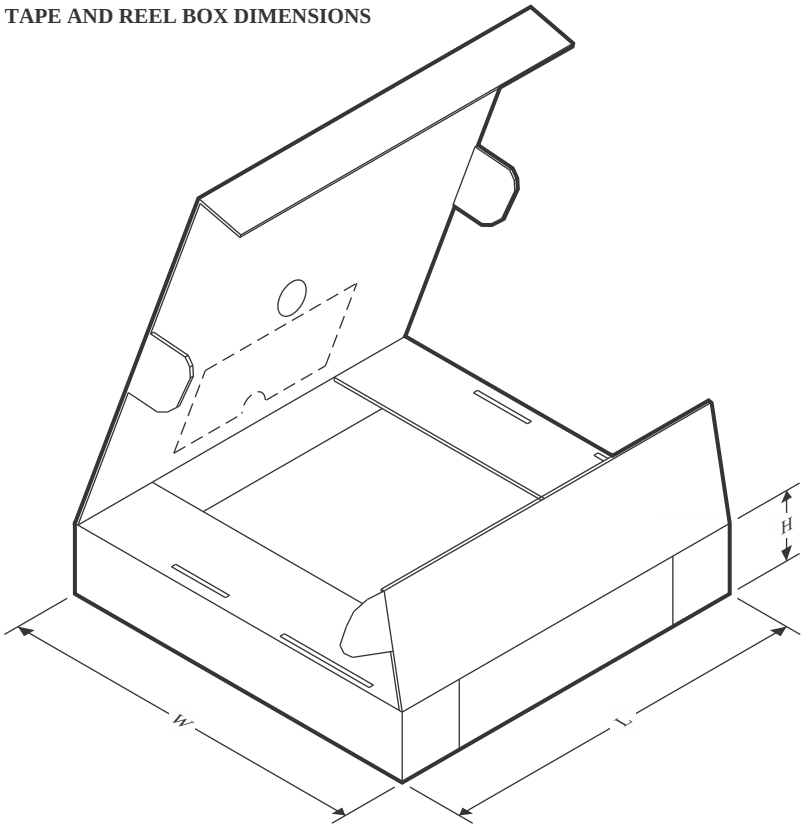
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD83325L	PICOSTAR	YJE	6	3000	180.0	8.4	1.25	2.34	0.32	4.0	8.0	Q1
CSD83325LT	PICOSTAR	YJE	6	250	180.0	8.4	1.25	2.34	0.32	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

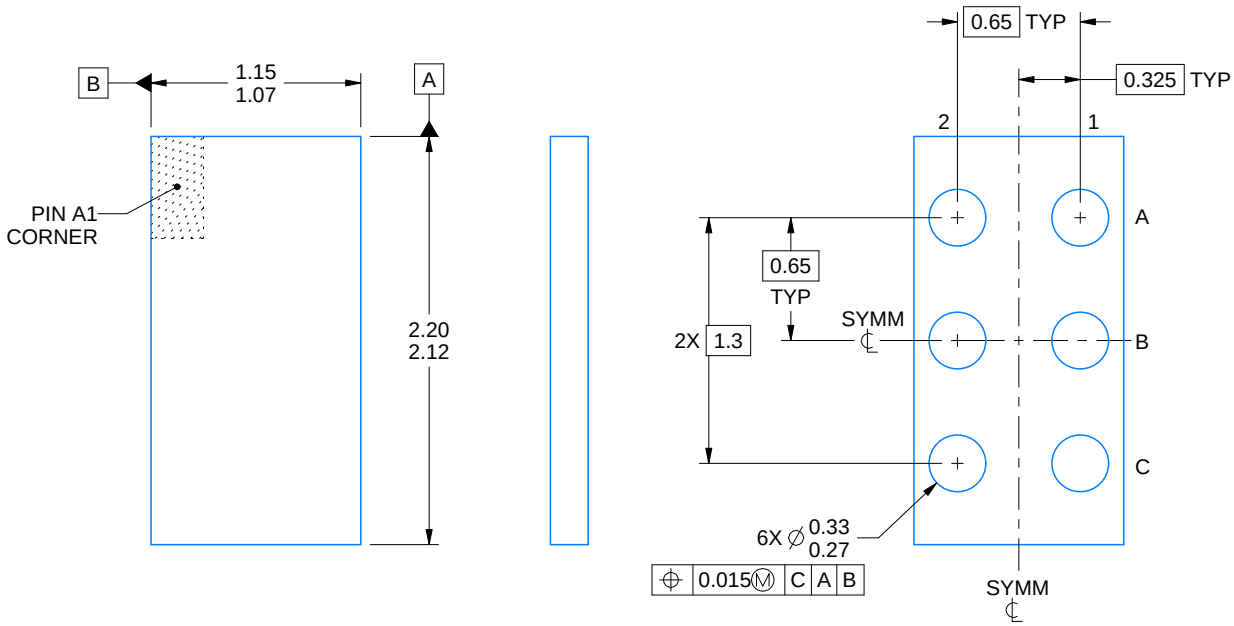
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD83325L	PICOSTAR	YJE	6	3000	182.0	182.0	20.0
CSD83325LT	PICOSTAR	YJE	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YJE0006A

PicoStar ™ - 0.22 mm max height

PicoStar



D: Max = 2.19 mm, Min = 2.13 mm

E: Max = 1.14 mm, Min = 1.08 mm

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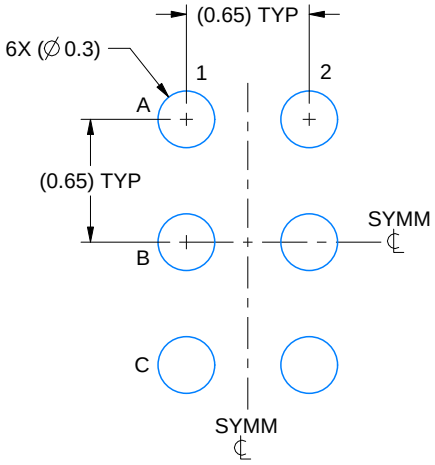
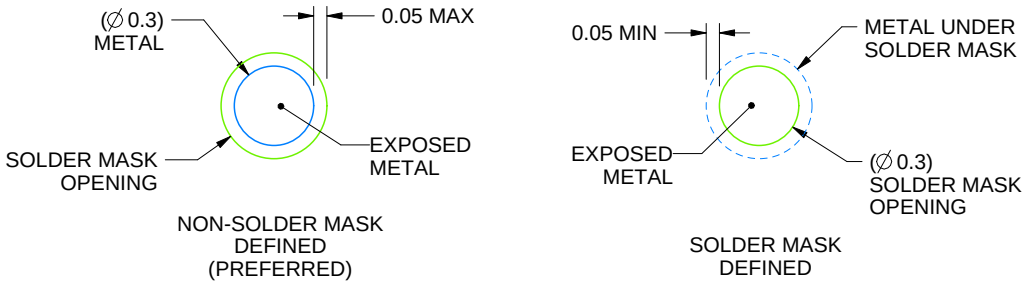
PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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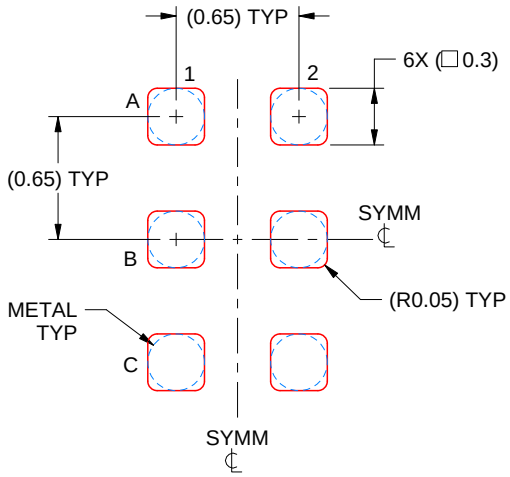
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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