CSD88539ND 双通道 60V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 雪崩级
- 无铅
- 符合 RoHS 标准
- 无卤素

2 应用范围

- 用于电机控制的半桥
- 同步降压转换器

3 说明

这款双通道 SO-8、60V、23mΩ NexFET™ 功率 MOSFET 设计用于在低电流电机控制应用中充当半桥。

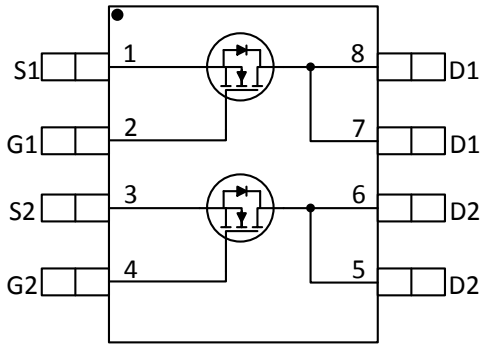


图 3-1. 顶视图

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	60		V
Q_g	栅极电荷总量 (10V)	7.2		nC
Q_{gd}	栅漏栅极电荷	1.1		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	27	mΩ
		V_{GS} = 10V	23	mΩ
$V_{GS(th)}$	阈值电压	3.0		V

订购信息(1)

器件	数量	介质	封装	出货
CSD88539ND	2500	13 英寸卷带	SO-8 塑料封装	卷带包装
CSD88539NDT	250	7 英寸卷带		

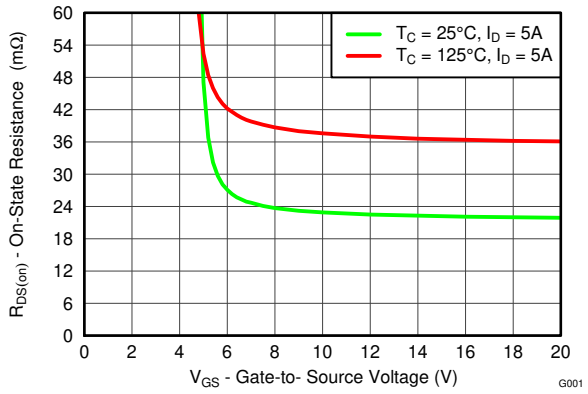
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

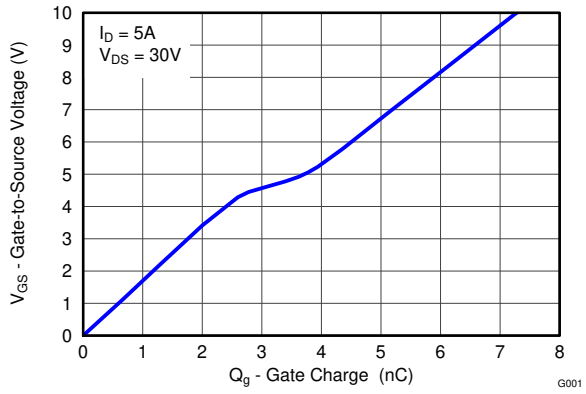
T_A = 25°C		值	单位
V_{DS}	漏源电压	60	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	15	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	11.7	
	持续漏极电流(1)	6.3	
I_{DM}	脉冲漏极电流(2)	46	A
P_D	功率耗散(1)	2.1	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D= 22A，L = 0.1mH，R_G = 25Ω	24	mJ

(1) $R_{\theta JA}$ = 60°C/W（典型值），在 0.06 英寸厚 FR4 PCB 上的 1 平方英寸、2oz. 铜焊盘上

(2) 脉冲持续时间 ≤ 300µs，占空比 ≤ 2%



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.6	3.0	3.6	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V, I_D = 5 A		27	34	mΩ
		V_{GS} = 10 V, I_D = 5 A		23	28	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 5 A		19		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		570	741	pF
C_{oss}	Output Capacitance			70	91	pF
C_{rss}	Reverse Transfer Capacitance			2.0	2.6	pF
R_G	Series Gate Resistance			6.6	13.2	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 30 V, I_D = 5 A		7.2	9.4	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			2.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.8		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		9.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 5 A, R_G = 0 Ω		5		ns
t_r	Rise Time			9		ns
$t_{d(off)}$	Turn Off Delay Time			14		ns
t_f	Fall Time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 5 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 5A, di/dt = 300A/µs		37		nC
t_{rr}	Reverse Recovery Time			21		ns

4.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JL}$	Junction-to-Lead Thermal Resistance(1)			20	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1) (2)			75	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

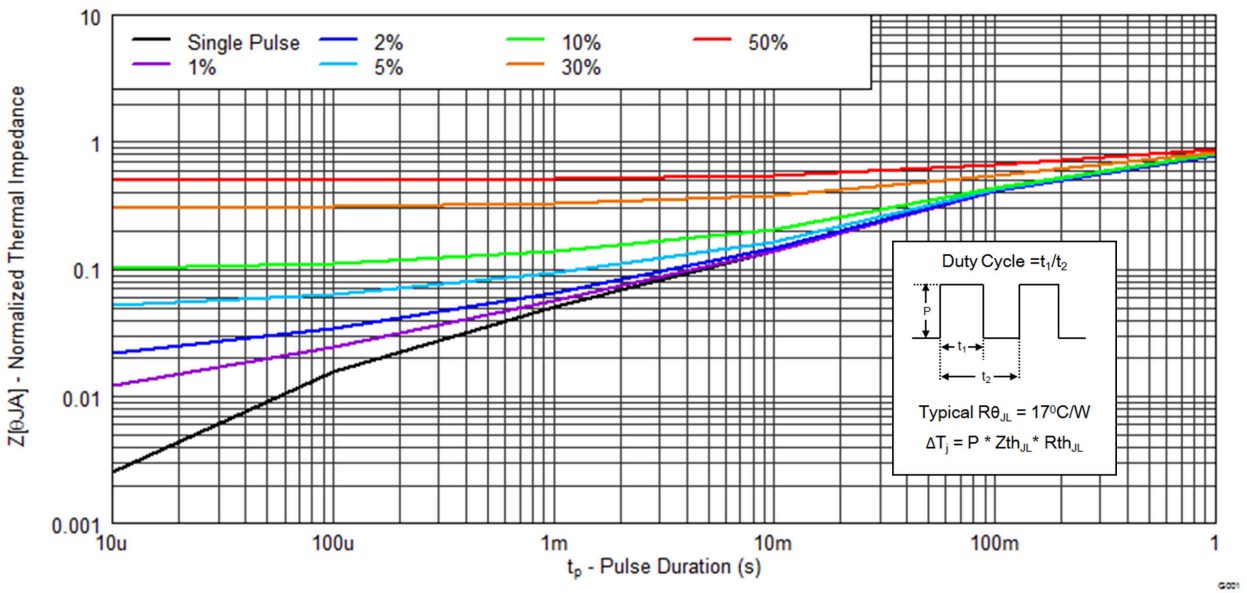


图 4-1. Transient Thermal Impedance

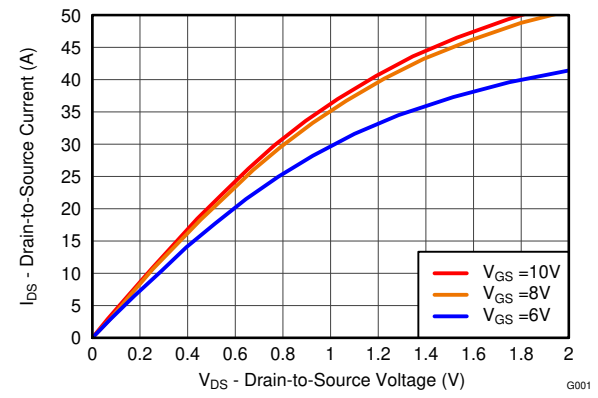


图 4-2. Saturation Characteristics

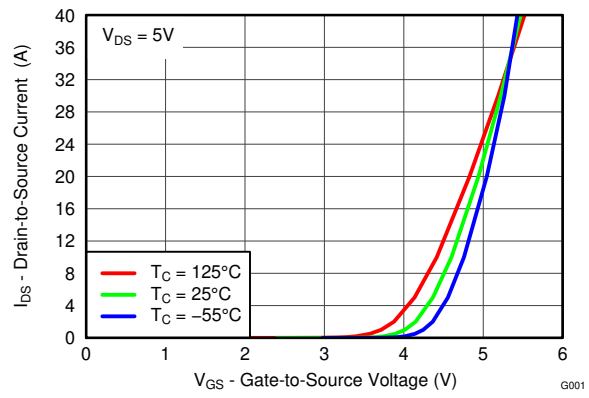


图 4-3. Transfer Characteristics

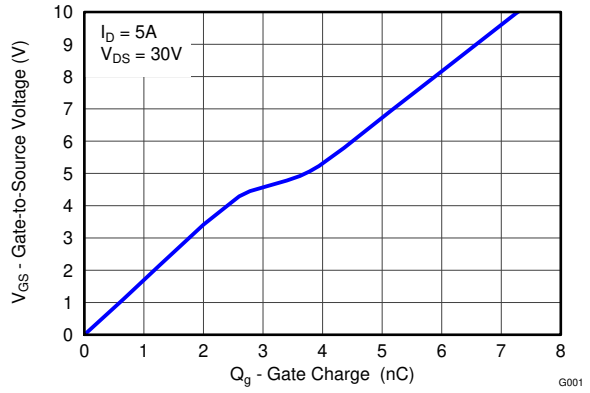


图 4-4. Gate Charge

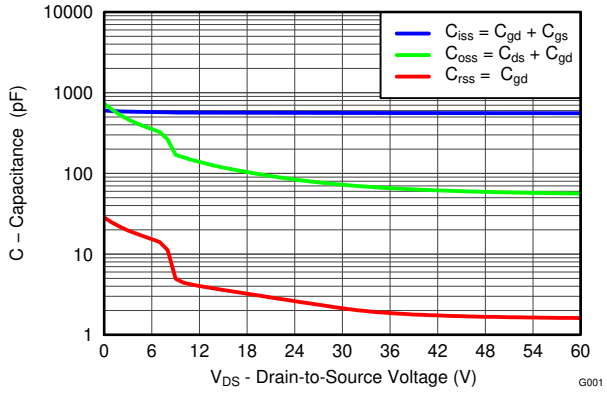


图 4-5. Capacitance

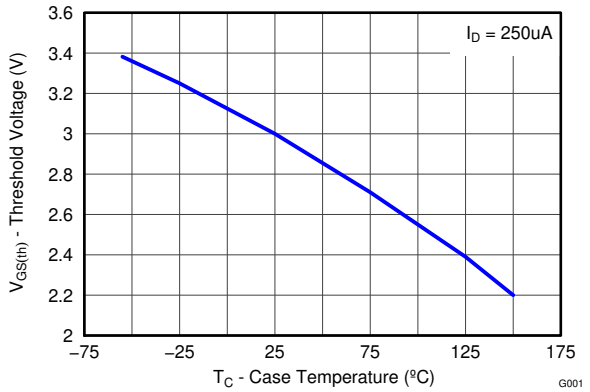


图 4-6. Threshold Voltage vs Temperature

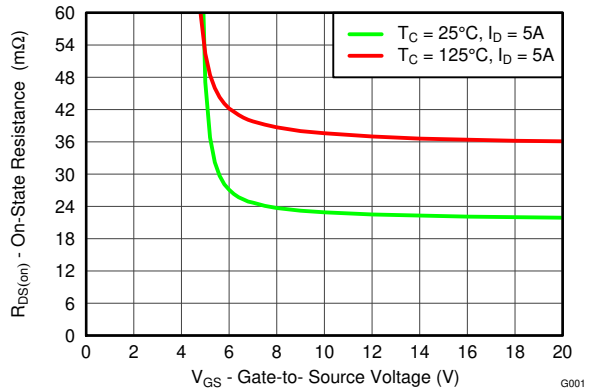


图 4-7. On-State Resistance vs Gate-to-Source Voltage

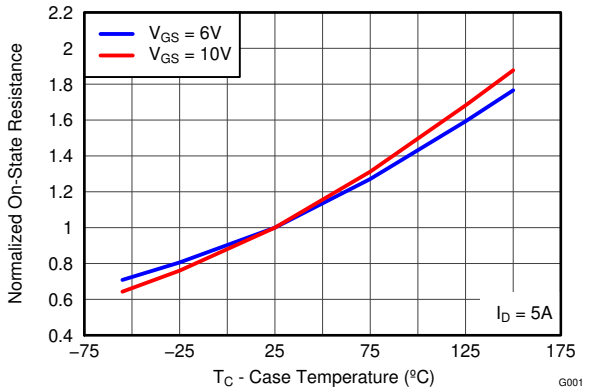


图 4-8. Normalized On-State Resistance vs Temperature

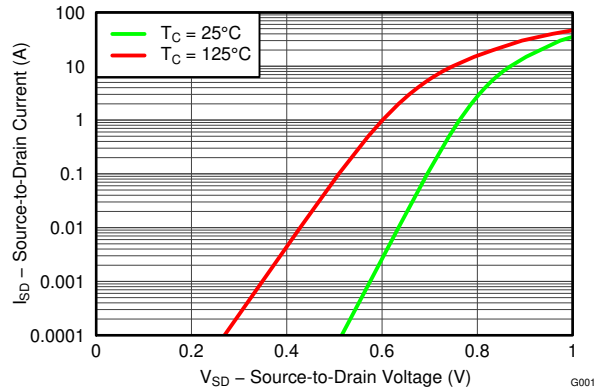


图 4-9. Typical Diode Forward Voltage

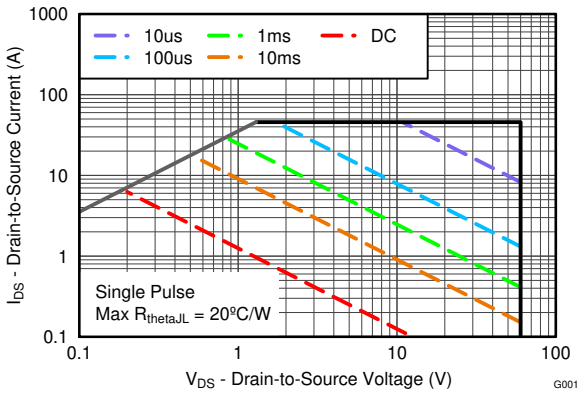


图 4-10. Maximum Safe Operating Area

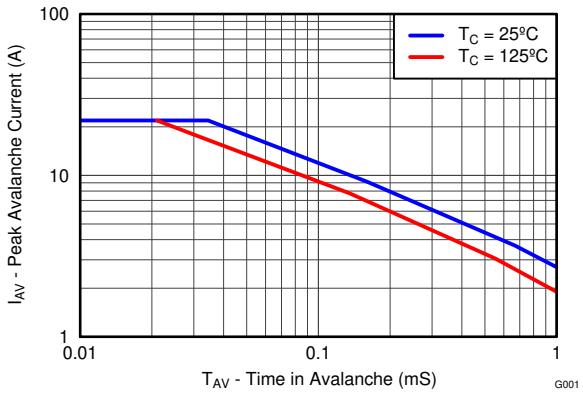


图 4-11. Single Pulse Unclamped Inductive Switching

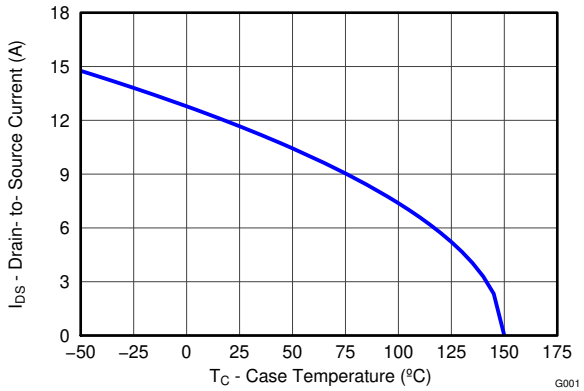


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Trademarks

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5.2 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (February 2014) to Revision A (December 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

7 Mechanical Data

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88539ND	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N	Samples
CSD88539NDT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

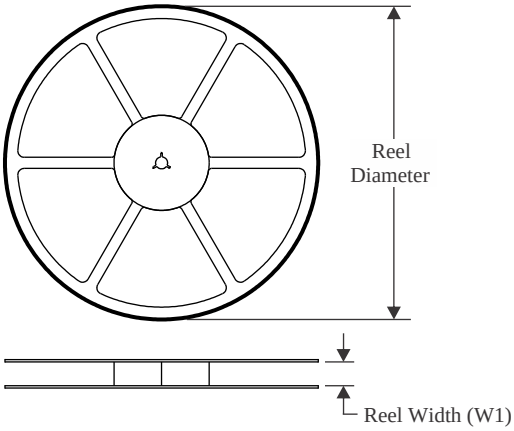
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

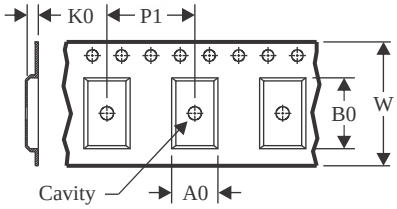
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

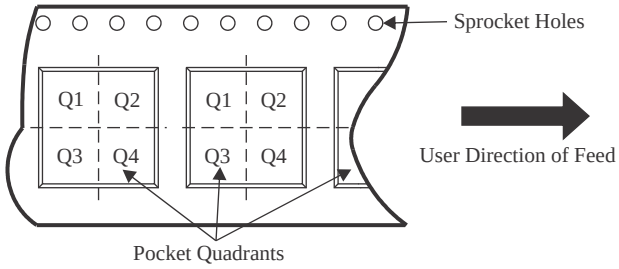


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

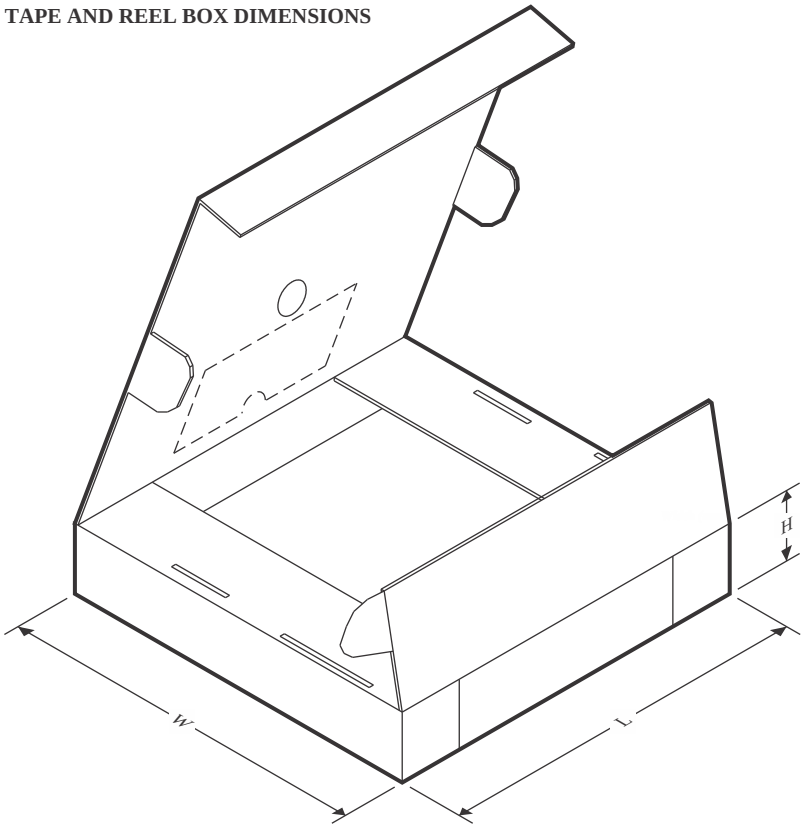
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD88539NDT	SOIC	D	8	250	178.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD88539NDT	SOIC	D	8	250	180.0	180.0	79.0

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