# CSD95379Q3M 同步降压 NexFET™ 功率级

## 1 特性

- 12A 电流下的系统效率达 92.5%
- 12A 电流时 1.8W 的超低功率损耗
- 最大额定持续电流为 20A，峰值电流为 45A
- 高频运行（高达 2MHz）
- 高密度 – 3.3mm × 3.3mm 小外形尺寸无引线封装 (SON) 尺寸
- 超低电感封装
- 系统已优化的印刷电路板 (PCB) 封装
- 低静态 (LQ) 和超低静态 (ULQ) 电流模式
- 与 3.3V 和 5V 脉宽调制 (PWM) 信号兼容
- 支持强制连续传导模式 (FCCM) 的二极管仿真模式
- 三态 PWM 输入
- 集成型自举二极管
- 击穿保护
- 符合 RoHS 标准 - 无铅引脚镀层
- 无卤素

## 2 应用范围

- NVDC 笔记本电脑/超极本 PC
- 平板电脑
- 网络互联、电信和计算系统中的负载点同步降压

## 3 说明

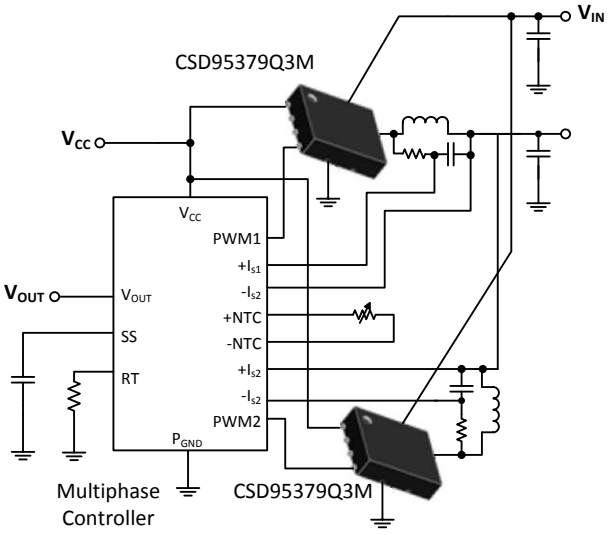
CSD95379Q3M NexFET™ 功率级的设计经过高度优化，适用于高功率、高密度同步降压转换器。 这个产品集成了驱动器集成电路 (IC) 和 NexFET 技术来完善功率级开关功能。 此驱动器 IC 具有一个内置可选二极管仿真功能，此功能可启用断续传导模式 (DCM) 运行来提升轻负载效率。 此外，驱动器 IC 支持 ULQ 模式，此模式支持针对 Windows® 8 的联网待机功能。 借助于三态 PWM 输入，静态电流可减少至 130µA，并支持立即响应。 当 SKIP# 保持在三态时，电流可减少至 8µA（恢复切换通常需要 20µs）。 这个组合在小型 3.3mm x 3.3mm 外形尺寸封装中提供高电流、高效和高速开关功能。 此外，PCB 封装已经过优化，可帮助减少设计时间并简化总体系统设计的完成。

器件信息(1)

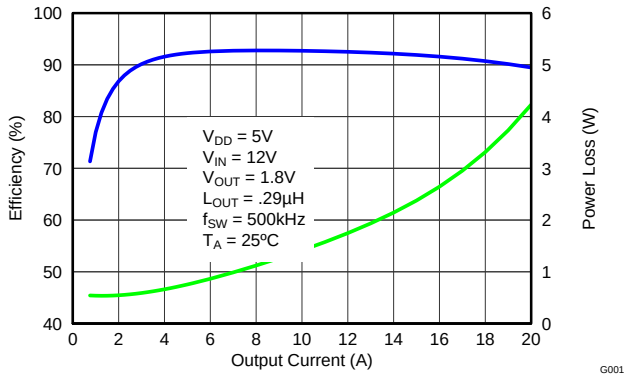
| 器件 | 介质 | 数量 | 封装 | 出货 |
|---|---|---|---|---|
| CSD95379Q3M | 13 英寸卷带 | 2500 | SON 3.3mm x 3.3mm 塑料封装 | 卷带封装 |
| CSD95379Q3MT | 7 英寸卷带 | 250 | | |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

应用图表




典型功率级效率与功率损耗



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## 4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (November 2014) to Revision C** **Page**

- Added footnote 1 under *Recommended Operating Conditions*. ... 4

**Changes from Revision A (August 2014) to Revision B** **Page**

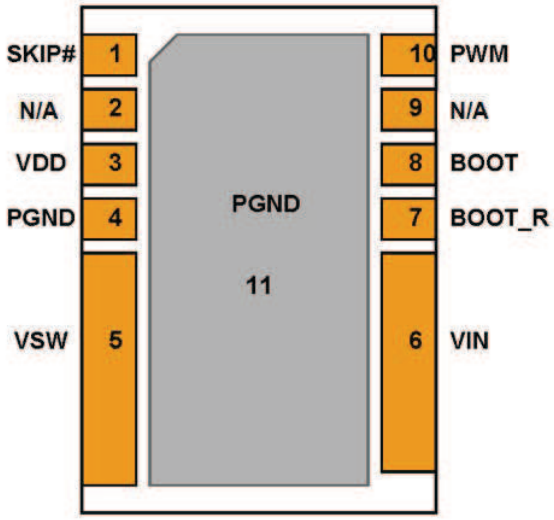
- 已更改器件状态至量产数据。 ... 1

**Changes from Original (April 2014) to Revision A** **Page**

- Increased $V_{IN}$ from 14.5 V to 16 V ... 4

# 5 Pin Configuration and Functions

**Top View**




**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NUMBER | |
| SKIP# | 1 | This pin enables the Diode Emulation function. When this pin is held low, Diode Emulation Mode is enabled for the sync FET. When SKIP# is high, the CSD95379Q3M operates in Forced Continuous Conduction Mode. A tri-state voltage on SKIP# puts the driver into a very-low power state. |
| $V_{DD}$ | 3 | Supply voltage to gate drivers and internal circuitry. |
| $P_{GND}$ | 4 | Power ground. Needs to be connected to pin 11 on the PCB. |
| $V_{SW}$ | 5 | Voltage switching node – pin connection to output inductor. |
| $V_{IN}$ | 6 | Input voltage pin. Connect input capacitors to close this pin. |
| BOOT_R | 7 | Bootstrap capacitor connection. Connect a minimum 0.1 µF 16 V X5R, ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated. |
| BOOT | 8 | |
| PWM | 10 | Pulse-width-modulated tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Open or High Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time ($T_{3HT}$) |
| $P_{GND}$ | 11 | Power ground. Needs to be connected to pin 4 on the PCB. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

$T_A$ = 25°C (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{IN}$ to $P_{GND}$ | –0.3 | 20 | V |
| $V_{SW}$ to $P_{GND}$ , $V_{IN}$ to $V_{SW}$ | –0.3 | 20 | V |
| $V_{SW}$ to $P_{GND}$, $V_{IN}$ to $V_{SW}$ (<10 ns) | –7 | 23 | V |
| $V_{DD}$ to $P_{GND}$ | –0.3 | 6 | V |
| PWM, SKIP# to $P_{GND}$ | –0.3 | 6 | V |
| BOOT to $P_{GND}$ | –0.3 | 25 | V |
| BOOT to $P_{GND}$ (<10 ns) | –2 | 28 | V |
| BOOT to BOOT_R | –0.3 | 6 | V |
| Power Dissipation, $P_D$ | | 6 | W |
| Operating Temperature Range, $T_J$ | –40 | 150 | °C |

(1) Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –55 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) | –2000 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –500 | 500 | V |

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

$T_A$ = 25° (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Gate Drive Voltage | | 4.5 | 5.5 | V |
| $V_{IN}$ | Input Supply Voltage(1) | | | 16 | V |
| $I_{OUT}$ | Continuous Output Current | $V_{IN}$ = 12 V, $V_{DD}$ = 5 V, $V_{OUT}$ = 1.8 V, $f_{SW}$ = 500 kHz, $L_{OUT}$ = 0.29 µH(2) | | 20 | A |
| $I_{OUT-PK}$ | Peak Output Current(3) | | | 45 | A |
| $f_{SW}$ | Switching Frequency | $C_{BST}$ = 0.1 µF (min) | | 2000 | kHz |
| | On Time Duty Cycle | | | 85% | |
| | Minimum PWM On Time | | 40 | | ns |
| | Operating Temperature | | –40 | 125 | °C |

(1) Operating at high $V_{IN}$ can create excessive AC voltage overshoots on the switch node ($V_{SW}$) during MOSFET switching transients. For reliable operation, the switch node ($V_{SW}$) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across $V_{IN}$ to $P_{GND}$ pins.
(3) System conditions as defined in Note 1. Peak Output Current is applied for $t_p$ = 10 ms, duty cycle ≤1%

## 6.4 Thermal Information

$T_A$ = 25°C (unless otherwise noted)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC(top)}$ | Junction-to-Case Thermal Resistance (Top of package)(1) | | | 22.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-Board Thermal Resistance(2) | | | 2.5 | |

(1) $R_{\theta JC(top)}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz (.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches, 0.06 inch (1.52 mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

## 6.5 Electrical Characteristics

$T_A$ = 25°C, $V_{DD}$ = POR to 5.5 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$P_{LOSS}$** | | | | | |
| Power Loss(1) | $V_{IN}$ = 12 V, $V_{DD}$ = 5 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 12 A, $f_{SW}$ = 500 kHz, $L_{OUT}$ = 0.29 µH , $T_J$ = 25°C | | 1.8 | | W |
| Power Loss(2) | $V_{IN}$ = 12 V, $V_{DD}$ = 5 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 12 A, $f_{SW}$ = 500 kHz, $L_{OUT}$ = 0.29 µH , $T_J$ = 125°C | | 2.3 | | W |
| **$V_{IN}$** | | | | | |
| $V_{IN}$ Quiescent Current, $I_Q$ | PWM = Float, $V_{IN}$ = 14.5 V, $V_{DD}$ = 5 V | | | 1 | µA |
| **$V_{DD}$** | | | | | |
| Standby Supply Current, $I_{DD}$ | PWM = Float, VSKIP# = $V_{DD}$ or 0 V | | 130 | | µA |
| | VSKIP# = Float | | 8 | | µA |
| Operating Supply Current, $I_{DD}$ | PWM = 50% Duty cycle, $f_{SW}$ = 500 kHz | | 5.5 | | mA |
| **POWER-ON RESET AND UNDERVOLTAGE LOCKOUT** | | | | | |
| Power-On Reset, $V_{DD}$ Rising | | | | 4.15 | V |
| UVLO, $V_{DD}$ Falling | | 3.7 | | | V |
| Hysteresis | | | 0.2 | | mV |
| **PWM AND SKIP# I/O SPECIFICATIONS** | | | | | |
| Input Impedance, $R_I$ | Pull up to $V_{DD}$ | | 1700 | | kΩ |
| | Pull Down to GND | | 800 | | kΩ |
| Logic Level High, $V_{IH}$ | | 2.65 | | | V |
| Logic Level Low, $V_{IL}$ | | | | 0.6 | V |
| Hysteresis, $V_{IH}$ | | | 0.2 | | V |
| Tri-State Voltage, $V_{TS}$ | | 1.3 | | 2 | V |
| Tri-State Activation (Falling) PWM, Time, $t_{HOLD(off1)}$(2) | | | 60 | | ns |
| Tri-State Activation (Rising) PWM, Time, $t_{HOLD(off2)}$(2) | | | 60 | | ns |
| Tri-State Activation (Falling) SKIP#, Time, $t_{TSKF}$(2) | | | 1 | | ns |
| Tri-State Activation (Rising) SKIP#, Time, $t_{TSKR}$(2) | | | 1 | | ns |
| Tri-State Exit Time PWM, $t_{3RD(PWM)}$(2) | | | | 100 | ns |
| Tri-State Exit Time SKIP#, $t_{3RD(SKIP\#)}$(2) | | | | 50 | us |
| **BOOTSTRAP SWITCH** | | | | | |
| Forward Voltage, $V_{FBOOT}$ | Measured from $V_{DD}$ to $V_{BOOT}$, $I_F$ = 20 mA | | 120 | 240 | mV |
| Reverse Leakage, $I_{RBOOT}$(1) | $V_{BOOT}$ – $V_{DD}$ = 25 V | | | 2 | µA |

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across $V_{IN}$ to $P_{GND}$ pins.
(2) Specified by design

## 6.6 Typical Characteristics

$T_J$ = 125°C, unless stated otherwise. The Typical CSD95379Q3M System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness. See the *Application and Implementation* section for detailed explanation.

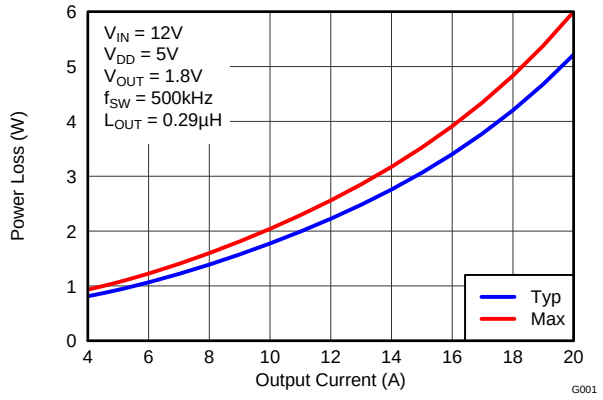



**Figure 1. Power Loss vs Output Current**

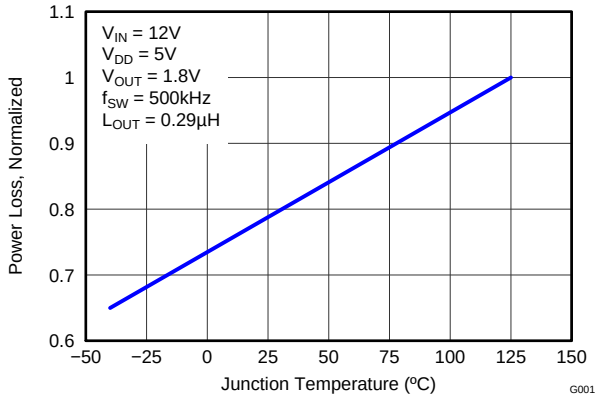



**Figure 2. Power Loss vs Temperature**

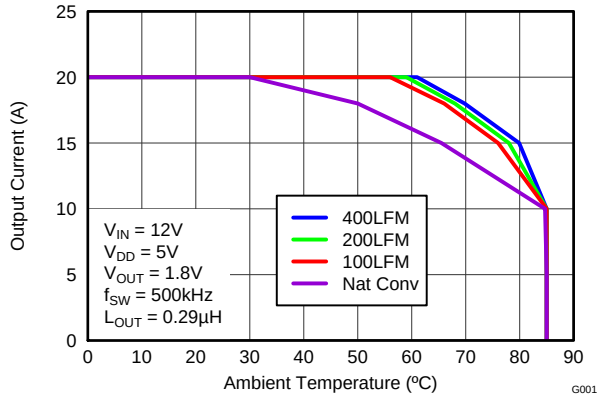



**Figure 3. Safe Operating Area (SOA) – PCB Horizontal Mount (1)**

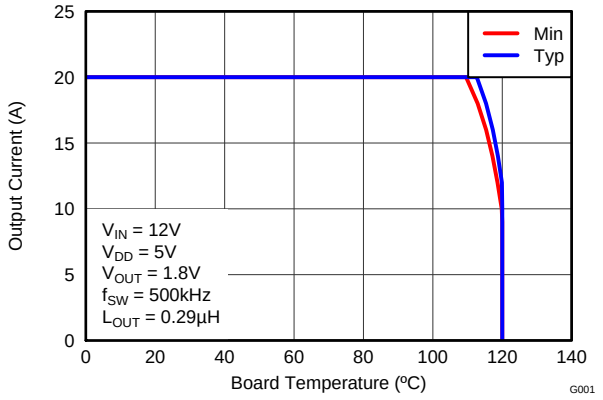



**Figure 4. Typical SOA (1)**

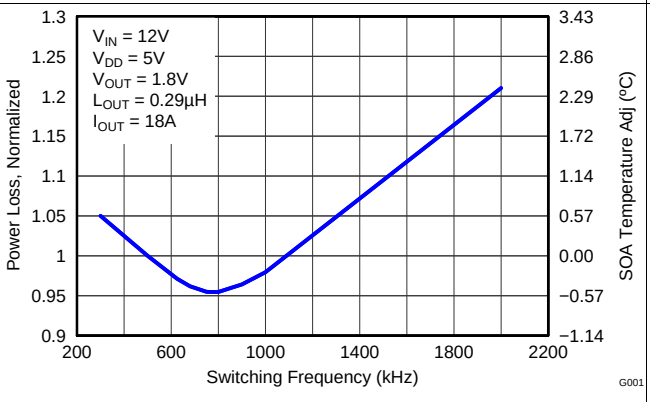



**Figure 5. Normalized Power Loss vs Frequency**

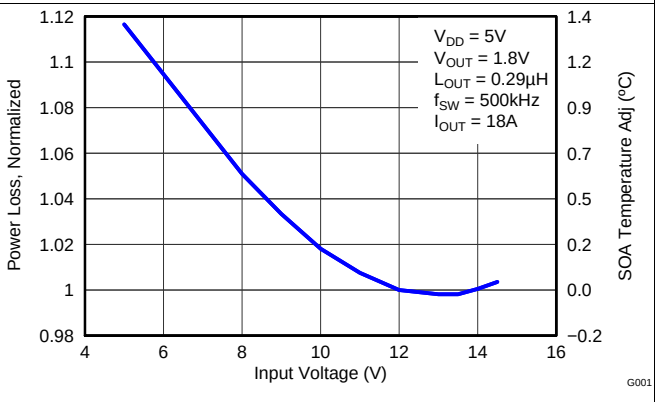



**Figure 6. Normalized Power Loss vs Input Voltage**

## Typical Characteristics (continued)

$T_J$ = 125°C, unless stated otherwise. The Typical CSD95379Q3M System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness. See the *Application and Implementation* section for detailed explanation.

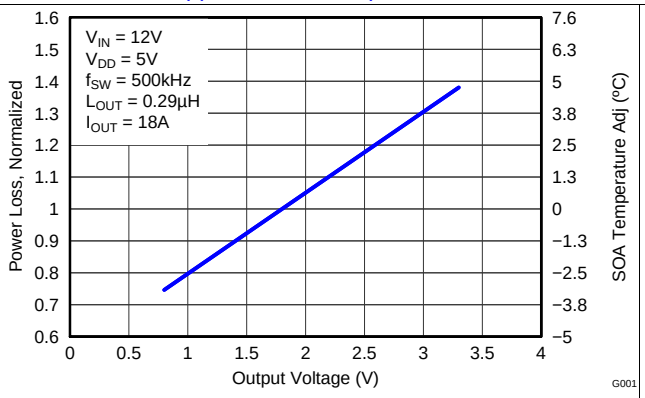



**Figure 7. Normalized Power Loss vs Output Voltage**

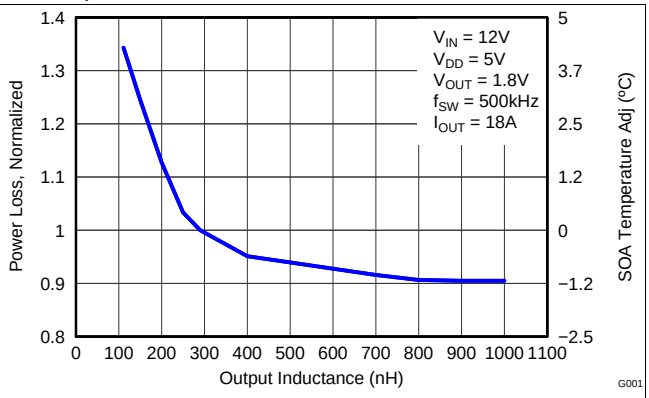



**Figure 8. Normalized Power Loss vs Output Inductance**

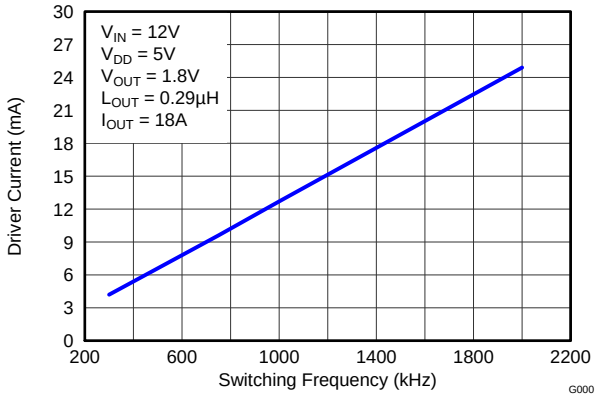
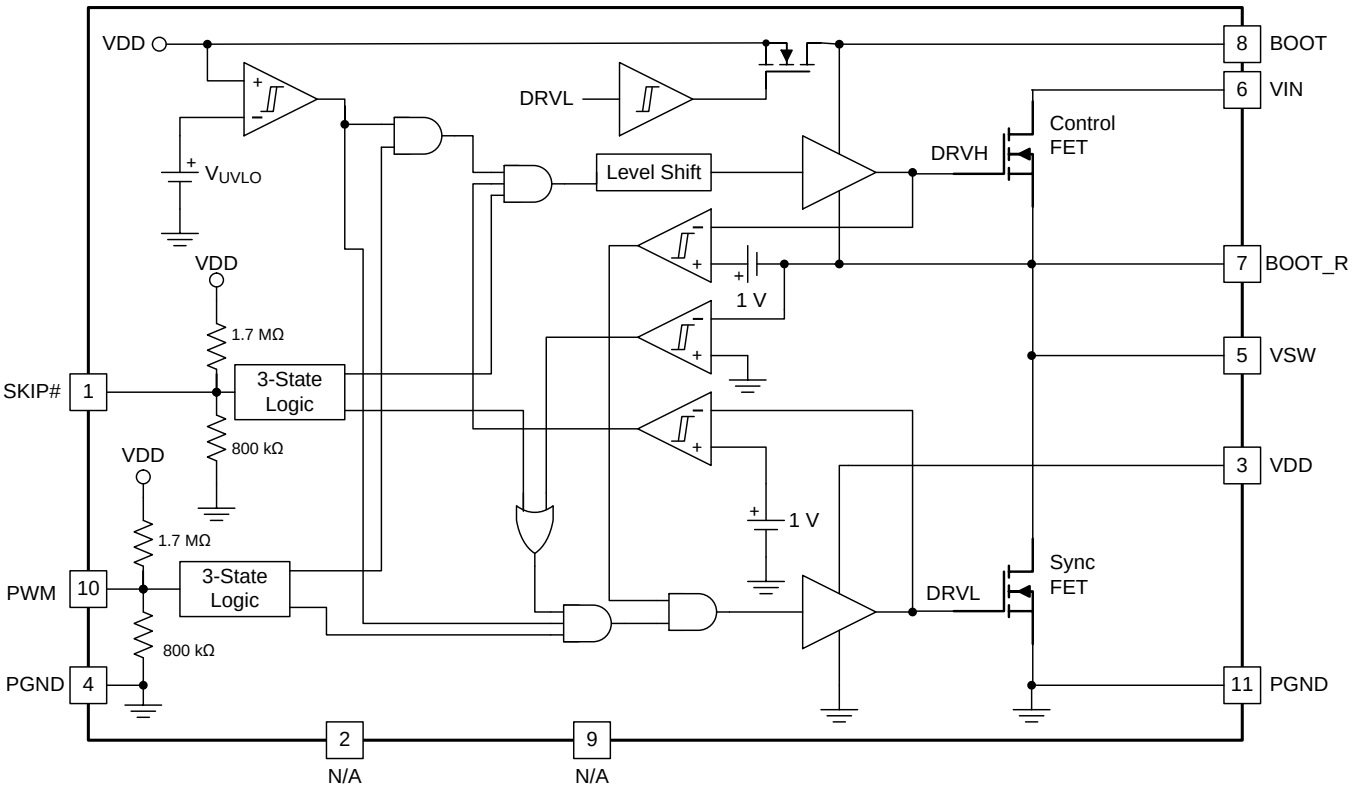



**Figure 9. Driver Current vs Frequency**

# 7 Detailed Description

## 7.1 Functional Block Diagram




## 7.2 Feature Description

### 7.2.1 Functional Description

#### *7.2.1.1 Powering CSD95379Q3M and Gate Drivers*

An external $V_{DD}$ voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETS. TI recommends a 1 µF 10 V X5R or higher ceramic capacitor to bypass $V_{DD}$ pin to $P_{GND}$. A bootstrap circuit to provide gate drive power for the control FET is also included. The bootstrap supply to drive the control FET is generated by connecting a 100 nF 16 V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional $R_{BOOT}$ resistor can be used to slow down the turn on speed of the control FET and reduce voltage spikes on the $V_{SW}$ node. A typical 1 to 4.7 Ω value is a compromise between switching loss and $V_{SW}$ spike amplitude.

## Feature Description (continued)

### 7.2.2 Undervoltage Lockout (UVLO) Protection

The UVLO comparator evaluates the VDD voltage level. As $V_{VDD}$ rises, both the control FET and sync FET gates hold actively low at all times until $V_{VDD}$ reaches the higher UVLO threshold ($V_{UVLO\_H}$). Then, the driver becomes operational and responds to PWM and SKIP# commands. If VDD falls below the lower UVLO threshold ($V_{UVLO\_L}$ = $V_{UVLO\_H}$ – Hysteresis), the device disables the driver and drives the outputs of the control FET and sync FET gates actively low. Figure 10 shows this function.

**CAUTION**

Do not start the driver in the very low power mode (SKIP# = Tri-state).

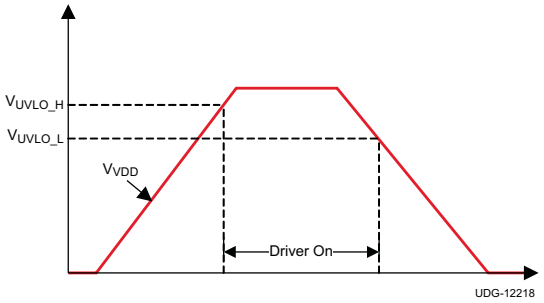



**Figure 10. UVLO Operation**

### 7.2.3 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pullup to maintain the voltage within the tri-state window during low-power modes. Operation into and out of tri-state mode follows the timing diagram outlined in Figure 11.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined as the PWM voltage range between PWM logic high ($V_{IH}$) and logic low ($V_{IL}$) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3 V (typical) and 5 V (typical) PWM drive signals.

When the PWM exits tri-state, the driver enters CCM for a period of 4 µs, regardless of the state of the SKIP# pin. Normal operation requires this time period in order for the auto-zero comparator to resume.

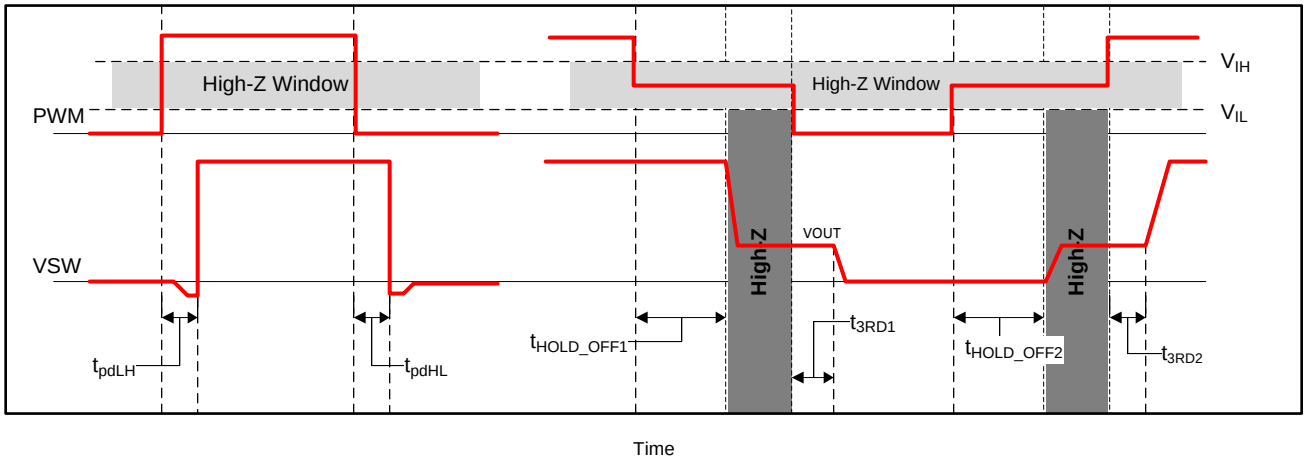



**Figure 11. PWM Tri-State Timing Diagram**

## Feature Description (continued)

### 7.2.4 SKIP# Pin

The SKIP# pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When SKIP# is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When SKIP# is high, the ZX comparator disables, and the converter enters FCCM mode. When both SKIP# and PWM are tri-stated, normal operation forces the gate driver outputs low and the driver enters a low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When SKIP# is pulled low, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

Table 1 shows the logic functions of UVLO, PWM, SKIP#, the control FET gate, and the sync FET gate.

**Table 1. Logic Functions of the Driver IC**

| UVLO | PWM | SKIP# | Sync FET Gate | Control FET Gate | MODE |
|---|---|---|---|---|---|
| Active | — | — | Low | Low | Disabled |
| Inactive | Low | Low | High(1) | Low | DCM(1) |
| Inactive | Low | High | High | Low | FCCM |
| Inactive | High | H or L | Low | High | — |
| Inactive | Tri-state | H or L | Low | Low | LQ |
| Inactive | — | Tri-state | Low | Low | ULQ |

(1) Until zero crossing protection occurs.

### 7.2.5 Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a valley, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The Power Stage CSD95379Q3M is a highly optimized design for synchronous buck applications using NexFET devices with a 5 V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

### 8.1.1 Power Loss Curves

MOSFET-centric parameters such as $R_{DS(ON)}$ and $Q_{gd}$ are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, TI has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD95379Q3M as a function of load current. This curve is measured by configuring and running the CSD95379Q3M as it would be in the final application (see Figure 12). The measured power loss is the CSD95379Q3M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperature of $T_J$ = 125°C under isothermal test conditions.

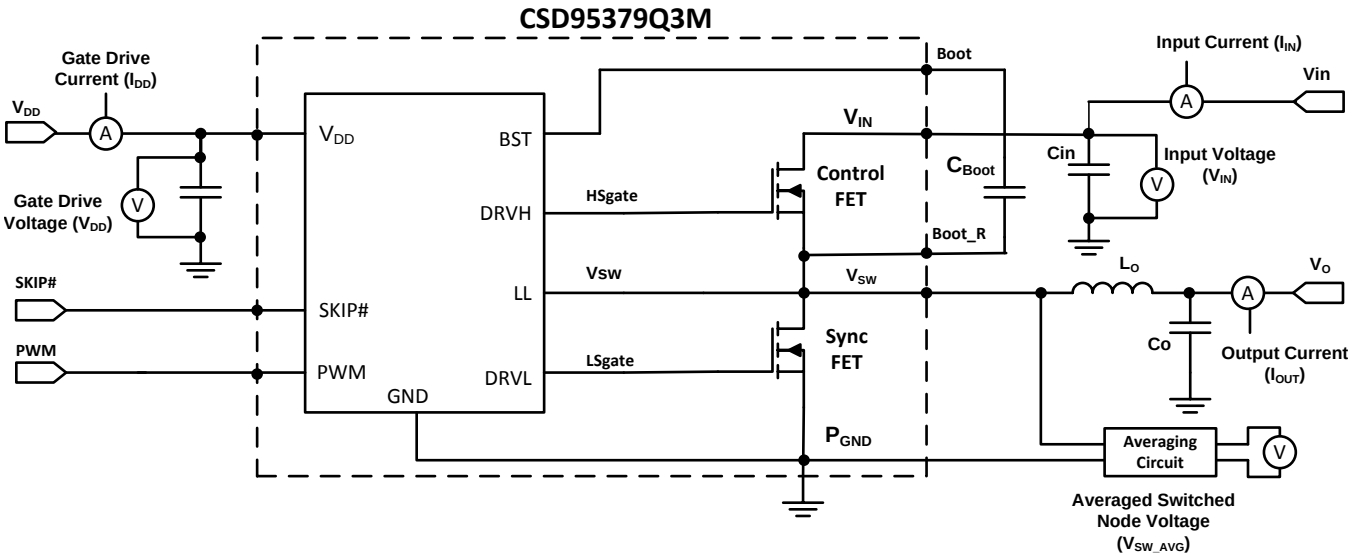



**Figure 12. Power Loss Test Circuit**

### 8.1.2 Safe Operating Curves (SOA)

The SOA curves in the CSD95379Q3M data sheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 and Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1 oz. copper thickness.

## Application Information (continued)

### 8.1.3 Normalized Curves

The normalized curves in the CSD95379Q3M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of systems conditions. The primary y-axis is the normalized change in power loss and the secondary y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

### 8.1.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see the *Design Example*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps engineers should take to predict product performance for any set of system conditions.

#### *8.1.4.1 Design Example*

Operating Conditions: Output Current ($I_{OUT}$) = 10 A, Input Voltage ($V_{IN}$ ) = 8 V, Output Voltage ($V_{OUT}$) = 1.5 V, Switching Frequency ($f_{SW}$) = 1500 kHz, Output Inductor ($L_{OUT}$) = 0.2 µH

#### *8.1.4.2 Calculating Power Loss*

- Typical Power Loss at 10 A = 1.8 W (Figure 1)
- Normalized Power Loss for switching frequency ≈ 1.09 (Figure 5)
- Normalized Power Loss for input voltage ≈ 1.05 (Figure 6)
- Normalized Power Loss for output voltage ≈ 0.92 (Figure 7)
- Normalized Power Loss for output inductor ≈ 1.1 (Figure 8)
- **Final calculated Power Loss = 1.8 W × 1.09 × 1.05 × 0.92 × 1.1 ≈ 2.1 W**

#### *8.1.4.3 Calculating SOA Adjustments*

- SOA adjustment for switching frequency ≈ 1.1°C (Figure 5)
- SOA adjustment for input voltage ≈ 0.6C (Figure 6)
- SOA adjustment for output voltage ≈ –0.9°C (Figure 7)
- SOA adjustment for output inductor ≈ 1.3°C (Figure 8)
- **Final calculated SOA adjustment = 1.1 + 0.6 + (–0.9) + 1.3 ≈ 2.1°C**

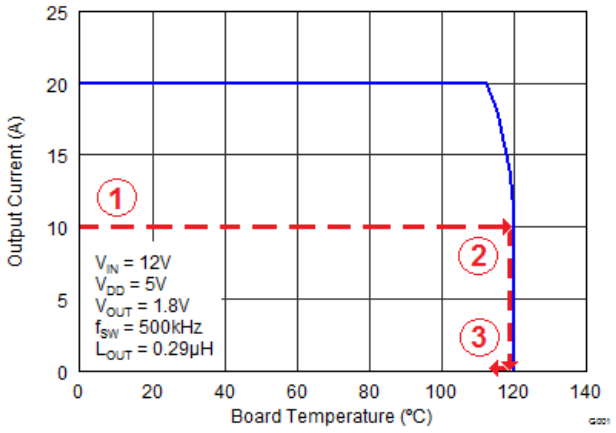



**Figure 13. Power Stage CSD95379Q3M SOA**

In the *Design Example*, the estimated power loss of the CSD95379Q3M would increase to 2.1 W. In addition, the maximum allowable board or ambient temperature, or both, would have to decrease by 2.1°C. Figure 13 graphically shows how the SOA curve would be adjusted accordingly.

## Application Information (continued)

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board or ambient temperature of 2.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

# 9 Layout

## 9.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter follows.

### 9.1.1 Electrical Performance

The CSD95379Q3M has the ability to switch at voltage rates greater than 10 kV/µs. Take special care with the PCB layout design and placement of the input capacitors, inductor, and output capacitors.

- The placement of the input capacitors relative to $V_{IN}$ and $P_{GND}$ pins of CSD95379Q3M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the $V_{IN}$ and $P_{GND}$ pins (see Figure 14). The example in Figure 14 uses 1 × 1 nF 0402 25 V and 3 × 10 µF 1206 25 V ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C8, C9, C10 and C11 should follow in order.
- The bootstrap capacitor C7 0.1 µF 0603 16 V ceramic capacitor should be closely connected between BOOT and BOOT_R pins.
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD95379Q3M $V_{SW}$ pins. Minimizing the $V_{SW}$ node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. (2)

### 9.1.2 Thermal Performance

The CSD95379Q3M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that wicks down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 14 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

## 9.2 Layout Example

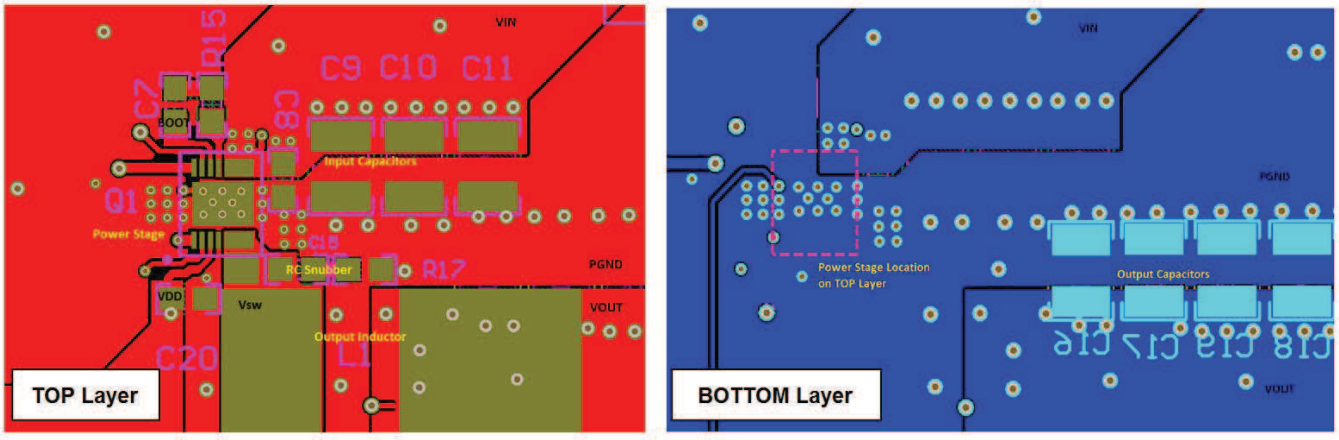



**Figure 14. Recommended PCB Layout (Top Down View)**

(2) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

# 10 器件和文档支持

## 10.1 商标

NexFET is a trademark of Texas Instruments.
Windows is a registered trademark of Microsoft Corporation.
All other trademarks are the property of their respective owners.

## 10.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 10.3 术语表

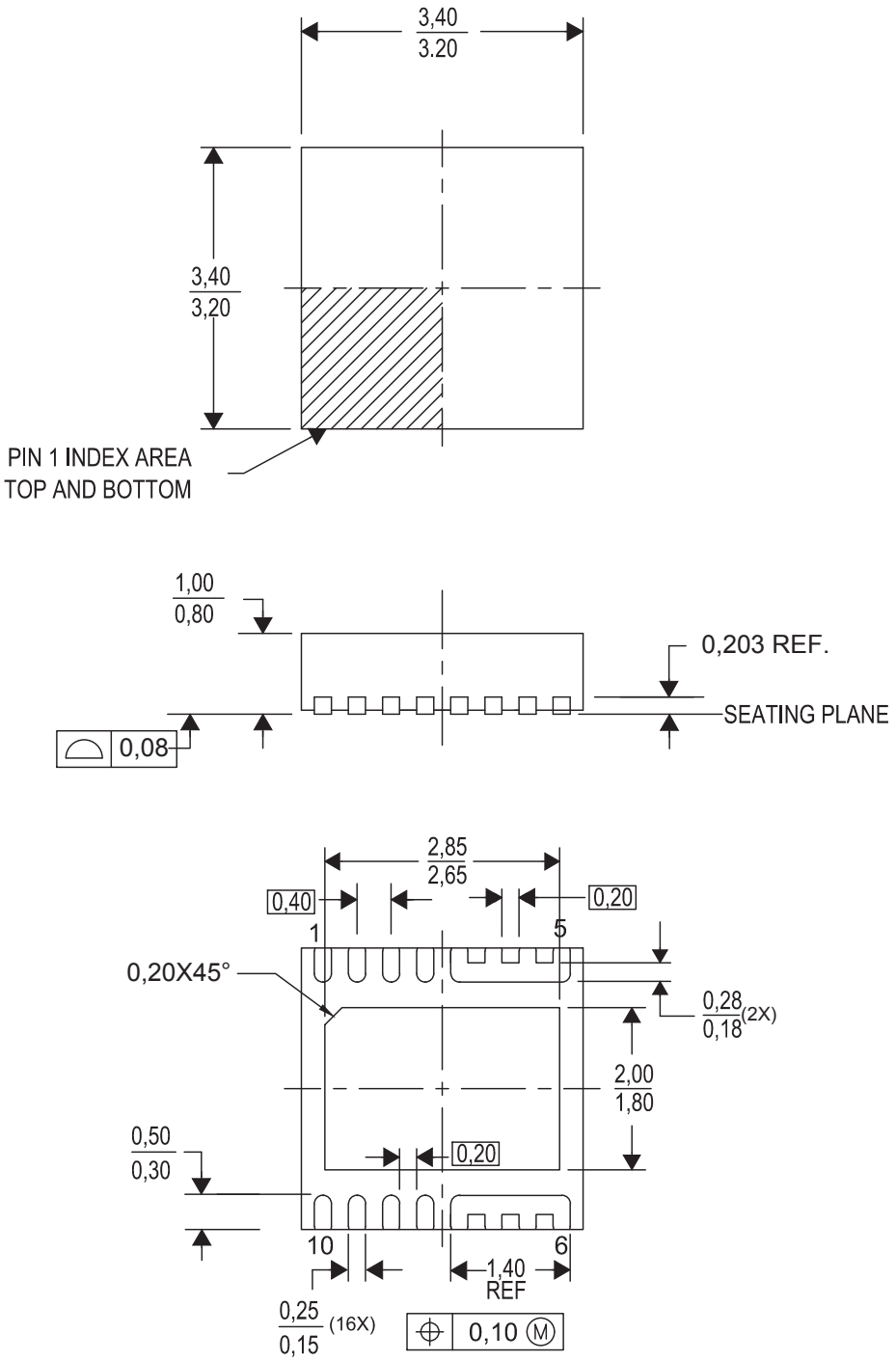
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

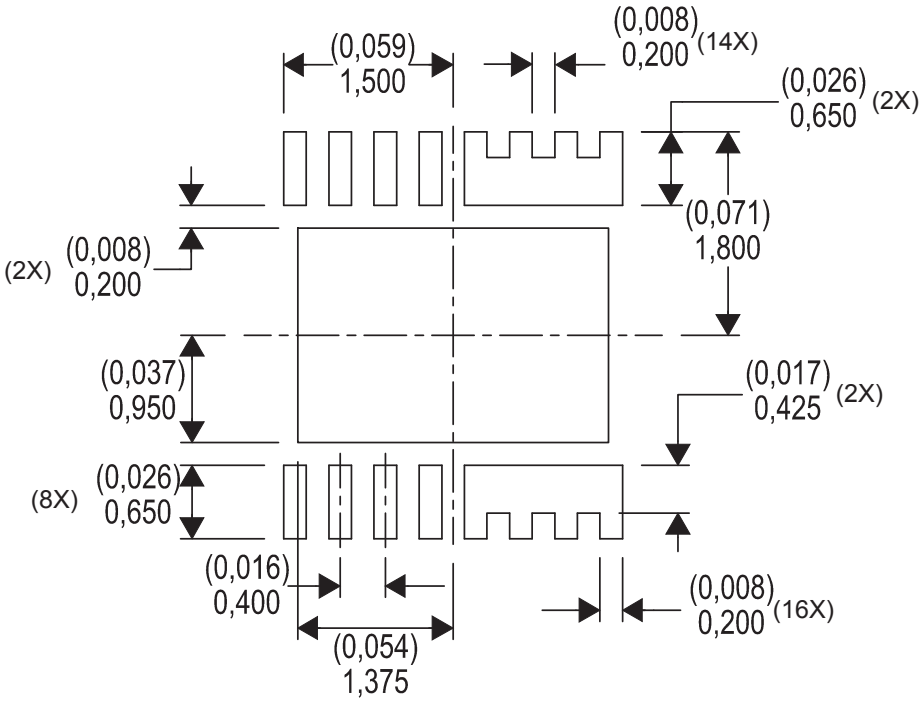
# 11 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 11.1 机械制图

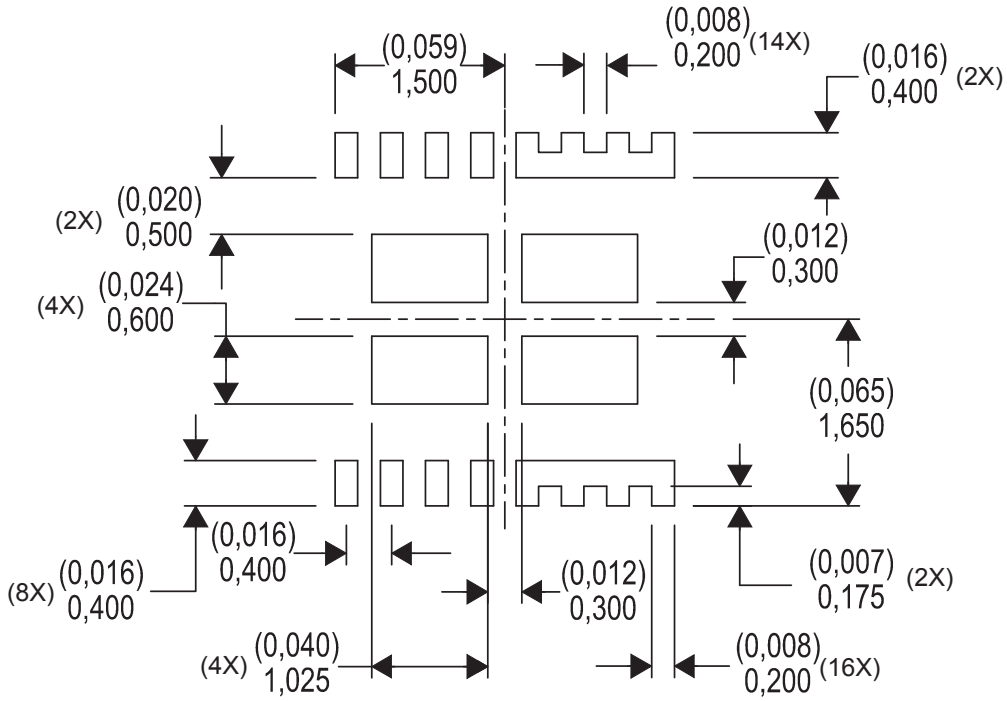


## 11.2 建议印刷电路板 (PCB) 焊盘图案




1. 尺寸单位为 mm（英寸）。

## 11.3 建议模板开口




1. 尺寸单位为 mm（英寸）。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD95379Q3M | ACTIVE | VSON-CLIP | DNS | 10 | 2500 | RoHS-Exempt & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 95379M | Samples |
| CSD95379Q3MT | ACTIVE | VSON-CLIP | DNS | 10 | 250 | RoHS-Exempt & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 95379M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

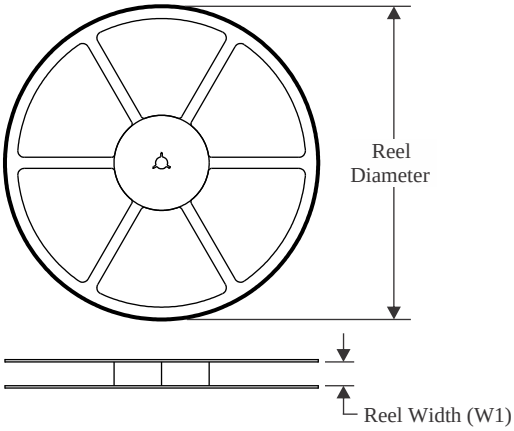
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

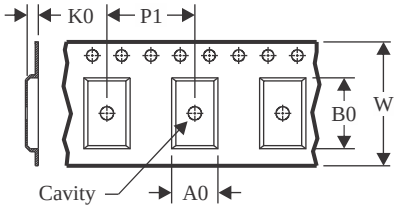
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

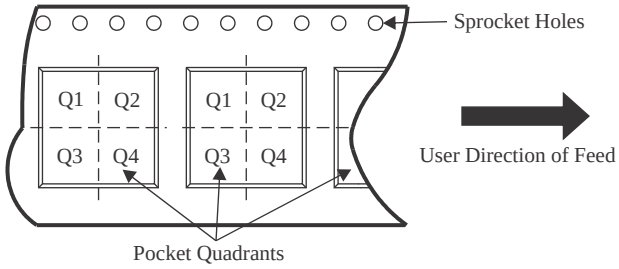



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

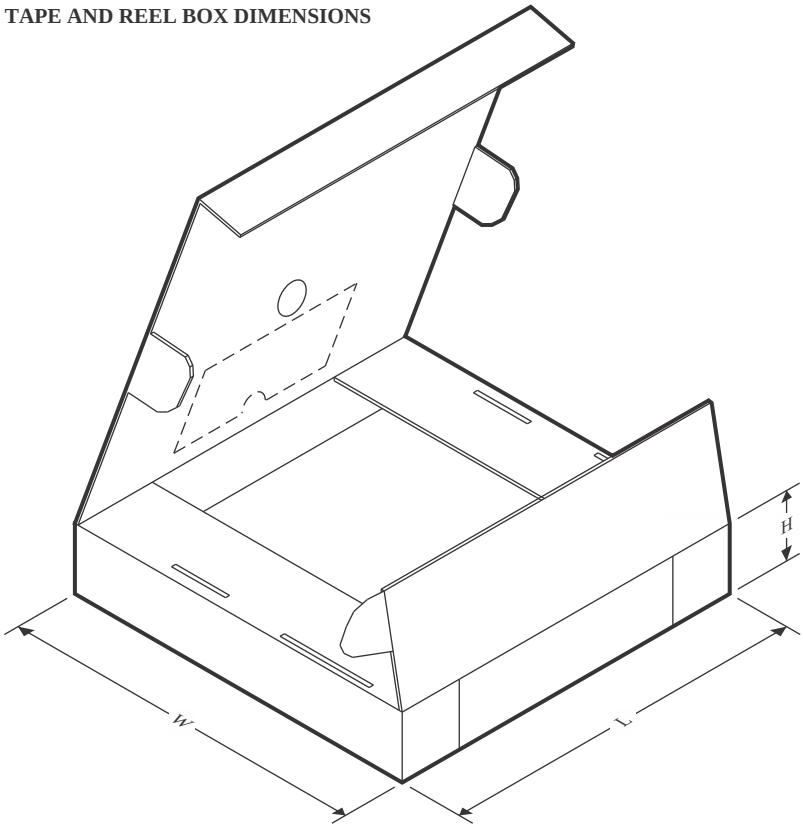
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD95379Q3M | VSON-CLIP | DNS | 10 | 2500 | 330.0 | 12.4 | 3.6 | 3.6 | 1.2 | 8.0 | 12.0 | Q2 |
| CSD95379Q3MT | VSON-CLIP | DNS | 10 | 250 | 180.0 | 12.4 | 3.6 | 3.6 | 1.2 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD95379Q3M | VSON-CLIP | DNS | 10 | 2500 | 346.0 | 346.0 | 33.0 |
| CSD95379Q3MT | VSON-CLIP | DNS | 10 | 250 | 210.0 | 185.0 | 35.0 |

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