DACx3004W 带自动检测型 I²C、SPI 或 PMBus 接口的 12 位和 10 位超低功耗、四路电压和电流输出智能 DAC

1 特性

- 具有灵活配置的可编程电压或电流输出：
  - 电压输出：
    - 1LSB DNL
    - 1x、1.5x、2x、3x 和 4x 增益
  - 电流输出：
    - 1LSB INL 和 DNL（8 位）
    - 25 µA 至 250 µA 的单极和双极输出范围选项
- 电压输出模式具有 35 µA/通道 I_{DD}
- 适合所有通道的可编程比较器模式
- 当 VDD 关闭时提供高阻抗输出
- 高阻抗和电阻下拉断电模式
- 50MHz SPI 兼容型接口
- 自动检测的 I²C、SPI 或 PMBus™ 接口
  - 1.62V V_{IH} (V_{DD} = 5.5V)
- 可配置为多种功能的通用输入/输出 (GPIO)
- 生成预定义的波形：正弦波、三角形波、锯齿波
- 用户可编程的非易失性存储器 (NVM)
- 内部、外部或电源作为基准
- 宽工作电压范围：
  - 电源：1.8V 至 5.5V
  - 温度范围：-40°C 至 +125°C
- 微型封装：16 引脚 DSBGA（1.75mm × 1.75mm）

2 应用

- 光学模块
- 脉搏血氧仪
- 标准笔记本电脑

3 说明

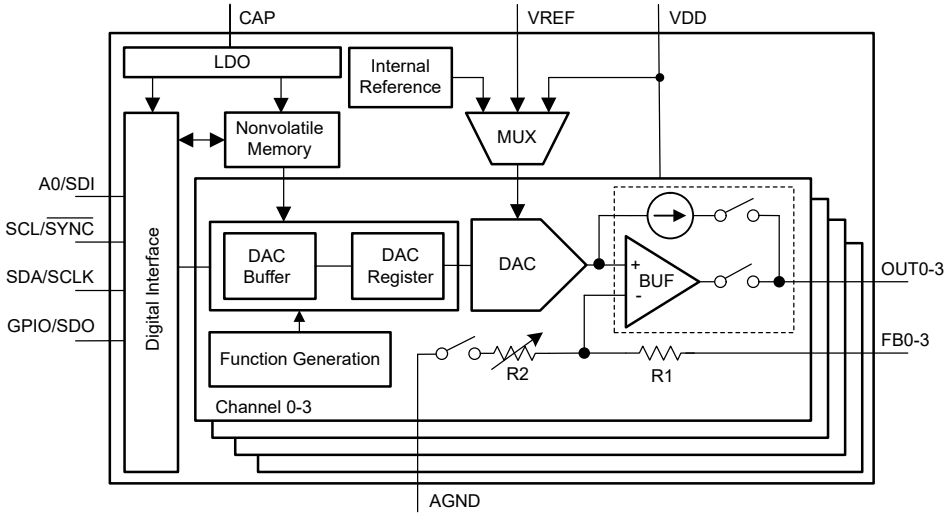
12 位 DAC63004W 和 10 位 DAC53004W (DACx3004W) 是引脚兼容系列四通道、缓冲型、电压输出和电流输出智能数模转换器 (DAC)。这些 DACx3004W 支持高阻态断电模式，并在断电情况下支持高阻态输出。DAC 输出提供一个强制检测选项，可用作可编程比较器和电流阱。多功能 GPIO、函数生成和 NVM 使这些智能 DAC 适用于无处理器的应用和设计重复使用。这些器件自动检测 I²C、SPI 和 PMBus 接口，并包含内部基准。

这些功能集与微型封装和低功耗相结合，使这些智能 DAC 成为电压裕量和调节、偏置和校准用直流设定点以及波形生成等应用的理想选择。

器件信息

器件型号	分辨率	封装(1)
DAC63004W	12 位	YBH（DSBGA，16）
DAC53004W	10 位	YBH（DSBGA，16）

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
March 2023	*	Initial Release

5 Pin Configuration and Functions

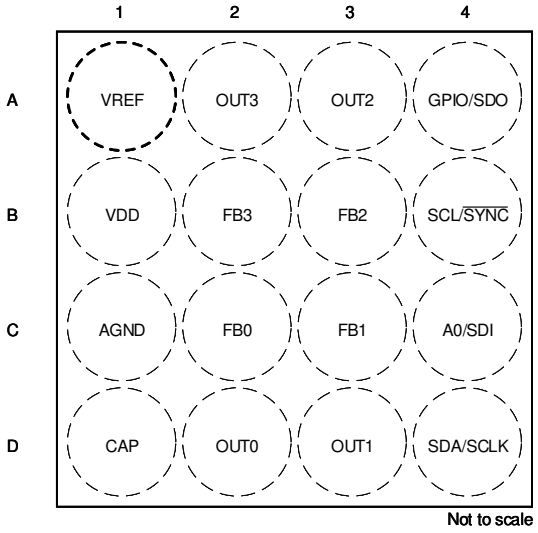


图 5-1. YBH Package, 16-pin DSBGA (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VREF	Power	External reference input. Connect a capacitor (approximately 0.1 µF) between VREF and AGND. Use a pullup resistor to VDD when the external reference is not used. Do not ramp up this pin before VDD. In case an external reference is used, make sure the reference ramps up after VDD.
A2	OUT3	Output	Analog output voltage from DAC channel 3.
A3	OUT2	Output	Analog output voltage from DAC channel 2.
A4	GPIO/SDO	Input/Output	General-purpose input/output configurable as $\overline{\text{LDAC}}$, PD, $\overline{\text{PROTECT}}$, $\overline{\text{RESET}}$, SDO, and $\overline{\text{STATUS}}$. For $\overline{\text{STATUS}}$ and SDO, connect the pin to the IO voltage with an external pullup resistor. If unused, connect the GPIO pin to VDD or AGND using an external resistor. This pin can ramp up before VDD.
B1	VDD	Power	Supply voltage.
B2	FB3	Input	Voltage feedback pin for channel 3. In voltage-output mode, connect to OUT3 for closed-loop amplifier output. In current-output mode, keep the FB3 pin unconnected to minimize leakage current.
B3	FB2	Input	Voltage feedback pin for channel 2. In voltage-output mode, connect to OUT2 for closed-loop amplifier output. In current-output mode, keep the FB2 pin unconnected to minimize leakage current.
B4	SCL/$\overline{\text{SYNC}}$	Output	I^2C serial interface clock or SPI chip select input. Connect this to the IO voltage using an external pullup resistor. This pin can ramp up before VDD.
C1	AGND	Ground	Ground reference point for all circuitry on the device.
C2	FB0	Input	Voltage feedback pin for channel 0. In voltage-output mode, connect to OUT0 for closed-loop amplifier output. In current-output mode, keep the FB0 pin unconnected to minimize leakage current.
C3	FB1	Input	Voltage feedback pin for channel 1. In voltage-output mode, connect to OUT1 for closed-loop amplifier output. In current-output mode, keep the FB1 pin unconnected to minimize leakage current.
C4	A0/SDI	Input	Address configuration pin for I^2C or serial data input for SPI. For A0, connect this pin to VDD, AGND, SDA, or SCL for address configuration (节 7.5.2.2.1). For SDI, this pin need not be pulled up or pulled down. This pin can ramp up before VDD.
D1	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
D2	OUT0	Output	Analog output voltage from DAC channel 0.
D3	OUT1	Output	Analog output voltage from DAC channel 1.
D4	SDA/SCLK	Input/Output	Bidirectional I^2C serial data bus or SPI clock input. Connect this pinto the IO voltage using an external pullup resistor in I^2C mode. This pin can ramp up before VDD.

6 规格

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to AGND	– 0.3	6	V
	Digital inputs to AGND	– 0.3	V_{DD} + 0.3	V
	V_{FBX} to AGND	– 0.3	V_{DD} + 0.3	V
	V_{OUTX} to AGND	– 0.3	V_{DD} + 0.3	V
V_{REF}	External reference, V_{REF} to AGND	– 0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx, VDD, and AGND pins	– 10	10	mA
T_J	Junction temperature	– 40	150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins((2))	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V_{REF}	External reference to ground (AGND)	1.7		V_{DD}	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ⩽ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
C_{CAP}	External capacitor on CAP pin	0.5		15	μF
T_A	Ambient temperature	– 40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DACx3004W YBH (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.3	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report*.

6.5 Electrical Characteristics: Voltage Output

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC63004W	12			Bits
		DAC53004W	10			
INL	Integral nonlinearity((1))	DAC63004W	–5		5	LSB
		DAC53004W	–1.25		1.25	
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error(4)	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
		Code 0d into DAC, internal V_{REF}, gain = 4 ×, V_{DD} = 5.5 V		6	15	
	Zero-code error temperature coefficient(4)			±10		µV/°C
	Offset error(4) (6)	1.7 V ≤ V_{DD} < 2.7 V, V_{FB} pin shorted to V_{OUT}, DAC code: 32d for 12-bit resolution	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, V_{FB} pin shorted to V_{OUT}, DAC code: 32d for 12-bit resolution	–0.5	0.25	0.5	
	Offset-error temperature coefficient(4)	V_{FB} pin shorted to V_{OUT}, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution		±0.0003		%FSR/°C
	Gain error(4)	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(4)	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution		±0.0008		%FSR/°C
	Full-scale error(4) (6)	1.7 V ≤ V_{DD} < 2.7 V, DAC at full-scale	–1		1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, DAC at full-scale	–0.5		0.5	
	Full-scale-error temperature coefficient(4)	DAC at full-scale		±0.0008		%FSR/°C
OUTPUT						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load(2)	R_L = infinite, phase margin = 30°			200	pF
		Phase margin = 30°			1000	
	Short-circuit current	V_{DD} = 1.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		15		mA
		V_{DD} = 2.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		50		
		V_{DD} = 5.5 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom(2)	To V_{DD} (DAC output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 V × gain + 0.2 V	0.2			V
		To V_{DD} and to AGND (DAC output unloaded, external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD})	0.8			%FSR
		To V_{DD} and to AGND (I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V), external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD})	10			

6.5 Electrical Characteristics: Voltage Output (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_O	V_{FB} dc output impedance(3)	DAC output enabled, internal reference (gain = 1.5 × or 2 ×) or external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	400	500	600	kΩ
		DAC output enabled, internal V_{REF}, gain = 3 × or 4 ×	325	400	485	
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2 ×, DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		20		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4 ×		25		
	Slew rate	V_{DD} = 5.5 V		0.3		V/µs
	Power-on glitch magnitude	At start-up (DAC output disabled)		75		mV
		At start-up (DAC output disabled), R_L = 100 kΩ		200		
	Output-enable glitch magnitude	DAC output disabled to enabled (DAC registers at zero scale), R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		50		μV_{PP}
		Internal V_{REF}, gain = 4 ×, f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		90		
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.35		µV/√Hz
		Internal V_{REF}, gain = 4 ×, f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.9		
	Power supply rejection ratio (ac)(3)	Internal V_{REF}, gain = 4 ×, 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		-68		dB
	Code change glitch impulse	±1 LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1 LSB change around midscale (including feedthrough)		15		mV
POWER						
I_{DD}	Current flowing into VDD(4) (5)	Normal operation, DACs at full scale, digital pins static, external reference at V_{DD} but the V_{REF} pin is not shorted to V_{DD}		35	50	µA/ch

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution.
(2) Specified by design and characterization, not production tested.
(3) Specified with 200-mV headroom with respect to reference value when internal reference is used.
(4) Measured with DAC output unloaded.
(5) The total power consumption is calculated by I_{DD} × (total number of channels powered on) + (sleep-mode current).
(6) When a DAC channel is configured in IOUT mode for long term and then switched to VOUT mode, the VOUT mode can show parametric drift.

6.6 Electrical Characteristics: Current Output

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, ±250-µA output range, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		8			Bits
INL	Integral nonlinearity	DAC codes between 10d and 255d for current output range of 0 µA to 25 µA, DAC codes between 0d and 255d for other ranges	–1		1	LSB
DNL	Differential nonlinearity	DAC codes between 10d and 255d for current output range of 0 µA to 25 µA, DAC codes between 0d and 255d for other ranges	–1		1	LSB
	Offset error	DAC output range: 0 µA to 25 µA, DAC at code 10d		±1.5		%FSR
	Offset error	DAC output ranges: 0 µA to 50 µA, 0 µA to 125 µA, and 0 µA to 250 µA; DAC at zero-scale		5		%FSR
	Offset error	all unipolar negative ranges, DAC at zero-scale		-5		%FSR
	Offset error	DAC output ranges: ±25 µA, ±50 µA, ±125 µA, and ±250 µA; DAC at midscale		±1		%FSR
	Gain error	DAC output range: 0 µA to 25 µA, DAC codes between 10d and 255d		±1.5		%FSR
	Gain error	DAC output ranges: 0 µA to 50 µA, 0 µA to 125 µA, and 0 µA to 250 µA; DAC codes between 0d and 255d		±1.5		%FSR
	Gain error	all unipolar negative ranges, DAC codes between 0d and 255d		±5		%FSR
	Gain error	DAC output ranges: ±25 µA, ±50 µA, ±125 µA, and ±250 µA; DAC codes between 0d and 255d		±1.3		%FSR
OUTPUT						
	Output compliance voltage(1)	DAC output range: 0 µA to 25 µA, to V_{DD} and to A_{GND}	200			mV
	Output compliance voltage(1)	DAC output ranges: 0 µA to 50 µA, 0 µA to 125 µA, and 0 µA to 250 µA; to V_{DD}	400			mV
	Output compliance voltage(1)	all unipolar negative ranges, to V_{DD}	400			mv
	Output compliance voltage(1)	DAC output ranges: ±25 µA, ±50 µA, ±125 µA, and ±250 µA; to V_{DD} and to AGND	400			mV
Z_O	I_{OUT} dc output impedance(2)	DAC at midscale, DAC output kept at V_{DD}/2	60			MΩ
	Power supply rejection ratio (dc)	DAC at midscale, output range: 0 µA to 25 µA, V_{DD} changed from 4.5 V to 5.5 V		0.28		LSB/V
	Power supply rejection ratio (dc)	DAC at midscale, all unipolar positive ranges, V_{DD} changed from 4.5 V to 5.5V		0.33		LSB/V
	Power supply rejection ratio (dc)	DAC at midscale, all unipolar negative ranges, V_{DD} changed from 4.5 V to 5.5V		0.83		LSB/V
	Power supply rejection ratio (dc)	DAC at midscale, all bipolar ranges, V_{DD} changed from 4.5V to 5.5V		0.23		LSB/V
DYNAMIC PERFORMANCE						
t_{sett}	Output current settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 1 LSB at 8-bit resolution, V_{DD} = 5.5 V, common-mode voltage at OUTx pin is V_{DD}/2		60		µs
V_n	Output noise current (peak to peak)	0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V, ±250-µA output range		150		nA_{PP}
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V, ±250-µA output range		1		nA/$\sqrt{Hz}$
	Power supply rejection ratio (ac)(3)	±250 µA output range, 200-mV 50-Hz or 60-Hz sine wave superimposed on power-supply voltage, DAC at midscale		0.65		LSB/V

6.6 Electrical Characteristics: Current Output (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, ±250-µA output range, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{DD}	Current flowing into VDD(3) (4)	Normal operation, DACs at midscale, all unipolar output ranges, digital pins static		18	24	µA/ch
I_{DD}	Current flowing into VDD(3) (4)	Normal operation, DACs at full scale, ±25-µA output range, digital pins static		42	50	µA/ch
		Normal operation, DACs at full scale, ±50-µA output range, digital pins static		56	70	
		Normal operation, DACs at full scale, ±125-µA output range, digital pins static		98	120	
		Normal operation, DACs at full scale, ±250-µA output range, digital pins static		167	200	

(1) Measured between DAC codes 0d and 255d.
(2) Specified by design and characterization, not production tested.
(3) The current flowing into V_{DD} does not account for the load current sourced or sunk on the OUTx pins. The V_{REF} pin is connected to V_{DD}.
(4) The total power consumption is calculated by I_{DD} × (total number of channels powered on) + (sleep-mode current).

6.7 Electrical Characteristics: Comparator Mode

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 × in voltage output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error(1) (2)	1.7 V ≤ V_{DD} ≤ 5.5 V; DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference.	–6	0	6	mV
	Offset error time drift(1)	V_{DD} = 5.5 V, external reference, T_A = 125°C, FB in Hi-Z mode, DAC at full scale and V_{FB} at 0 V or DAC at zero scale and V_{FB} at 1.84 V, drift specified for 10 years of continuous operation		4		mV
OUTPUT						
	Input voltage	V_{REF} connected to V_{DD}, V_{FB} resistor network connected to ground	0		V_{DD}	V
		V_{REF} connected to V_{DD}, V_{FB} resistor network disconnected from ground	0		V_{DD} × (1/3 – 1/100)	
V_{OL}	Logic low output voltage	I_{LOAD} = 100 µA, output in open-drain mode		0.1		V
DYNAMIC PERFORMANCE						
t_{resp}	Output response time	DAC at midscale with 10-bit resolution, FB input at Hi-Z, and transition step at FB node is (V_{DAC} – 2 LSB) to (V_{DAC} + 2 LSB), transition time measured between 10% and 90% of output, output current of 100 µA, comparator output configured in push-pull mode, load capacitor at DAC output is 25 pF		10		µs

(1) Specified by design and characterization, not production tested.
(2) This specification does not include the total unadjusted error (TUE) of the DAC.

6.8 Electrical Characteristics: General

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 × in voltage output mode or ±250-µA output range in current output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) in voltage-output mode and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C	1.1979	1.212	1.224	V
	Reference output temperature coefficient(1) (2)				50	ppm/°C
EXTERNAL REFERENCE						
	V_{REF} input impedance(1) (3)			192		kΩ-ch
EEPROM						
	Endurance(1)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A = 125°C		1000		
	Data retention(1)	T_A = 25°C		50		Years
	EEPROM programming write cycle time(1)				200	ms
	Device boot-up time(1)	Time taken from power valid (V_{DD} ≥ 1.7 V) to output valid state (output state as programmed in EEPROM), 0.5-µF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER-DOWN MODE						
I_{DD}	Current flowing into VDD	DAC in deep-sleep mode, internal reference powered down, SDO mode disabled		1.5	3	µA
I_{DD}	Current flowing into VDD	DAC in sleep mode, internal reference powered down, external reference at 5.5 V			28	µA
I_{DD}	Current flowing into VDD(1)	DAC in sleep mode, internal reference enabled, additional current through internal reference		10		µA
I_{DD}	Current flowing into VDD(1)	DAC channels enabled, internal reference enabled, additional current through internal reference per DAC channel in voltage-output mode		12.5		µA
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, 1.7 V ≤ V_{DD} ≤ 5.5 V		10		nA
		V_{DD} = 0 V, V_{OUT} ≤ 1.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		200		nA
		V_{DD} = 0 V, 1.5 V < V_{OUT} ≤ 5.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		500		nA
		100 kΩ between V_{DD} and AGND, V_{OUT} ≤ 1.25 V, series resistance of 10 kΩ at OUT pin		±2		µA

(1) Specified by design and characterization, not production tested.
(2) Measured at –40°C and +125°C and calculated the slope.
(3) Impedances for the DAC channels are connected in parallel.

6.9 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCL}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs

6.10 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCL}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs

6.11 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCL}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs

6.12 Timing Requirements: SPI Write Operation

all input signals are specified with t_r = t_f = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	10			ns
t_{CSHIGH}	$\overline{CS}$ high time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time (time between subsequent $\overline{LDAC}$ falling edges) for same channel	2			µs
$t_{BCASTWAIT}$	Broadcast DAC update wait time (time between subsequent $\overline{LDAC}$ falling edges)	2			µs

6.13 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with t_r = t_f = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 0

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
$t_{SCLKHIGH}$	SCLK high time	350			ns
$t_{SCLKLOW}$	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	400			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

6.14 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with t_r = t_f = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 1

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
$t_{SCLKHIGH}$	SCLK high time	175			ns
$t_{SCLKLOW}$	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	300			ns

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ⩽ V_{IO} ⩽ 5.5 V, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and FSDO = 1

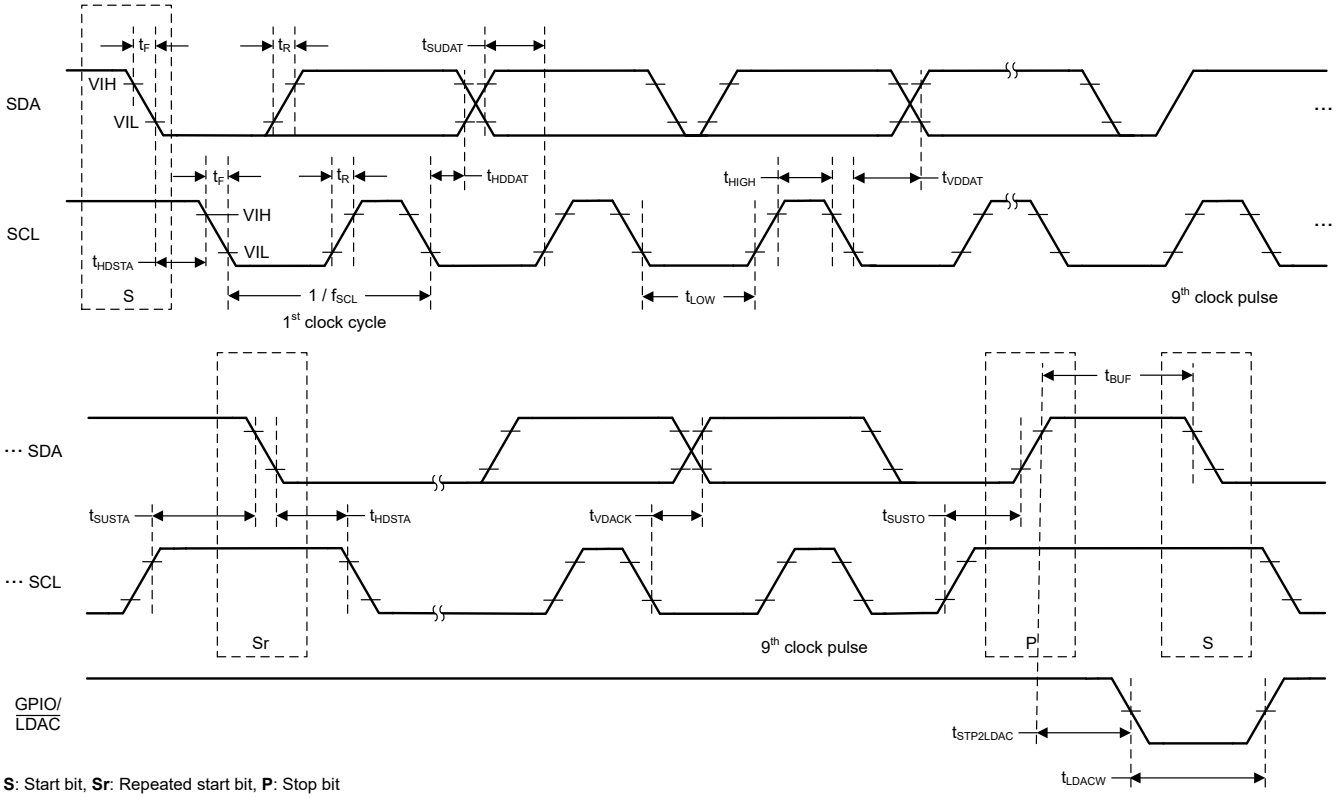
		MIN	NOM	MAX	UNIT
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ⩽ 5 mA, C_L = 20 pF.			300	ns

6.15 Timing Requirements: GPIO

all input signals are specified with $t_r = t_f = 1$ V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$t_{GPIHIGH}$	GPI high time	2			µs
t_{GPILOW}	GPI low time	2			µs
t_{GPAWGD}	$\overline{LDAC}$ falling edge to DAC update delay			2	µs
$t_{CS2LDAC}$	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge	1			µs
$t_{STP2LDAC}$	I^2C stop bit rising edge to $\overline{LDAC}$ falling edge	1			µs
t_{LDACW}	$\overline{LDAC}$ low time	2			µs

6.16 Timing Diagrams



S: Start bit, **Sr**: Repeated start bit, **P**: Stop bit

图 6-1. I^2C Timing Diagram

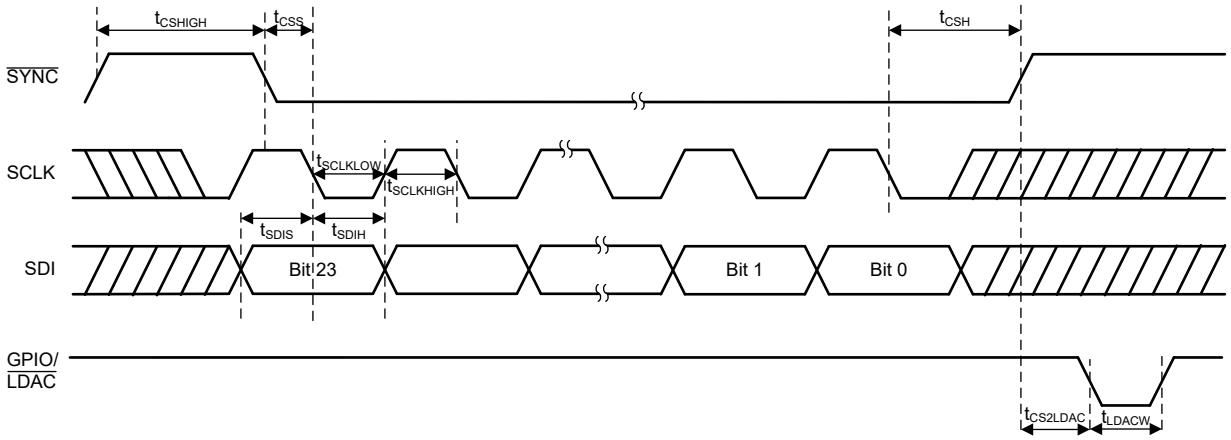


图 6-2. SPI Write Timing Diagram

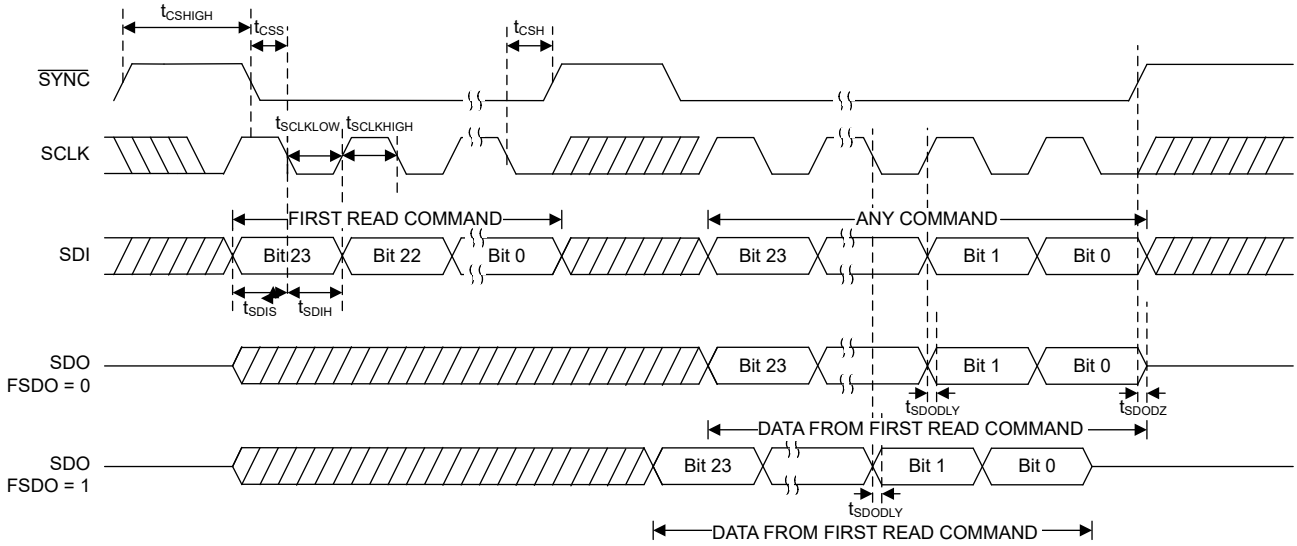


图 6-3. SPI Read Timing Diagram

6.17 Typical Characteristics: Voltage Output

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

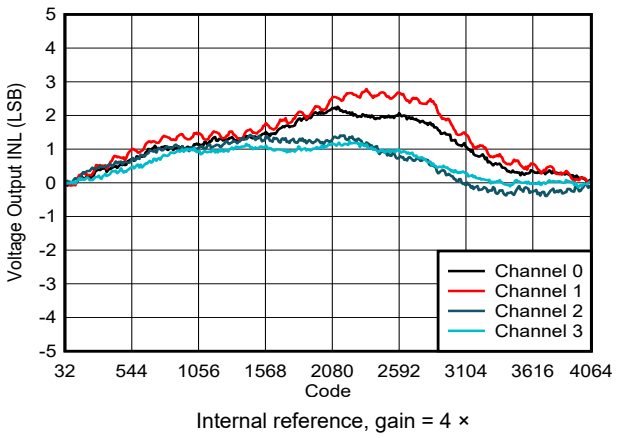


图 6-4. Voltage Output INL vs Digital Input Code

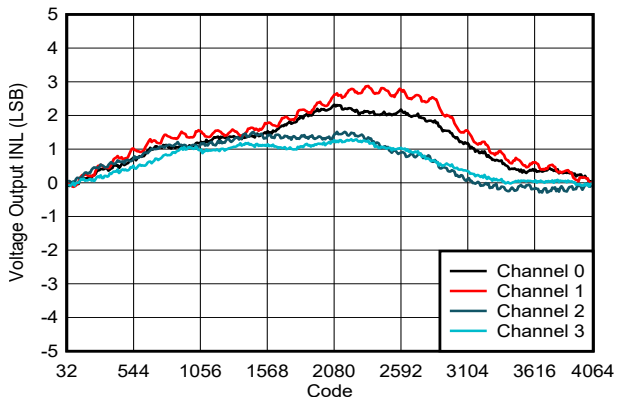


图 6-5. Voltage Output INL vs Digital Input Code

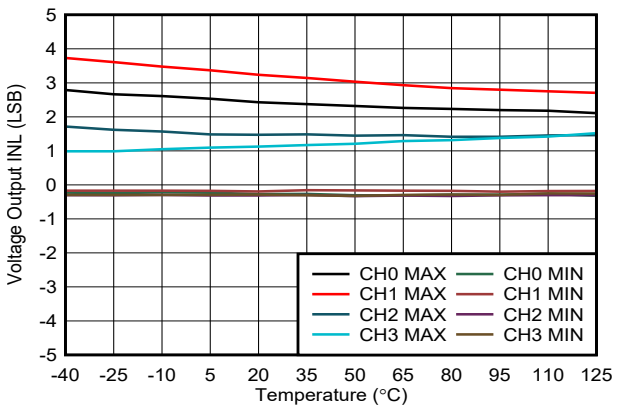


图 6-6. Voltage Output INL vs Temperature

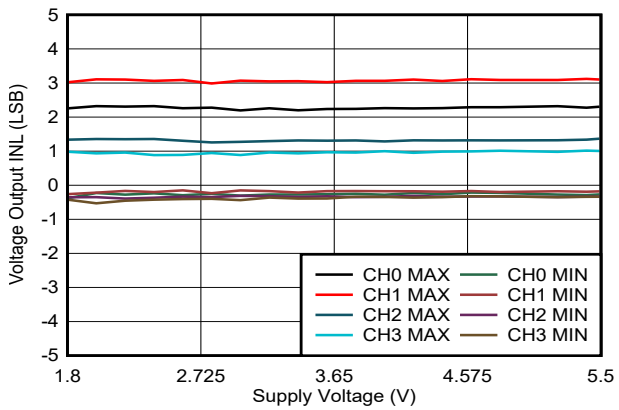


图 6-7. Voltage Output INL vs Supply Voltage

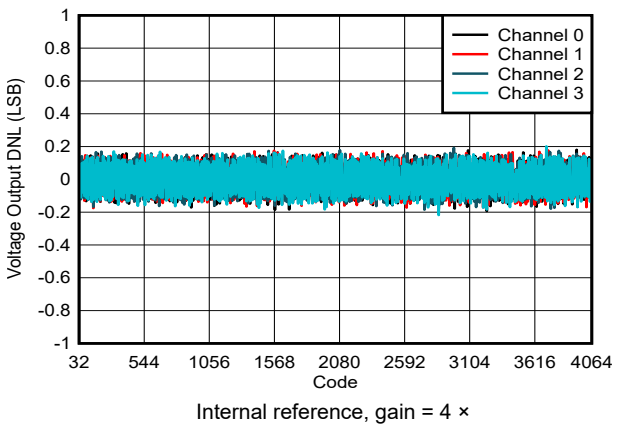


图 6-8. Voltage Output DNL vs Digital Input Code

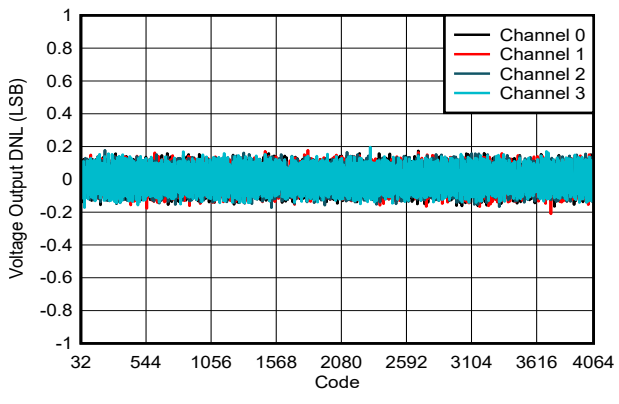


图 6-9. Voltage Output DNL vs Digital Input Code

6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

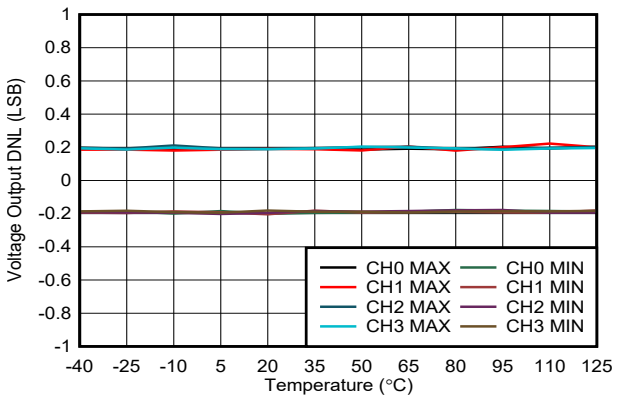


图 6-10. Voltage Output DNL vs Temperature

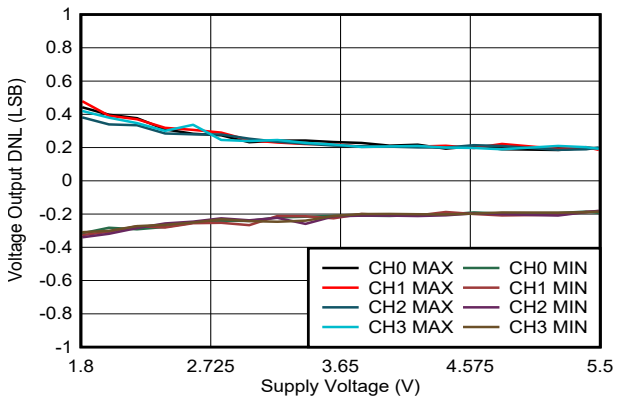
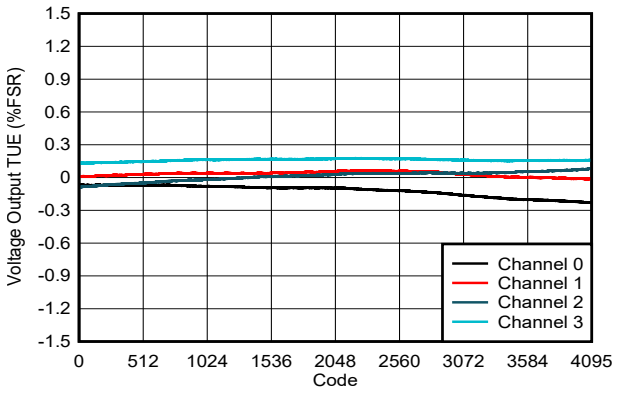


图 6-11. Voltage Output DNL vs Supply Voltage



Internal reference, gain = 4 ×

图 6-12. Voltage Output TUE vs Digital Input Code

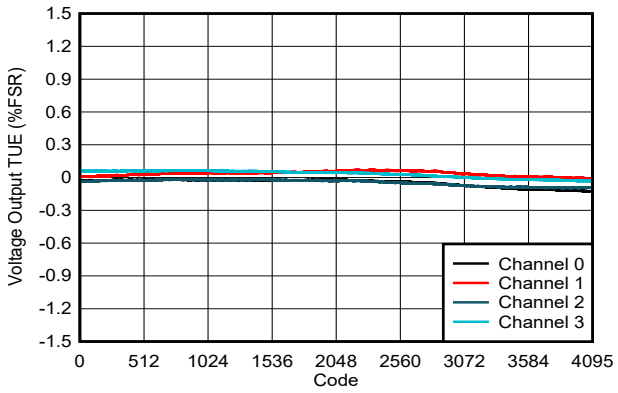
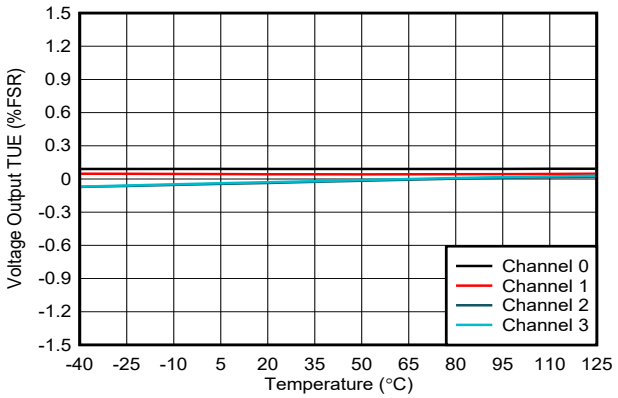
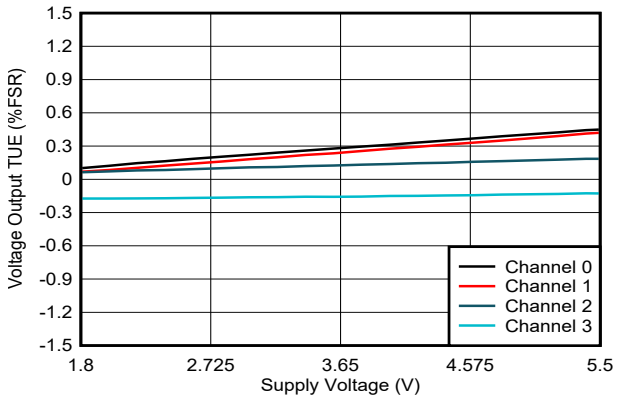


图 6-13. Voltage Output TUE vs Digital Input Code



DAC channels at midscale

图 6-14. Voltage Output TUE vs Temperature



DAC channels at midscale

图 6-15. Voltage Output TUE vs Supply Voltage

6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

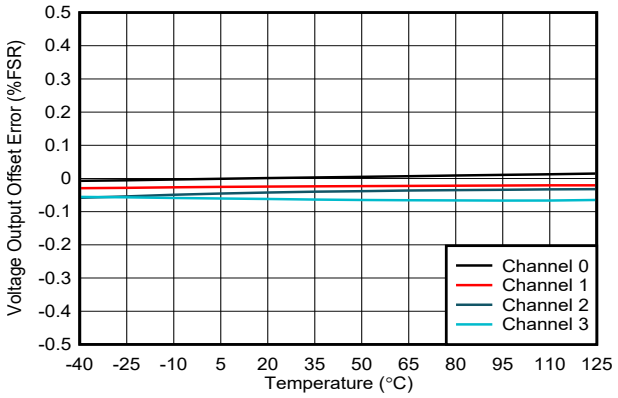


图 6-16. Voltage Output Offset Error vs Temperature

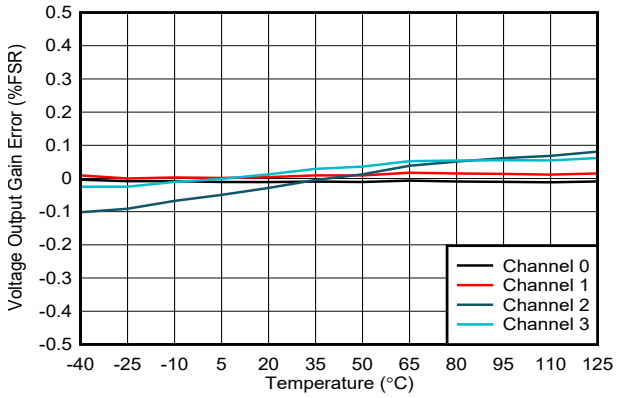
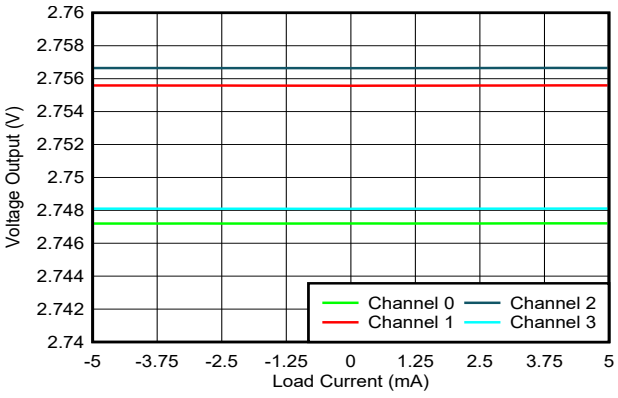


图 6-17. Voltage Output Gain Error vs Temperature



DAC channels at midscale

图 6-18. Voltage Output vs Load Current

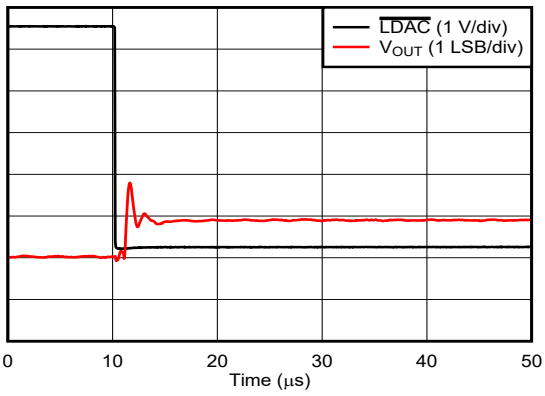


图 6-19. Voltage Output Code-to-Code Glitch - Rising Edge

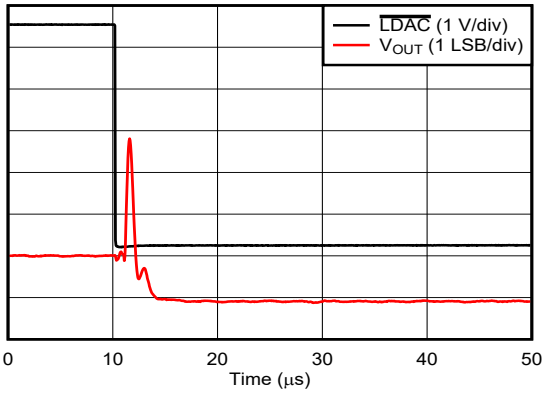
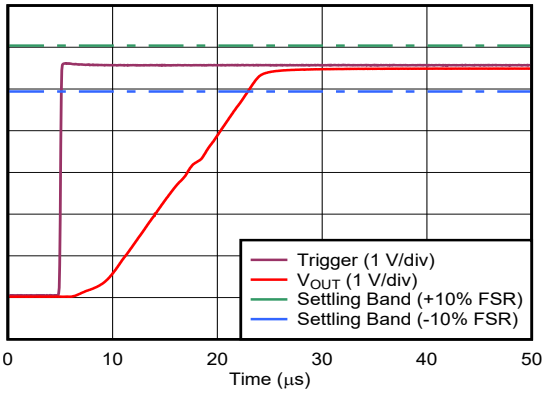


图 6-20. Voltage Output Code-to-Code Glitch: Falling Edge

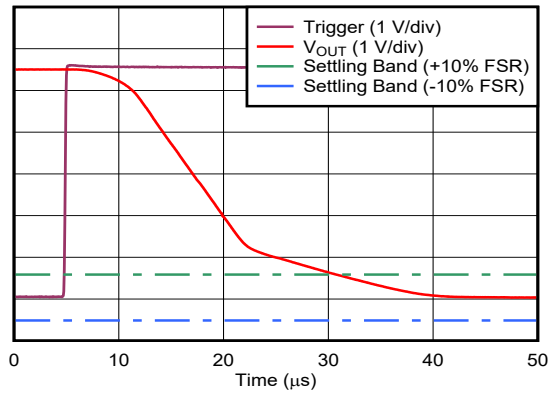


Zero scale to full scale swing

图 6-21. Voltage Output Setting Time: Rising Edge

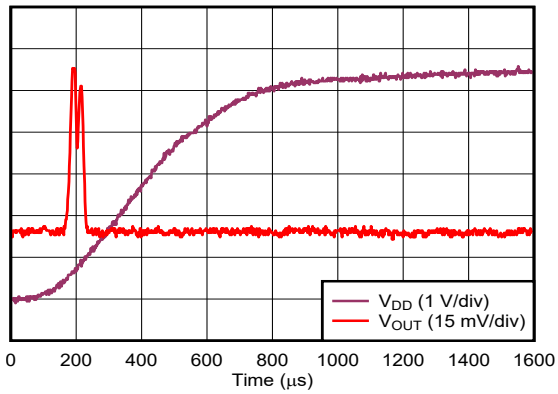
6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



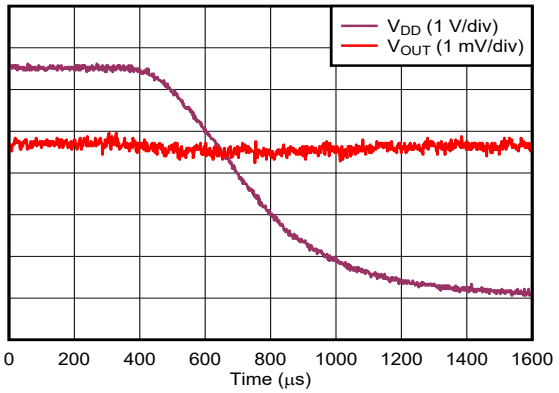
Full scale to zero scale swing

图 6-22. Voltage Output Setting Time: Falling Edge



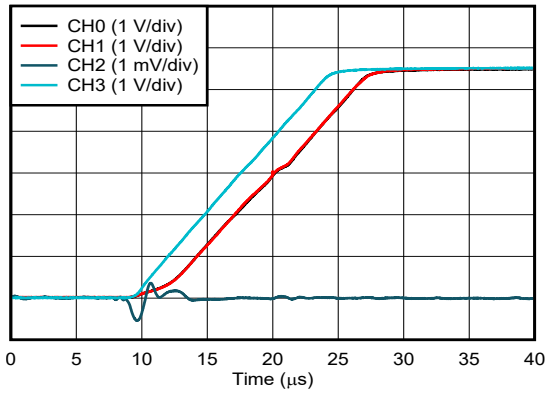
DAC in Hi-Z power-down mode

图 6-23. Voltage Output Power-On Glitch



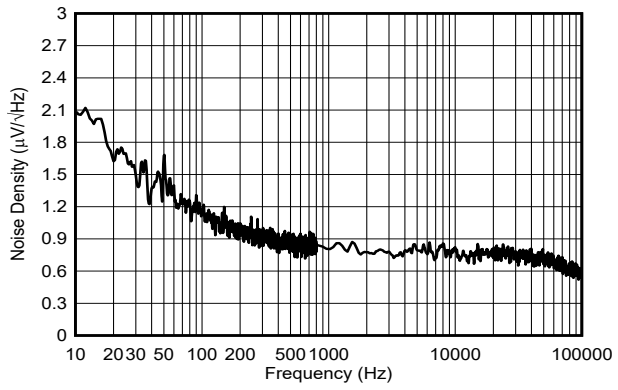
DAC at zero scale

图 6-24. Voltage Output Power-Off Glitch



Channel 2 is resident, all other channels are interferers

图 6-25. Voltage Output Channel-to-Channel Crosstalk



Internal reference, gain = 4 ×

图 6-26. Voltage Output Noise Density

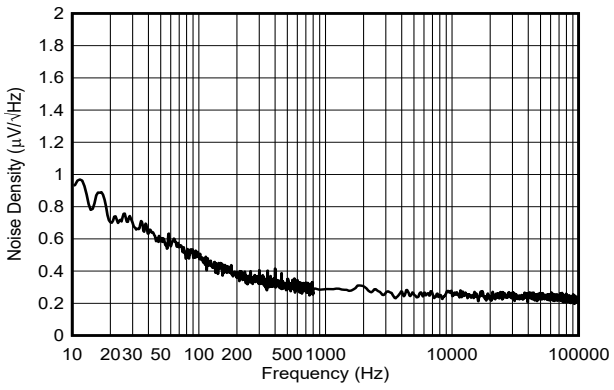
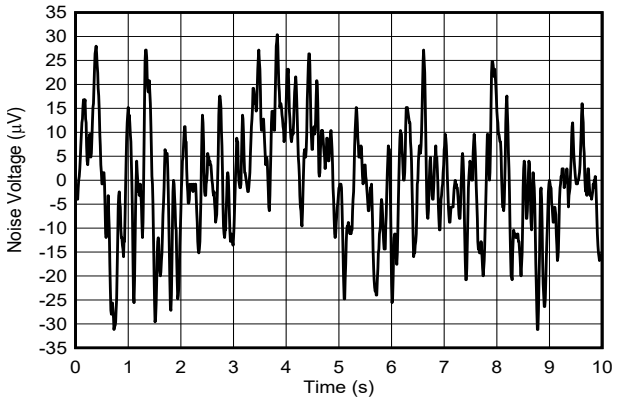


图 6-27. Voltage Output Noise Density

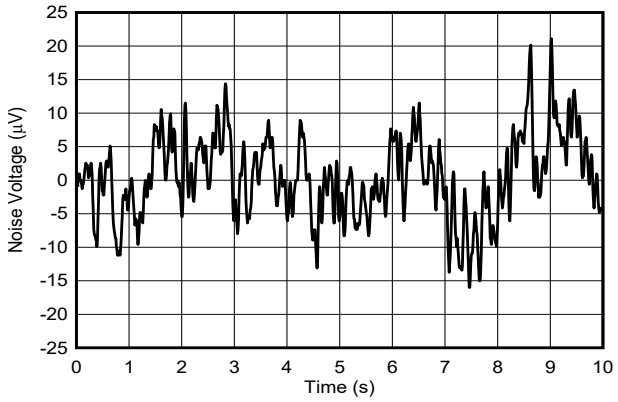
6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



Internal reference, gain = 4 ×, f = 0.1 Hz to 10 Hz

图 6-28. Voltage Output Flicker Noise



f = 0.1 Hz to 10 Hz

图 6-29. Voltage Output Flicker Noise

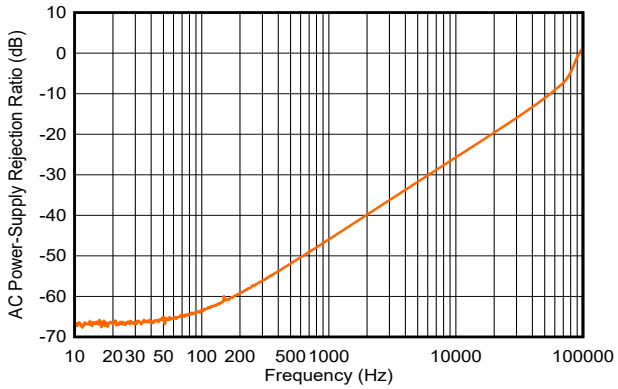


图 6-30. Voltage Output AC PSRR vs Frequency

6.18 Typical Characteristics: Current Output

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)

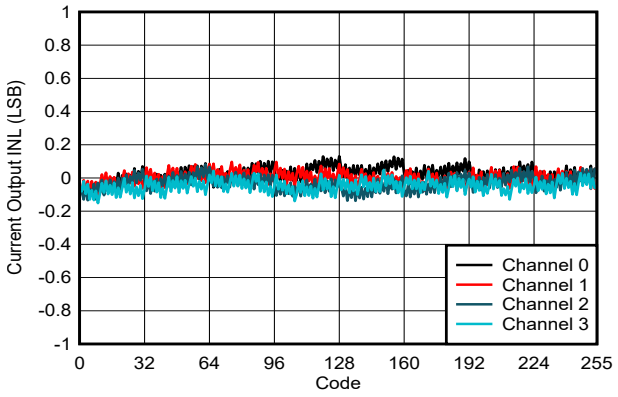
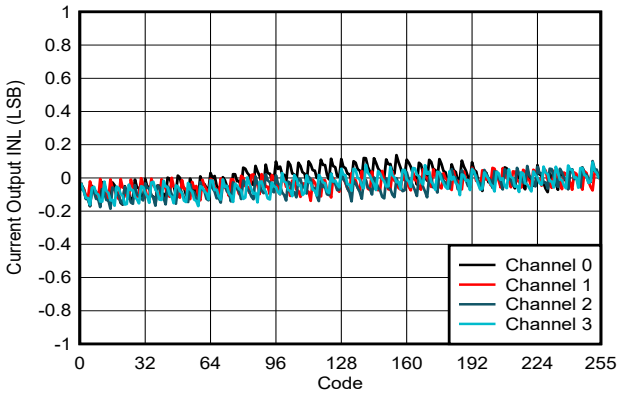
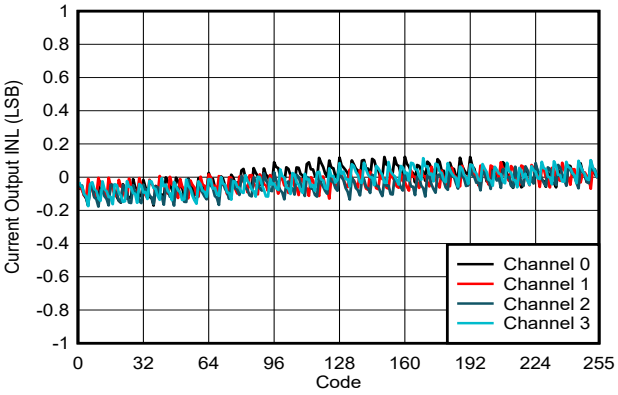


图 6-31. Current Output INL vs Digital Input Code



Output range: 0 μA to 250 μA

图 6-32. Current Output INL vs Digital Input Code



Output range: 0 μA to –240 μA

图 6-33. Current Output INL vs Digital Input Code

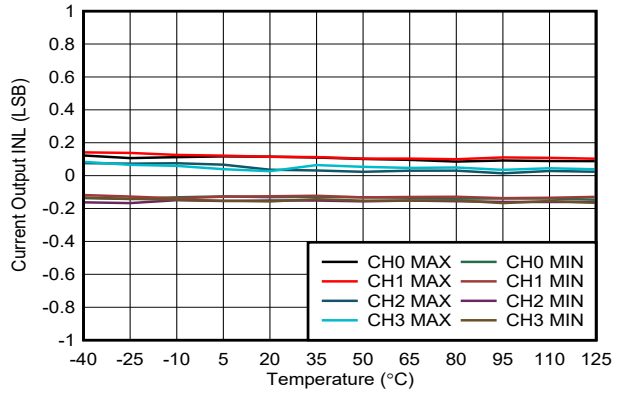


图 6-34. Current Output INL vs Temperature

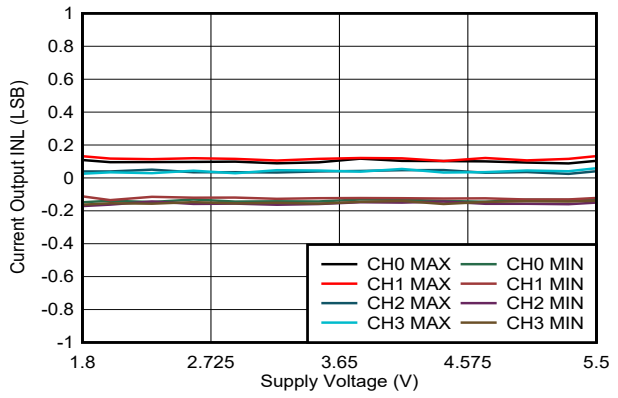


图 6-35. Current Output INL vs Supply Voltage

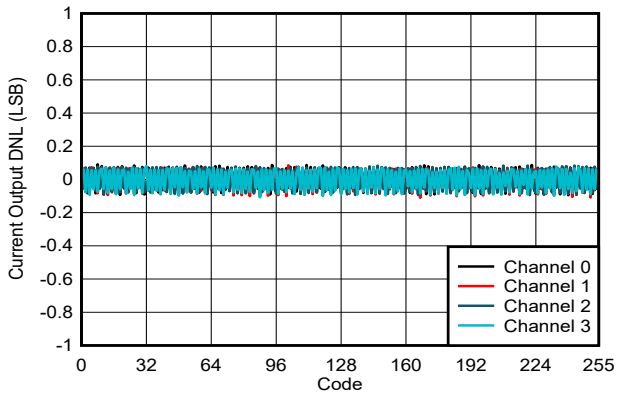
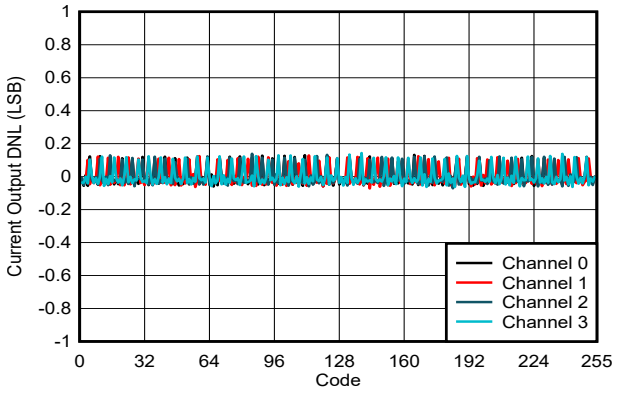


图 6-36. Current Output DNL vs Digital Input Code

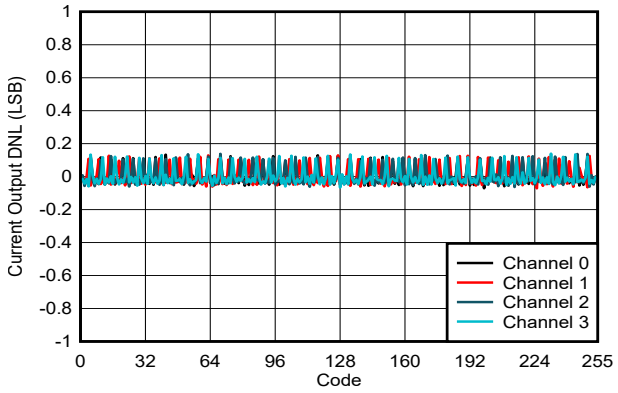
6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)



Output range: 0 μA to 250 μA

图 6-37. Current Output DNL vs Digital Input Code



Output range: 0 μA to –240 μA

图 6-38. Current Output DNL vs Digital Input Code

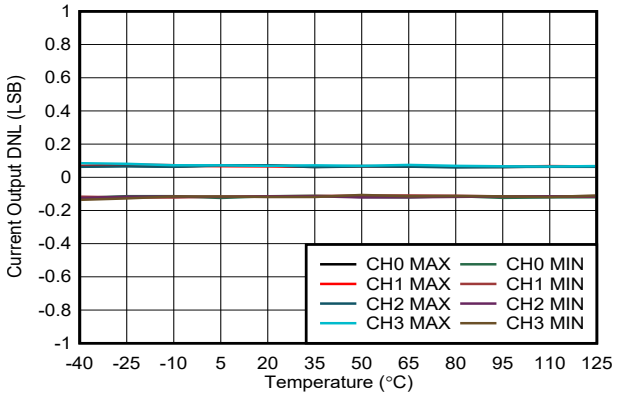


图 6-39. Current Output DNL vs Temperature

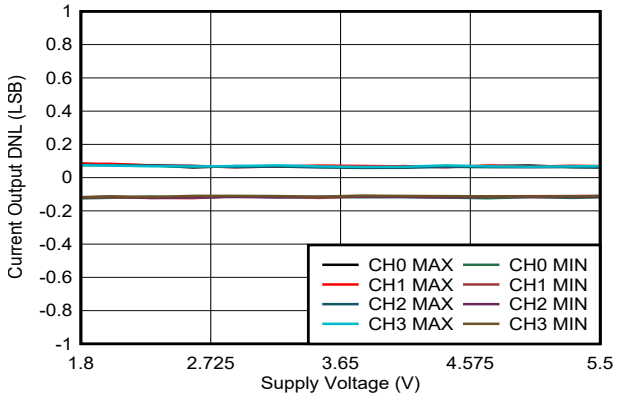


图 6-40. Current Output DNL vs Supply Voltage

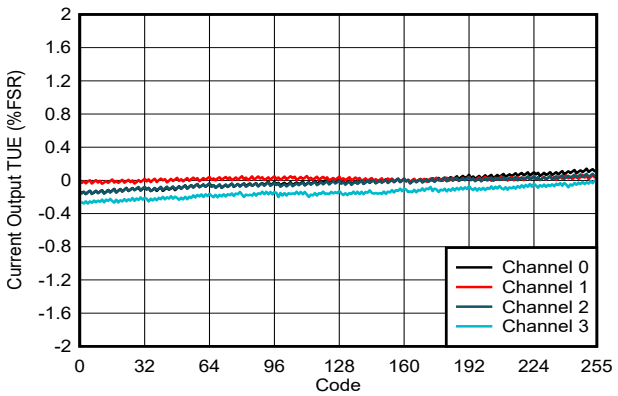
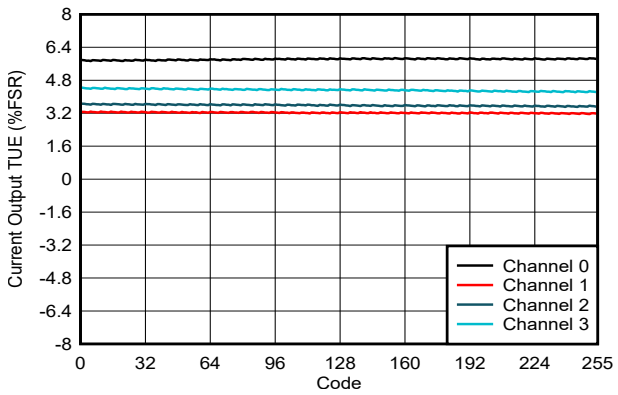


图 6-41. Current Output TUE vs Digital Input Code

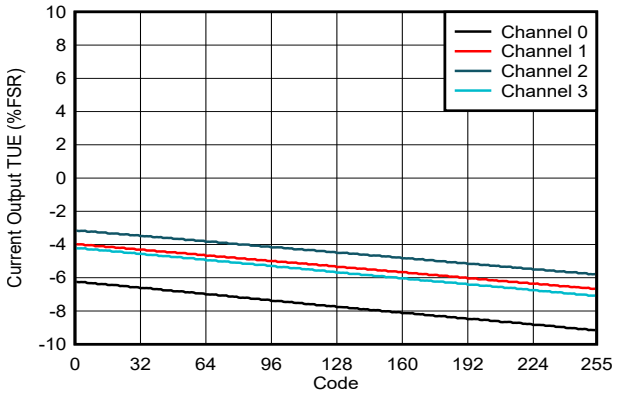


Output range: 0 μA to 250 μA

图 6-42. Current Output TUE vs Digital Input Code

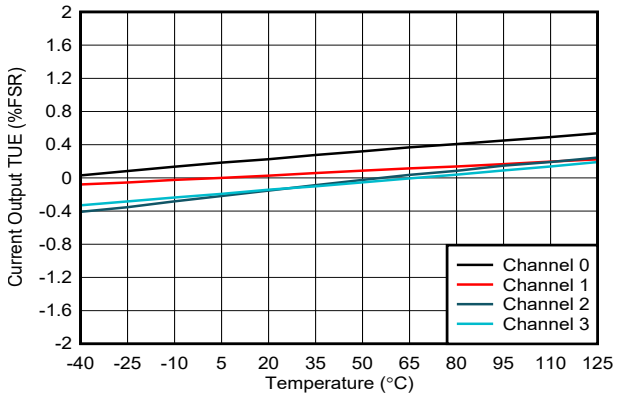
6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)



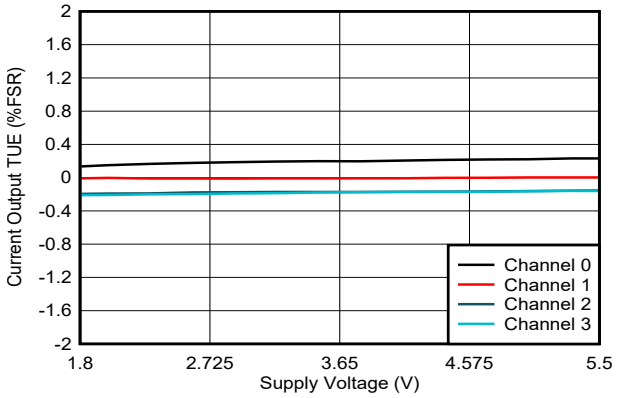
Output range: 0 μA to –240 μA

图 6-43. Current Output TUE vs Digital Input Code



DAC channels at midscale

图 6-44. Current Output TUE vs Temperature



DAC channels at midscale

图 6-45. Current Output TUE vs Supply Voltage

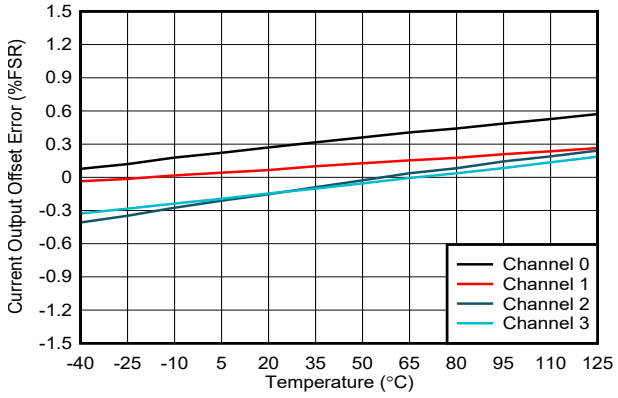


图 6-46. Current Output Offset Error vs Temperature

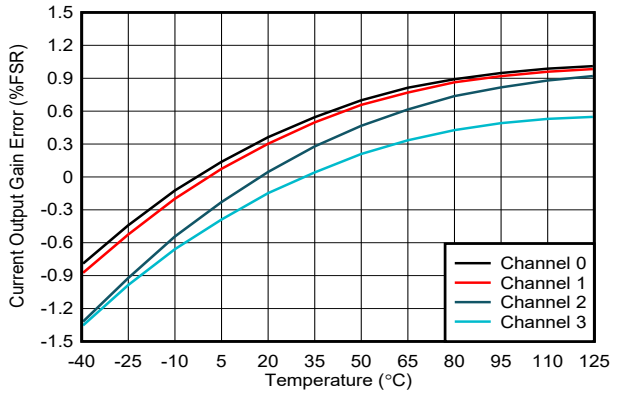


图 6-47. Current Output Gain Error vs Temperature

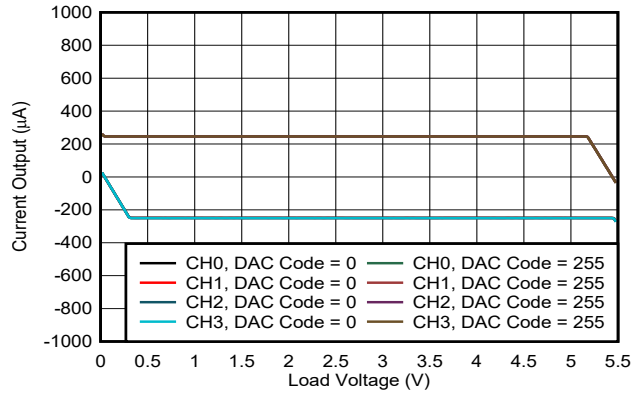


图 6-48. Current Output vs Load Voltage

6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)

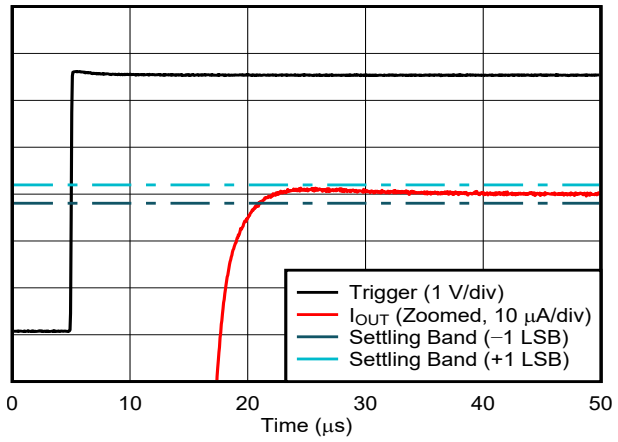


图 6-49. Current Output Settling Time: Rising Edge (¼ to ¾ scale)

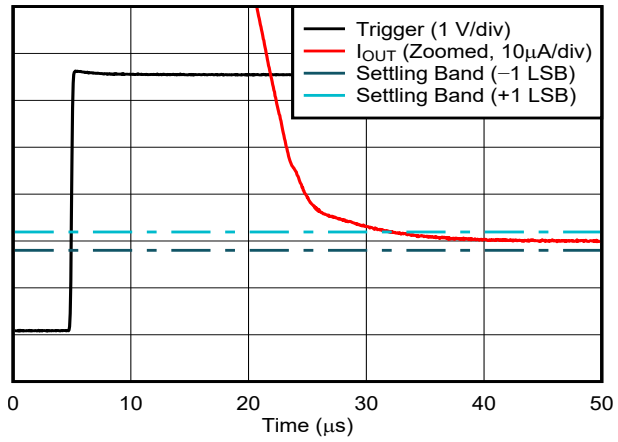
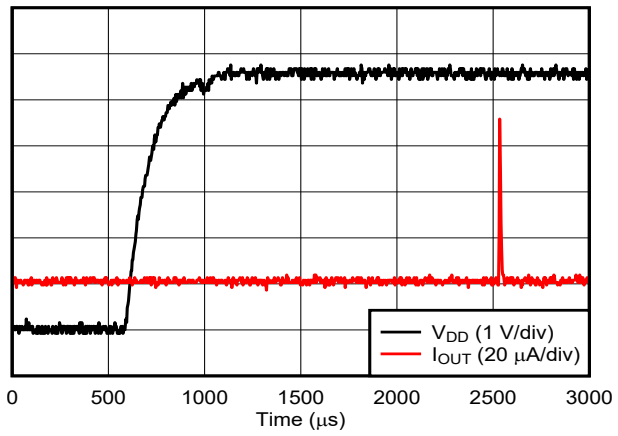
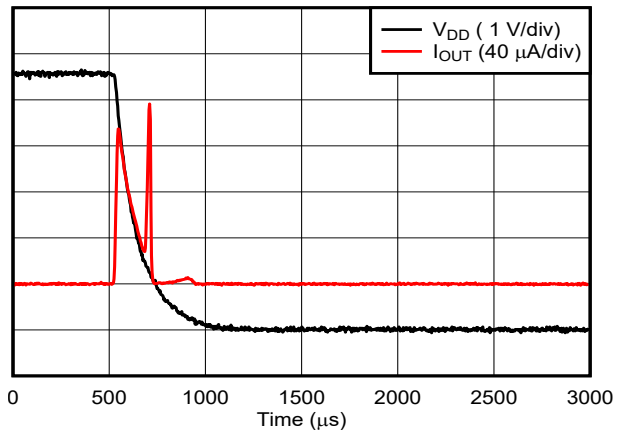


图 6-50. Current Output Settling Time: Falling Edge (¾ to ¼ scale)



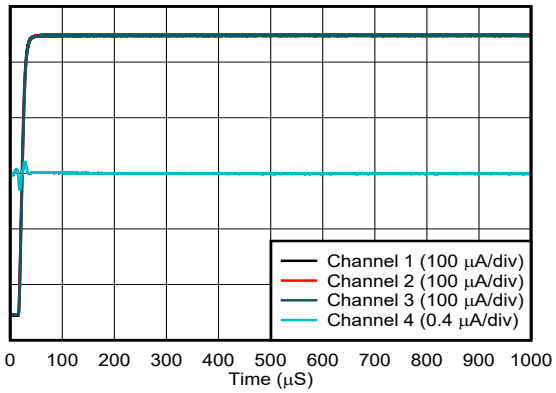
DAC at mid scale (0 μA) stored in EEPROM

图 6-51. Current Output Power-On Glitch



DAC at mid scale (0 μA)

图 6-52. Current Output Power-Off Glitch



Channel 4 is resident, all other channels are interferers

图 6-53. Current Output Channel-to-Channel Crosstalk

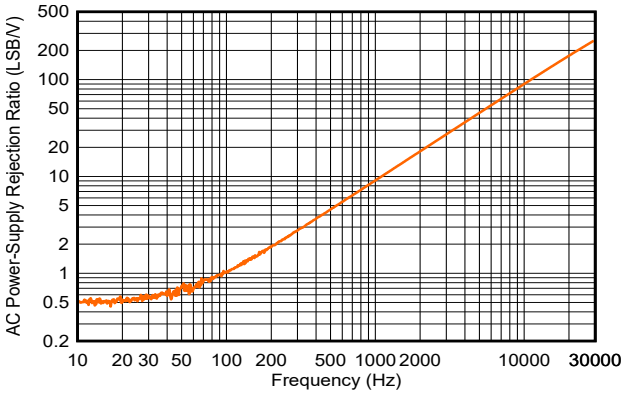
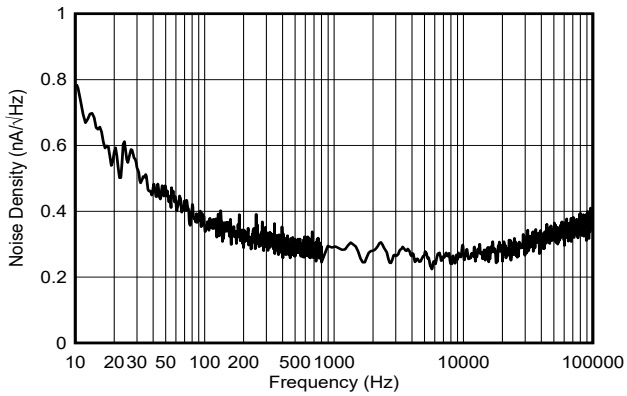


图 6-54. Current Output AC PSRR vs Frequency

6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)



Output range: 0 μA to 250 μA

图 6-55. Current Output Noise Density

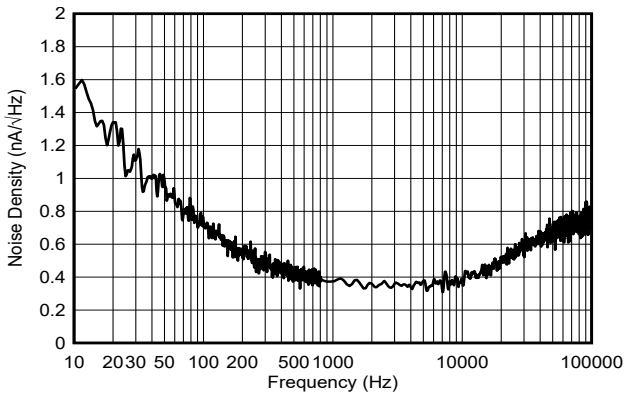
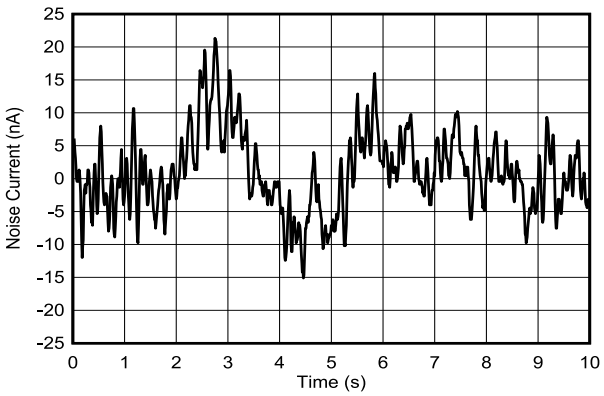
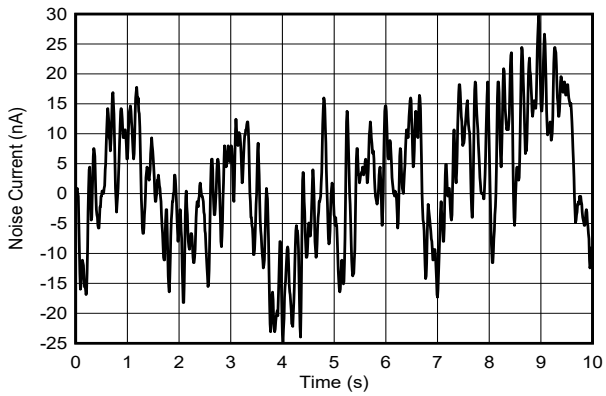


图 6-56. Current Output Noise Density



Output range: 0 μA to 250 μA, f = 0.1 Hz to 10 Hz

图 6-57. Current Output Flicker Noise

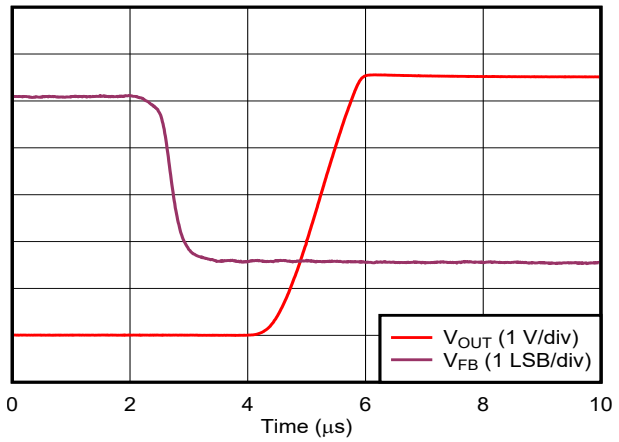


f = 0.1 Hz to 10 Hz

图 6-58. Current Output Flicker Noise

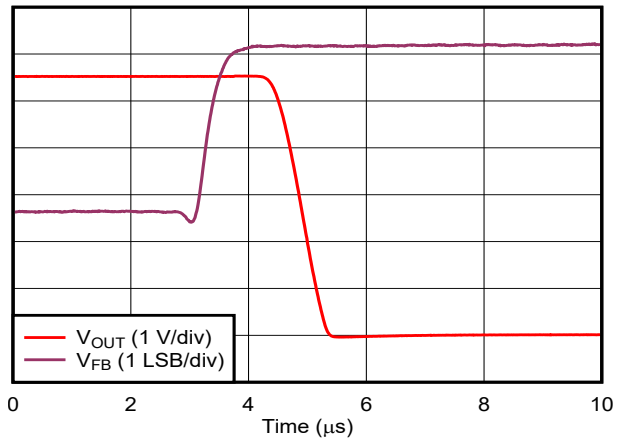
6.19 Typical Characteristics: Comparator

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, FBx pin in Hi-Z mode, and DAC outputs unloaded (unless otherwise noted)



Comparator output in push-pull mode

图 6-59. Comparator Response Time: Low-to-High Transition



Comparator output in push-pull mode

图 6-60. Comparator Response Time: High-to-Low Transition

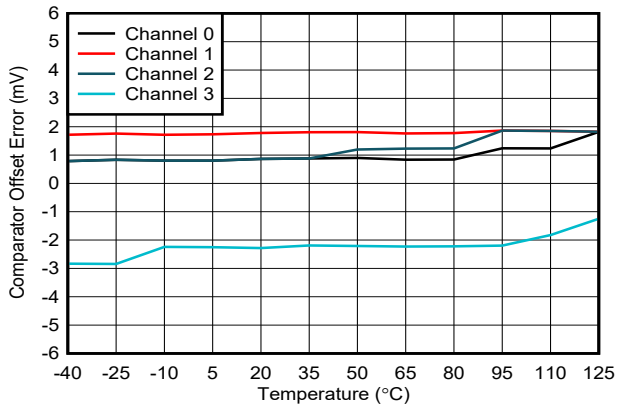
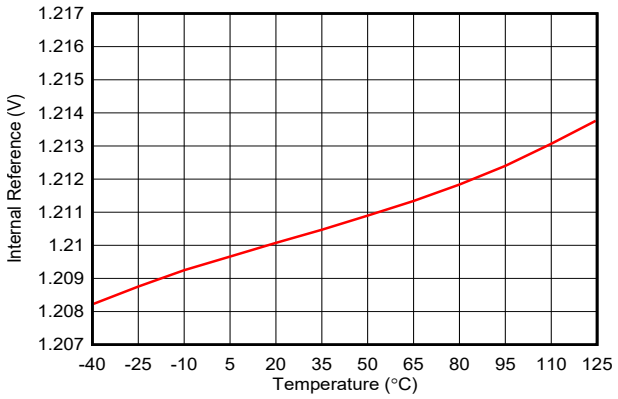


图 6-61. Comparator Offset Error vs Temperature

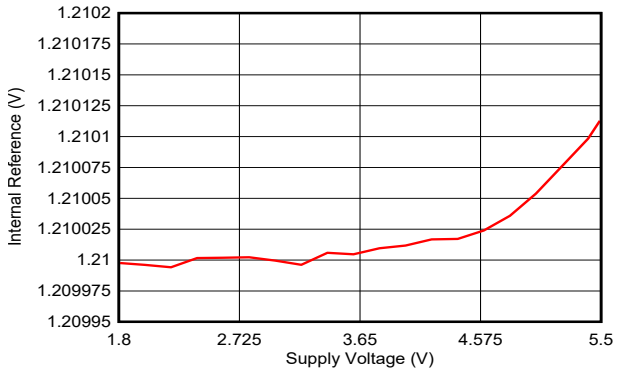
6.20 Typical Characteristics: General

at T_A = 25°C, V_{DD} = 5.5 V, and DAC outputs unloaded (unless otherwise noted)



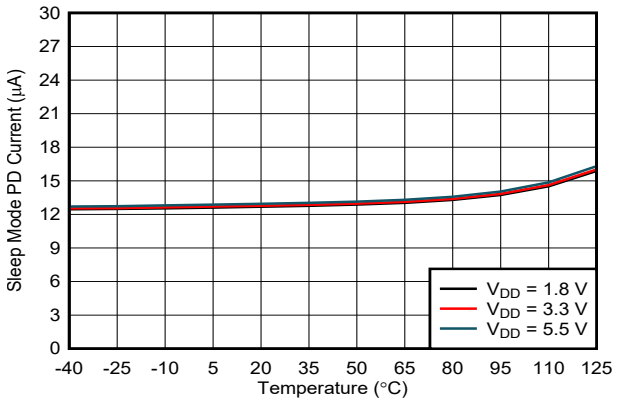
Internal reference

图 6-62. Internal Reference vs Temperature



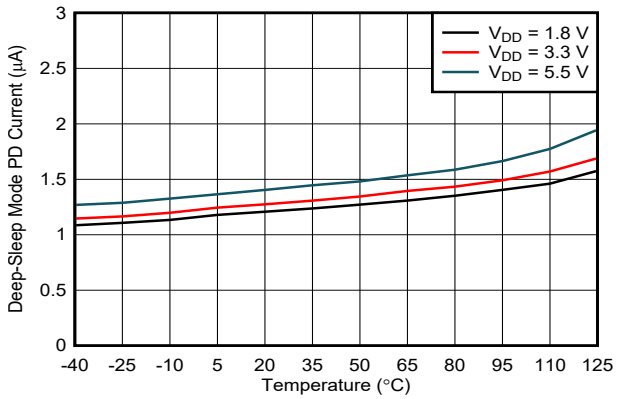
Internal reference

图 6-63. Internal Reference vs Supply Voltage



Sleep mode, internal reference disabled

图 6-64. Power-Down Current vs Temperature



Deep-sleep mode

图 6-65. Power-Down Current vs Temperature

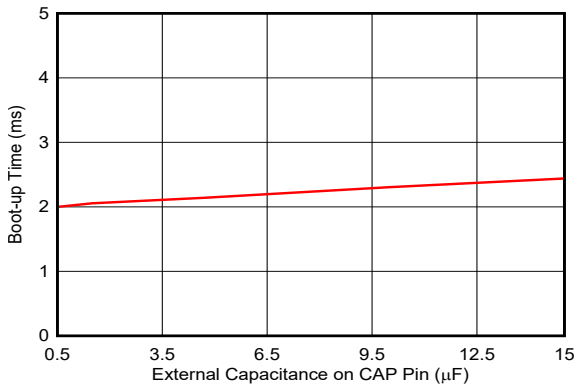


图 6-66. Boot-up Time vs Capacitance on CAP pin

7 详细说明

7.1 Overview

The 12-bit DAC63004W and 10-bit DAC53004W (DACx3004W) are a pin-compatible family of quad-channel, buffered, voltage-output and current-output, smart digital-to-analog converters (DACs). The DAC channels are independently configurable as voltage or current output. The DAC outputs change to Hi-Z when VDD is off. This feature is useful in voltage-margining applications. These smart DACs contain nonvolatile memory (NVM), an internal reference, automatically detectable SPI or I^2C interface, PMBus-compatibility in I^2C mode, force-sense output, and a general-purpose input. These devices support Hi-Z power-down modes by default, which can be configured to 10 kΩ-GND or 100 kΩ-GND using the NVM. The DACx3004W have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The DACx3004W operate with either an internal reference, external reference, or with a power supply as the reference, and provide a full-scale output of 1.8 V to 5.5 V.

The DACx3004W devices support I^2C standard mode (100Kbps), fast mode (400Kbps), and fast mode plus (1Mbps). The I^2C interface can be configured with four target addresses using the A0 pin. These devices also support specific PMBus commands such as *turn on/off*, *margin high or low*, and more. The SPI mode supports a three-wire interface by default with up to a 50-MHz SCLK input. The GPIO input can be configured as SDO in the NVM for SPI read capability. The GPIO input can alternatively be configured as the $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, $\overline{\text{FAULT-DUMP}}$, $\overline{\text{RESET}}$, or $\overline{\text{PROTECT}}$ function.

The DACx3004W also include digital slew rate control, and support standard waveform generation such as *sine and cosine*, *triangular*, and *sawtooth* waveforms. These devices can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB pin. The force-sense outputs of the DAC channels can be used as programmable comparators. The comparator mode allows programmable hysteresis, latching comparator, window comparator, and fault-dump to the NVM. These features enable the DACx3004W to go beyond the limitations of a conventional DAC that depends on a processor to function. As a result of *processor-less* operation and the *smart* feature set, the DACx3004W are called smart DACs.

7.2 Functional Block Diagram

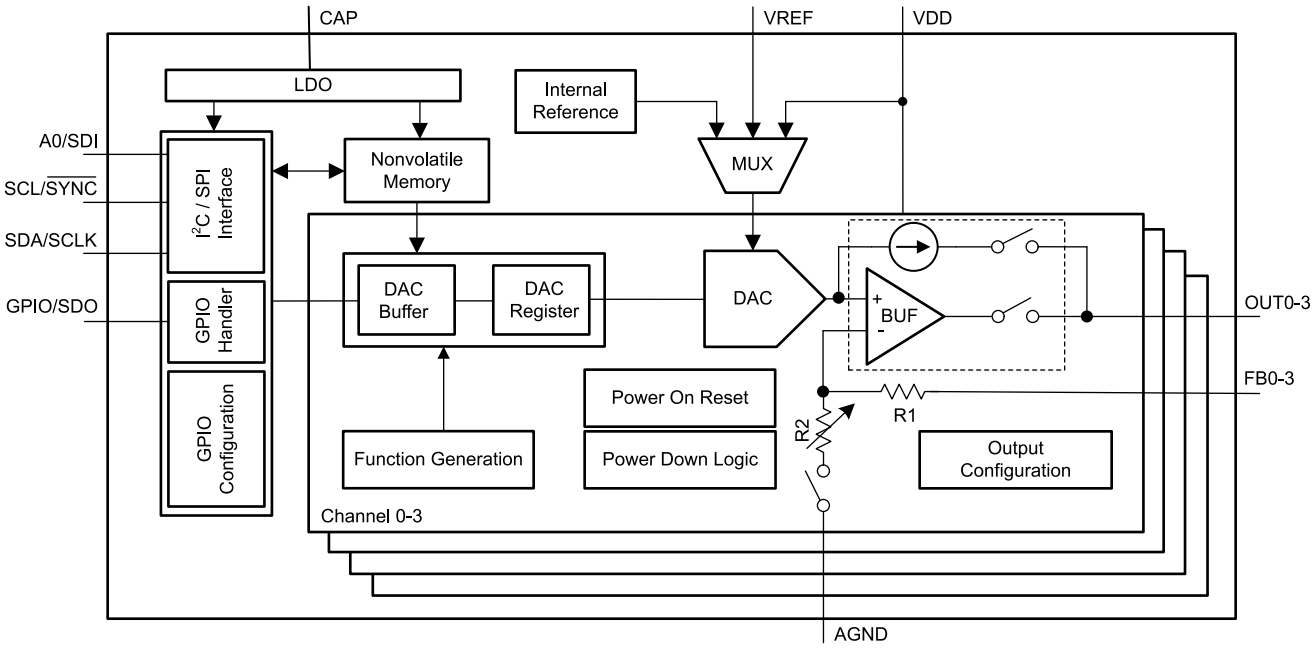


图 7-1. Functional Block Diagram

7.3 特性说明

7.3.1 智能数模转换器 (DAC) 架构

DACx3004W 器件采用串式架构,每个通道均具有一个电压输出放大器,一个外部 FB 引脚和电压电流转换器。节 7.2 显示了方框图中的 DAC 架构，该架构采用 1.8V 至 5.5V 电源供电。DAC 的内部电压基准为 1.21V。有一个选项可以选择 VREF 引脚上的外部基准或以电源作为基准。电压输出模式使用这三个基准选项之一。电流输出模式使用内部带隙来生成电流输出。电压和电流输出模式均支持多个可编程输出范围。

DACx3004W 器件在 VDD 关闭时支持高阻态输出，能够在强制电压高达 1.25V 的条件下在输出引脚上保持极低的泄漏电流。默认情况下，DAC 输出引脚也以高阻抗模式启动，这使得这些器件非常适合电压裕量和调节应用。要将加电模式更改为 10kΩ GND 或 100kΩ GND，需对 COMMON-CONFIG 寄存器中相应的 VOUT-PDN-X 字段进行编程，并将这些位加载到器件 NVM 中。

DACx3004W 器件支持每个通道的独立比较器模式。相应的 FBx 引脚充当比较器的输入。DAC 架构支持使用寄存器设置反转比较器输出。比较器输出可以是推挽式或开漏式。比较器模式支持使用*裕度高*和*裕度低*寄存器字段的可编程迟滞、锁存比较器和窗口比较器。比较器输出可由器件在内部访问。

DACx3004W 器件包括一个*智能*功能集，可实现无处理器运行和高度集成。NVM 支持可预测的启动。在没有处理器时，或者处理器或软件出现故障时，GPIO 在没有 I^2C 接口的情况下触发 DAC 输出。集成功能和 FBx 引脚可为控制应用启用 PWM 输出。FBx 引脚使该器件能够用作可编程比较器。数字转换率控制和高阻态断电模式可实现轻松的电压裕量和调节功能。

7.3.2 数字输入/输出

DACx3004W 有四个数字 IO 引脚，其中包括 I^2C、SPI、PMBus 和 GPIO 接口。这些器件会在加电后首次成功通信时自动检测 I^2C 和 SPI 协议，然后连接到检测到的接口。连接接口协议后，协议中的任何更改都将被忽略。I^2C 接口使用 A0 引脚从四个地址选项中进行选择。SPI 接口默认为 3 线接口。此模式下没有回读功能。GPIO 引脚可在寄存器映射中配置，然后编程到 NVM 中作为 SDO 引脚。SPI 回读模式比写入模式慢。编程接口引脚为：

- I^2C：SCL、SDA、A0
- SPI：SCLK、SDI、$\overline{\text{SYNC}}$、SDO/GPIO

GPIO 可配置为 SDO 以外的多种功能。这些是 $\overline{\text{LDAC}}$、$\overline{\text{PD}}$、$\overline{\text{STATUS}}$、$\overline{\text{PROTECT}}$、$\overline{\text{FAULT-DUMP}}$ 和 $\overline{\text{RESET}}$。当用作输出时，所有数字引脚都是开漏。因此，必须使用外部电阻器将所有输出引脚上拉至所需的 IO 电压。

7.3.3 Nonvolatile Memory (NVM)

The DACx3004W contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in the highlighted gray cells in the *Register Map* section, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG is an autoresetting bit. The default values for all the registers in the DACx3004W are loaded from NVM as soon as a POR event is issued.

The DACx3004W also implement NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. After completion, the device autoresets the NVM-RELOAD bit to 0. During the NVM write or reload operation, all read/write operations to the device are blocked. The *Electrical Characteristics: General* section provides the timing specification for the NVM write cycle. The processor must wait for the specified duration before resuming any read or write operation on the SPI or I^2C interface.

7.3.4 Power Consumption

The power consumption of the DACx3004W in sleep mode and deep-sleep mode are provided in the *Typical Characteristics: General* section. In normal operation, the total power consumption of the device depends on the number of channels powered on and the output mode of each channel (voltage or current). In current-output mode, the I_{DD} also depends on the output range. The I_{DD} calculation excludes the load current. For example, in the ±250 μA output mode with a DAC setting of +125 μA, the total current drawn through the VDD pin is the total I_{DD} plus 125 μA. The total I_{DD} in normal operation can be calculated using 方程式 1.

$$P_{NORMAL\_MODE} = V_{DD} \times \left(I_{DD\_SLEEP} + I_{DD\_REF}\right) + \sum_{X=0}^{3} \left(V_{DD} \times I_{DD\_X}\right) \quad (1)$$

where:

- I_{DD_SLEEP} is the current through V_{DD} in sleep mode when all the channels and internal reference are powered down.
- I_{DD_REF} is the reference current, which is:
  - either the current drawn by the reference input impedance when V_{DD} is used as reference
  - or the current drawn by the internal reference, if enabled
- I_{DD_X} is the current through V_{DD} for every powered-on channel-*X*.

备注

When an external reference is used, the current is calculated mainly as the current sourced from the external reference, which is equal to the reference voltage divided by the input impedance of the VREF pin.

7.4 器件功能模式

7.4.1 电压输出模式

通过在 COMMON-CONFIG 寄存器的 VOUT-PDN-X 字段中选择加电选项，并使用同一寄存器中的 IOUT-PDN-X 位同时为各个通道的电流输出选项断电，可以进入每个 DAC 通道的电压输出模式。将相应通道的 OUTx 和 FBx 引脚从外部短接可以实现闭环放大器输出。FBx 引脚开路会使放大器输出饱和。要获得所需的电压输出，请选择正确的基准选项，为所需的输出范围选择放大器增益，并在相应通道的 DAC-X-DATA 寄存器中对 DAC 代码进行编程。

7.4.1.1 电压基准和 DAC 传递函数

DACx3004W 可以支持以下三种电压基准选项：内部基准、外部基准，以及以电源作为基准，如图 7-2 所示。电压输出和比较器模式下的 DAC 传递函数会根据电压基准选择而变化。

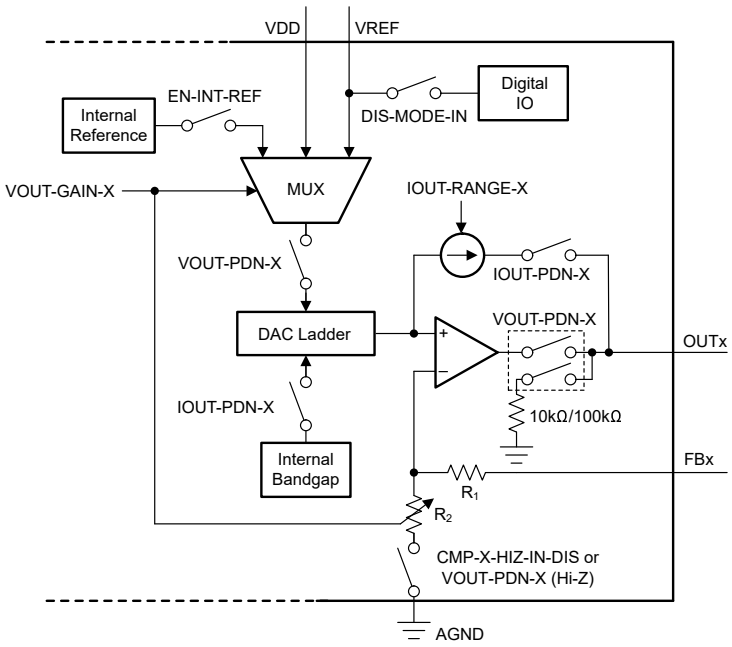


图 7-2. 电压基准选择与断电逻辑

7.4.1.1.1 Internal Reference

The DACx3004W contain an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-X bit in the DAC-X-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V_{OUT}). 方程式 2 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \quad (2)$$

where:

- N is the resolution in bits, 10 (DAC53004W) or 12 (DAC63004W).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit in the DAC-X-DATA register. DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V (typical).
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-GAIN-X bits.

7.4.1.1.2 External Reference

By default, the DACx3004W operate from an external reference input. The external reference option can also be selected by configuring the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register appropriately. Write 1 to the DIS-MODE-IN bit in the DEVICE-MODE-CONFIG register to minimize I_{DD}. The external reference can be between 1.7 V and VDD. 方程式 3 shows DAC transfer function when the external reference is used. The gain at the output stage of the DAC is always 1 × in the external reference mode.

备注

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (3)$$

where:

- N is the resolution in bits, 10 (DAC53004W) or 12 (DAC63004W).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register. DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the external reference voltage.

7.4.1.1.3 Power-Supply as Reference

The DACx3004W can operate with the power-supply pin (VDD) as a reference. 方程式 4 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1x.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \quad (4)$$

where:

- N is the resolution in bits, 10 (DAC53004W) or 12 (DAC63004W).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{DD} is used as the DAC reference voltage.

7.4.2 Current-Output Mode

To enter current-output mode for each DAC channel, disable the respective IOUT-PDN-X bits in the COMMON-CONFIG register, and set the respective VOUT-PDN-X bits in the same register to Hi-Z power-down mode. Select the desired current-output range by writing to the IOUT-RANGE-X bit in the DAC-X-IOUT-MISC-CONFIG register. To minimize leakage in current-output mode, disconnect the FBx pin. For the best power-on glitch performance, program the NVM with IOUT mode using the smallest output range before powering on the output channel, and then immediately program the DAC code and desired output range. The transfer function of the output current is shown in the following equation:

$$I_{OUT} = \frac{DAC\_DATA \times (I_{MAX} - I_{MIN})}{2^8} + I_{MIN} \quad (5)$$

where:

- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bits specified in 节 7.6.8 or the DAC-X-DATA-8BIT bits specified in 节 7.6.19. DAC_DATA ranges from 0 to 255.
- I_{MAX} is the signed maximum current in the IOUT-RANGE-X setting specified in 节 7.6.5.
- I_{MIN} is the signed minimum current in the IOUT-RANGE-X setting specified in 节 7.6.5.

7.4.3 比较器模式

在电压输出模式下，所有 DAC 通道均可配置为可编程比较器。要进入某个通道的比较器模式，需向相应 DAC-X-VOUT-CMP-CONFIG 寄存器的 CMP-X-EN 位中写入 1。比较器输出可使用 CMP-X-OD-EN 位配置为推挽或开漏输出。要启用输出引脚上的比较器输出，需向 CMP-X-OUT-EN 位写入 1。要反转比较器输出，需向 CMP-X-INV-EN 位写入 1。FBx 引脚具有有限阻抗。默认情况下，FBx 引脚处于高阻抗模式。要禁用 FBx 引脚上的高阻抗，需向 CMP-X-HIZ-IN-DIS 位写入 1。表 7-1 显示了不同位设置条件下该引脚上的比较器输出。

备注

在高阻态输入模式下，比较器输入范围限制为：

- 对于 GAIN = 1x、1.5x 或 2x：$V_{FB} \leq (V_{REF} \times GAIN) / 3$
- 对于 GAIN = 3x 或 4x：$V_{FB} \leq (V_{REF} \times GAIN) / 6$

任何较高的输入电压都会被削波。

表 7-1. 比较器输出配置

CMP-X-EN	CMP-X-OUT-EN	CMP-X-OD-EN	CMP-X-INV-EN	CMPX-OUT PIN
0	X	X	X	比较器未启用
1	0	X	X	无输出
1	1	0	0	推挽式输出
1	1	0	1	推挽和反相输出
1	1	1	0	开漏输出
1	1	1	1	开漏和反相输出

图 7-3 显示了所有 DAC 通道均配置为比较器时的接口电路。可编程比较器操作如图 7-4 所示。在无迟滞、带迟滞和窗口比较器模式下，可以使用相应 DAC-X-CMP-MODE-CONFIG 寄存器中的 CMP-X-MODE 位来配置各个比较器通道，如表 7-2 所示。

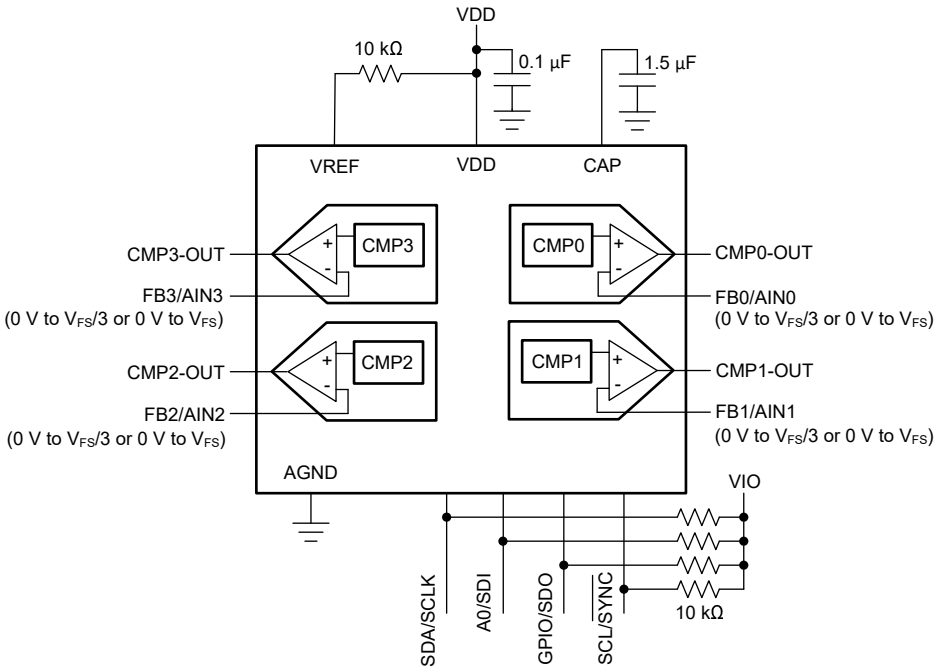


图 7-3. 比较器接口

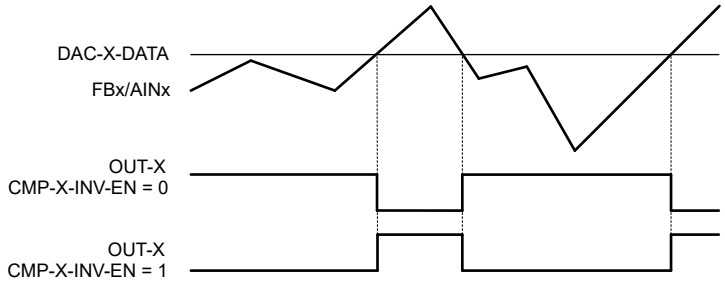


图 7-4. 可编程比较器操作

表 7-2. 比较器模式选择

CMP-X-MODE 位字段	比较器配置
00	正常比较器模式。无迟滞或窗口操作。
01	迟滞比较器模式。DAC-X-MARGIN-HIGH 和 DAC-X-MARGIN-LOW 寄存器设置迟滞。
10	窗口比较器模式。DAC-X-MARGIN-HIGH 和 DAC-X-MARGIN-LOW 寄存器设置窗口边界。
11	无效设置

7.4.3.1 可编程迟滞比较器

当 CMP-X-MODE 位设置为 01b 时，比较器模式提供迟滞，如表 7-2 所示。迟滞由 DAC-X-MARGIN-HIGH 和 DAC-X-MARGIN-LOW 寄存器提供，如图 7-5 所示。

当 DAC-X-MARGIN-HIGH 设置为全代码或 DAC-X-MARGIN-LOW 设置为零代码时，比较器用作锁存比较器，即在超过阈值后锁存输出。通过写入 COMMON DAC-TRIG 寄存器中相应的 RST-CMP-FLAG-X 位，可以复位锁存输出。图 7-6 显示了具有低电平有效输出的闭锁比较器的行为，而图 7-7 显示了具有高电平有效输出的闭锁比较器的行为。

备注

DAC-X-MARGIN-HIGH 寄存器的值必须大于 DAC-X-MARGIN-LOW 寄存器的值。迟滞模式下的比较器输出只能是同相的，即 DAC-X-VOUT-CMP-CONFIG 寄存器中的 CMP-X-INV-EN 位必须设置为 0。在锁存模式下，为了使复位生效，输入电压必须在 DAC-X-MARGIN-HIGH 和 DAC-X-MARGIN-LOW 范围内。

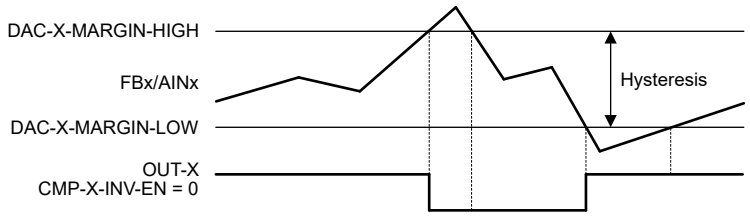


图 7-5. 不带锁存输出的可编程迟滞

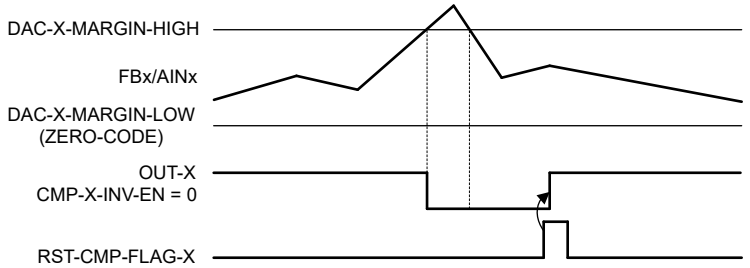


图 7-6. 具有低电平有效输出的闭锁比较器

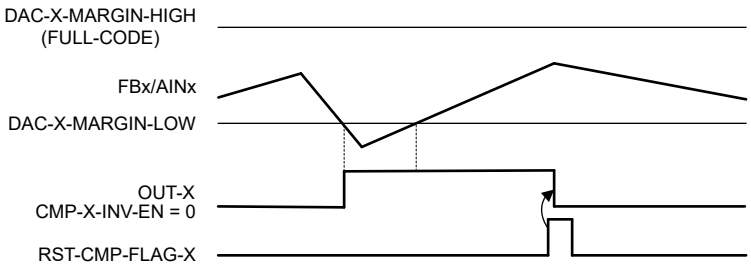


图 7-7. 具有高电平有效输出的锁存比较器

7.4.3.2 Programmable Window Comparator

Window comparator mode is enabled by setting the CMP-X-MODE bit to 10b, as shown in 表 7-2. The window bounds are set by the DAC-X-MARGIN-HIGH and the DAC-X-MARGIN-LOW registers, as shown in 图 7-8. The output of the window comparator for a given channel is indicated by the respective WIN-CMP-X bit in the CMP-STATUS register. The comparator output (WIN-CMP-X) can be latched by writing 1 to the WIN-LATCH-EN bit in the COMMON-CONFIG register. After being latched, the comparator output can be reset using the corresponding RST-CMP-FLAG-X bit in the COMMON-DAC-TRIG register. For the reset to take effect, the input must be within the window bounds.

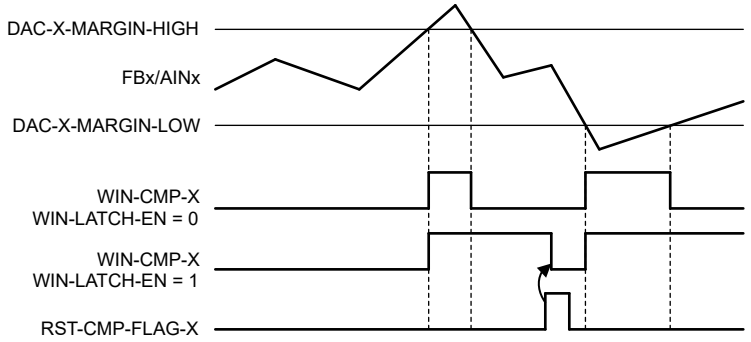


图 7-8. Window Comparator Operation

A single comparator is used per channel to check both the *margin-high* and *margin-low* limits of the window. Therefore, the window comparator function has a finite response time as specified in the *Electrical Characteristics: Comparator Mode* section. Also, the static behavior of the WIN-CMP-X bit is not reflected at the output pins. Set the CMP-X-OUT-EN bit to 0. The WIN-CMP-X bit must be read digitally using the communication interface. This bit can also be mapped to the GPIO pin, as shown in 表 7-19.

备注

- The value of the DAC-X-MARGIN-HIGH register must be greater than that of the DAC-X-MARGIN-LOW register.
- Set the SLEW-RATE-X bit to 0000b (no-slew) and LOG-SLEW-EN-X bit to 0b in the DAC-X-FUNC-CONFIG register to get the best response time from the window comparator.
- The CMP-X-OUT-EN bit in the DAC-X-VOUT-CMP-CONFIG register can be set to 0b to eliminate undesired toggling of the OUT pin.

7.4.4 故障转储模式

DACx3004W 提供了一项功能，可在 FAULT-DUMP 位触发时或映射到故障转储的 GPIO（如表 7-18 所示）时将几个寄存器内容保存到 NVM 中。此功能在系统级故障管理中非常有用，可用于捕获就在故障触发之前的器件或系统状态，以便在故障发生后进行诊断。故障转储触发时保存的寄存器为：

- CMP-STATUS[7:0]
- DAC-0-DATA[15:8]
- DAC-1-DATA[15:8]
- DAC-2-DATA[15:8]
- DAC-3-DATA[15:8]

备注

在故障转储期间，数据中的任何更改都会破坏最终结果。确保比较器和 DAC 代码在 NVM 写入周期期间保持稳定。

表 7-3 显示了 NVM 中寄存器的存储格式。

表 7-3. 故障转储 NVM 存储格式

NVM 行	B31-B24	B23-B16	B15-B8	B7-B0
行 1	CMP-STATUS[7:0]	不用考虑		
行 2	DAC-0-DATA[15:8]	DAC-1-DATA[15:8]	DAC-2-DATA[15:8]	DAC-3-DATA[15:8]

故障转储后在 NVM 中捕获的数据可按特定顺序读取：

1. 将 COMMON-CONFIG 寄存器中的 EE-READ-ADDR 位设置为 0b，以选择 NVM 的行 1。
2. 通过向 COMMON-TRIGGER 寄存器中的 READ-ONE-TRIG 写入 1 来触发所选 NVM 行的读取；该位会自动复位。此操作会将数据从选定的 NVM 行复制到 SRAM 地址 0x9D（LSB 16 位来自 NVM）和 0x9E（MSB 16 位来自 NVM）。
3. 要读取 SRAM 数据，需按照以下步骤操作：
   a. 将 0x009D 写入 SRAM-CONFIG 寄存器。
   b. 从 SRAM-DATA 寄存器中读取数据以获得 LSB 16 位。
   c. 将 0x009E 写入 SRAM-CONFIG 寄存器。
   d. 再次从 SRAM-DATA 寄存器读取数据以获得 MSB 位。
4. 将 COMMON-CONFIG 寄存器中的 EE-READ-ADDR 位设置为 1b，以选择 NVM 的行 2。重复步骤 2 和 3。

7.4.5 应用特定模式

本节详细介绍了 DACx3004W 中提供的各个应用特定功能模式。

7.4.5.1 电压裕量和调节

电压裕量和调节是 DACx3004W 的一种主要应用。本节介绍了可用于此类应用的具体功能，例如高阻态输出、转换率控制、$\overline{\text{PROTECT}}$ 输入和 PMBus 兼容性。

7.4.5.1.1 高阻抗输出和 $\overline{\text{PROTECT}}$ 输入

当 VDD 关闭时，所有 DAC 输出通道都保持高阻抗状态（高阻态）。图 7-9 显示了在电压裕量调节应用中使用 DACx3004W 的简化原理图。串联电阻器 R_S 在电压输出模式下是必需的，但在电流输出模式下是可选的。几乎所有线性稳压器和直流/直流转换器都具有 ≤ 1.25V 的反馈电压。对于 V_{FB} ≤ 1.25V，输出端保持低泄漏电流。因此，对于所有实际用途，当 DAC 的 VDD 在电压裕量和调节应用中处于关闭时，DAC 输出显示为高阻态。此功能允许将 DACx3004W 无缝集成到系统中，而无需为 DAC 进行额外的电源时序控制。

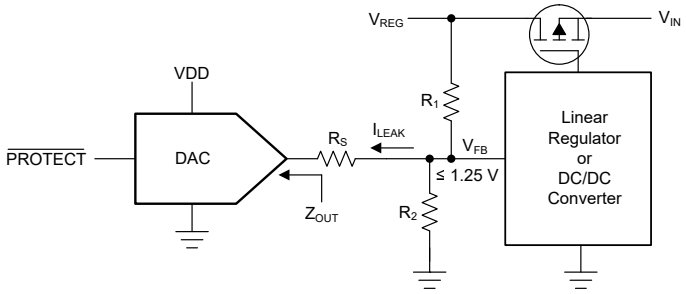


图 7-9. 高阻抗（高阻态）输出和 $\overline{\text{PROTECT}}$ 输入

DAC 通道在启动时断电至高阻态。输出可以使用与直流/直流转换器或线性稳压器的标称输出相对应的预编程代码加电。此功能可实现 DAC 的平稳加电和断电，而不影响直流/直流转换器或线性稳压器的反馈环路。

DACx3004W 的 GPIO 引脚可配置为 $\overline{\text{PROTECT}}$ 功能，如表 7-18 所示。$\overline{\text{PROTECT}}$ 通过转换或直接转换将 DAC 输出变为可预测状态。在故障条件（如欠压）、子系统故障或软件崩溃要求 DAC 输出达到预定义状态而不涉及处理器的系统中，此功能非常有用。检测到的事件可以馈送到配置为 $\overline{\text{PROTECT}}$ 输入的 GPIO 引脚。$\overline{\text{PROTECT}}$ 功能可以使用 COMMON-TRIGGER 寄存器中的 PROTECT 位来触发。$\overline{\text{PROTECT}}$ 功能的行为可以使用 DEVICE-MODE-CONFIG 寄存器的 PROTECT-CONFIG 字段配置，如表 7-4 所示。

备注

- 在 $\overline{\text{PROTECT}}$ 功能触发后，通信接口上的写入功能会被禁用，直到该功能完成。
- 当 $\overline{\text{PROTECT}}$ 功能触发时，CMP-STATUS 寄存器中的 PROTECT-FLAG 位会设置为 1。该位可以通过读取 CMP-STATUS 寄存器来轮询。在 $\overline{\text{PROTECT}}$ 功能完成后，CMP-STATUS 寄存器上的读取命令会将 PROTECT-FLAG 位复位。

表 7-4. $\overline{\text{PROTECT}}$ 功能配置

PROTECT-CONFIG 字段	功能
00	切换至高阻态断电模式（无转换）。
01	切换到存储在 NVM 中的 DAC 代码（无转换），然后切换到高阻态断电模式。
10	转换为裕度低代码，然后切换到高阻态断电模式。
11	转换为裕度高代码，然后切换到高阻态断电模式。

7.4.5.1.2 Programmable Slew-Rate Control

When the DAC data registers are written, the voltage on DAC output (V_{OUT}) immediately transitions to the new code following the slew rate and settling time specified in the *Electrical Characteristics*.

The slew rate control feature allows the user to control the rate at which the output voltage (V_{OUT}) changes. When this feature is enabled (using the SLEW-RATE-X[3:0] bits), the DAC output changes from the current code to the code in the DAC-X-MARGIN-HIGH or DAC-X-MARGIN-LOW registers (when margin high or low commands are issued to the DAC) using the step size and time-period per step set in CODE-STEP-X and SLEW-RATE-X bits in the DAC-X-FUNC-CONFIG register:

- SLEW-RATE-X defines the time-period per step at which the digital slew updates.
- CODE-STEP-X defines the number of LSBs by which the output value changes at each update, for the corresponding channels.

表 7-5 and 表 7-6 show different settings available for CODE-STEP-X and SLEW-RATE-X. With the default slew rate control setting of no-slew, the output changes immediately at a rate limited by the output drive circuitry and the attached load.

When the slew rate control feature is used, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output as shown in 图 7-10. Do not write to CODE-STEP-X, SLEW-RATE-X, or DAC-X-DATA during the output slew operation. 方程式 6 provides the equation for the calculating the slew time (t_{SLEW}).

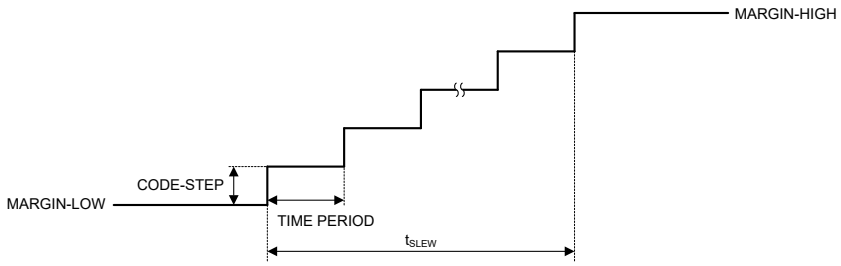


图 7-10. Programmable Slew-Rate Control

$$t_{SLEW} = SLEW\_RATE \times CEILING\left(\frac{MARGIN\_HIGH - MARGIN\_LOW}{CODE\_STEP} + 1\right) \quad (6)$$

where:

- SLEW_RATE is the SLEW-RATE-X setting as specified in 表 7-6.
- CODE_STEP is the CODE-STEP-X setting as specified in 表 7-5.
- MARGIN_HIGH is the decimal value of the DAC-X-MAGIN-HIGH bits specified in the DAC-X-MARGIN-HIGH register.
- MARGIN_LOW is the decimal value of the DAC-X-MAGIN-LOW bits specified in the DAC-X-MARGIN-LOW register.

表 7-5. Code Step

REGISTER	CODE-STEP-X[2]	CODE-STEP-X[1]	CODE-STEP-X[0]	CODE STEP SIZE
DAC-X-FUNC-CONFIG	0	0	0	1 LSB (default)
	0	0	1	2 LSB
	0	1	0	3 LSB
	0	1	1	4 LSB
	1	0	0	6 LSB
	1	0	1	8 LSB
	1	1	0	16 LSB
	1	1	1	32 LSB

表 7-6. Slew Rate

REGISTER	SLEW-RATE-X[3]	SLEW-RATE-X[2]	SLEW-RATE-X[1]	SLEW-RATE-X[0]	TIME PERIOD (PER STEP)
DAC-X-FUNC-CONFIG	0	0	0	0	No slew (default)
	0	0	0	1	4 µs
	0	0	1	0	8 µs
	0	0	1	1	12 µs
	0	1	0	0	18 µs
	0	1	0	1	27.04 µs
	0	1	1	0	40.48 µs
	0	1	1	1	60.72 µs
	1	0	0	0	91.12 µs
	1	0	0	1	136.72 µs
	1	0	1	0	239.2 µs
	1	0	1	1	418.64 µs
	1	1	0	0	732.56 µs
	1	1	0	1	1282 µs
	1	1	1	0	2563.96 µs
	1	1	1	1	5127.92 µs

7.4.5.1.3 PMBus Compatibility Mode

The PMBus protocol is an I^{2}C-based communication standard for power-supply management. PMBus contains standard command codes tailored to power supply applications. The DACx3004W implement some PMBus commands such as *Turn Off*, *Turn On*, *Margin Low*, *Margin High*, *Communication Failure Alert Bit (CML)*, as well as *PMBUS revision*. 图 7-11 shows typical PMBus connections. The EN-PMBUS bit in the INTERFACE-CONFIG register must be set to 1 to enable the PMBus protocol.

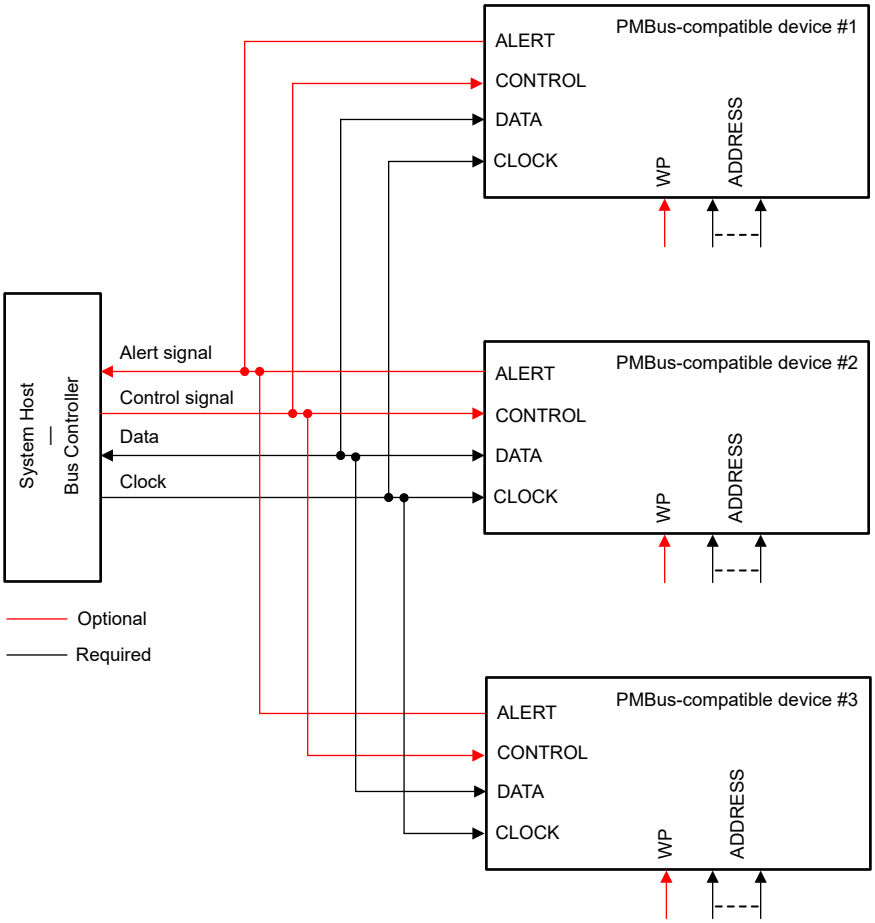


图 7-11. PMBus Connections

Similar to I²C, PMBus is a variable length packet of 8-bit data bytes, each with a receiver acknowledge, wrapped between a start and stop bit. The first byte is always a 7-bit *target address* followed by a *write* bit, sometimes called the *even address* that identifies the intended receiver of the packet. The second byte is an 8-bit *command* byte, identifying the PMBus command being transmitted using the respective command code. After the command byte, the transmitter either sends data associated with the command to write to the receiver command register (from least significant byte to most significant byte, as shown in 表 7-7), or sends a new start bit indicating the desire to read the data associated with the command register from the receiver. Then the receiver transmits the data following the same least significant byte first format (see 表 7-8).

表 7-7. PMBus Update Sequence

MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte 节 7.5.2.2.1				Command byte 节 7.5.2.2.2				Data byte - LSDB				Data byte - MSDB (Optional)			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

表 7-8. PMBus Read Sequence

S	MSB	...	R/$\overline{W}$ (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/$\overline{W}$ (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
	ADDRESS BYTE 节 7.5.2.2.1				COMMAND BYTE 节 7.5.2.2.2				Sr	ADDRESS BYTE 节 7.5.2.2.1				LSDB				MSDB (Optional)			
From Controller				Target	From Controller			Target	From Controller				Target	From Target			Controller	From Target			Controller

The DACx3004W I²C interface implements some of the PMBus commands. 表 7-9 shows the supported PMBus commands that are implemented in DACx3004W. The DAC uses DAC-X-MARGIN-LOW, DAC-X-MARGIN-HIGH bits, SLEW-RATE-X, and CODE-STEP-X bits for PMBUS-OPERATION-CMD-X. To access multiple channels, write the PMBus page address as specified in the *Register Names* table in the *Register Map* section to the PMBUS-PAGE register first, followed by a write to the channel-specific register.

表 7-9. PMBus Operation Commands

REGISTER	PMBUS-OPERATION-CMD-X[15:8]	DESCRIPTION
PMBUS-OP-CMD-X	00h	Turn off
	80h	Turn on
	94h	Margin low
	A4h	Margin high

The DACx3004W also implement PMBus features such as group command protocol and communication time-out failure. The CML bit in the PMBUS-CML register indicates a communication fault in the PMBus. This bit is reset by writing 1.

To get the PMBus version, read the PMBUS-VERSION register.

7.4.5.2 函数生成

DACx3004W 实施了连续函数或波形生成功能。这些器件可以为每个通道独立生成三角波、锯齿波和正弦波。

7.4.5.2.1 Triangular Waveform Generation

图 7-12 shows that the triangular waveform uses the DAC-X-MARGIN-LOW (FUNCTION-MIN) and DAC-X-MARGIN-HIGH (FUNCTION-MAX) registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in 方程式 7. An external RC load with a time-constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Writing 0b000 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects triangular waveform.

$$f_{TRIANGLE} = \frac{1}{2 \times TIME\_STEP \times CEILING\left(\frac{FUNCTION\_MAX - FUNCTION\_MIN}{CODE\_STEP}\right)} \quad (7)$$

where:

- TIME_STEP is the SLEW-RATE-X setting as specified in 表 7-6.
- CODE_STEP is the CODE-STEP-X setting as specified in 表 7-5.
- FUNCTION_MAX is the decimal value of DAC-X-MAGIN-HIGH bits specified in the DAC-X-MARGIN-HIGH register.
- FUNCTION_MIN is the decimal value of the DAC-X-MAGIN-LOW bits specified in the DAC-X-MARGIN-LOW register.

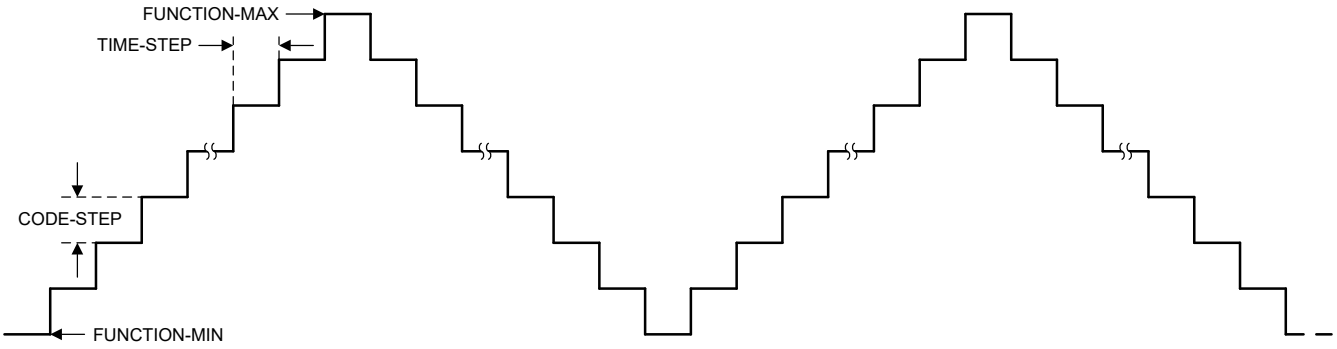


图 7-12. Triangle Waveform

7.4.5.2.2 Sawtooth Waveform Generation

图 7-13 shows the sawtooth and the inverse sawtooth waveforms use the DAC-X-MARGIN-LOW (FUNCTION-MIN) and DAC-X-MARGIN-HIGH (FUNCTION-MAX) registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in 方程式 8. An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Write 0b001 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register to select sawtooth waveform, and write 0b010 to select inverse sawtooth waveform.

$$f_{SAWTOOTH} = \frac{1}{TIME\_STEP \times CEILING\left(\frac{FUNCTION\_MAX - FUNCTION\_MIN}{CODE\_STEP} + 1\right)} \quad (8)$$

where:

- TIME_STEP is the SLEW-RATE-X setting as specified in 表 7-6.
- CODE_STEP is the CODE-STEP-X setting as specified in 表 7-5.
- FUNCTION_MAX is the decimal value of the DAC-X-MAGIN-HIGH bits specified in the DAC-X-MARGIN-HIGH register.
- FUNCTION_MIN is the decimal value of the DAC-X-MAGIN-LOW bits specified in the DAC-X-MARGIN-LOW.

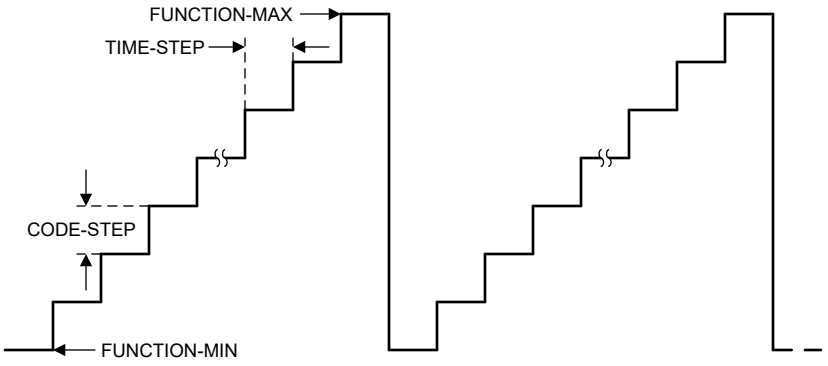


图 7-13. Sawtooth Waveform

7.4.5.2.3 Sine Waveform Generation

The sine wave function uses 24 preprogrammed points per cycle. The frequency of the sine wave depends on the SLEW-RATE settings as shown in 方程式 9:

$$f_{SINE\_WAVE} = \frac{1}{24 \times SLEW\_RATE} \quad (9)$$

where SLEW_RATE is the SLEW-RATE-X setting as specified in 表 7-6.

An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The SLEW-RATE-X setting is available in the DAC-X-FUNC-CONFIG register. Writing 0b100 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects sine wave. The codes for the sine wave are fixed. Use the gain settings at the output amplifier for changing the full-scale output using the internal reference option. The gain settings are accessible through the VOUT-GAIN-X bits in the DAC-X-VOUT-CMP-CONFIG register. 表 7-10 shows the list of hard-coded discrete points for the sine wave with 12-bit resolution and 图 7-14 shows the pictorial representation of the sine wave. There are four phase settings available for the sine wave that are selected using the PHASE-SEL-X bit in the DAC-X-FUNC-CONFIG register.

表 7-10. Sine Wave Data Points

SEQUENCE	12-BIT VALUE		SEQUENCE	12-BIT VALUE
0 (0° phase start)	0x800		12	0x800
1	0x9A8		13	0x658
2	0xB33		14	0x4CD
3	0xC87		15	0x379
4	0xD8B		16 (240° phase start)	0x275
5	0xE2F		17	0x1D1
6 (90° phase start)	0xE66		18	0x19A
7	0xE2F		19	0x1D1
8 (120° phase start)	0xD8B		20	0x275
9	0xC87		21	0x379
10	0xB33		22	0x4CD
11	0x9A8		23	0x658

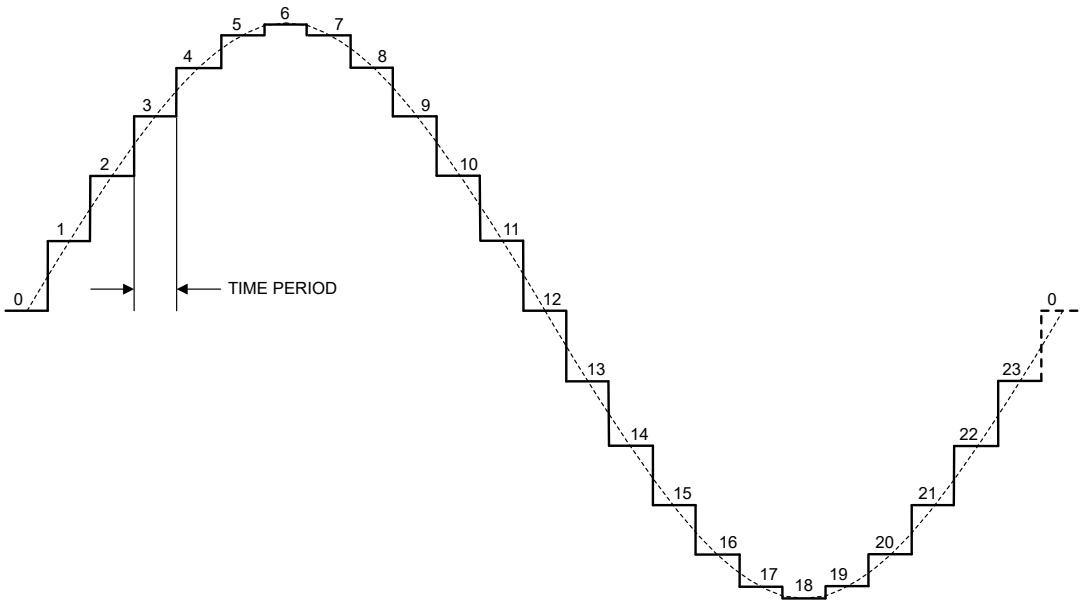


图 7-14. Sine Wave Generation

7.4.6 器件复位和故障管理

本节详细介绍了 DACx3004W 的上电复位 (POR)、软件复位以及其他诊断和故障管理功能。

7.4.6.1 上电复位 (POR)

DACx3004W 系列器件包含上电复位 (POR) 功能，可在加电时控制输出电压。在建立 V_{DD} 电源后，便会发出 POR 事件。POR 使所有寄存器初始化为默认值，只有在 POR（启动）延迟之后，与该器件的通信才有效。一旦发生 POR 事件，DACx3004W 中所有寄存器的默认值都将立即从 NVM 加载。

该器件加电时，POR 电路将器件设置为默认模式。POR 电路需要特定的 V_{DD} 电平（如图 7-15 所示）才能确保内部电容器在加电时放电并使器件复位。为了确保发生 POR，V_{DD} 小于 0.7V 的时间必须至少为 1ms。当 V_{DD} 降至低于 1.65V 但仍高于 0.7V（显示为未定义区域）时，该器件在所有指定的温度和电源条件下可能会也可能不会复位。在这种情况下，需启动 POR。当 V_{DD} 保持为大于 1.65V 时，不会发生 POR。

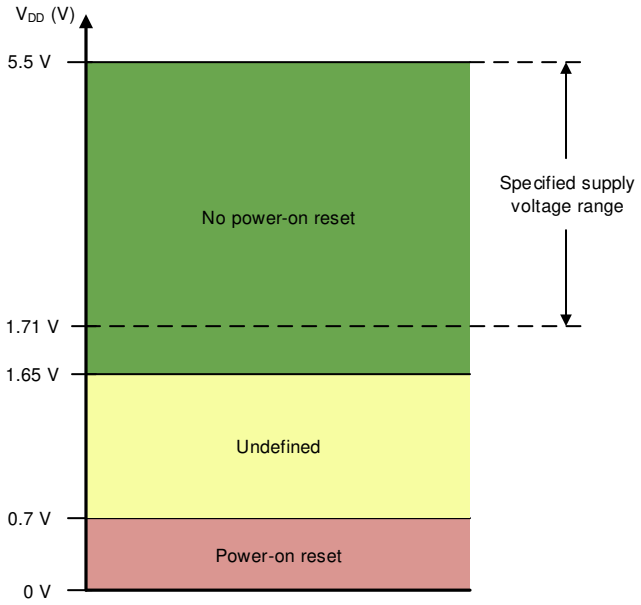


图 7-15. V_{DD} POR 电路的阈值电平

7.4.6.2 External Reset

An external reset to the device can be triggered through the GPIO pin or through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event. The GPIO pin can be configured as a $\overline{\text{RESET}}$ pin as shown in 表 7-18. This configuration must be programmed into the NVM so that the setting is not cleared after the device reset. The $\overline{\text{RESET}}$ input must be a low pulse. The device starts the boot-up sequence after the falling edge of the $\overline{\text{RESET}}$ input. The rising edge of the $\overline{\text{RESET}}$ input does not have any effect.

7.4.6.3 Register-Map Lock

The DACx3004W implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I^2C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4.6.4 NVM 循环冗余校验 (CRC)

DACx3004W 为 NVM 实施循环冗余校验 (CRC) 功能，以确保存储在 NVM 中的数据不被损坏。DACx3004W 中实现了两种类型的 CRC 报警位：

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

NVM-CRC-FAIL-USER 位指示用户可编程 NVM 位的状态，而 NVM-CRC-FAIL-INT 位指示内部 NVM 位的状态。CRC 功能通过在每次执行 NVM 程序操作（写入或重新加载）时以及在器件启动期间，存储 16 位 CRC (CRC-16-CCITT) 以及 NVM 数据来实现。器件会读取 NVM 数据并使用存储的 CRC 来验证数据。CRC 报警位（GENERAL-STATUS 寄存器中的 NVM-CRC-FAIL-USER 和 NVM-CRC-FAIL-INT）报告从器件 NVM 读取数据后的任何错误。报警位仅在启动时设置。

7.4.6.4.1 NVM-CRC-FAIL-USER 位

NVM-CRC-FAIL-USER 位为逻辑 1 表示用户可编程的 NVM 上数据已损坏。在这种情况下，DAC 中的所有寄存器都会使用出厂复位值进行初始化，并且任何 DAC 寄存器都可以写入或读取。要将报警位复位为 0，需发出软件复位（请参阅 *节 7.4.6.2*）命令或对 DAC 执行循环通电。软件复位或执行循环通电也会重新加载用户可编程的 NVM 位。如果故障仍然存在，需重新对 NVM 进行编程。

7.4.6.4.2 NVM-CRC-FAIL-INT 位

NVM-CRC-FAIL-INT 位为逻辑 1 表示内部 NVM 数据已损坏。在这种情况下，DAC 中的所有寄存器都会使用出厂复位值进行初始化，并且任何 DAC 寄存器都可以写入或读取。在发生临时故障时，要将报警位复位为 0，需发出软件复位（请参阅 *节 7.4.6.2*）命令或对 DAC 执行循环通电。NVM 中的永久故障会导致器件无法使用。

7.4.7 Power-Down Mode

The DACx3004W output amplifier and internal reference can be independently powered down through the EN-INT-REF, VOUT-PDN-X, and IOUT-PDN-X bits in the COMMON-CONFIG register, as shown in 图 7-2. At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the DAC outputs (OUTx pins) are in a high-impedance state. To change this state to 10 kΩ-AGND or 100 kΩ-AGND in the voltage-output mode (at power up), use the VOUT-PDN-X bits. The power-down state for current-output mode is always high-impedance.

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. 表 7-11 shows the DAC power-down bits. The individual channel power-down bits or the global device power-down function can be mapped to the GPIO pin using the GPIO-CONFIG register.

表 7-11. DAC Power-Down Bits

REGISTER	VOUT-PDN-X[1]	VOUT-PDN-X[0]	IOUT-PDN-X	DESCRIPTION
COMMON-CONFIG	0	0	1	Power up VOUT-X.
	0	1	1	Power down VOUT-X with 10 kΩ to AGND. Power down IOUT-X to Hi-Z.
	1	0	1	Power down VOUT-X with 100 kΩ to AGND. Power down IOUT-X to Hi-Z.
	1	1	1	Power down VOUT-X to Hi-Z. Power down IOUT-X to Hi-Z (default).
	1	1	0	Power down VOUT-X to Hi-Z. Power up IOUT-X.

7.5 编程

DACx3004W 通过 3 线 SPI 或 2 线 I²C 接口进行编程。4 线 SPI 模式通过将 GPIO 引脚映射为 SDO 来启用。SPI 回读操作的 SCLK 低于标准 SPI 写入操作。接口类型根据器件加电后的第一个通信协议来确定。在确定接口类型后，器件会在器件开启时忽略类型的任何更改。接口类型可以在下电上电后更改。

7.5.1 SPI 编程模式

通过将 $\overline{\text{SYNC}}$ 引脚置于低电平，可以启动 DACx3004W 的 SPI 访问周期。串行时钟 SCLK 可以是连续时钟或选通时钟。SDI 数据在 SCLK 下降沿上传输。DACx3004W 的 SPI 帧长度为 24 位。因此，$\overline{\text{SYNC}}$ 引脚必须保持低电平至少 24 个 SCLK 下降沿。当 $\overline{\text{SYNC}}$ 引脚取消置位为高电平时，访问周期结束。如果访问周期包含的时钟边沿小于最小值，则通信将被忽略。默认情况下，SDO 引脚未启用（三线 SPI）。在三线 SPI 模式下，如果访问周期包含的时钟边沿大于最小值，则器件仅使用前 24 位。当 $\overline{\text{SYNC}}$ 为高电平时，SCLK 和 SDI 信号会被阻止，同时 SDO 变为高阻态，以允许从总线上连接的其他器件回读数据。

表 7-12 和图 7-16 介绍了 24 位 SPI 访问周期的格式。SDI 的第一个字节输入是指令周期。指令周期将请求标识为读或写命令以及要访问的 7 位地址。周期中的最后 16 位构成数据周期。

表 7-12. SPI 读/写访问周期

位	字段	说明
23	R/$\overline{\text{W}}$	将通信标识为地址寄存器的读或写命令：R/$\overline{\text{W}}$ = 0 设置写入操作。R/$\overline{\text{W}}$ = 1 设置读取操作
22-16	A[6:0]	寄存器地址：指定在读取或写入操作期间要访问的寄存器
15-0	DI[15:0]	数据周期位：如果是写入命令，则数据周期位是要写入地址为 A[6:0] 的寄存器的值。如果是读取命令，则数据周期位为*不用考虑*值。

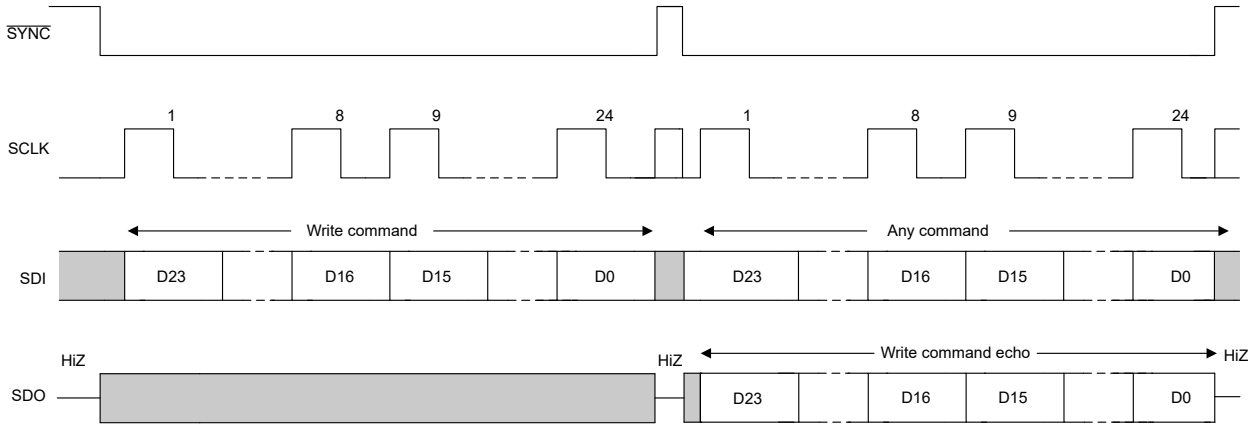


图 7-16. SPI 写入周期

读取操作要求首先通过设置 INTERFACE-CONFIG 寄存器中的 SDO-EN 位来启用 SDO 引脚。此配置称为四线 SPI。读取操作通过发出读取命令访问周期来启动。读取命令后，必须发出第二个访问周期来获取请求的数据。表 7-13 和图 7-17 显示了输出数据格式。根据 FSDO 位，数据通过 SDO 引脚在 SCLK 的下降沿或上升沿输出，如图 6-3 所示。

表 7-13. SDO 输出访问周期

位	字段	说明
23	R/$\overline{\text{W}}$	来自上一访问周期的回波 R/$\overline{\text{W}}$
22-16	A[6:0]	来自上一访问周期的回波寄存器地址
15-0	DI[15:0]	上一访问周期中请求的回读数据

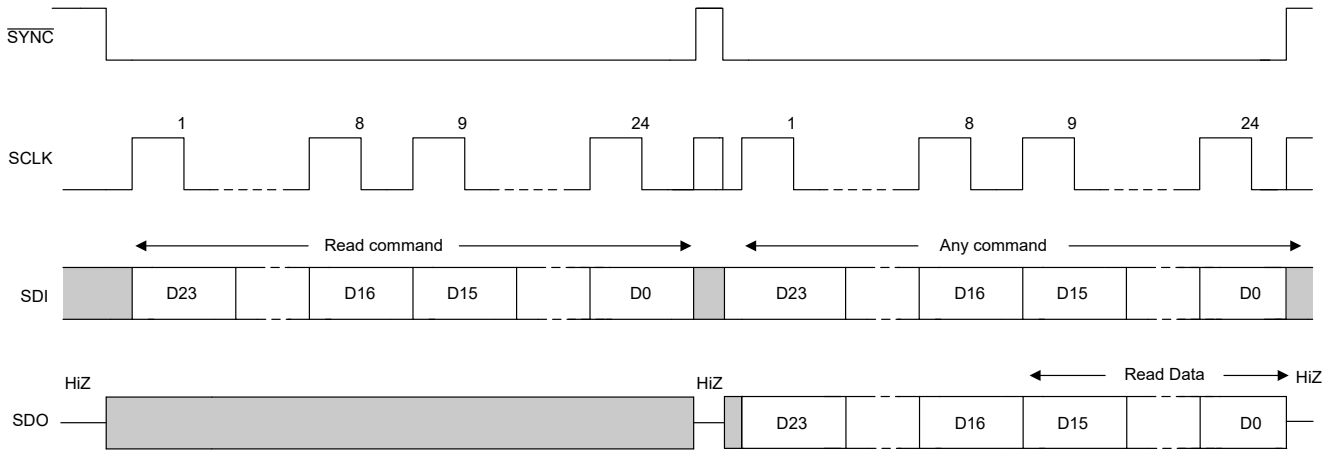


图 7-17. SPI 读取周期

菊花链操作也通过 SDO 引脚启用。在菊花链模式下，多个器件采用*菱式*连接，其中一个器件的 SDO 引脚连接到以下器件的 SDI 引脚，如图 7-18 所示。SPI 主机驱动链中第一个器件的 SDI 引脚。链中最后一个器件的 SDO 引脚连接到 SPI 主机的 POCI 引脚。在四线 SPI 模式下，如果访问周期包含 24 个时钟边沿的倍数，则链中的第一个器件仅使用最后 24 个位。如果访问周期包含的时钟边沿不是 24 的倍数，则器件会忽略 SPI 数据包。图 7-19 介绍了菊花链写入周期的数据包格式。

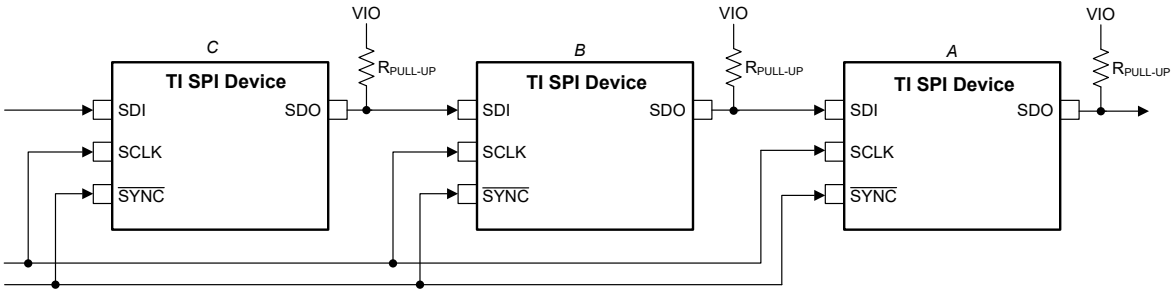


图 7-18. SPI 菊花链连接

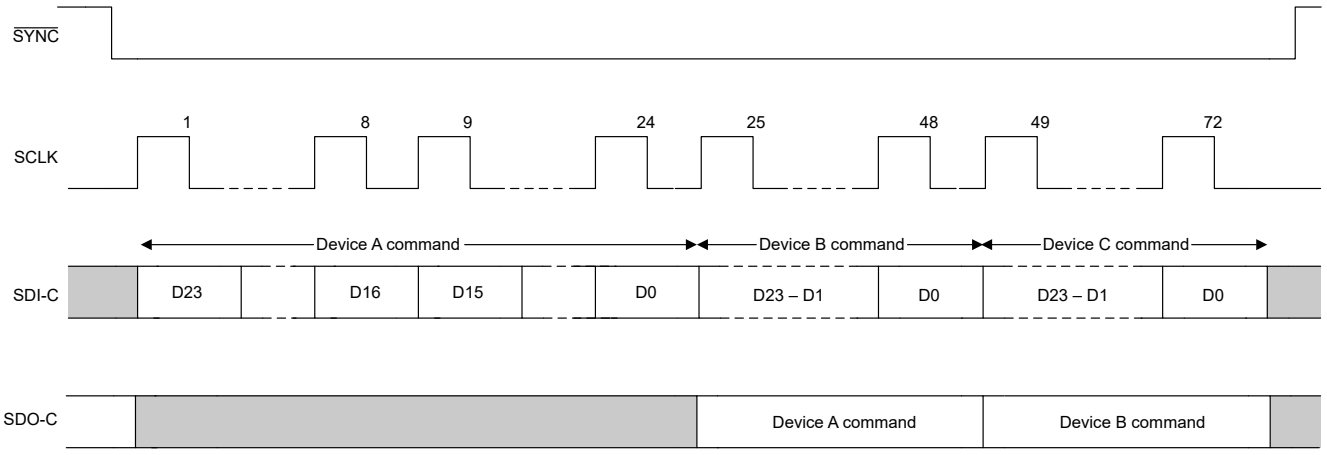


图 7-19. SPI 菊花链写入周期

7.5.2 I²C Programming Mode

The DACx3004W devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in the *Pin Configuration and Functions* section. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The DACx3004W family operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the DACx3004W family operates as a target receiver. A controller writes to the DACx3004W, a target receiver. However, if a controller requires the DACx3004W internal register data, the DACx3004W operate as a target transmitter. In this case, the controller reads from the DACx3004W. According to I²C terminology, read and write refer to the controller.

The DACx3004W family supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The DACx3004W family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in 图 7-20.

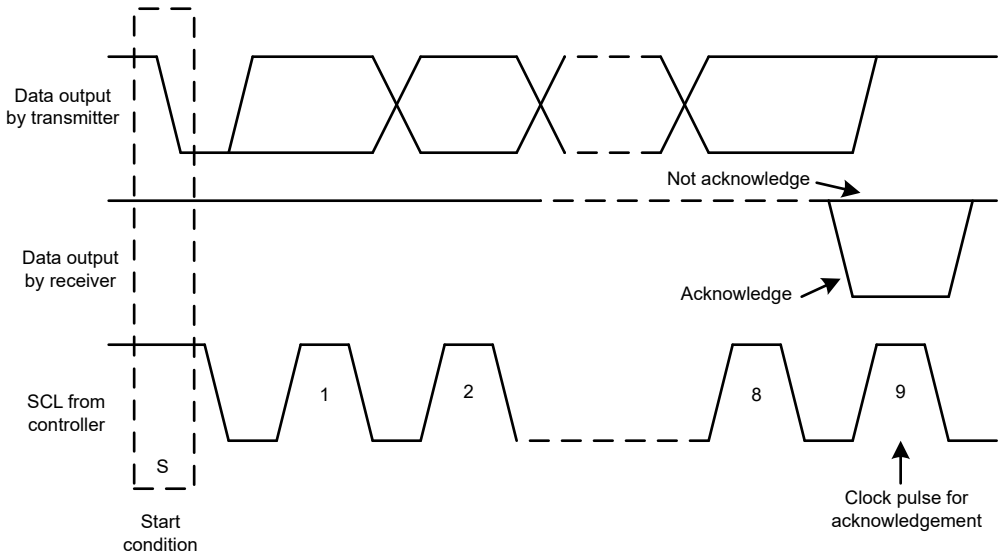


图 7-20. Acknowledge and Not Acknowledge on the I²C Bus

7.5.2.1 F/S 模式协议

以下步骤说明了 F/S 模式下的完整事务。

1. 控制器通过产生启动条件来启动数据传输。启动条件是当 SCL 为高电平时在 SDA 线上发生从高到低的转换，如图 7-21 所示。所有与 I²C 兼容的器件都会识别启动条件。
2. 控制器随后产生 SCL 脉冲，并在 SDA 线上发送 7 位地址和读取/写入方向位 (R/$\overline{W}$)。在所有传输期间，控制器确保数据有效。有效数据条件要求 SDA 线在时钟脉冲的整个高电平期间保持稳定，如图 7-22 所示。所有器件都识别控制器发送的地址，并将其与相应内部固定地址进行比较。只有具有匹配地址的目标器件才会通过在第 9 个 SCL 周期的整个高电平期间拉低 SDA 线来生成确认，如图 7-20 所示。当控制器检测到此确认时，则表示与目标的通信链路已建立。
3. 控制器产生更多的 SCL 周期，以便向目标器件发送（R/$\overline{W}$ 位为 0）数据或接收（R/$\overline{W}$ 位为 1）数据。在任一种情况下，接收器都必须确认发送器发送的数据。因此，确认信号可由控制器或目标器件生成，具体取决于哪一方是接收器。9 位有效数据序列包含 8 个数据位和 1 个确认位，并可根据需要继续。
4. 为了用信号指示数据传输结束，控制器通过在 SCL 线处于高电平期间将 SDA 线从高电平拉低来产生停止条件，如图 7-21 所示。此操作将释放总线并停止与寻址的目标器件之间的通信链路。所有与 I²C 兼容的器件都会识别停止条件。在收到停止条件后，将释放总线，然后所有目标器件等待启动条件，接着是匹配的地址。

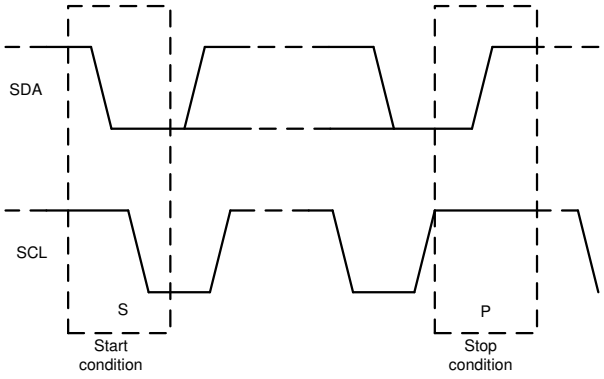


图 7-21. 启动和停止条件

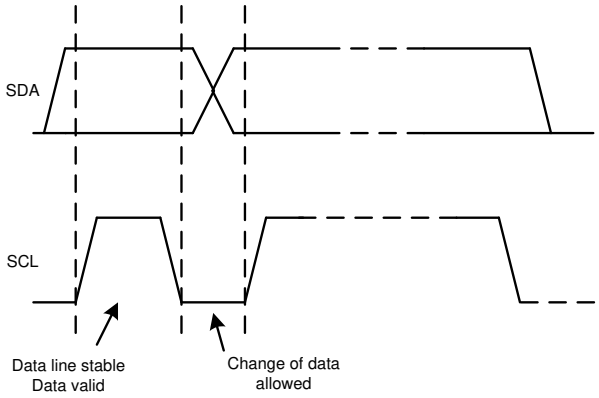


图 7-22. 在 I²C 总线上的位传输

7.5.2.2 I²C 更新序列

对于单次更新，DACx3004W 需要一个开始条件、一个有效的 I²C 地址字节、一个命令字节以及两个数据字节，如表 7-14 中所列。

表 7-14. 更新序列

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
地址 (A) 字节 节 7.5.2.2.1				命令字节 节 7.5.2.2.2				数据字节 - MSDB				数据字节 - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

收到每个字节后，DACx3004W 系列通过在单个时钟脉冲的高电平期间拉低 SDA 线来确认该字节，如图 7-23 所示。这四个字节和确认周期构成了单次更新所需的 36 个时钟周期。一个有效的 I²C 地址字节选择 DACx3004W。

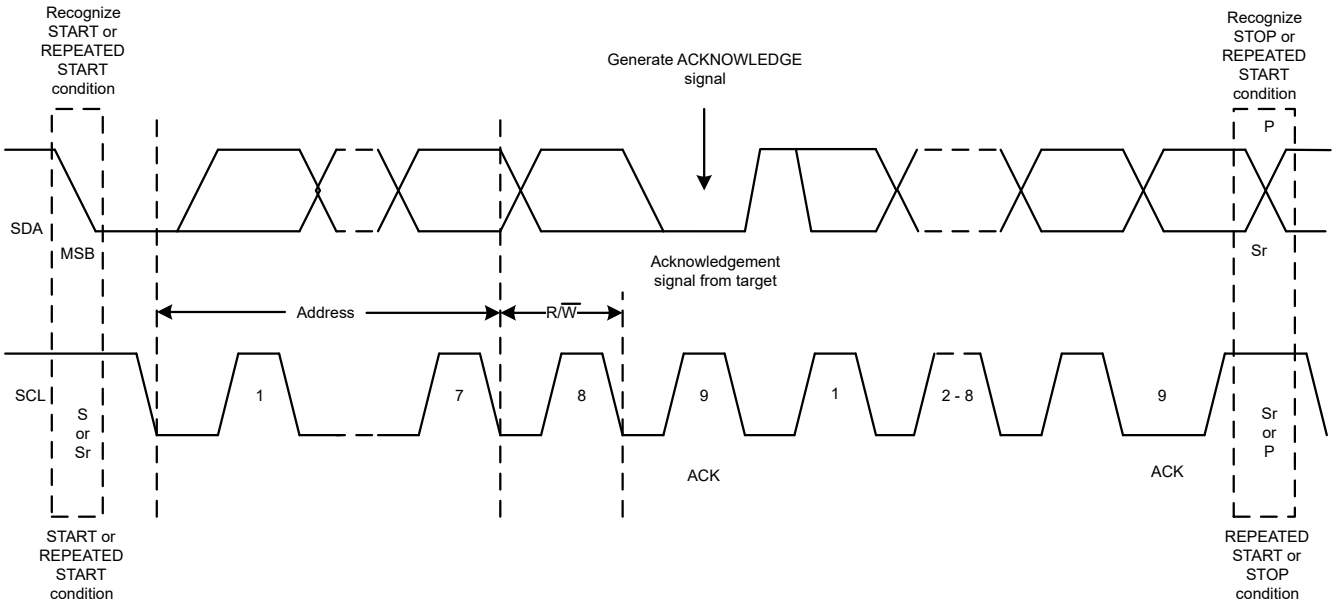


图 7-23. I²C 总线协议

命令字节设置所选 DACx3004W 器件的工作模式。如果要在通过该字节选择工作模式时进行数据更新，DACx3004W 器件必须接收两个数据字节：最高有效数据字节 (MSDB) 和最低有效数据字节 (LSDB)。DACx3004W 器件在 LSDB 之后的确认信号下降沿执行更新。

使用快速模式 (时钟 = 400kHz) 时，最大 DAC 更新速率限制为 10kSPS。使用超快速模式 (时钟 = 1MHz) 时，最大 DAC 更新速率限制为 25kSPS。收到停止条件后，DACx3004W 器件将释放 I²C 总线并等待新的启动条件。

7.5.2.2.1 地址字节

地址字节（如表 7-15 所示）是在启动条件之后从控制器器件接收的第一个字节。地址的前四位 (MSB) 出厂预设为 1001b。地址的接下来三位由 A0 引脚控制。A0 引脚输入可以连接到 VDD、AGND、SCL 或 SDA。在每个数据帧的第一个字节期间对 A0 引脚进行采样以确定地址。该器件会锁存地址引脚的值，因此会根据表 7-16 响应该特定地址。

表 7-15. 地址字节

注释	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
一般地址	1	0	0	1	请参阅表 7-16（目标地址列）			0 或 1
广播地址	1	0	0	0	1	1	1	0

表 7-16. 地址格式

目标地址	A0 引脚
000	AGND
001	VDD
010	SDA
011	SCL

DACx3004W 支持使用广播地址来同步更新或关闭多个 DACx3004W 器件。使用广播地址时，无论地址引脚状态如何，DACx3004W 都会进行响应。仅在写入模式下支持广播。

7.5.2.2.2 Command Byte

The *Register Names* table in the *Register Map* section lists the command byte in the ADDRESS column.

7.5.2.3 I^2C 读取序列

要读取任何寄存器，必须使用以下命令序列：

1. 发送启动或重复启动命令（使用目标器件地址并将 R/$\overline{W}$ 位设置为 0 以进行写入）。该器件将确认此事件。
2. 针对要读取的寄存器发送一个命令字节。该器件将再次确认此事件。
3. 发送重复启动命令（使用目标器件地址并将 R/$\overline{W}$ 位设置为 1 以进行读取）。该器件将确认此事件。
4. 该器件将写入寻址到的寄存器的 MSDB 字节。控制器必须确认此字节。
5. 最后，该器件将写出寄存器的 LSDB。

广播地址不能用于读取。

表 7-17. 读取序列

S	MSB	···	R/$\overline{W}$ (0)	ACK	MSB	···	LSB	ACK	Sr	MSB	···	R/$\overline{W}$ (1)	ACK	MSB	···	LSB	ACK	MSB	···	LSB	ACK
	地址字节 节 7.5.2.2.1				命令字节 节 7.5.2.2.2				Sr	地址字节 节 7.5.2.2.1				MSDB				LSDB			
来自控制器				目标	来自控制器			目标	来自控制器				目标	来自目标器件			控制器	来自目标器件			控制器

7.5.3 通用输入/输出 (GPIO) 模式

借助 I^2C 和 SPI，DACx3004W 还支持一个可在 NVM 中配置来提供多种功能的 GPIO。此引脚允许在不使用编程接口的情况下更新 DAC 输出通道和读取状态位，从而实现无处理器运行。在 GPIO-CONFIG 寄存器中，向 GPI-EN 位写入 1 以将 GPIO 引脚设置为输入，或向 GPO-EN 位写入 1 以将该引脚设置为输出。GPIO 引脚上映射了全局功能和特定于通道的功能。对于特定于通道的功能，需使用 GPIO-CONFIG 寄存器中的 GPI-CH-SEL 字段选择通道。表 7-18 列出了 GPIO 作为输入的可用功能选项，而 表 7-19 列出了 GPIO 作为输出的功能选项。一些 GP 输入操作在器件启动后由边沿触发。电源上升后，器件会寄存 GPI 电平并执行相关命令。此功能让用户可以配置加电时的初始输出状态。默认情况下，GPIO 引脚不映射到任何操作。当 GPIO 引脚映射到特定的输入功能时，相应的软件位功能会被禁用，以避免出现竞态条件。当用作 $\overline{RESET}$ 输入时，GPIO 引脚必须发送低电平有效脉冲来触发器件复位。这些功能的所有其他限制都应用于基于 GPIO 的触发器。

备注

未使用时，将 GPIO 引脚拉至高电平或低电平。当 GPIO 引脚用作 $\overline{RESET}$ 时，必须将配置编程到 NVM 中。否则，该设置会在器件复位后被清除。

表 7-18. 通用输入功能映射

寄存器	位字段	值	通道	GPIO 边沿/电平	功能
GPIO-CONFIG	GPI-CONFIG	0000	全部	下降沿	触发 $\overline{\text{DEEP-SLEEP}}$ 模式。
				上升沿	使器件退出深度睡眠模式。
		0010	全部	下降沿	触发 $\overline{\text{FAULT-DUMP}}$
				上升沿	没有影响
		0011	依据 GPI-CH-SEL 标准	下降沿	IOUT 断电
				上升沿	IOUT 加电
		0100	依据 GPI-CH-SEL 标准	下降沿	VOUT 断电。根据 VOUT-PDN-X 设置的下拉电阻器
				上升沿	VOUT 加电
		0101	全部	下降沿	触发 $\overline{\text{PROTECT}}$ 功能
				上升沿	没有影响
		0111	全部	下降沿	触发 $\overline{\text{CLR}}$ 功能
				上升沿	没有影响
		1000	依据 GPI-CH-SEL 标准。必须为每个通道配置 SYNC-CONFIG-X 和 GPI-CH-SEL。	下降沿	触发 $\overline{\text{LDAC}}$ 功能
				上升沿	没有影响
		1001	依据 GPI-CH-SEL 标准	下降沿	停止函数生成
				上升沿	开始函数生成
		1010	依据 GPI-CH-SEL 标准	下降沿	触发裕度低
				上升沿	触发裕度高
		1011	全部	低电平脉冲	触发器件 $\overline{\text{RESET}}$。$\overline{\text{RESET}}$ 配置必须编程到 NVM 中。
				上升沿	没有影响
		1100	全部	下降沿	允许 NVM 编程
				上升沿	阻止 NVM 编程
		1101	全部	下降沿	允许更新寄存器映射
				上升沿	阻止寄存器映射写入，但通过 I^2C 或 SPI 写入 DEV-UNLOCK 字段和通过 I^2C 写入 RESET 字段除外
		其他	不适用	不适用	不适用

表 7-19. 通用输出 ($\overline{\text{STATUS}}$) 功能映射

寄存器	位字段	值	功能
GPIO-CONFIG	GPO-CONFIG	0001	NVM-BUSY
		0100	DAC-0-BUSY
		0101	DAC-1-BUSY
		0110	DAC-2-BUSY
		0111	DAC-3-BUSY
		1000	WIN-CMP-0
		1001	WIN-CMP-1
		1010	WIN-CMP-2
		1011	WIN-CMP-3
		其他	不可用

7.6 Register Map

表 7-20. Register Map

REGISTER(1) (2)	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-X-MARGIN-HIGH	DAC-X-MARGIN-HIGH												X			
DAC-X-MARGIN-LOW	DAC-X-MARGIN-LOW												X			
DAC-X-VOUT-CMP-CONFIG	X			VOUT-GAIN-X			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
DAC-X-IOUT-MISC-CONFIG	X			IOUT-X-RANGE				X								
DAC-X-CMP-MODE-CONFIG	X				CMP-X-MODE		X									
DAC-X-FUNC-CONFIG	CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK-X												
DAC-X-DATA	DAC-X-DATA												X			
COMMON-CONFIG	WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-3		IOUT-PDN-3	VOUT-PDN-2		IOUT-PDN-2	VOUT-PDN-1		IOUT-PDN-1	VOUT-PDN-0		IOUT-PDN-0
COMMON-TRIGGER	DEV-UNLOCK				RESET				LDAC	CLR	X	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD
COMMON-DAC-TRIG	RST-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RST-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	RST-CMP-FLAG-2	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	RST-CMP-FLAG-3	TRIG-MAR-LO-3	TRIG-MAR-HI-3	START-FUNC-3
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-BUSY-3	DAC-BUSY-2	DAC-BUSY-1	DAC-BUSY-0	NVM-BUSY	DEVICE-ID							
CMP-STATUS	X							PROTECT-FLAG	WIN-CMP-3	WIN-CMP-2	WIN-CMP-1	WIN-CMP-0	CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
GPIO-CONFIG	GF-EN	DEEP-SLEEP-EN	GPO-EN	GPO-CONFIG				GPI-CH-SEL				GPI-CONFIG				GPI-EN
DEVICE-MODE-CONFIG	RESERVED		DIS-MODE-IN	RESERVED			PROTECT-CONFIG		RESERVED			X				
INTERFACE-CONFIG	X			TIMEOUT-EN	X			EN-PMBUS	X					FSDO-EN	X	SDO-EN
SRAM-CONFIG	X								SRAM-ADDR							
SRAM-DATA	SRAM-DATA															
DAC-X-DATA-8BIT	DAC-X-DATA-8BIT								X							
BRDCAST-DATA	BRDCAST-DATA												X			
PMBUS-PAGE	PMBUS-PAGE								NA							
PMBUS-OP-CMD	PMBUS-OPERATION-CMD-X								NA							
PMBUS-CML	X						CML	X	NA							
PMBUS-VERSION	PMBUS-VERSON								NA							

(1) The highlighted gray cells indicate the register bits or fields that are stored in the NVM.
(2) X = Don't care.

表 7-21. Register Names

I²C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
00h	FFh	D0h	NOP	节 7.6.1
01h	00h	25h	DAC-0-MARGIN-HIGH	节 7.6.2
02h	00h	26h	DAC-0-MARGIN-LOW	节 7.6.3
03h	FFh	D1h	DAC-0-VOUT-CMP-CONFIG	节 7.6.4
04h	FFh	D2h	DAC-0-IOUT-MISC-CONFIG	节 7.6.5
05h	FFh	D3h	DAC-0-CMP-MODE-CONFIG	节 7.6.6
06h	FFh	D4h	DAC-0-FUNC-CONFIG	节 7.6.7
07h	01h	25h	DAC-1-MARGIN-HIGH	节 7.6.2
08h	01h	26h	DAC-1-MARGIN-LOW	节 7.6.3
09h	FFh	D5h	DAC-1-VOUT-CMP-CONFIG	节 7.6.4
0Ah	FFh	D6h	DAC-1-IOUT-MISC-CONFIG	节 7.6.5
0Bh	FFh	D7h	DAC-1-CMP-MODE-CONFIG	节 7.6.6
0Ch	FFh	D8h	DAC-1-FUNC-CONFIG	节 7.6.7
0Dh	02h	25h	DAC-2-MARGIN-HIGH	节 7.6.2
0Eh	02h	26h	DAC-2-MARGIN-LOW	节 7.6.3
0Fh	FFh	D9h	DAC-2-VOUT-CMP-CONFIG	节 7.6.4
10h	FFh	DAh	DAC-2-IOUT-MISC-CONFIG	节 7.6.5
11h	FFh	DBh	DAC-2-CMP-MODE-CONFIG	节 7.6.6
12h	FFh	DCh	DAC-2-FUNC-CONFIG	节 7.6.7
13h	03h	25h	DAC-3-MARGIN-HIGH	节 7.6.2
14h	03h	26h	DAC-3-MARGIN-LOW	节 7.6.3
15h	FFh	DDh	DAC-3-VOUT-CMP-CONFIG	节 7.6.4
16h	FFh	DEh	DAC-3-IOUT-MISC-CONFIG	节 7.6.5
17h	FFh	DFh	DAC-3-CMP-MODE-CONFIG	节 7.6.6
18h	FFh	E0h	DAC-3-FUNC-CONFIG	节 7.6.7
19h	00h	21h	DAC-0-DATA	节 7.6.8
1Ah	01h	21h	DAC-1-DATA	节 7.6.8
1Bh	02h	21h	DAC-2-DATA	节 7.6.8
1Ch	03h	21h	DAC-3-DATA	节 7.6.8
1Fh	FFh	E3h	COMMON-CONFIG	节 7.6.9

表 7-21. Register Names (continued)

I²C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
20h	FFh	E4h	COMMON-TRIGGER	节 7.6.10
21h	FFh	E5h	COMMON-DAC-TRIG	节 7.6.11
22h	FFh	E6h	GENERAL-STATUS	节 7.6.12
23h	FFh	E7h	CMP-STATUS	节 7.6.13
24h	FFh	E8h	GPIO-CONFIG	节 7.6.14
25h	FFh	E9h	DEVICE-MODE-CONFIG	节 7.6.15
26h	FFh	EAh	INTERFACE-CONFIG	节 7.6.16
2Bh	FFh	EFh	SRAM-CONFIG	节 7.6.17
2Ch	FFh	F0h	SRAM-DATA	节 7.6.18
40h	NA	NA	DAC-0-DATA-8BIT	节 7.6.19
41h	NA	NA	DAC-1-DATA-8BIT	节 7.6.19
42h	NA	NA	DAC-2-DATA-8BIT	节 7.6.19
43h	NA	NA	DAC-3-DATA-8BIT	节 7.6.19
50h	FFh	F1h	BRDCAST-DATA	节 7.6.20
NA	All pages	00h	PMBUS-PAGE	节 7.6.21
NA	00h	01h	PMBIS-OP-CMD-0	节 7.6.22
NA	01h	01h	PMBUS-OP-CMD-1	节 7.6.22
NA	02h	01h	PMBUS-OP-CMD-2	节 7.6.22
NA	03h	01h	PMBUS-OP-CMD-3	节 7.6.22
NA	All pages	78h	PMBUS-CML	节 7.6.23
NA	All pages	98h	PMBUS-VERSION	节 7.6.24

表 7-22. Access Type Codes

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

表 7-22. Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

7.6.1 NOP Register (address = 00h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D0h

图 7-24. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R-0h															

表 7-23. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R	0000h	No operation

7.6.2 DAC-X-MARGIN-HIGH Register (address = 01h, 07h, 0Dh, 13h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 25h

图 7-25. DAC-X-MARGIN-HIGH Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-MARGIN-HIGH[11:0] DAC-X-MARGIN-HIGH[9:0]												X			
R/W-000h												X-0h			

表 7-24. DAC-X-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-X-MARGIN-HIGH[11:0] DAC-X-MARGIN-HIGH[9:0]	R/W	000h	Margin-high code for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004W VOUT: {DAC-X-MARGIN-HIGH[11:0]} DAC53004W VOUT: {DAC-X-MARGIN-HIGH[9:0], X, X} X = Don't care bits.
3-0	X	X	0	Don't care

7.6.3 DAC-X-MARGIN-LOW Register (address = 02h, 08h, 0Eh, 14h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 26h

图 7-26. DAC-X-MARGIN-LOW Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-MARGIN-LOW[11:0] DAC-X-MARGIN-LOW[9:0]												X			
R/W-000h												X-0h			

表 7-25. DAC-X-MARGIN-LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-X-MARGIN-LOW[11:0] DAC-X-MARGIN-LOW[9:0]	R/W	000h	Margin-low code for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004W VOUT: {DAC-X-MARGIN-LOW[11:0]} DAC53004W VOUT: {DAC-X-MARGIN-LOW[9:0], X, X} X = Don't care bits.
3-0	X	X	0	Don't care

7.6.4 DAC-X-VOUT-CMP-CONFIG Register (address = 03h, 09h, 0Fh, 15h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D1h, D5h, D9h, DDh

图 7-27. DAC-X-VOUT-CMP-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-X			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
X-0h			R/W-0h			X-0h					R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-26. DAC-X-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	VOUT-GAIN-X	R/W	0h	000: Gain = 1x, external reference on VREF pin 001: Gain = 1x, VDD as reference 010: Gain = 1.5x, internal reference 011: Gain = 2x, internal reference 100: Gain = 3x, internal reference 101: Gain = 4x, internal reference Others: Invalid
9-5	X	X	0h	Don't care
4	CMP-X-OD-EN	R/W	0	0: Set OUTx pin as push-pull 1: Set OUTx pin as open-drain in comparator mode (CMP-X-EN = 1 and CMP-X-OUT-EN = 1)
3	CMP-X-OUT-EN	R/W	0	0: Generate comparator output but consume internally 1: Bring comparator output to the respective OUTx pin
2	CMP-X-HIZ-IN-DIS	R/W	0	0: FBx input has high-impedance. Input voltage range is limited. 1: FBx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-X-INV-EN	R/W	0	0: Don't invert the comparator output 1: Invert the comparator output
0	CMP-X-EN	R/W	0	0: Disable comparator mode 1: Enable comparator mode. Current-output must be in power-down. Voltage-output mode must be enabled.

7.6.5 DAC-X-IOUT-MISC-CONFIG Register (address = 04h, 0Ah, 10h, 16h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D2h, D6h, DAh, DEh

图 7-28. DAC-X-IOUT-MISC-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			IOUT-RANGE-X				X								
X-0h			R/W-0h				X-0h								

表 7-27. DAC-X-IOUT-MISC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-9	IOUT-RANGE-X	R/W	0000	0000: 0 µA to 25 µA 0001: 0 µA to 50 µA 0010: 0 µA to 125 µA 0011: 0 µA to 250 µA 0100: 0 µA to –24 µA 0101: 0 µA to –48 µA 0110: 0 µA to –120 µA 0111: 0 µA to –240 µA 1000: –25 µA to +25 µA 1001: –50 µA to +50 µA 1010: –125 µA to +125 µA 1011: –250 µA to +250 µA Others: Invalid
8-0	X	X	000h	Don't care

7.6.6 DAC-X-CMP-MODE-CONFIG Register (address = 05h, 0Bh, 11h, 17h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D3h, D7h, DBh, DFh

图 7-29. DAC-X-CMP-MODE-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				CMP-X-MODE		X									
X-0h				R/W-0h		X-0h									

表 7-28. DAC-X-CMP-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	00h	Don't care
11-10	CMP-X-MODE	R/W	00	00: No hysteresis or window function 01: Hysteresis provided using DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers 10: Window comparator mode with DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers setting window bounds 11: Invalid
9-0	X	X	000h	Don't care

7.6.7 DAC-X-FUNC-CONFIG Register (address = 06h, 0Ch, 12h, 18h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D4h, D8h, DCh, E0h

图 7-30. DAC-X-FUNC-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK												
R/W-0h	R/W-0h	R/W-0h	R/W-000h												

表 7-29. DAC-X-FUNC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR-SEL-X	R/W	0	0: Clear DAC-X to zero-scale 1: Clear DAC-X to mid-scale
14	SYNC-CONFIG-X	R/W	0	0: DAC-X output updates immediately after a write command 1: DAC-X output updates with $\overline{\text{LDAC}}$ pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1
13	BRD-CONFIG-X	R/W	0	0: Don't update DAC-X with broadcast command 1: Update DAC-X with broadcast command

表 7-30. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-X	R/W	0	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-X	R/W	0	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-X	R/W	0	0: Enable linear slew
6-4	CODE-STEP-X	R/W	0	CODE-STEP for linear slew mode: 000: 1-LSB 001: 2-LSB 010: 3-LSB 011: 4-LSB 100: 6-LSB 101: 8-LSB 110: 16-LSB 111: 32-LSB
3-0	SLEW-RATE-X	R/W	0	SLEW-RATE for linear slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4 µs/step 0010: 8 µs/step 0011: 12 µs/step 0100: 18 µs/step 0101: 27.04 µs/step 0110: 40.48 µs/step 0111: 60.72 µs/step 1000: 91.12 µs/step 1001: 136.72 µs/step 1010: 239.2 µs/step 1011: 418.64 µs/step 1100: 732.56 µs/step 1101: 1282 µs/step 1110: 2563.96 µs/step 1111: 5127.92 µs/step

表 7-31. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-X	R/W	0	00: 0° 01: 120° 10: 240° 11: 90°
10 - 8	FUNC-CONFIG-X	R/W	0	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-X	R/W	0	1: Enable logarithmic slew. In logarithmic slew mode, the DAC output moves from the DAC-X-MARGIN-LOW code to the DAC-X-MARGIN-HIGH code, or vice versa, in 3.125% steps. When slewing in the positive direction, the next step is (1 + 0.03125) times the current step. When slewing in the negative direction, the next step is (1 – 0.03125) times the current step. When DAC-X-MARGIN-LOW is 0, the slew starts from code 1. The time interval for each step is defined by RISE-SLEW-X and FALL-SLEW-X.
6-4	RISE-SLEW-X	R/W	0	SLEW-RATE for logarithmic slew mode (DAC-X-MARGIN-LOW to DAC-X-MARGIN-HIGH): 000: 4 µs/step 001: 12 µs/step 010: 27.04 µs/step 011: 60.72 µs/step 100: 136.72 µs/step 101: 418.64 µs/step 110: 1282 µs/step 111: 5127.92 µs/step
3-1	FALL-SLEW-X	R/W	0	SLEW-RATE for logarithmic slew mode (DAC-X-MARGIN-HIGH to DAC-X-MARGIN-LOW): 000: 4 µs/step 001: 12 µs/step 010: 27.04 µs/step 011: 60.72 µs/step 100: 136.72 µs/step 101: 418.64 µs/step 110: 1282 µs/step 111: 5127.92 µs/step
0	X	X	0	Don't care

7.6.8 DAC-X-DATA Register (address = 19h, 1Ah, 1Bh, 1Ch) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 21h

图 7-31. DAC-X-DATA Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-DATA[11:0] DAC-X-DATA[9:0]												X			
R/W-000h												X-0h			

表 7-32. DAC-X-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC-X-DATA[11:0] DAC-X-DATA[9:0]	R/W	000h	Data for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004W VOUT: {DAC-X-DATA[11:0]} DAC53004W VOUT: {DAC-X-DATA[9:0], X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

7.6.9 COMMON-CONFIG Register (address = 1Fh) [reset = 0FFFh]

PMBus page address = FFh, PMBus register address = E3h

图 7-32. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-3		IOUT-PDN-3	VOUT-PDN-2		IOUT-PDN-2	VOUT-PDN-1		IOUT-PDN-1	VOUT-PDN-0		IOUT-PDN-0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-11b		R/W-1b	R/W-11b		R/W-1b	R/W-11b		R/W-1b	R/W-11b		R/W-1b

表 7-33. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	WIN-LATCH-EN	R/W	0	0: Non-latching window-comparator output 1: Latching window-comparator output
14	DEV-LOCK	R/W	0	0: Device not locked. 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	EE-READ-ADDR	R/W	0	0: Fault-dump read enable at address 0x00 1: Fault-dump read enable at address 0x01
12	EN-INT-REF	R/W	0	0: Disable internal reference. 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10, 8-7, 5-4, 2-1	VOUT-PDN-X	R/W	11	00: Power-up VOUT-X 01: Power-down VOUT-X with 10 KΩ to AGND 10: Power-down VOUT-X with 100 KΩ to AGND 11: Power-down VOUT-X with Hi-Z to AGND
9, 6, 3, 0	IOUT-PDN-X	R/W	1	0: Power-up IOUT-X 1: Power-down IOUT-X

7.6.10 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E4h

图 7-33. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				LDAC	CLR	X	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD
R/W-0h				R/W-0h				R/W-0h	R/W-0h	X-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-34. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. To unlock device, write this unlock password first, followed by a write 0 to the DEV-LOCK bit in the COMMON-CONFIG register. Others: Don't care
11 - 8	RESET	W	0000	1010: POR reset triggered. This bit self-resets. Others: Don't care
7	LDAC	R/W	0	0: LDAC operation not triggered 1: LDAC operation triggered if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1. This bit self-resets.
6	CLR	R/W	0	0: DAC registers and outputs unaffected 1: DAC registers and outputs set to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register. This bit self-resets.
5	X	X	0	Don't care
4	FAULT-DUMP	R/W	0	0: Fault-dump is not triggered 1: Triggers fault-dump sequence. This bit self-resets.
3	PROTECT	R/W	0	0: PROTECT function not triggered 1: Trigger PROTECT function. This bit is self-resetting.
2	READ-ONE-TRIG	R/W	0	0: Fault-dump read not triggered 1: Read one row of NVM for fault-dump. This bit self-resets.
1	NVM-PROG	R/W	0	0: NVM write not triggered 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered 1: Reload data from NVM to register map. This bit self-resets.

7.6.11 COMMON-DAC-TRIG Register (address = 21h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E5h

图 7-34. COMMON-DAC-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RESET-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	RESET-CMP-FLAG-2	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	RESET-CMP-FLAG-2	TRIG-MAR-LO-3	TRIG-MAR-HI-3	START-FUNC-3
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h

表 7-35. COMMON-DAC-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15, 11, 7, 3	RESET-CMP-FLAG-X	W	0	0: Latching-comparator output unaffected 1: Reset latching-comparator and window-comparator output. This bit self-resets.
14, 10, 6, 2	TRIG-MAR-LO-X	W	0	0: Don't care 1: Trigger margin-low command. This bit self-resets.
13, 9, 5, 1	TRIG-MAR-HI-X	W	0	0: Don't care 1: Trigger margin-high command. This bit self-resets.
12, 8, 4, 0	START-FUNC-X	R/W	0	0: Stop function generation 1: Start function generation as per FUNC-GEN-CONFIG-X in the DAC-X-FUNC-CONFIG register.

7.6.12 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

PMBus page address = FFh, PMBus register address = E6h

图 7-35. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-3-BUSY	DAC-2-BUSY	DAC-1-BUSY	DAC-0-BUSY	X	DEVICE-ID						VERSION-ID	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	X-0h	R						R-0h	

表 7-36. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	X	R	0	Don't care
12	DAC-3-BUSY	R	0	0: DAC-3 channel can accept commands 1: DAC-3 channel does not accept commands
11	DAC-2-BUSY	R	0	0: DAC-2 channel can accept commands 1: DAC-2 channel does not accept commands
10	DAC-1-BUSY	R	0	0: DAC-1 channel can accept commands 1: DAC-1 channel does not accept commands
9	DAC-0-BUSY	R	0	0: DAC-0 channel can accept commands 1: DAC-0 channel does not accept commands
8	X	R	0	Don't care
7-2	DEVICE-ID	R	DAC53004W: 05h DAC63004W: 04h	Device identifier
1-0	VERSION-ID	R	00	Version identifier

7.6.13 CMP-STATUS 寄存器（地址 = 23h）[复位 = 0000h]

PMBus 页面地址 = FFh，PMBus 寄存器地址 = E7h

图 7-36. CMP-STATUS 寄存器

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X							PROTECT-FLAG	WIN-CMP-3	WIN-CMP-2	WIN-CMP-1	WIN-CMP-0	CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
X-0h							R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 7-37. CMP-STATUS 寄存器字段说明

位	字段	类型	复位	说明
15-9	X	X	0	不用考虑
8	PROTECT-FLAG	R	0	0：PROTECT 操作不会触发。 1：PROTECT 功能已完成或正在进行中。读取时该位复位为 0。
7、6、5、4	WIN-CMP-X	R	0	来自相应通道的窗口比较器输出。输出根据 COMMON-CONFIG 寄存器中的 WINDOW-LATCH-EN 设置来锁存或取消锁存。
3、2、1、0	CMP-FLAG-X	R	0	来自相应通道的同步比较器输出。

7.6.14 GPIO-CONFIG Register (address = 24h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E8h

图 7-37. GPIO-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GF-EN	DEEP-SLEEP-EN	GPO-EN	GPO-CONFIG				GPI-CH-SEL				GPI-CONFIG				GPI-EN
R/$\overline{W}$-0h	R/$\overline{W}$-0h	R/$\overline{W}$-0h	R/$\overline{W}$-0h				R/$\overline{W}$-0h				R/$\overline{W}$-0h				R/$\overline{W}$-0h

表 7-38. GPIO-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GF-EN	R/$\overline{W}$	0	0: Glitch filter disabled for GP input. This setting provides faster response. 1: Glitch filter enabled for GP input. This setting introduces additional propagation delay but provides robustness.
14	DEEP-SLEEP-EN	R/$\overline{W}$	0	0: Deep-sleep mode disabled 1: Deep-sleep mode enabled for GP input
13	GPO-EN	R/$\overline{W}$	0	0: Disable output mode for GPIO pin 1: Enable output mode for GPIO pin
12-9	GPO-CONFIG	R/$\overline{W}$	0000	$\overline{STATUS}$ function setting. The GPIO pin is mapped to the following register bits as output: 0001: NVM-BUSY 0100: DAC-0-BUSY 0101: DAC-1-BUSY 0110: DAC-2-BUSY 0111: DAC-3-BUSY 1000: WIN-CMP-0 1001: WIN-CMP-1 1010: WIN-CMP-2 1011:WIN-CMP-3 Others: Invalid

表 7-38. GPIO-CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-5	GPI-CH-SEL	R/W	0000	Each bit corresponds to a DAC channel. 0b is *disabled* and 1b is *enabled*. GPI-CH-SEL[0]: Channel 0 GPI-CH-SEL[1]: Channel 1 GPI-CH-SEL[2]: Channel 2 GPI-CH-SEL[3]: Channel 3 Example: when GPI-CH-SEL is 0101, both channel-0 and channel-2 are enabled and both channel-1 and channel-3 are disabled.
4-1	GPI-CONFIG	R/W	0000	GPIO pin input configuration. Global settings act on the entire device. Channel-specific settings depend on the channel selection by the GPI-CH-SEL bits: 0000: $\overline{\text{DEEP-SLEEP}}$ (global). GPIO falling-edge triggers deep-sleep mode, GPIO rising-edge takes the device out of deep-sleep mode. 0010: $\overline{\text{FAULT-DUMP}}$ (global). GPIO falling-edge triggers fault-dump, GPIO = 1 has no effect. 0011: IOUT power-up, down (channel-specific). GPIO falling-edge triggers power-down, GPIO rising-edge triggers power-up. 0100: VOUT power-up/down (channel-specific). The output load is as per the VOUT-PDN-X setting. GPIO falling-edge triggers power-down, GPIO rising-edge triggers power-up. 0101: $\overline{\text{PROTECT}}$ input (global). GPIO falling-edge asserts $\overline{\text{PROTECT}}$ function, GPIO = 1 has no effect. 0111: $\overline{\text{CLR}}$ input (global). GPIO = 0 asserts $\overline{\text{CLR}}$ function, GPIO = 1 has no effect. 1000: $\overline{\text{LDAC}}$ input (channel-specific). GPIO falling-edge asserts $\overline{\text{LDAC}}$ function, GPIO = 1 has no effect. Both the SYNC-CONFIG-X and the GPI-CH-SEL must be configured for every channel. 1001: Start, stop function generation (channel-specific). GPIO falling-edge stops function generation. GPIO rising-edge starts function generation. 1010: Trigger margin-high, low (channel-specific). GPIO falling-edge triggers margin-low. GPIO rising-edge triggers margin-high. 1011: $\overline{\text{RESET}}$ input (global). The falling-edge of the GPIO pin asserts the $\overline{\text{RESET}}$ function. The $\overline{\text{RESET}}$ input must be a pulse. The GPIO rising-edge brings the device out of reset. The $\overline{\text{RESET}}$ configuration must be programmed into the NVM. Otherwise, the setting is cleared after the device reset. 1100: NVM write-protection (global). GPIO falling-edge allows NVM programming. GPIO rising-edge blocks NVM programming. 1101: Register-map lock (global). GPIO falling-edge allows update to the register map. GPIO rising-edge blocks any register map update except a write to the DEV-UNLOCK field through I^2C or SPI and to the RESET field through I^2C. Others: Not applicable
0	GPI-EN	R/W	0	0: Disable input mode for GPIO pin 1: Enable input mode for GPIO pin

7.6.15 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E9h

图 7-38. DEVICE-MODE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DIS-MODE-IN	RESERVED			PROTECT-CONFIG		RESERVED			X				
R/W-0h		R/W-0h	R/W-0h			R/W-0h		R/W-0h			X-0h				

表 7-39. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	00	Always write 0b00
13	DIS-MODE-IN	R/W	0	Write 1 to this bit for low-power consumption.
12-10	RESERVED	R/W	0	Always write 0b000
9-8	PROTECT-CONFIG	R/W	00	00: Switch to Hi-Z power-down (no slew) 01: Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down 10: Slew to margin-low code and then switch to Hi-Z power-down 11: Slew to margin-high code and then switch to Hi-Z power-down
7-5	RESERVED	R/W	0	Always write 0b000
4-0	X	R/W	00h	Don't care

7.6.16 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

图 7-39. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			TIMEOUT-EN	X			EN-PMBUS	X					FSDO-EN	X	SDO-EN
X-0h			R/W-0h	X-0h			R/W-0h	X-0h					R/W-0h	X-0h	R/W-0h

表 7-40. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12	TIMEOUT-EN	R/W	0	0: I^2C timeout disabled 1: I^2C timeout enabled
11-9	X	X	0h	Don't care
8	EN-PMBUS	R/W	0	0: PMBus disabled 1: Enable PMBus
7-3	X	X	00h	Don't care
2	FSDO-EN	R/W	0	0: Fast SDO (FSDO) disabled 1: Fast SDO enabled
1	X	X	0	Don't care
0	SDO-EN	R/W	0	0: SDO disabled 1: SDO enabled on GPIO pin

7.6.17 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

PMBus page address = FFh, PMBus register address = EFh

图 7-40. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/W-00h							

表 7-41. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

7.6.18 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F0h

图 7-41. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0000h															

表 7-42. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. Data are written to or read from the address configured in the SRAM-CONFIG register.

7.6.19 DAC-X-DATA-8BIT Register (address = 40h, 41h, 42h, 43h) [reset = 0000h]

PMBus page address = Not applicable, PMBus register address = Not applicable

图 7-42. DAC-X-DATA-8BIT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-DATA-8BIT[7:0]								X							
R/W-00h								X-00h							

表 7-43. DAC-X-DATA-8BIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	DAC-X-DATA-8BIT[7:0]	R/W	00h	8-bit data for current output. This register provides faster update rate in the I^2C mode. Data are in straight-binary format.
7-0	X	X	00h	Not applicable

7.6.20 BRDCAST-DATA Register (address = 50h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F1h

图 7-43. BRDCAST-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[11:0] BRDCAST-DATA[9:0]												X			
R/W-000h												X-0h			

表 7-44. BRDCAST-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	BRDCAST-DATA[11:0] BRDCAST-DATA[9:0]	R/W	000h	Broadcast code for all DAC channels Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004W VOUT: {BRDCAST-DATA[11:0]} DAC53004W VOUT: {BRDCAST-DATA[9:0], X, X} X = Don't care bits. The BRD-CONFIG-X bit in the DAC-X-FUNC-CONFIG register must be enabled for the respective channels.
3-0	X	X	0h	Don't care.

7.6.21 PMBUS-PAGE Register [reset = 0300h]

PMBus page address = X, PMBus register address = 00h

图 7-44. PMBUS-PAGE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-PAGE								X							
R/W-03h								X-00h							

表 7-45. PMBUS-PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-PAGE	R/W	03h	8-bit PMBus page address as specified in the *Register Names* table in the *Register Map* section.
7-0	X	X	00h	Not applicable

7.6.22 PMBUS-OP-CMD-X Register [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 01h

图 7-45. PMBUS-OP-CMD-X Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-OPERATION-CMD-X								X							
R/W-00h								X-00h							

表 7-46. PMBUS-OP-CMD-X Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-OPERATION-CMD-X	R/W	00h	PMBus operation commands: 00h: Turn off 80h: Turn on A4h: Margin high, DAC output margins high to DAC-X-MARGIN-HIGH code 94h: Margin low, DAC output margins low to DAC-X-MARGIN-LOW code
7-0	X	X	00h	Not applicable

7.6.23 PMBUS-CML Register [reset = 0000h]

PMBus page address = X, PMBus register address = 78h

图 7-46. PMBUS-CML Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X						CML	X	N/A							
X-00h						R/W-0h	X-0h	X-00h							

表 7-47. PMBUS-CML Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	X	X	00h	Don't care
9	CML	R/W	0	0: No communication fault 1: PMBus communication fault for write with incorrect number of clocks, read before write command, invalid command address, and invalid or unsupported data value; reset this bit by writing 1.
8	X	X	0h	Don't care
7-0	X	X	00h	Not applicable

7.6.24 PMBUS-VERSION 寄存器 [复位 = 2200h]

PMBus 页面地址 = X，PMBus 寄存器地址 = 98h

图 7-47. PMBUS-VERSION 寄存器

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-VERSION								X							
R-22h								X-00h							

表 7-48. PMBUS-VERSION 寄存器字段说明

位	字段	类型	复位	说明
15-8	PMBUS-VERSION	R	22h	PMBus 版本
7-0	X	X	00h	不可用

8 应用和实现

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The DACx3004W are quad-channel buffered, force-sense output, voltage-output and current-output smart DACs that include an NVM and internal reference, and are available in a tiny 1.75-mm × 1.75-mm DSBGA package. The external reference must not exceed V_{DD}, either during transient or steady-state conditions. For the best Hi-Z output performance, use a pullup resistor on the VREF pin to VDD. In case the VDD pin remains floating during the off condition, place a 100-kΩ resistor to AGND for proper detection of the VDD pin *off* condition. All the digital outputs are open drain; use external pullup resistors on these pins. The interface protocol is detected at power-on, and the device locks to the protocol as long as V_{DD} is on. In I^2C mode, when allocating the I^2C addresses in the system, also consider the broadcast address. I^2C timeout can be enabled for robustness. SPI mode is three-wire by default. Configure the GPIO pin as SDO in the NVM for SPI readback capability. The SPI clock speed in readback mode is slower than in write mode. Power-down mode sets the DAC outputs in Hi-Z by default. Change the configuration appropriately for different power-down settings. The DAC channels can also power-up with a programmed DAC code in the NVM.

8.2 Typical Application

The DACx3004W can be used as a programmable current source using an external MOSFET for current values greater than 250 µA. The force-sense outputs of DACx3004W can be used to compensate for the gate-source voltage drop caused by temperature, drain current, and aging of the MOSFET. The GPIO pin can be used to switch the output current on or off without the need for run-time software. The slew between the on and off values can be programmed. 图 8-1 shows how the DACx3004W is used as a programmable current source. A resistor, R_{SET}, connected to the source of the MOSFET sets the output current range. This circuit can be used in optical modules that require a high current output with a small size.

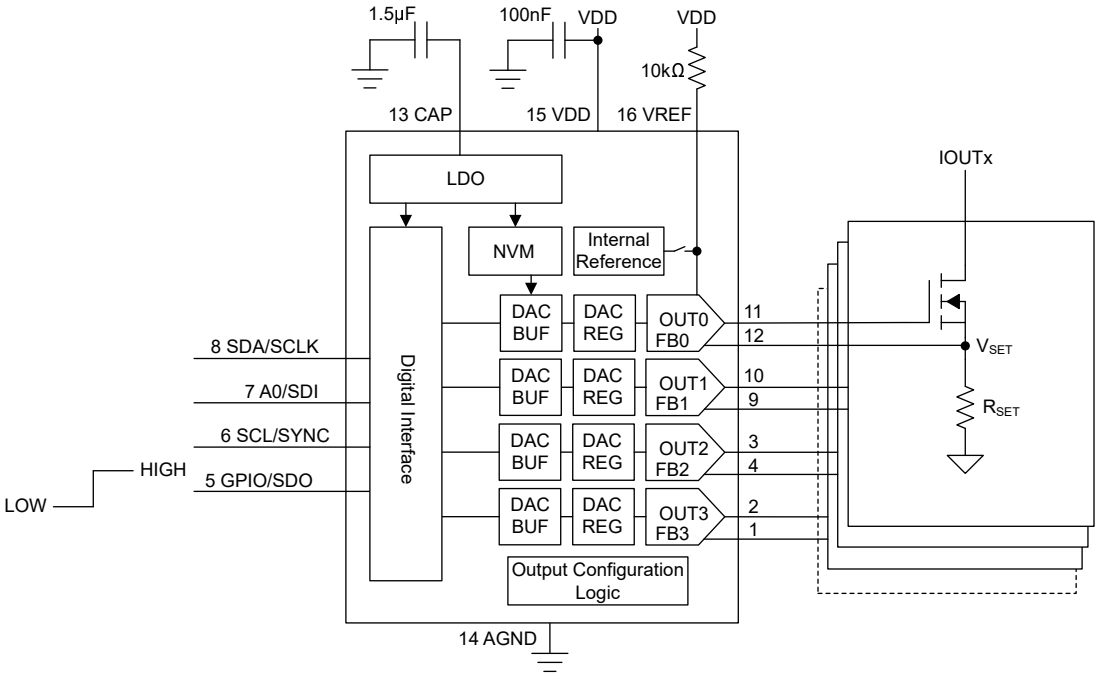


图 8-1. Current Source

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Current output range	0 mA to 200 mA
DAC range	0 V to 0.6 V
R_{SET}	3 Ω

8.2.2 Detailed Design Procedure

V_{SET} is controlled by the DACx3004W to adjust the current output. R_{SET} sets the output range of the current source. Choose a small V_{SET} so that the power dissipation across R_{SET} is minimum. 方程式 10 calculates R_{SET}.

$$R_{SET} = \frac{V_{SET}}{I_{OUT}} \tag{10}$$

A 0.6-V max V_{SET} is used in this example. 方程式 11 shows that R_{SET} is calculated to be 3 Ω. Choose an R_{SET} with a power rating of at least 120 mW.

$$R_{SET} = \frac{0.6\,V}{200\,mA} = 3\,\Omega \tag{11}$$

方程式 12 shows how to calculate the DAC code for a given output voltage, reference, and gain setting.

$$DAC\_DATA = \frac{V_{OUT} \times 2^N}{V_{REF} \times GAIN} \tag{12}$$

方程式 13 calculates the DAC code for an output voltage, V_{SET}, of 0.6V, the internal 1.21-V reference, and the 1.5 × gain setting.

$$DAC\_DATA = \frac{0.6\,V \times 2^{12}}{1.21\,V \times 1.5} = 1354d \tag{13}$$

The GPIO pin can be configured as an input to trigger the DACx3x04W output to turn on and off, which turns the current source on and off. Configure the GPIO in the GPIO-CONFIG register. The GPI-EN bit enables the GPIO pin as an input. The GPI-CH-SEL field selects which channels are controlled by the GPI. The GPI-CONFIG field selects the GPI function. 表 7-18 defines the functions for the GPI-CONFIG field. Choose the trigger margin-high or margin-low function if programmable slew is needed, or VOUT power up or down if programmable slew is not needed.

The programmable slew is configured by the CODE-STEP and SLEW-RATE fields in the DAC-X-FUNC-CONFIG Register. The programmable slew is only available when toggling between two values stored in the DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW Registers. 节 7.4.5.1.2 discusses how to set the programmable slew. This application example uses a SLEW-RATE of 8 µV/s and a CODE-STEP of 8-LSB to achieve a 1.36-ms slew time.

The pseudo code for this application example is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Set gain setting to 1.5x internal reference (1.8 V) (repeat for all channels)
WRITE DAC-0-VOUT-CMP-CONFIG(0x3), 0x08, 0x00
//Power-up voltage output on all channels and enable the internal reference
WRITE COMMON-CONFIG(0x1F),0x12, 0x49
//Configure GPI for Margin-High, Low trigger for all channels
WRITE GPIO-CONFIG(0x24), 0x01, 0xF5
//Set slew rate and code step (repeat for all channels)
//CODE_STEP: 8 LSB, SLEW_RATE: 8 µs/step
WRITE DAC-0-FUNC-CONFIG(0x06), 0x00, 0x52
//Write DAC margin high code (repeat for all channels)
//For a 1.8-V output range, the 12-bit hex code for 0.6 V is 0x54A. With 16-bit left alignment,
this becomes 0x54A0
WRITE DAC-0-MARGIN-HIGH(0x01), 0x54, 0xA0
//Write DAC margin low code (repeat for all channels)
//The 12-bit hex code for 0 V is 0x000. With 16-bit left alignment, this
becomes 0x0000
WRITE DAC-0-MARGIN-LOW(0x02), 0x00, 0x00
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

8.2.3 Application Curve

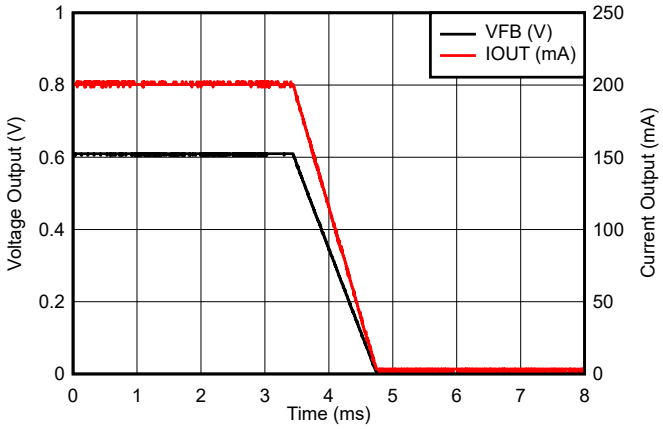


图 8-2. IOUT and VFB On-to-Off Transition

8.3 Power Supply Recommendations

The DACx3004W family of devices does not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 µF for the CAP pin.

8.4 布局

8.4.1 布局指南

DACx3004W 引脚配置将模拟、数字和电源引脚分开以实现优化布局。为了保证信号完整性，需将数字和模拟走线分开，并将去耦电容器放置在器件引脚附近。

8.4.2 Layout Example

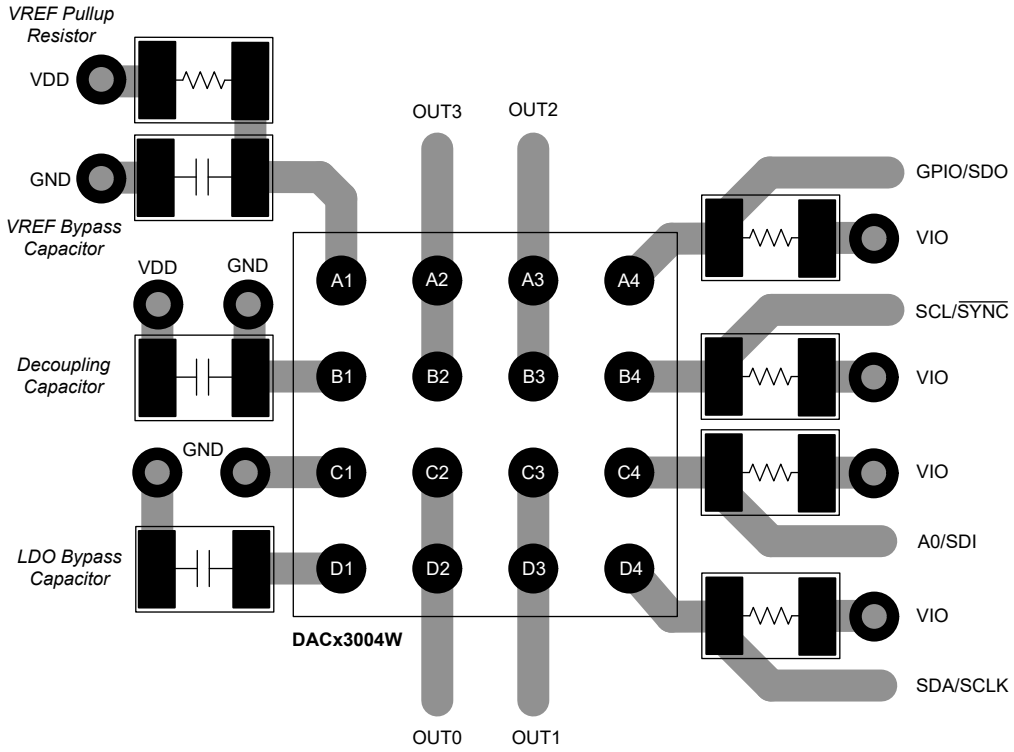


图 8-3. Layout Example

Note: The ground and power planes have been omitted for clarity.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

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9.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC53004YBHR	ACTIVE	DSBGA	YBH	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DAC 53004	Samples
DAC63004YBHR	ACTIVE	DSBGA	YBH	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DAC 63004	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

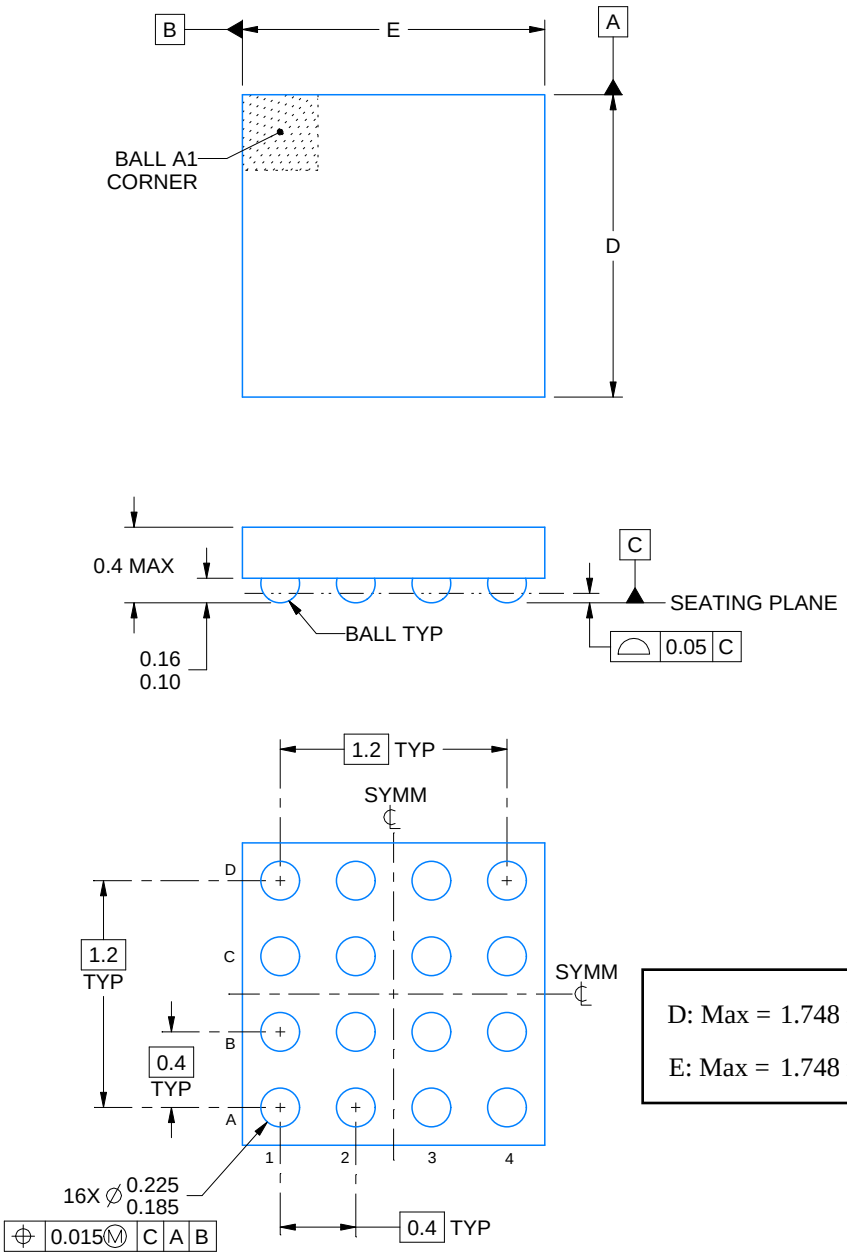
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



D: Max = 1.748 mm, Min =1.687 mm

E: Max = 1.748 mm, Min =1.687 mm

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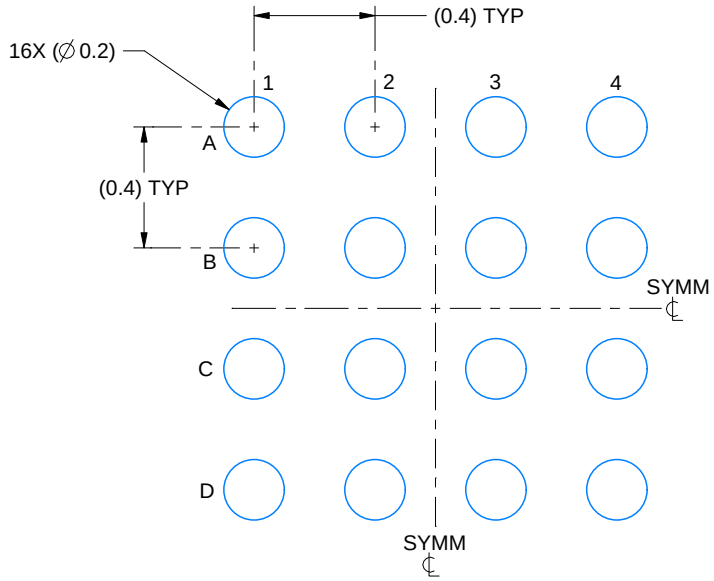
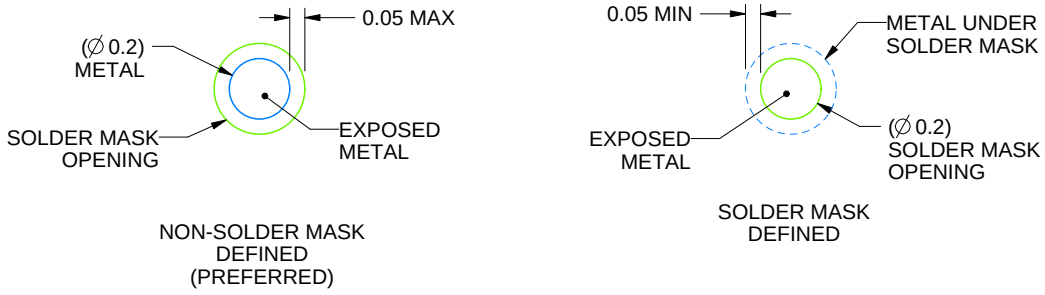
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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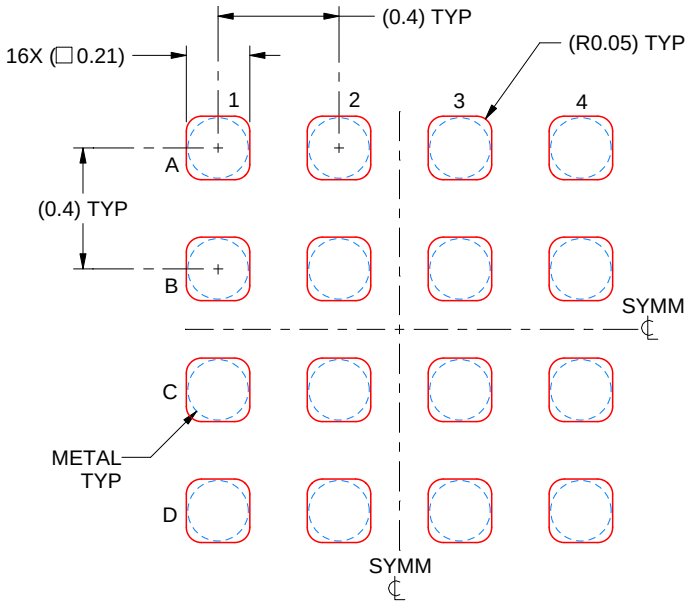
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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