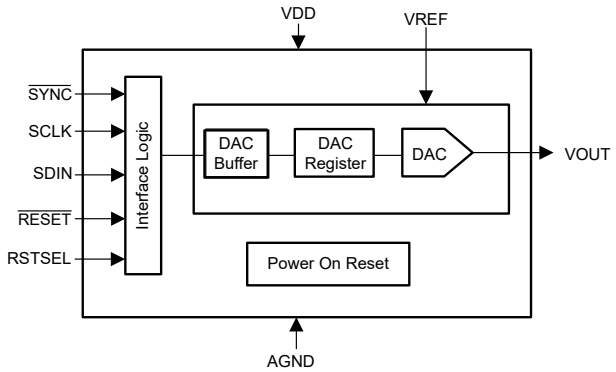
DAC82001 16 位、低毛刺脉冲、单通道电压输出、非缓冲 DAC

1 特性

- 16 位性能：1-LSB DNL 和 2-LSB INL
- 低毛刺脉冲能量：0.5nV-s
- 快速稳定：1μs
- 宽电源：2.7V 至 5.5V
- 宽基准范围：2.0 V 至 V_{DD}
- 低功耗：250μA（5.0 V 时）
- 3 线制串行外设接口 (SPI)，频率高达 50MHz
- 复位至零标度或中标度
- 1.62V V_{IH} (V_{DD} = 5.5V)
- 温度范围：–40°C 至 +85°C
- 封装：微型 10 引脚 WSON

2 应用

- 示波器 (DSO)
- 电池测试
- 半导体测试
- 超声波扫描仪
- 直流电源、交流电源、电子负载



功能方框图

3 说明

16 位 DAC82001 是一款具有非缓冲电压输出的高精度、低功耗、单通道数模转换器 (DAC)。

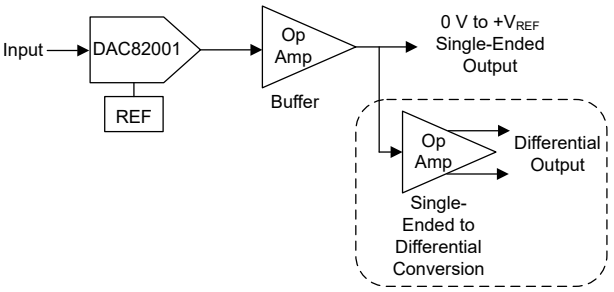
DAC82001 由 3.3V 和 5V 电源供电，并提供 1-LSB DNL 和 2-LSB INL 的线性度。高精度与微型封装相结合，使得该器件成为增益和偏移校准、电压设定点生成和电源控制等应用的理想选择。DAC82001 包含一个上电复位 (POR) 电路。POR 电路可确保 DAC 输出根据 RSTSEL 引脚的状态在零刻度或中间刻度上电，并保持在该刻度，直到将有效代码写入器件。所有内部寄存器都会在 $\overline{\text{RESET}}$ 引脚被拉低后异步复位。

DAC82001 使用一个以高达 50MHz 的时钟速率运行的多功能 3 线制串行外设接口 (SPI)。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
DAC82001	DRX（WSON，10）	2.50mm × 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



用于生成时间增益补偿 (TGC) 控制的 DAC82001

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2022) to Revision A (November 2022)	Page
• 将器件状态从“预告信息（预发布）”更改为“量产数据（正在供货）”	1

5 Pin Configuration and Functions

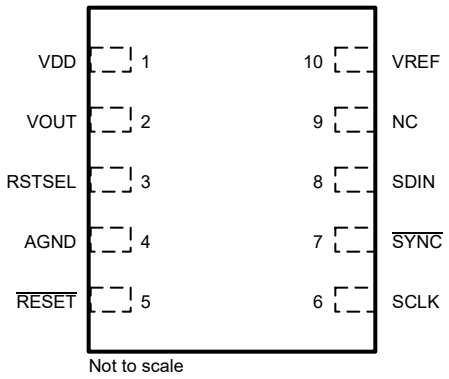


图 5-1. DRX (10-Pin WSON) Package, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	4	Ground	Ground reference point for all circuitry on the device.
NC	9	—	Do not connect
$\overline{\text{RESET}}$	5	Input	Asynchronous reset. Active low. If $\overline{\text{RESET}}$ is low, all DAC channels reset either to zero-scale (RSTSEL = AGND) or to midscale (RSTSEL = V_{DD}).
RSTSEL	3	Input	Reset select pin. DAC powers up to zero scale if RSTSEL = AGND. DAC powers up to midscale if RSTSEL = V_{DD}.
SCLK	6	Input	Serial interface clock of SPI.
SDIN	8	Input	Serial interface data input of SPI. Data are clocked into the input shift register on each falling edge of the SCLK pin.
$\overline{\text{SYNC}}$	7	Input	Serial data enable of SPI. Active low. This input is the frame-synchronization signal for the serial data. When the signal goes low, the serial interface input shift register is enabled.
VDD	1	Power	Analog supply voltage (2.7 V to 5.5 V)
VOUT	2	Output	Analog output voltage from DAC
VREF	10	Input	This pin is the external reference input to the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Input voltage	VDD to AGND	– 0.3	6	V
		VREF to AGND	– 0.3	V_{DD} + 0.3	
		Digital inputs to AGND	– 0.3	V_{DD} + 0.3	
	Output voltage, VOUT to AGND		– 0.3	V_{DD} + 0.3	V
	Input current into any digital pin		– 10	10	mA
T_J	Junction temperature		– 40	150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
V_S	Positive supply voltage to ground, VDD to AGND	2.7		5.5	V
DIGITAL INPUTS					
V_{IH}	Input high voltage	1.62			V
V_{IL}	Input low voltage			0.45	V
REFERENCE INPUT					
V_{REF}	Reference voltage to ground, VREF to AGND	2.0		V_{DD}	V
TEMPERATURE					
T_A	Operating temperature	– 40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		DAC82001 DRX (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W

THERMAL METRIC(1)		DAC82001 DRX (WSON) 10 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	35.7	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

all minimum and maximum values at T_A = –40°C to +85°C and all typical values at T_A = 25°C, 2.7 V ⩽ V_{DD} ⩽ 5.5 V, 2.0 V ⩽ V_{REF} ⩽ 5.5 V , AGND = 0 V, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		16			Bits
INL	Integral nonlinearity		–2	±0.6	2	LSB
DNL	Differential nonlinearity		–1	±0.5	1	LSB
TUE	Total unadjusted error		–0.06	0.04	0.06	%FSR
	Zero code error		–2.6	0.5	2.6	LSB
	Zero code error temperature coefficient			±0.02		ppm/°C
	Gain error		–20	4	20	LSB
	Gain error temperature coefficient			±0.1		ppm/°C
OUTPUT CHARACTERISTICS						
V_O	Output voltage		0		V_{REF}	V
Z_O	Output impedance			6.25		kΩ
PSRR DC	Power supply rejection ratio (dc)	DAC at midscale; V_{DD} = 5 V ±10%, V_{REF} = 2.5 V		5		µV/V
DYNAMIC PERFORMANCE						
t_s	Output voltage settling time	To 1/2 LSB of FS, C_L = 10 pF		1		µs
	Output noise	DAC at midcode, 0.1 Hz to 10 Hz		0.1		μV_{PP}
	Output noise density	DAC at midcode, measured at 10 kHz		10		nV/$\sqrt{Hz}$
SFDR	Spurious free dynamic range	1-kHz sinusoid at DAC output (unbuffered, full scale), DAC updated at 200 kSPS with 40-kHz low-pass filter, include up to 7th harmonics		–96		dB
THD	Total harmonic distortion	1-kHz sinusoid at DAC output (unbuffered, full scale), DAC updated at 200 kSPS with 40-kHz low-pass filter, include up to 7th harmonics		–91		dB
PSRR AC	Power supply rejection ratio (ac)	DAC at midscale, V_{REF} = 2.5 V, V_{DD} = 5 V ±200 mV at 10 kHz		–72		dB
	Code change glitch impulse	±1 LSB around major carry		0.5		nV-s
	Digital feedthrough			0.5		nV-s
	Power on glitch magnitude	C_{LOAD} = 10 pF		0.8		V
VOLTAGE REFERENCE INPUT						
	Reference input voltage		2.0		V_{DD}	V
Z_{REF}	Reference input impedance		5			kΩ
C_{REF}	Reference input capacitance			75		pF
DIGITAL INPUTS						
	Hysteresis voltage			0.4		V
	Input current		–5		5	µA

6.5 Electrical Characteristics (continued)

all minimum and maximum values at T_A = –40°C to +85°C and all typical values at T_A = 25°C, 2.7 V ⩽ V_{DD} ⩽ 5.5 V, 2.0 V ⩽ V_{REF} ⩽ 5.5 V , AGND = 0 V, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Power-supply current	V_{DD} = 3 V		250	350	µA
		V_{DD} = 5 V		250	350	
	Power	V_{DD} = 3 V		750	1050	µW
		V_{DD} = 5 V		1250	1750	

6.6 Timing Requirements

all input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of (V_{IL} + V_{IH}) / 2. 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{IH} = 1.62 V, V_{IL} = 0.15 V, 2.0 V ≤ V_{REF} ≤ 5.5 V, and T_A = –40°C to +85°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	10			ns
t_{SYNCS}	$\overline{SYNC}$ falling edge to SCLK falling edge setup	13			ns
t_{SYNCH}	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
$t_{SYNCHIGH}$	$\overline{SYNC}$ high time	160			ns
$t_{SYNCIGNORE}$	SCLK falling edge to $\overline{SYNC}$ ignore	15			ns
$t_{DACWAIT}$	Sequential DAC update wait time	1			µs

6.7 Timing Diagram

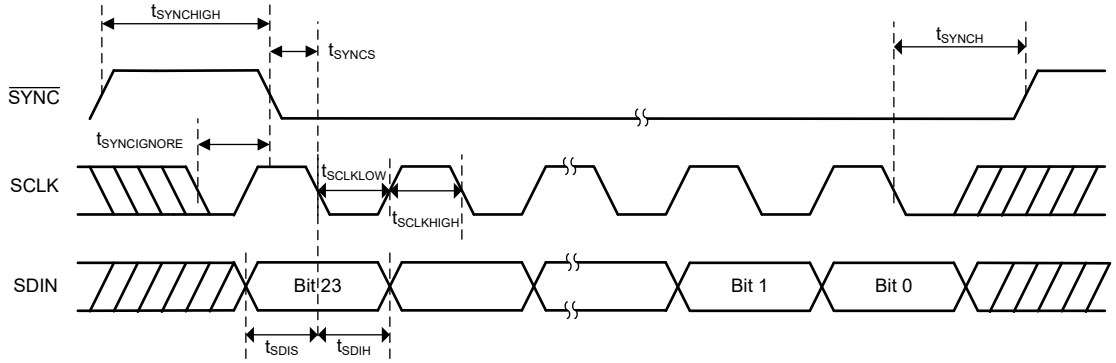
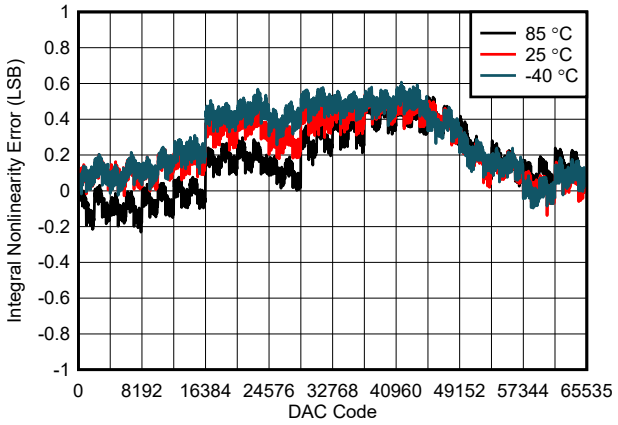


图 6-1. Timing Diagram

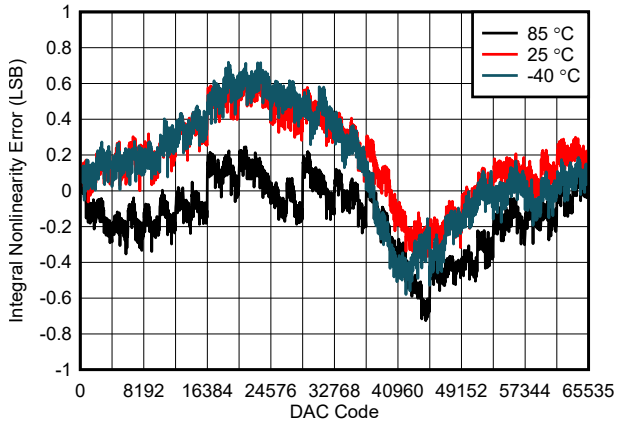
6.8 Typical Characteristics

at T_A = 25°C, channel output shown, and DAC outputs unloaded (unless otherwise noted)



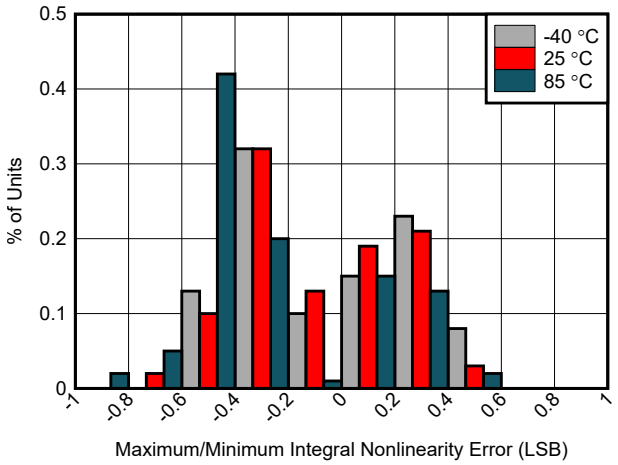
V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-2. Integral Linearity Error vs Digital Input Code



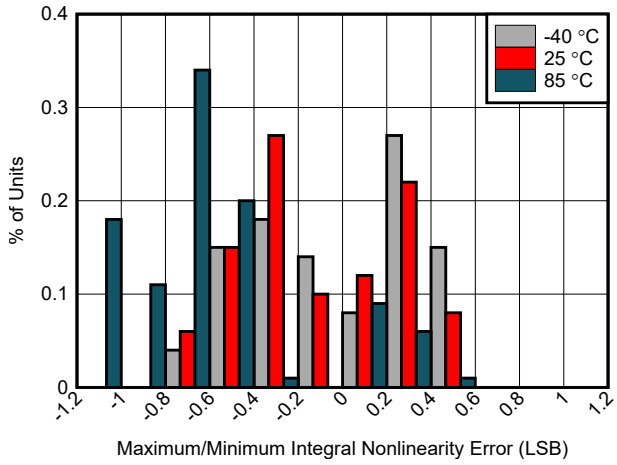
V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-3. Integrated Linearity Error vs Digital Input Code



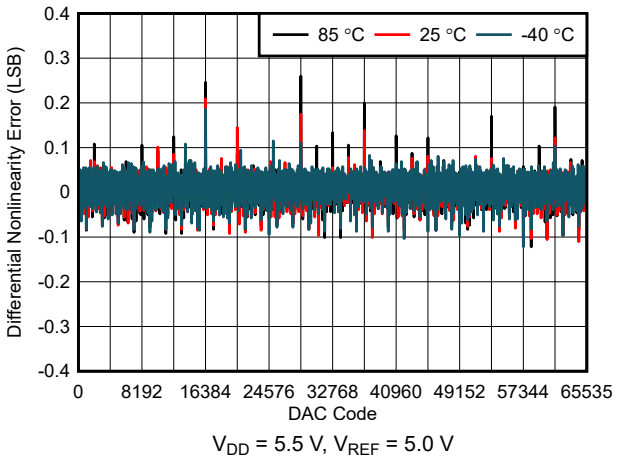
V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-4. Integral Linearity Error Histogram



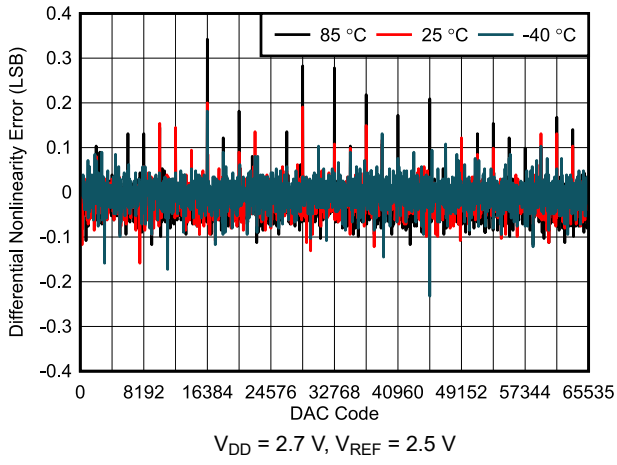
V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-5. Integrated Linearity Error Histogram



V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-6. Differential Linearity Error vs Digital Input Code

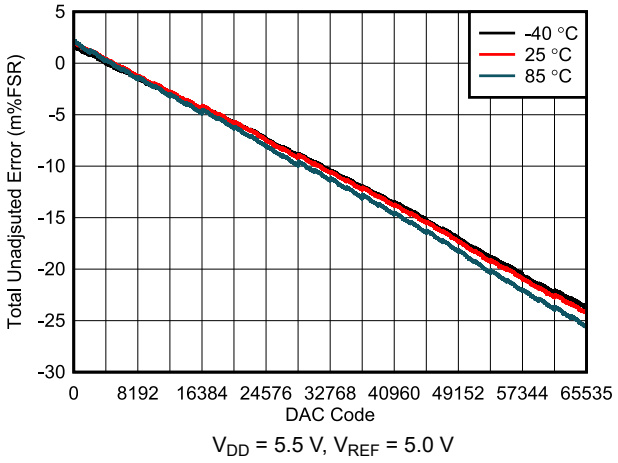


V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-7. Differential Linearity Error vs Digital Input Code

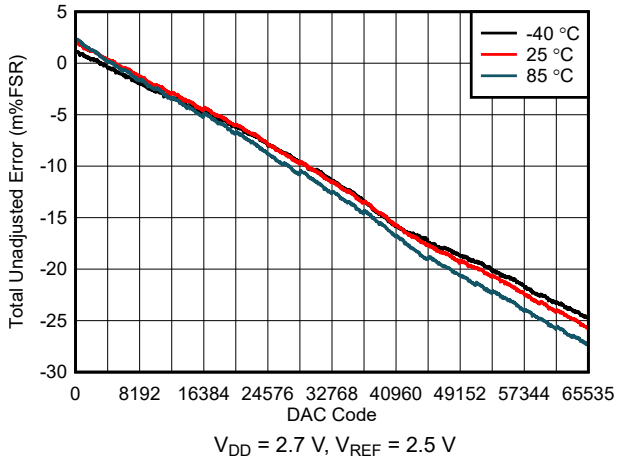
6.8 Typical Characteristics (continued)

at T_A = 25°C, channel output shown, and DAC outputs unloaded (unless otherwise noted)



V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-8. Total Unadjusted Error vs Digital Input Code



V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-9. Total Unadjusted Error vs Digital Input Code

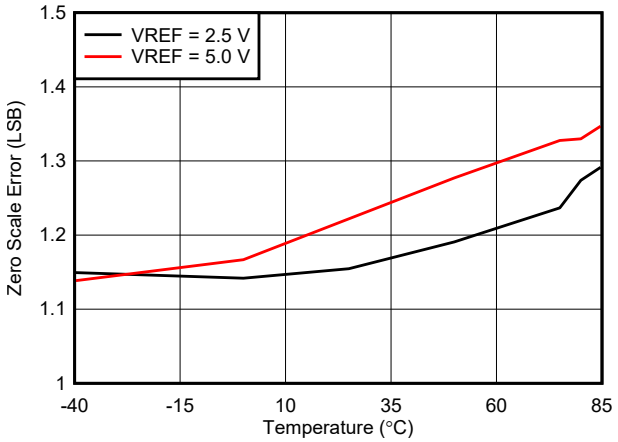


图 6-10. Zero-Code Error vs Temperature

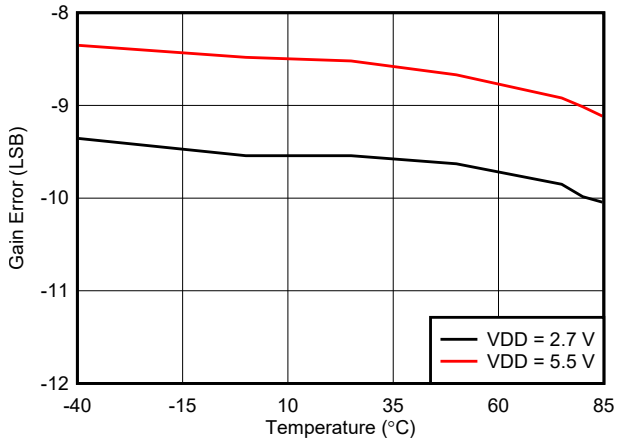


图 6-11. Gain Error vs Temperature

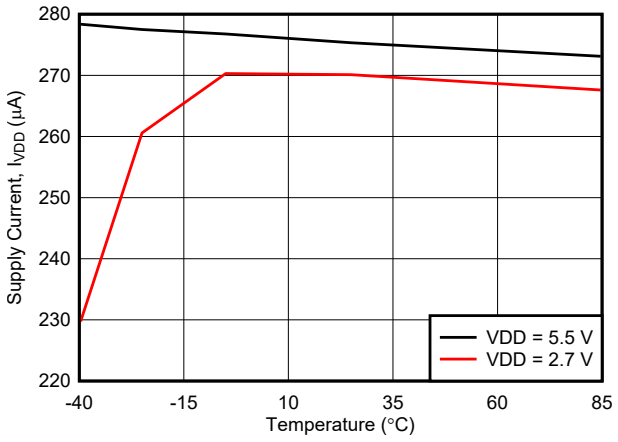


图 6-12. Supply Current vs Temperature

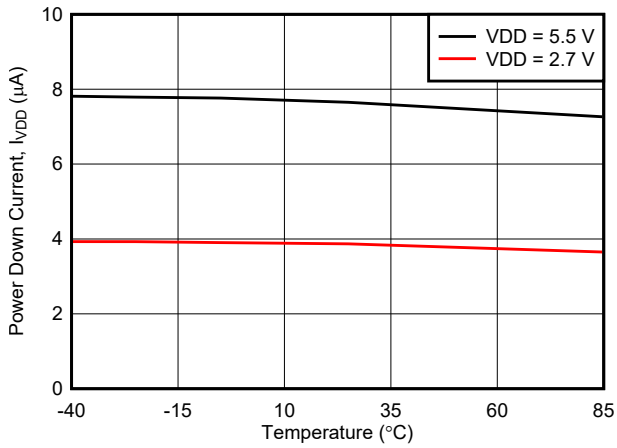
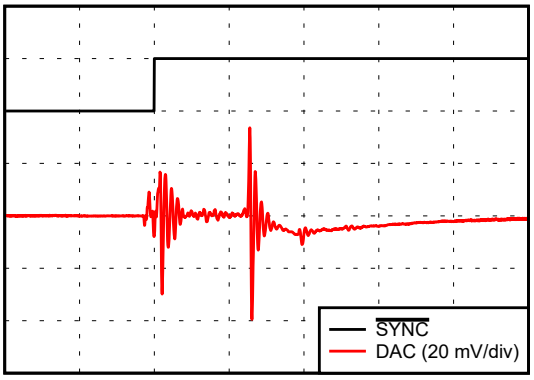


图 6-13. Power-down Current vs Temperature

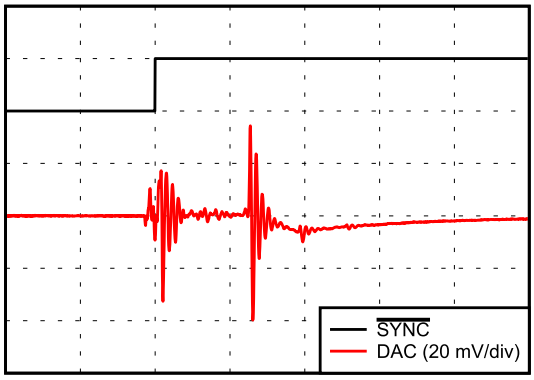
6.8 Typical Characteristics (continued)

at T_A = 25°C, channel output shown, and DAC outputs unloaded (unless otherwise noted)



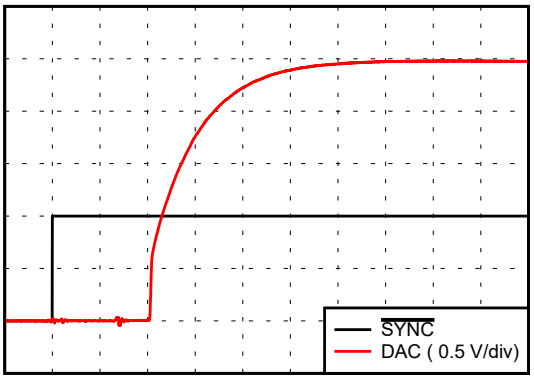
V_{DD} = 5.5 V, V_{REF} = 5.0 V,
DAC code transition from midscale – 1 to midscale LSB

图 6-14. Glitch Impulse, Rising Edge, 1-LSB Step



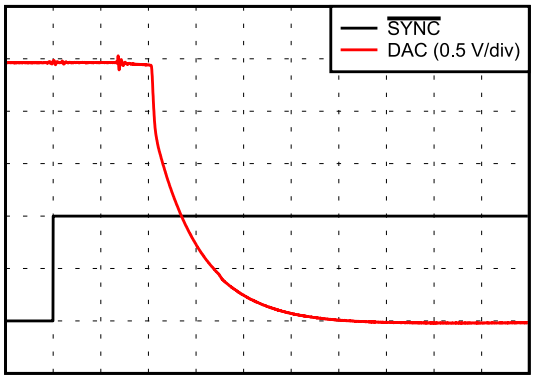
V_{DD} = 5.5 V, V_{REF} = 5.0 V,
DAC code transition from midscale to midscale - 1 LSB

图 6-15. Glitch Impulse, Falling Edge, 1-LSB Step



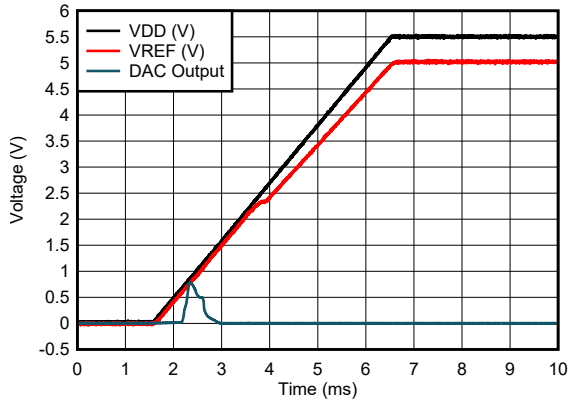
V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-16. Full-Scale Settling Time, Rising Edge



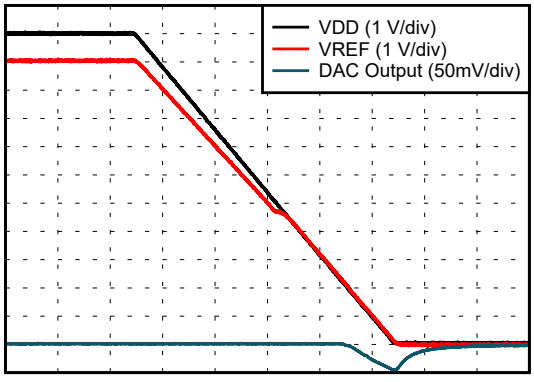
V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-17. Full-Scale Settling Time, Falling Edge



V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-18. Power-On Glitch

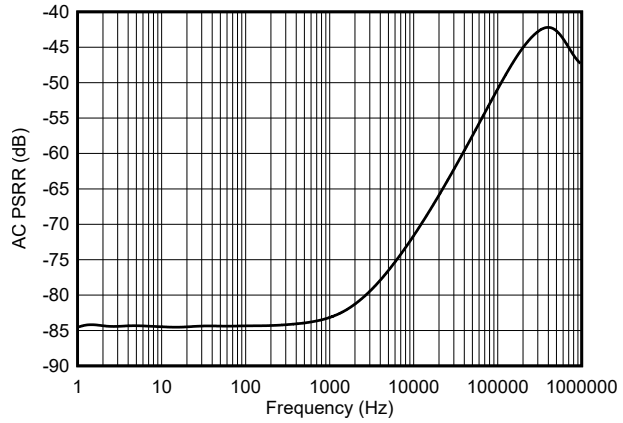


V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-19. Power-Off Glitch

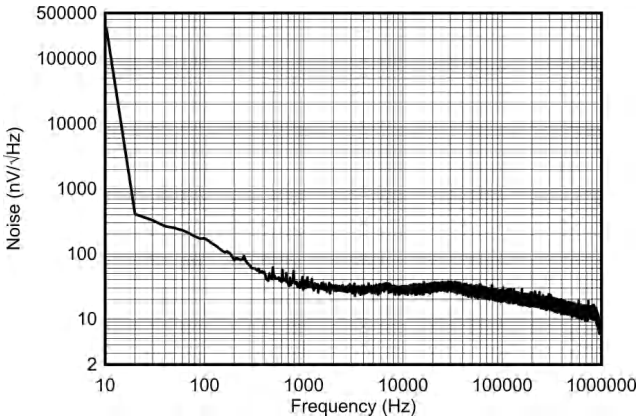
6.8 Typical Characteristics (continued)

at T_A = 25°C, channel output shown, and DAC outputs unloaded (unless otherwise noted)



V_{DD} = 5.5 V, DAC code at midscale

图 6-20. Power-Supply Rejection Ratio (PSRR)



V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-21. Output Noise Density vs Frequency

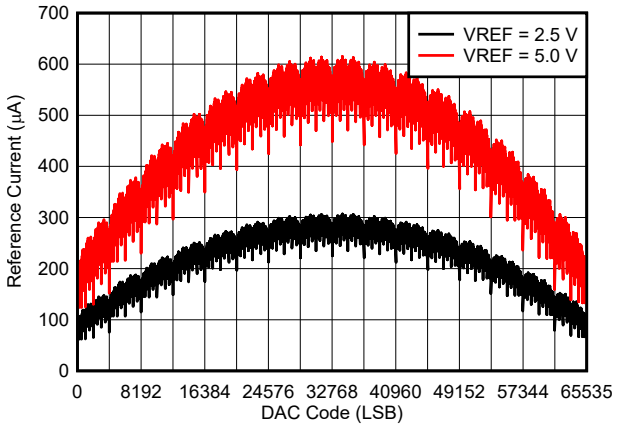
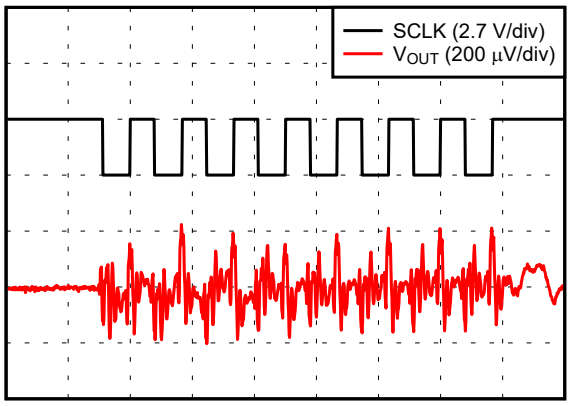


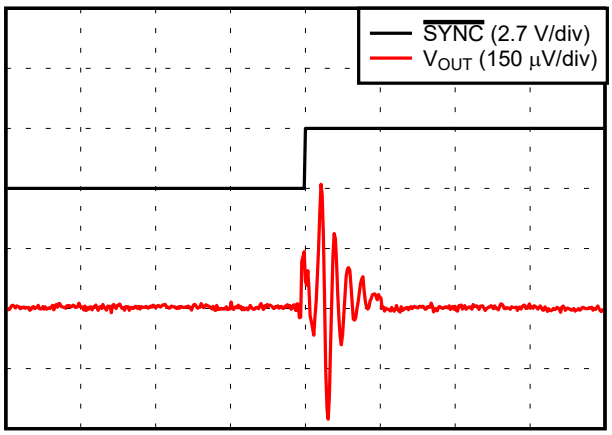
图 6-22. Reference Current vs Digital Input Code



Time (100 ns/div)

V_{DD} = 2.7 V, V_{REF} = 2.5 V

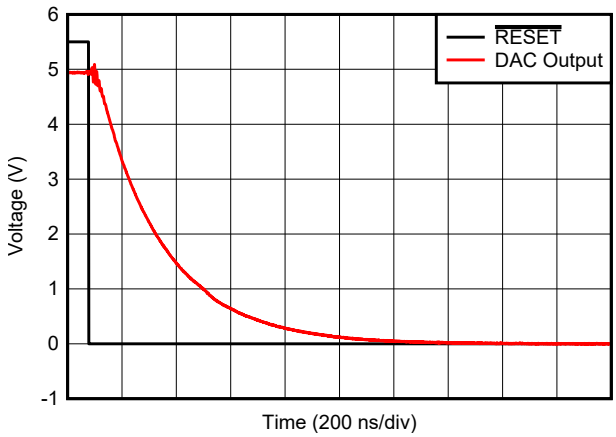
图 6-23. Clock Feedthrough



Time (50 ns/div)

V_{DD} = 2.7 V, V_{REF} = 2.5 V

图 6-24. Control Feedthrough



V_{DD} = 5.5 V, V_{REF} = 5.0 V

图 6-25. $\overline{\text{RESET}}$ Response

7 Detailed Description

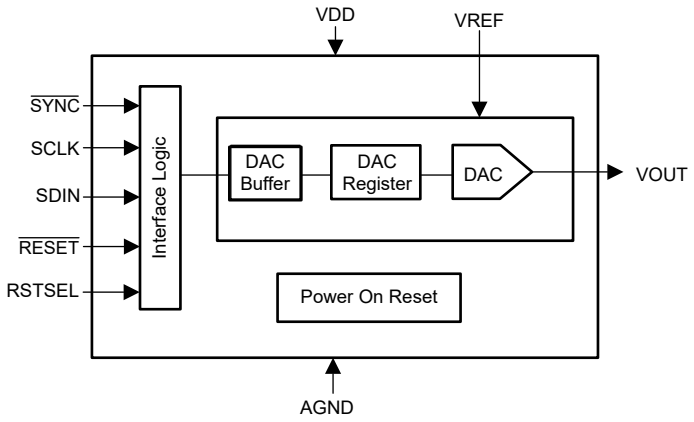
7.1 Overview

The DAC82001 device is a single-channel, unbuffered voltage output, 16-bit digital-to-analog converter (DAC) operating from a single 3.3-V to 5-V power supply. This converter provides 1-LSB DNL and 2-LSB INL linearity. With a 10-pF load, the output of the DAC82001 settles to ½ LSB of full scale at 1 µs. The glitch impulse of 1-LSB code change around major carry is 0.5 nV-s.

The device incorporates a power-on-reset circuit to make sure that the DAC output powers up at zero scale or midscale, depending on status of the RSTSEL pin, and remains at that scale until a valid code is written to the device. All internal registers are asynchronously reset after the $\overline{\text{RESET}}$ pin is pulled low. Similar to the power-on-reset, the $\overline{\text{RESET}}$ signal sets the DAC output to zero scale or midscale based on the status of the RSTSEL pin.

The digital interface of the DAC82001 uses a 3-wire serial peripheral interface (SPI) that operates at clock rates of up to 50 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital-to-Analog Converter (DAC) Architecture

The output channel in the DAC82001 device consists of a segmented R-2R architecture. 图 7-1 shows a block diagram of the DAC architecture. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or VREF. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

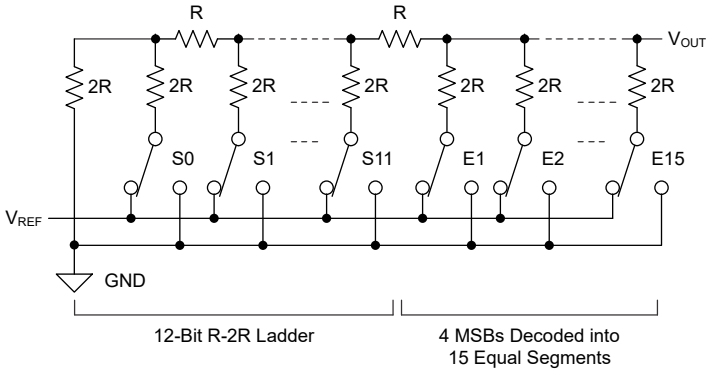


图 7-1. DAC82001 DAC Block Diagram

7.3.1.1 DAC Transfer Function

The input data writes to the individual DAC data registers in straight binary format. After a power-on or a reset event, all DAC registers are set to zero code (RSTSEL = AGND) or midscale code (RSTSEL = V_{DD}). The DAC transfer function is shown by 方程式 1.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (1)$$

where:

- N = 16 (resolution in bits)
- DAC_DATA = decimal equivalent of the binary code that is loaded to the DAC register (address 8h), DAC_DATA ranges from 0 to $2^N - 1$
- V_{REF} = DAC external reference voltage. V_{REF} ranges from 2.0 V to V_{DD}

7.3.1.2 DAC Register Structure

Data written to the DAC data registers are initially stored in the DAC buffer registers. The update mode of the DAC output is determined by the status of the DAC_SYNC_EN bit (address 2h).

In asynchronous mode (default, DAC_SYNC_EN = 0), a write to the DAC buffer register results in an immediate update of the DAC active register. The DAC output (VOUT pin) updates on the rising edge of $\overline{SYNC}$.

In synchronous mode (DAC_SYNC_EN = 1), writing to the DAC buffer register does not automatically update the DAC active register. Instead, the update occurs only after a software LDAC trigger event. A software LDAC trigger generates through the LDAC bit in the TRIGGER register (address 5h).

7.3.2 Power-On Reset (POR)

The DAC82001 device includes a power-on reset function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 250-µs, power-on-reset delay. The default value for all DACs is zero code if RSTSEL = AGND, and midscale code if RSTSEL = V_{DD}. The DAC channel remains at the power-up voltage until a valid command is written to the channel.

When the device powers up, a POR circuit sets the device to the default mode. 图 7-2 shows that the POR circuit requires specific V_{DD} levels to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 2.2 V but remains greater than 0.7 V (shown as the undefined region in 图 7-2), the device may or may not reset under all specified temperature and power-supply conditions; in this case, initiate a POR. When V_{DD} remains greater than 2.2 V, a POR does not occur.

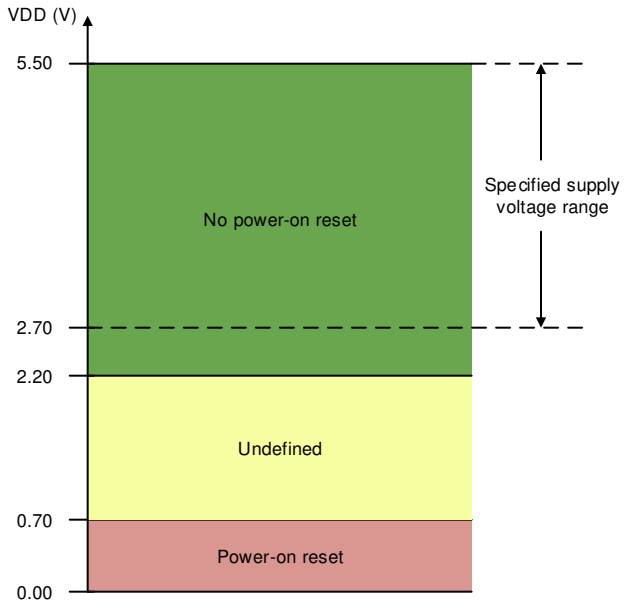


图 7-2. Threshold Levels for the V_{DD} POR Circuit

7.3.3 Hardware Reset

The DAC output is asynchronously set to zero code if RSTSEL = AGND, and midscale code if RSTSEL = V_{DD}, immediately after the $\overline{\text{RESET}}$ pin is brought low. The $\overline{\text{RESET}}$ signal resets all internal registers, meaning all registers initialize to default values. Bring the $\overline{\text{RESET}}$ pin back to high before a write sequence starts. Similar to the POR delay, communication with the device is valid only after a 250-µs delay. The default value for the DAC channel remains at the reset voltage until a valid command is written to the channel. The RSTSEL pin can be reconfigured without a power cycle. The DAC output always reflects the current RSTSEL status when the $\overline{\text{RESET}}$ pin is pulled low.

7.3.4 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to the SOFT-RESET bits in the TRIGGER register (address 5h). A software reset initiates a POR event.

7.4 Device Functional Modes

The DAC82001 has one mode of operation: normal.

In normal mode, the DAC82001 is fully operational. The device translates digital input or reset input to corresponding analog output.

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI)

The DAC82001 is controlled through a 3-wire serial peripheral interface (SPI) using $\overline{\text{SYNC}}$, SCLK, and SDIN. The serial interface operates at up to 50 MHz. The input shift register is 24-bits wide.

表 7-1 shows the SPI frame format.

表 7-1. SPI Frame Format

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESC	$\overline{\text{W}}$	Register Address - Command Byte							16-Bit MSB-Aligned DAC Data															

Serial clock SCLK is a continuous or a gated clock. The first falling edge of $\overline{\text{SYNC}}$ starts the operation cycle. When $\overline{\text{SYNC}}$ is high, the SCLK and SDIN signals are blocked. The device internal registers are updated from the shift register on the rising edge of $\overline{\text{SYNC}}$.

7.5.1.1 $\overline{\text{SYNC}}$ Interrupt

For SPI operation, the $\overline{\text{SYNC}}$ line stays low for at least 24 falling edges of SCLK, and the addressed DAC register updates on the $\overline{\text{SYNC}}$ rising edge. However, if the $\overline{\text{SYNC}}$ line is brought high before the 24th SCLK falling edge, this event acts as an interrupt to the write sequence. The shift register resets and the write sequence is discarded. As 图 7-3 shows, the data buffer contents and the DAC register contents do not update, and the operating mode does not change.

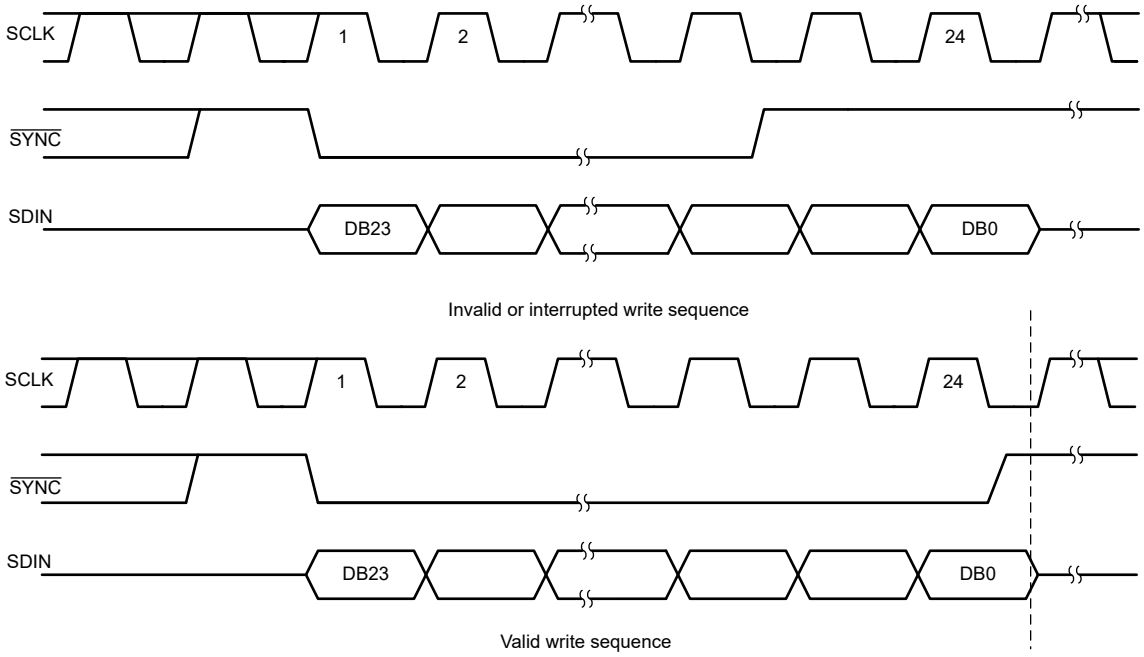


图 7-3. $\overline{\text{SYNC}}$ Interrupt

7.6 Register Maps

7.6.1 Registers

表 7-2. DAC82001 Registers

Offset	Register Description	Section
0h	No Operation	NOOP Register
2h	Synchronization	SYNC Register
5h	Trigger	TRIGGER Register
8h	DAC	DAC Register

7.6.1.1 NOOP Register (offset = 0h) [reset = 0000h]

图 7-4. NOOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOOP															
W-0h															

表 7-3. NOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOOP	W	0h	No operation command

7.6.1.2 SYNC Register (offset = 2h) [reset = 0000h]

图 7-5. SYNC Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DAC-SYNC-EN
W-0h															W-0h

表 7-4. SYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	W	0h	These bits are reserved.
0	DAC-SYNC-EN	W	0h	When set to 1, the DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0, the DAC output is set to update immediately (asynchronous mode), default.

7.6.1.3 TRIGGER Register (offset = 5h) [reset = 0000h]

图 7-6. TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											LDAC	SOFT-RESET [3:0]			
W-0h											W-0h	W-0h			

表 7-5. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	W	0h	These bits are reserved.
4	LDAC	W	0h	Set this bit to 1 to synchronously load the DAC that is set to synchronous mode in the SYNC register. This bit self-resets.
3-0	SOFT-RESET [3:0]	W	0h	When set to reserved code 1010, this bit resets the device to the default state. This bit self-resets.

7.6.1.4 DAC Register (offset = 8h) [reset = 0000h when RSTSEL is logic low, or reset = 8000h when RSTSEL is logic high]

图 7-7. DAC Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-DATA [15:0]															
W-0000h when RSTSEL is logic low or 8000h when RSTSEL is logic high															

表 7-6. DAC Data Register Field Descriptions (8h)

Bit	Field	Type	Reset	Description
15-0	DAC-DATA [15:0]	W	0000h when RSTSEL is logic low or 8000h when RSTSEL is logic high	Data are MSB aligned in straight binary format.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Generating accurate, stable, programmable dc voltages is a key requirement in most precision end equipment. The DAC82001 serves a wide range of end equipment, such as battery testers, communications equipment, factory automation and control, test and measurement. The DAC82001 tiny package, high resolution, fast settling, and simple interface makes this device an excellent choice for applications such as offset and gain control, arbitrary waveform generation (AWG), closed-loop control, and bipolar analog outputs. A wide variety of operational amplifiers can be used as output buffers for the DAC82002, allowing the user to choose components that best fit their design.

8.2 Typical Applications

8.2.1 Arbitrary Waveform Generator

Arbitrary waveform generation (AWG) circuits are common in test and measurement equipment. These circuits are used to generate ac waveforms for test applications. The key performance parameters in test and measurement circuits are total harmonic distortion and noise (THD+N), signal-to-noise ratio (SNR), and the update rate. 图 8-1 shows a basic example of an AWG circuit using the DAC82001.

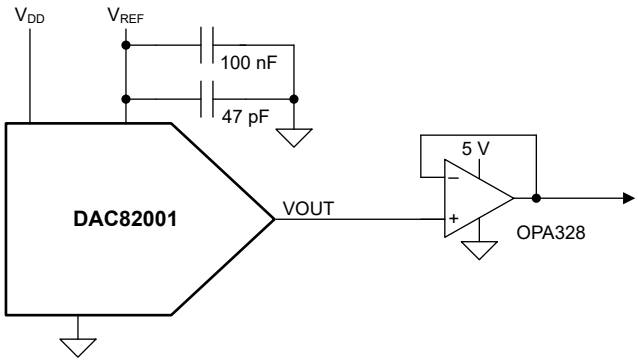


图 8-1. Arbitrary Waveform Generator

8.2.1.1 Design Requirements

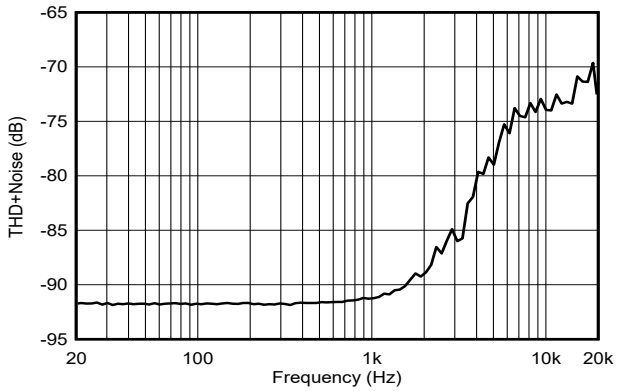
- DAC output range: 0 V to 2.5 V
- THD+N at 1 kHz: < –91 dB
- Update rate: 200 kHz

8.2.1.2 Detailed Design Procedure

图 8-1 shows a simplified circuit diagram of an arbitrary waveform generator. The DAC82001 specifies a THD+N of –91 dB at 1 kHz. The OPA328 provides a great balance between fast settling, bandwidth, and voltage and current noise. The buffer must have a negative voltage supply rail or an output offset to make sure the DAC output is not clipped. Attach two decoupling capacitors as close as possible to the VREF pin. Use 100 nF for the first capacitor to provide very good noise performance for the system. Use 47 pF for the second capacitor to allow for a good dynamic response performance that improves any code-to-code glitch. The REF5025 is a low-noise, very low-drift, precise voltage reference that generates a 2.5-V reference for this application.

8.2.1.3 Application Curves

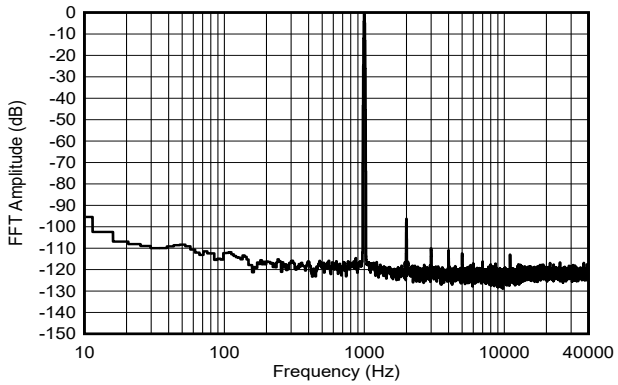
图 8-2 shows the THD+N plot vs frequency of the buffer output using a 20-Hz to 20-kHz sine wave sweep with a DAC code range of 0x81FF ± 0x7E00 to prevent voltage clipping. A 40-kHz low-pass filter is also used in the measurement tool.



20-Hz to 20-kHz sine wave sweep with a code range of 0x81FF ± 0x7E00
40-kHz low-pass filter

图 8-2. THD+N vs Frequency

图 8-3 shows the FFT of the buffer output using a 1-kHz sine wave with a code range of 0x81FF ± 0x7E00 to prevent voltage clipping. 32768 bins, 8 averages, and a 40-kHz low-pass filter are also used in the measurement tool.



1-kHz sine wave with a code range of 0x81FF ± 0x7E00
32768 bins, 8 averages, 40-kHz low-pass filter

图 8-3. FFT Amplitude vs Frequency

8.2.2 Bipolar Analog Output Configuration

Programmable logic circuits (PLCs) have analog output modules that typically output ±10 V. This bipolar analog output circuit converts the unipolar DAC output to a bipolar ±10-V output. The key performance parameters of these circuits are noise and slew rate. The circuit can also be used to force voltage in semiconductor test applications. 图 8-4 shows the example configuration using the DAC82001.

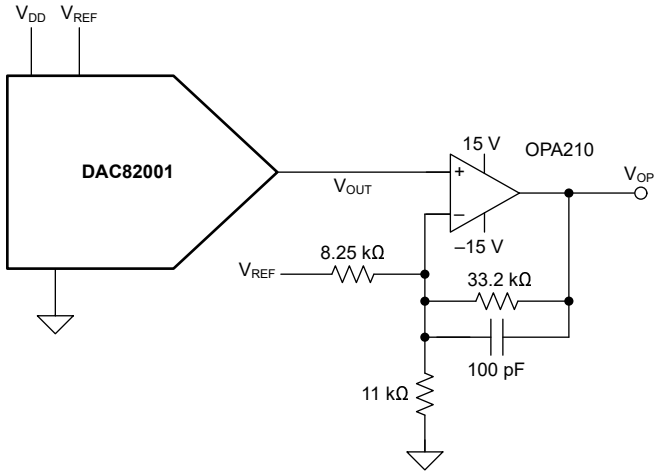


图 8-4. Bipolar Analog Output Circuit

8.2.2.1 Design Requirements

- DAC output range: 0 V to 2.5 V
- PLC analog output range: – 10 V to +10 V
- Noise: < 3 μV/ √Hz
- Slew rate: > 1 V/μs

8.2.2.2 Detailed Design Procedure

The OPA210 output buffer provides a balance between fast settling, bandwidth, voltage and current noise, and wide voltage rails. The buffer uses ±15-V voltage rails to make sure there is no voltage clipping. The REF5025 is a low-noise, very low-drift, precise voltage reference and is used to generate a stable 2.5-V reference for this application. To further reduce noise, use a 100-pF capacitor between the non-inverting input pin and the output of the OPA210.

8.2.2.3 Application Curves

图 8-5 shows the noise on the buffer output vs frequency using a 100-Hz to 1-MHz frequency sweep with a grounded reference to isolate the noise in the circuit.

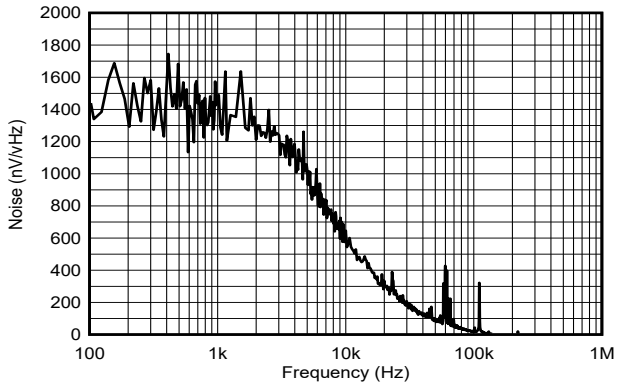
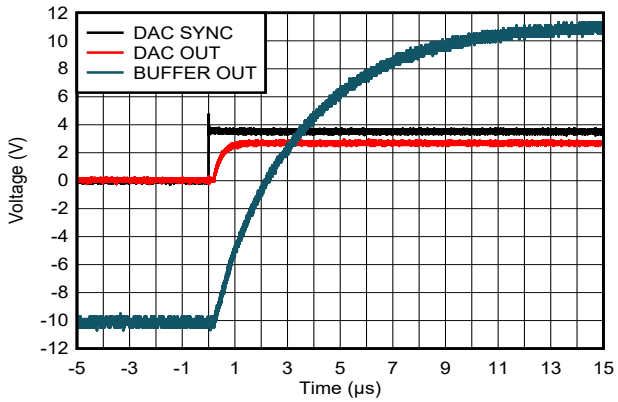


图 8-5. Noise vs Frequency

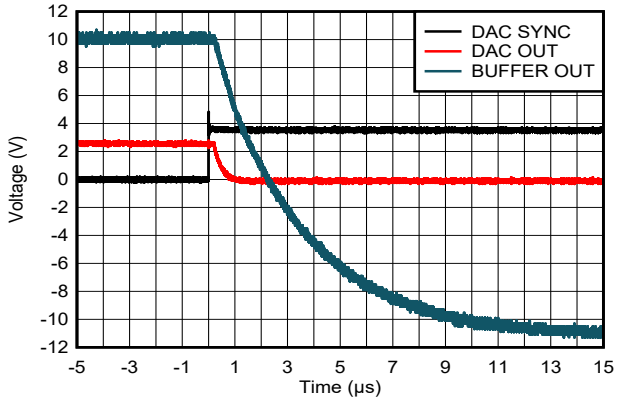
图 8-6 shows the output of the circuit rising from – 10 V to +10 V, with the DAC starting at code 0x0000 and ending at code 0xFFFF. The measured slew rate is 2.5 V/µs. The REF5025 is used as a 2.5-V reference.



DAC at code 0x0000 rising to code 0xFFFF

图 8-6. Bipolar Output Rising Slew Rate

图 8-7 shows the output of the circuit falling from +10 V to – 10 V, with the DAC starting at code 0xFFFF and ending at code 0x0000. This measured slew rate is 2.5 V/µs. The REF5025 is used as a 2.5-V reference.



DAC at code 0xFFFF falling to code 0x0000

图 8-7. Bipolar Output Falling Slew Rate

8.3 Power Supply Recommendations

The DAC82001 operates within the specified V_{DD} supply range of 2.7 V to 5.5 V. The DAC82001 does not require specific supply sequencing, but V_{REF} must be less than V_{DD}, as noted in the *Absolute Maximum Ratings*. The V_{DD} supply must be well-regulated and low-noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. Digital components also create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, include a 1-μF to 10-μF capacitor and 0.1-μF bypass capacitor.

8.4 Layout

8.4.1 Layout Guidelines

A precision analog component requires careful layout. The following list provides some insight into good layout practices.

- Bypass the VDD to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1-μF to 0.22-μF ceramic capacitor, with a X7R or NP0 dielectric.
- Bypass VREF to ground with low ESR ceramic bypass capacitors.
- Place power supplies and REF bypass capacitors close to the pins to minimize inductance and optimize performance.
- The output pin, VOUT, has relatively high impedance and is susceptible to high parasitic capacitance. Use short and direct traces when routing VOUT.

8.4.2 Layout Example

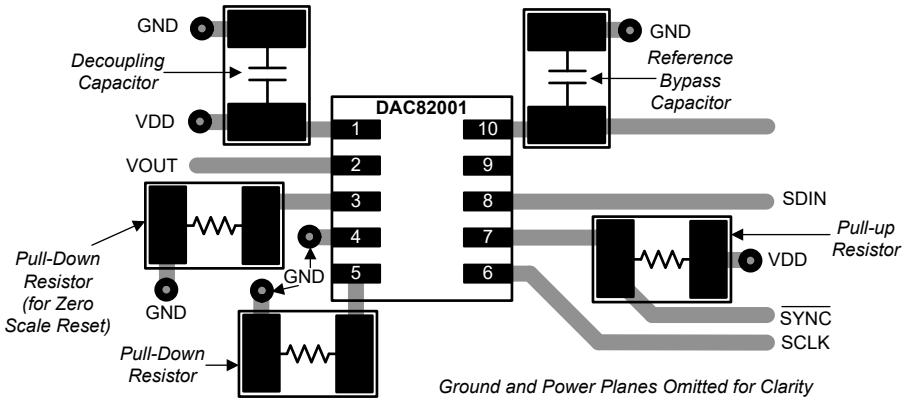


图 8-8. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *DAC82002EVM* user's guide

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC82001DRXR	Active	Production	WSON (DRX) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D821
DAC82001DRXR.A	Active	Production	WSON (DRX) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D821

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

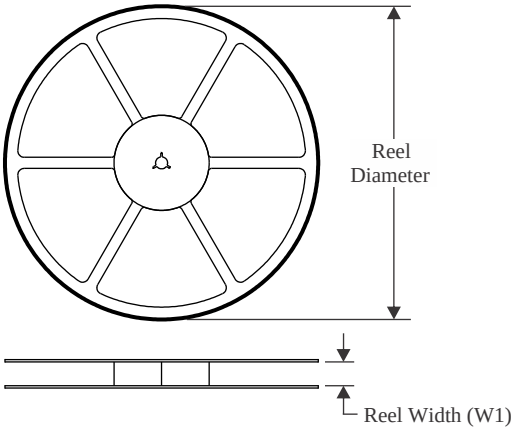
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

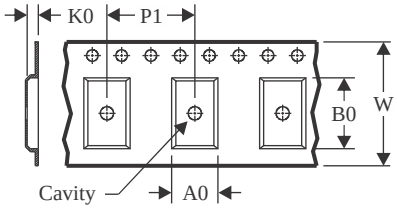
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

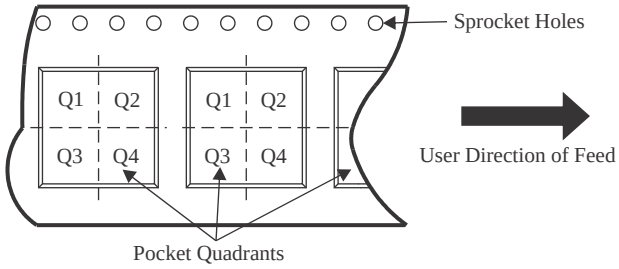


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

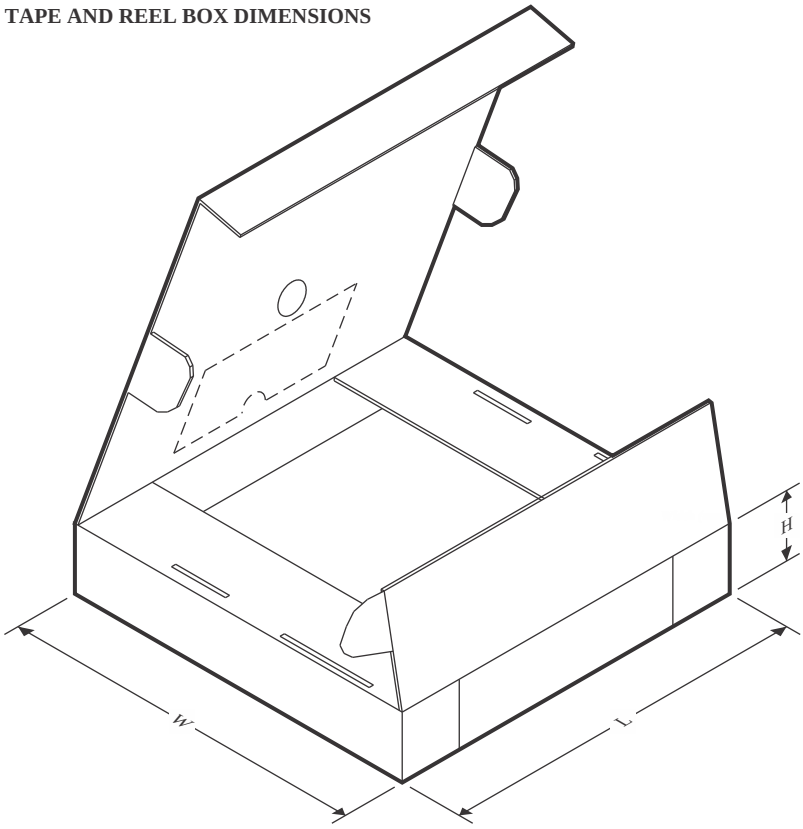
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC82001DRXR	WSON	DRX	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

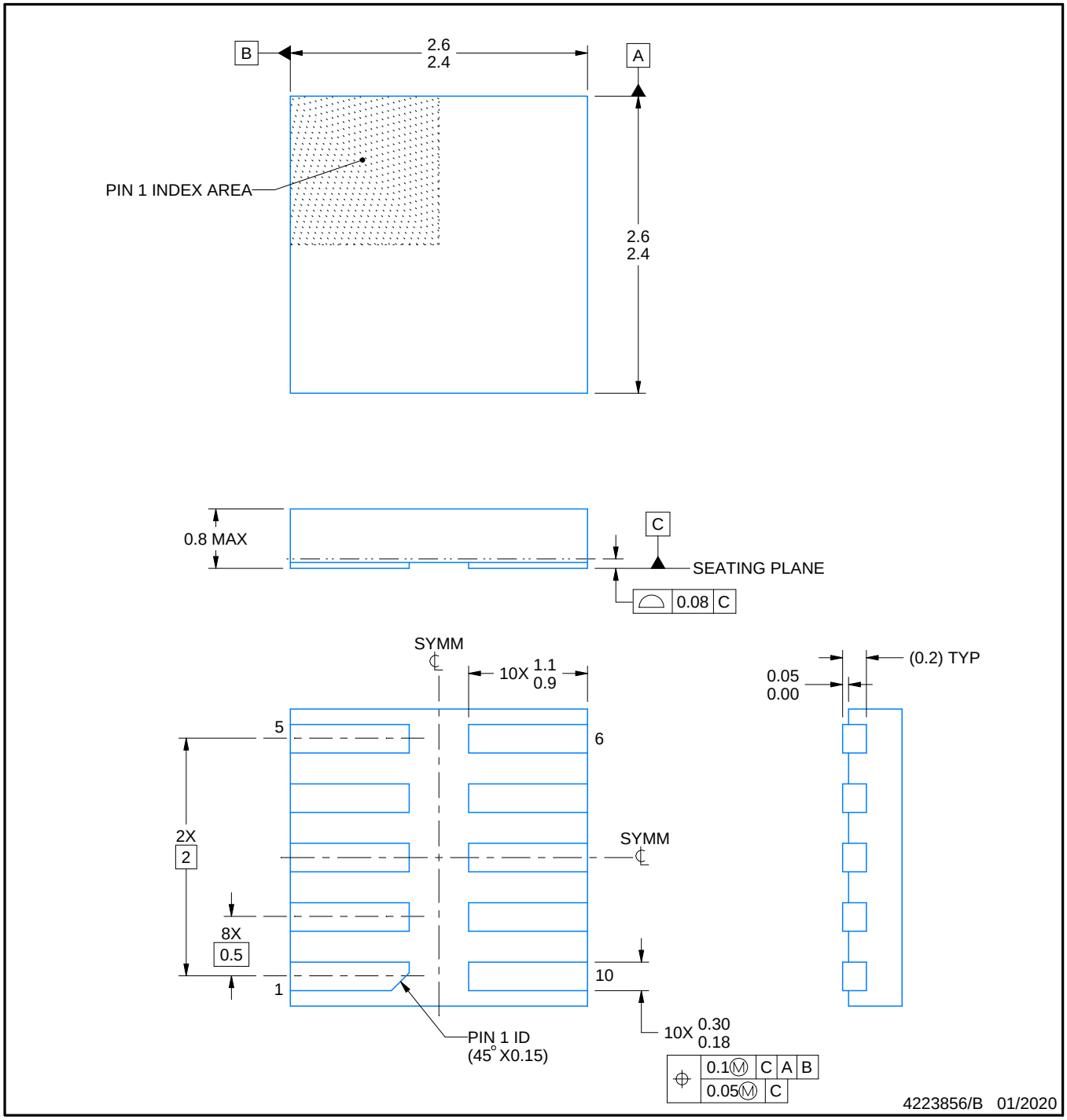
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC82001DRXR	WSON	DRX	10	3000	205.0	200.0	33.0

PACKAGE OUTLINE

DRX0010A

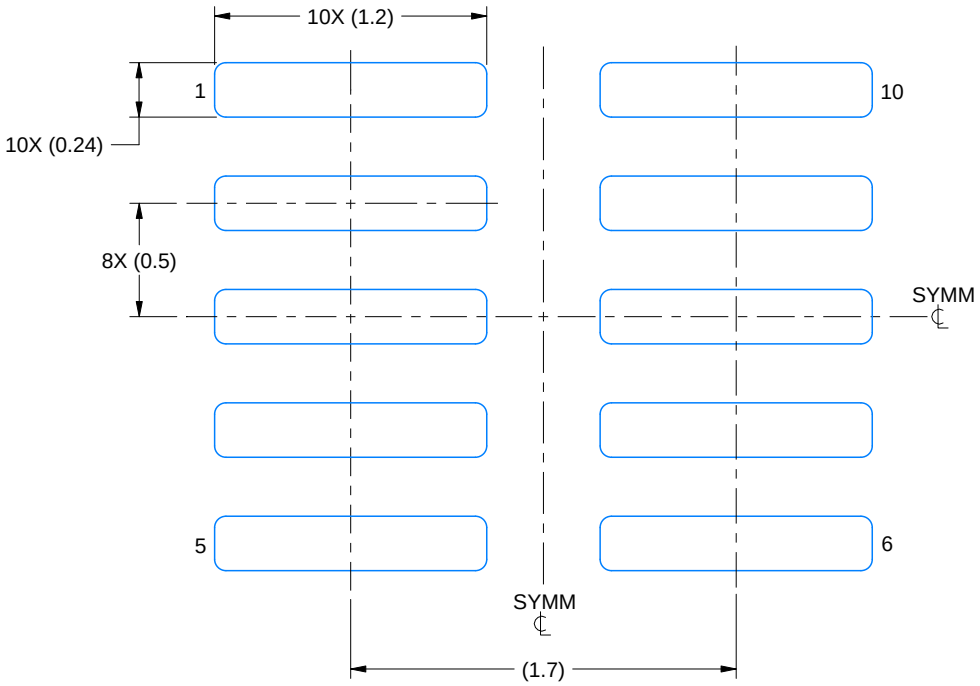
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

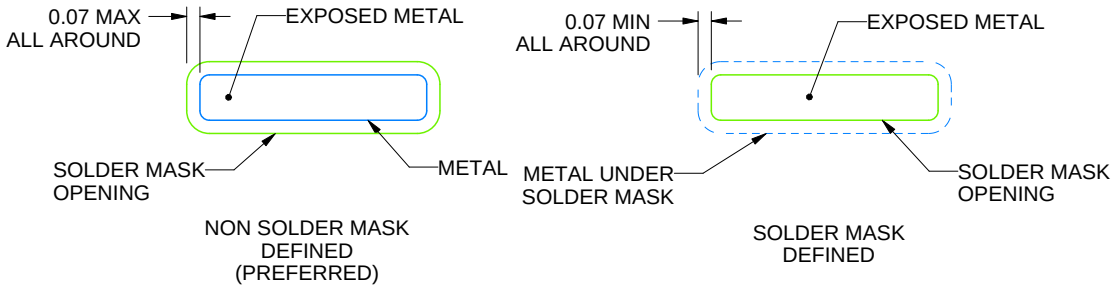


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

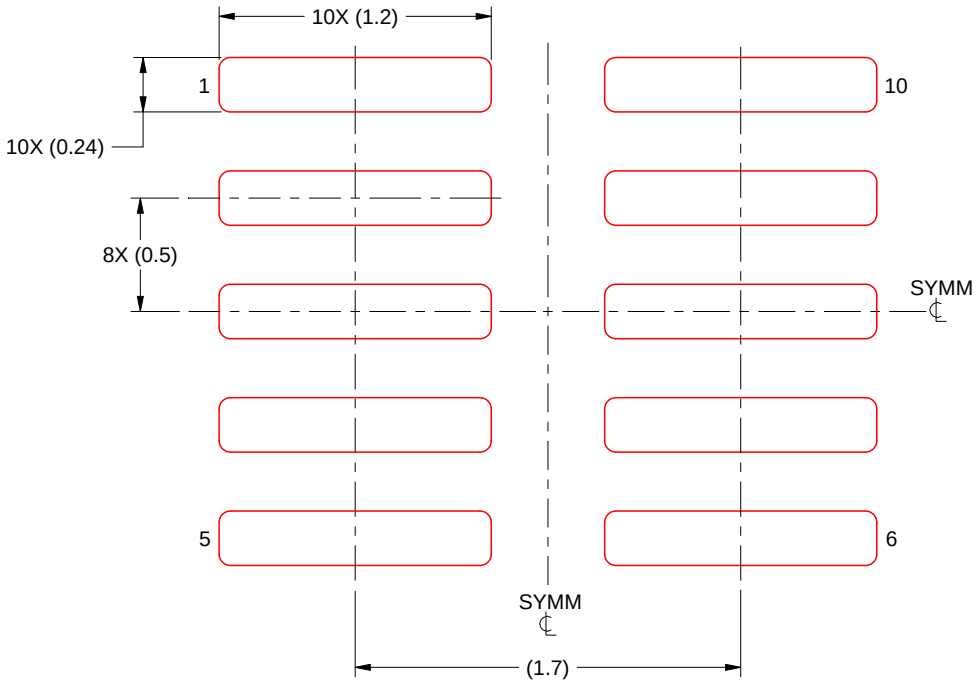
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRX0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月