

# DAC8881 16 位单通道低噪声电压输出 数模转换器

## 1 特性

- 相对精度:  $\pm 0.5\text{LSB}$
- 全温度范围内的 16 位单调性
- 低噪声:  $24\text{nV}/\sqrt{\text{Hz}}$
- 快速稳定:  $5\mu\text{s}$
- 支持轨至轨运行的片上输出缓冲放大器
- 单个宽电源电压范围:  $+2.7\text{V}$  至  $+5.5\text{V}$
- DAC 负载控制
- 可选择的上电复位至零电平或中间电平
- 掉电模式
- 单极直接二进制或二进制补码输入模式
- 具有施密特触发输入的快速 SPI™ 接口: 高达  $50\text{MHz}$ ,  $1.8\text{V}/3\text{V}/5\text{V}$  逻辑电平
- 小型封装: QFN-24,  $4\times 4\text{mm}$

## 2 应用

- 工业过程控制
- 数据采集系统
- 自动测试设备
- 通信
- 光纤网络

## 3 说明

DAC8881 是一款 16 位单通道电压输出数模转换器 (DAC), 可提供低功耗运行和灵活的 SPI 串行接口。该器件还具有 16 位单调性、卓越的线性度以及快速稳定性能。片上精密输出放大器可在  $2.7\text{V}$  至  $5.5\text{V}$  的完整电压范围内实现轨至轨输出摆幅。

该器件支持标准 SPI 串行接口, 这种接口可在高达  $50\text{MHz}$  的输入数据时钟频率下工作。DAC8881 需要外部基准电压来设置 DAC 通道的输出范围。该器件还采用了可编程上电复位电路, 确保 DAC 输出可以零电平或中间电平加电并保持, 直到写入一个有效代码。

而且, 该器件能够在单极直接二进制或二进制补码模式下运行。DAC8881 可提供通过 PDN 引脚实现的断电功能, 从而在  $5\text{V}$  时将电流消耗减少到  $25\mu\text{A}$ 。  $5\text{V}$  时的功耗为  $6\text{mW}$ , 断电模式下降低至  $125\mu\text{W}$ 。

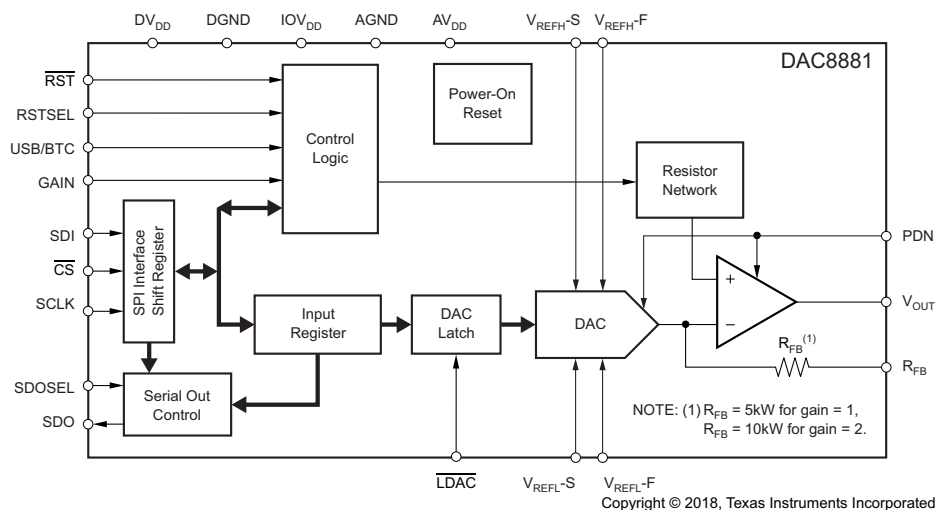
DAC8881 采用  $4\times 4\text{mm}$  QFN-24 封装, 指定工作温度为  $-40^{\circ}\text{C}$  至  $+105^{\circ}\text{C}$ 。

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8881	VQFN	$4.00\text{mm} \times 4.00\text{mm}$

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

框图



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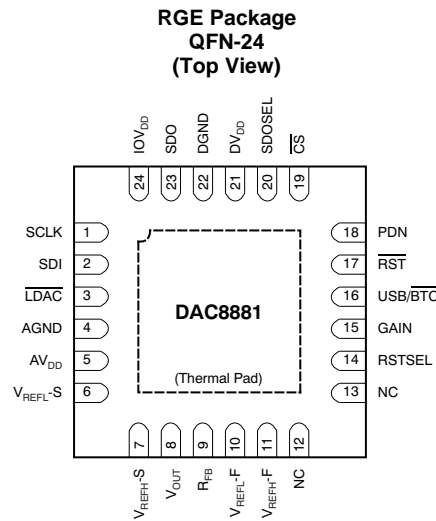
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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (September 2007) to Revision B	Page
• 增加了器件信息表、ESD 额定值表、建议运行条件表、特性 说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。 .....	1
• Changed the text in the <i>Input Data Format</i> section .....	28
• Changed <a href="#">Table 3</a> .....	29

## 5 Pin Configuration and Functions



- (1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI bus serial clock input
2	SDI	I	SPI bus serial data input
3	$\overline{\text{LDAC}}$	I	Load DAC latch control input (active low). When $\overline{\text{LDAC}}$ is low, the DAC latch is transparent, and the contents of the input register are transferred to the DAC latch. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated.
4	AGND	I	Analog ground
5	AVDD	I	Analog power supply
6	VREFL-S	I	Reference low input sense
7	VREFH-S	I	Reference high input sense
8	VOUT	O	Output of output buffer
9	RFB	I	Feedback resistor connected to the inverting input of the output buffer.
10	VREFL-F	I	Reference low input force
11	VREFH-F	I	Reference high input force
12	NC	—	Do not connect.
13	NC	—	Do not connect.
14	RSTSEL	I	Selects the value of the output from the VOUT pin after power-on or hardware reset. If RSTSEL = IOVDD, then register data = 8000h. If RSTSEL = DGND, then register data = 0000h.
15	GAIN	I	Buffer gain setting. Gain = 1 when the pin is connected to DGND; Gain = 2 when the pin is connected to IOVDD.
16	USB/BTC	I	Input data format selection. Input data are straight binary format when the pin is connected to IOVDD, and in two's complement format when the pin is connected to DGND.
17	$\overline{\text{RST}}$	I	Reset input (active low). Logic low on this pin causes the device to perform a reset.
18	PDN	I	Power-down input (active high). Logic high on this pin forces the device into power-down status. In power-down, the VOUT pin connects to AGND through 10kΩ resistor.
19	$\overline{\text{CS}}$	I	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, SDO is in high-impedance status.
20	SDOSEL	I	SPI serial data output selection. When SDOSEL is tied to IOVDD, the contents of the existing input register are shifted out from the SDO pin; this is Stand-Alone mode. When SDOSEL is tied to DGND, the contents in the SPI input shift register are shifted out from the SDO pin; this is Daisy-Chain mode for daisy chaining communication.
21	DVDD	I	Digital power supply (connect to AVDD, pin 5)
22	DGND	I	Digital ground
23	SDO	O	SPI bus serial data output. Refer to the <a href="#">Timing Diagrams</a> for further detail.
24	IOVDD	I	Interface power. Connect to +1.8V for 1.8V logic, +3V for 3V logic, and to +5V for 5V logic.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
AV <sub>DD</sub> to AGND	−0.3	6	V
DV <sub>DD</sub> to DGND	−0.3	6	V
IOV <sub>DD</sub> to DGND	−0.3	6	V
Digital input voltage to DGND	−0.3	IOV <sub>DD</sub> + 0.3	V
V <sub>OUT</sub> to AGND	−0.3	AV <sub>DD</sub> + 0.3	V
Operating temperature range	−40	105	°C
Storage temperature range	−65	150	°C
Storage temperature, T <sub>stg</sub>		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AV <sub>DD</sub>	Analog power supply	2.7		5.5	V
IOV <sub>DD</sub>	Interface power supply	1.7		AV <sub>DD</sub>	V
V <sub>REFH</sub>	Reference high input voltage	AV <sub>DD</sub> = 5.5 V		AV <sub>DD</sub>	V
		AV <sub>DD</sub> = 3 V		AV <sub>DD</sub>	V
V <sub>REFL</sub>	Reference low input voltage	−0.2	0	0.2	V
	Specified performance	−40		105	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DAC8881	UNIT
		RGE (VQFN)	
		24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	33.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	37.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	11.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	11.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $AV_{DD} = DV_{DD} = +2.7\text{ V}$  to  $+5.5\text{ V}$ ,  $IOV_{DD} = +1.8\text{ V}$  to  $+5.5\text{ V}$ , gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS		DAC8881			UNIT
			MIN	TYP	MAX	
ACCURACY						
Linearity error	Measured by line passing through codes 0200h and FE00h		±0.5	±1	LSB	
Differential linearity error	Measured by line passing through codes 0200h and FE00h		±0.25	±1	LSB	
Monotonicity			16		Bits	
Zero-scale error	T <sub>A</sub> = +25°C, code = 0200h			±4	LSB	
	T <sub>MIN</sub> to T <sub>MAX</sub> , code = 0200h			±8	LSB	
Zero-scale drift	Code = 0200h		±0.5	±1	ppm/°C of FSR	
Gain error	T <sub>A</sub> = +25°C, Measured by line passing through codes 0200h and FE00h		±4	±8	LSB	
Gain temperature drift	Measured by line passing through codes 0200h and FE00h		±0.5	±1	ppm/°C	
PSRR	V <sub>OUT</sub> = full-scale, AV <sub>DD</sub> = +5 V ±10%			2	LSB/V	
ANALOG OUTPUT <sup>(1)</sup>						
Voltage output <sup>(2)</sup>			0	AV <sub>DD</sub>	V	
Output voltage drift vs time	Device operating for 500 hours		5			ppm of FSR
	Device operating for 1000 hours		8			ppm of FSR
Output current			2.5			mA
Maximum load capacitance			200			pF
Short-circuit current			+31, -50			mA
REFERENCE INPUT <sup>(1)</sup>						
V <sub>REFH</sub> input voltage range	AV <sub>DD</sub> = +5.5 V		1.25	5.0	AV <sub>DD</sub>	V
	AV <sub>DD</sub> = +3 V		1.25	2.5	AV <sub>DD</sub>	V
V <sub>REFH</sub> input capacitance			5			pF
V <sub>REFH</sub> input impedance			4.5			kΩ
V <sub>REFL</sub> input voltage range			-0.2	0	+0.2	V
V <sub>REFL</sub> input capacitance			4.5			pF
V <sub>REFL</sub> input impedance			5			kΩ
DYNAMIC PERFORMANCE <sup>(1)</sup>						
Settling time	To ±0.003% FS, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF, code 1000h to F000h		5			μs
Slew rate	From 10% to 90% of 0 V to +5 V		2.5			V/μs
Code change glitch	Code = 7FFFh to 8000h to 7FFFh	V <sub>REFH</sub> = 5 V, gain = 1X mode	37			nV-s
		V <sub>REFH</sub> = 2.5 V, gain = 1X mode	18			nV-s
		V <sub>REFH</sub> = 1.25 V, gain = 1X mode	9			nV-s
		V <sub>REFH</sub> = 2.5 V, gain = 2X mode	21			nV-s
		V <sub>REFH</sub> = 1.25 V, gain = 2X mode	10			nV-s
Digital feedthrough			1			nV-s
Output noise voltage density	f = 1 kHz to 100 kHz, full-scale output	Gain = 1	24	30	nV/√Hz	
		Gain = 2	40	48	nV/√Hz	
Output noise voltage	f = 0.1Hz to 10Hz, full-scale output		2			μV <sub>PP</sub>

(1) Specified by design. Not production tested.

(2) The output from the  $V_{OUT}$  pin =  $[(V_{REFH} - V_{REFL})/65536] \times \text{CODE} \times \text{Buffer GAIN} + V_{REFL}$ . The maximum range of  $V_{OUT}$  is 0 V to  $AV_{DD}$ . The full-scale of the output must be less than  $AV_{DD}$ ; otherwise, output saturation occurs.

**DAC8881**

ZHCSHA4B – JULY 2007 – REVISED JANUARY 2018

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**Electrical Characteristics (continued)**

All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $AV_{DD} = DV_{DD} = +2.7\text{ V}$  to  $+5.5\text{ V}$ ,  $IOV_{DD} = +1.8\text{ V}$  to  $+5.5\text{ V}$ , gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8881			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS <sup>(1)</sup>					
High-level input voltage, V <sub>IH</sub>	IOV <sub>DD</sub> = 4.5 V to 5.5 V	3.8	IOV <sub>DD</sub> + 0.3	V	
	IOV <sub>DD</sub> = 2.7 V to 3.3 V	2.1	IOV <sub>DD</sub> + 0.3	V	
	IOV <sub>DD</sub> = 1.7 V to 2 V	1.5	IOV <sub>DD</sub> + 0.3	V	
Low-level input voltage, V <sub>IL</sub>	IOV <sub>DD</sub> = 4.5 V to 5.5 V	−0.3	0.8	V	
	IOV <sub>DD</sub> = 2.7 V to 3.3 V	−0.3	0.6	V	
	IOV <sub>DD</sub> = 1.7 V to 2 V	−0.3	0.3	V	
Digital input current (I <sub>IN</sub> )		±1	±10	μA	
Digital input capacitance		5		pF	
DIGITAL OUTPUT <sup>(1)</sup>					
High-level output voltage, V <sub>OH</sub>	IOV <sub>DD</sub> = 2.7 V to 5.5 V, I <sub>OH</sub> = −1 mA	IOV <sub>DD</sub> − 0.2		V	
	IOV <sub>DD</sub> = 1.7 V to 2 V, I <sub>OH</sub> = −500 μA	IOV <sub>DD</sub> − 0.2		V	
Low-level output voltage, V <sub>OL</sub>	IOV <sub>DD</sub> = 2.7 V to 5.5 V, I <sub>OL</sub> = 1 mA	0.2		V	
	IOV <sub>DD</sub> = 1.7 V to 2 V, I <sub>OL</sub> = 500 μA	0.2		V	
POWER SUPPLY					
AV <sub>DD</sub>		+2.7	+5.5	V	
DV <sub>DD</sub>		+2.7	+5.5	V	
IOV <sub>DD</sub>		+1.7	DV <sub>DD</sub>	V	
AI <sub>DD</sub>	V <sub>IH</sub> = IOV <sub>DD</sub> , V <sub>IL</sub> = DGND		1.5	mA	
DI <sub>DD</sub>	V <sub>IH</sub> = IOV <sub>DD</sub> , V <sub>IL</sub> = DGND	1	10	μA	
IOI <sub>DD</sub>	V <sub>IH</sub> = IOV <sub>DD</sub> , V <sub>IL</sub> = DGND	1	10	μA	
AI <sub>DD</sub> power-down	PDN = IOV <sub>DD</sub>	25	50	μA	
Power dissipation	AV <sub>DD</sub> = DV <sub>DD</sub> = 5.0V	6	7.5	mW	
TEMPERATURE RANGE					
Specified performance		−40	+105	°C	

## 6.6 Timing Characteristics for Figure 1 (1) (2) (3)

At –40°C to +105°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f <sub>SCLK</sub>	Maximum clock frequency	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		40	MHz
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		50	MHz
t <sub>1</sub>	Minumum $\overline{\text{CS}}$ high time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	50		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	30		ns
t <sub>2</sub>	$\overline{\text{CS}}$ falling edge to SCLK rising edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	8		ns
t <sub>3</sub>	SCLK falling edge to $\overline{\text{CS}}$ falling edge setup time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
t <sub>4</sub>	SCLK low time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
t <sub>5</sub>	SCLK high time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	15		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
t <sub>6</sub>	SCLK cycle time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	25		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	20		ns
t <sub>7</sub>	SCLK rising edge to $\overline{\text{CS}}$ rising edge	2.7 ≤ DV <sub>DD</sub> < 3.6V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
t <sub>8</sub>	Input data setup time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	8		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
t <sub>9</sub>	Input data hold time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
t <sub>14</sub>	$\overline{\text{CS}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
t <sub>15</sub>	$\overline{\text{LDAC}}$ pulse width	2.7 ≤ DV <sub>DD</sub> < 3.6V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	15		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns

- (1) All input signals are specified with t<sub>R</sub> = t<sub>F</sub> = 2ns (10% to 90% of IOV<sub>DD</sub>) and timed from a voltage level of IOV<sub>DD</sub>/2.
- (2) Specified by design. Not production tested.
- (3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

## 6.7 Timing Characteristics for Figure 2 and Figure 3 <sup>(1) (2) (3)</sup>

At –40°C to +105°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f <sub>SCLK</sub>	Maximum clock frequency	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		20	MHz
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		25	MHz
t <sub>1</sub>	Minimum $\overline{\text{CS}}$ high time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	50		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	30		ns
t <sub>2</sub>	$\overline{\text{CS}}$ falling edge to SCLK rising edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	8		ns
t <sub>3</sub>	SCLK falling edge to $\overline{\text{CS}}$ falling edge setup time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
t <sub>4</sub>	SCLK low time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	25		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	20		ns
t <sub>5</sub>	SCLK high time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	25		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	20		ns
t <sub>6</sub>	SCLK cycle time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	50		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	40		ns
t <sub>7</sub>	SCLK rising edge to $\overline{\text{CS}}$ rising edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
t <sub>8</sub>	Input data setup time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
t <sub>9</sub>	Input data hold time	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
t <sub>10</sub>	SDO active from $\overline{\text{CS}}$ falling edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		15	ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		10	ns
t <sub>11</sub>	SDO data valid from SCLK falling edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		20	ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		15	ns
t <sub>12</sub>	SDO data hold from SCLK rising edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	25		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	20		ns
t <sub>13</sub>	SDO High-Z from $\overline{\text{CS}}$ rising edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		8	ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>		5	ns
t <sub>14</sub>	$\overline{\text{CS}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	5		ns
t <sub>15</sub>	$\overline{\text{LDAC}}$ pulse width	2.7 ≤ DV <sub>DD</sub> < 3.6 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	15		ns
		3.6 ≤ DV <sub>DD</sub> ≤ 5.5 V, 2.7 ≤ IOV <sub>DD</sub> ≤ DV <sub>DD</sub>	10		ns

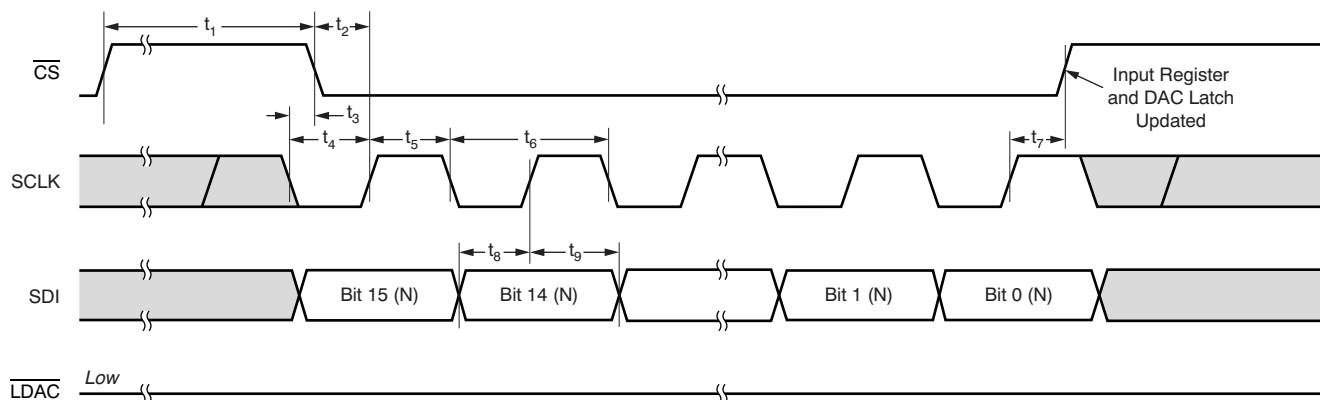
(1) All input signals are specified with t<sub>R</sub> = t<sub>F</sub> = 2ns (10% to 90% of IOV<sub>DD</sub>) and timed from a voltage level of IOV<sub>DD</sub>/2.

(2) Specified by design. Not production tested.

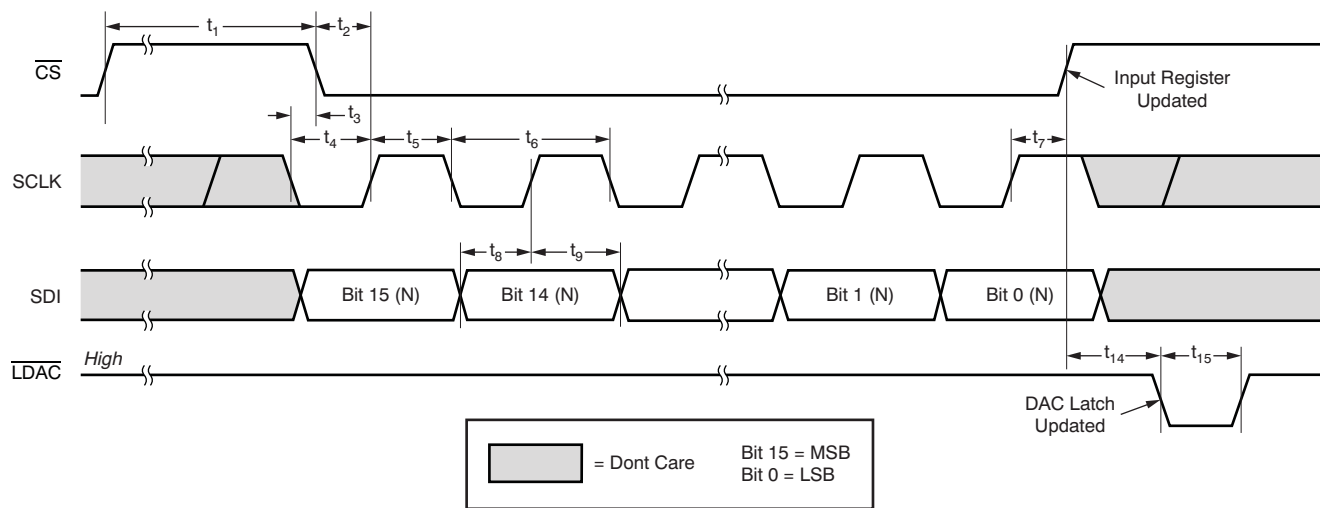
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.



Case 1: Standalone operation without SDO,  $\overline{\text{LDAC}}$  tied low.



Case 2: Standalone operation without SDO,  $\overline{\text{LDAC}}$  active.

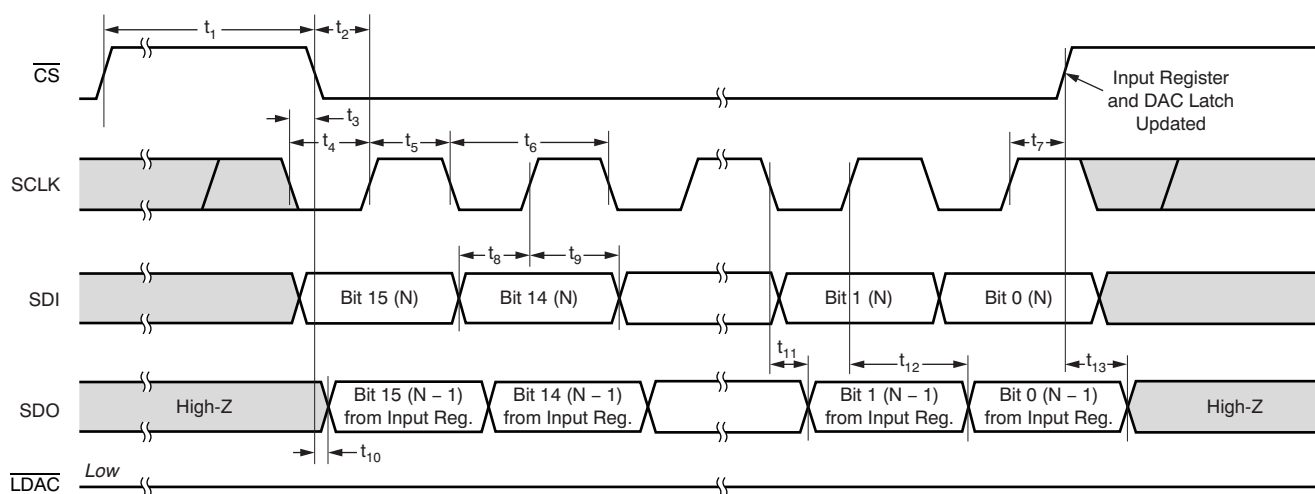
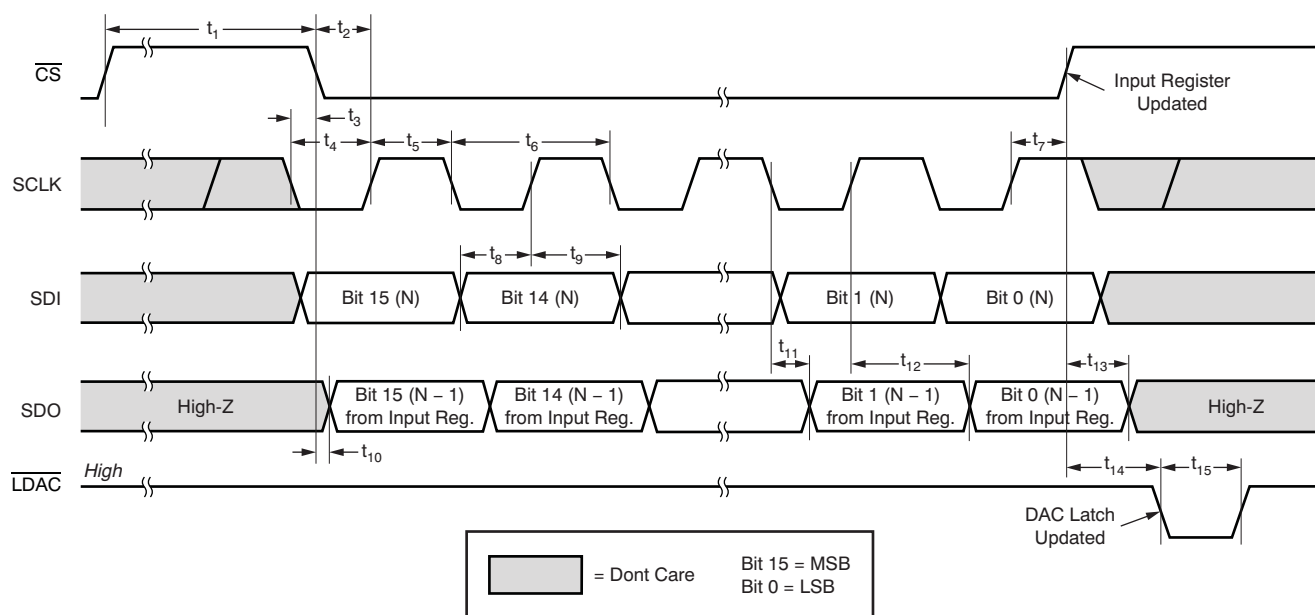


**Figure 1. Timing Diagram of Standalone Operation Without SDO**

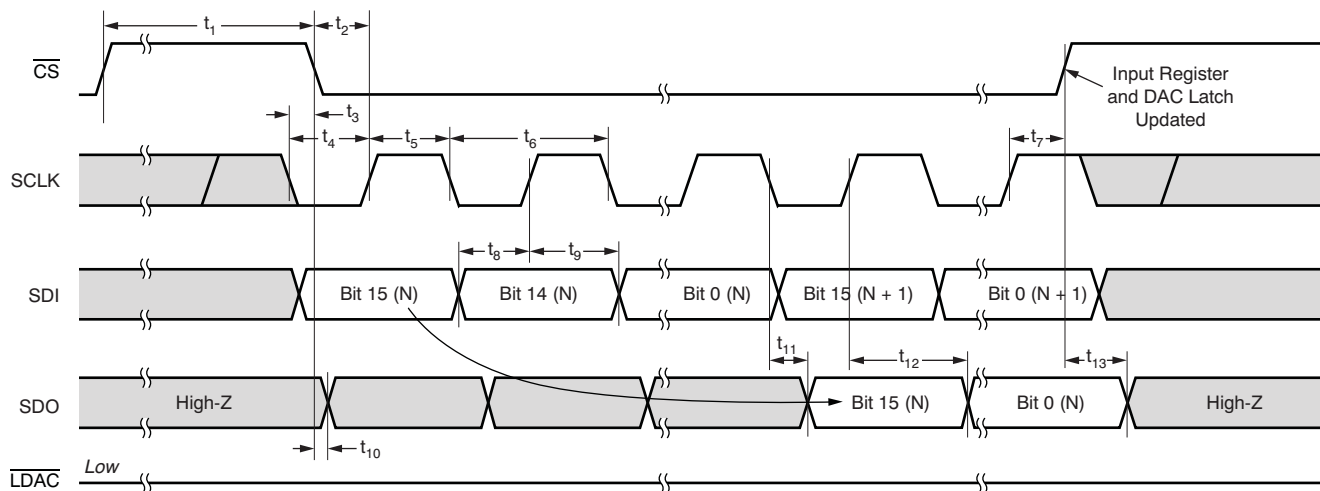
**DAC8881**

ZHCSHA4B – JULY 2007 – REVISED JANUARY 2018

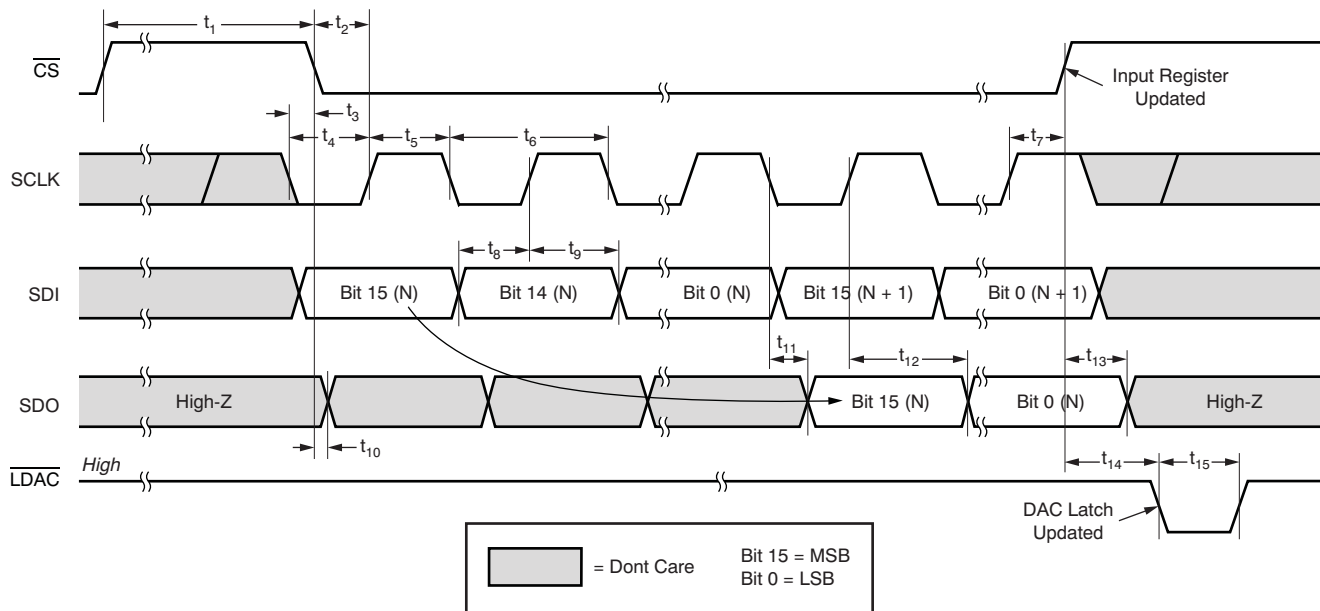
[www.ti.com.cn](http://www.ti.com.cn)

 Case 1: Standalone operation with output from SDO,  $\overline{\text{LDAC}}$  tied low.

 Case 2: Standalone operation with output from SDO,  $\overline{\text{LDAC}}$  active.

**Figure 2. Timing Diagram of Standalone Operation With SDO**

Case 1: Daisy Chain,  $\overline{\text{LDAC}}$  tied low.



Case 2: Daisy Chain,  $\overline{\text{LDAC}}$  active.



**Figure 3. Timing Diagram of Daisy Chain Mode, Two Cascaded Devices**

## 6.8 Typical Characteristics: $V_{DD} = +5\text{ V}$

At  $T_A = +25^\circ\text{C}$ ,  $V_{REFH} = +5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , and Gain = 1X Mode, unless otherwise noted.

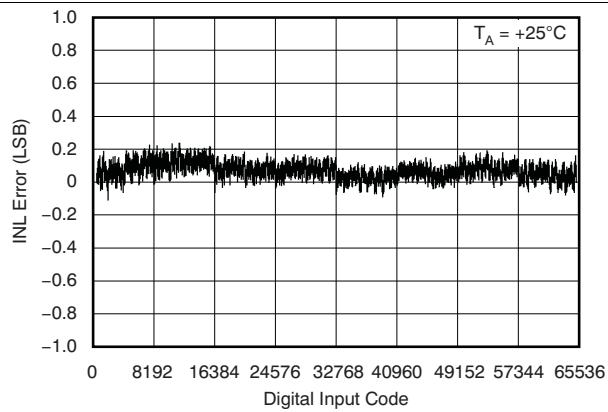


Figure 4. Linearity Error vs Digital Input Code

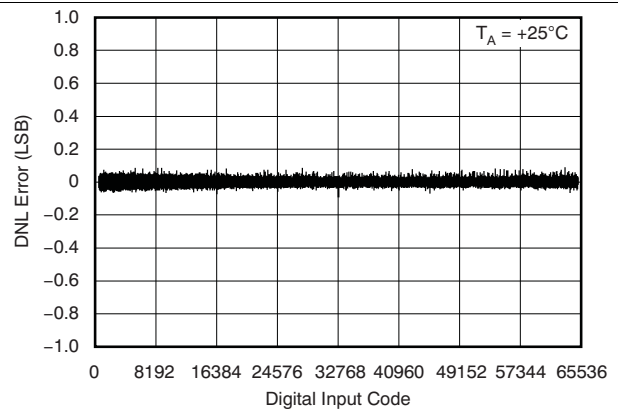


Figure 5. Differential Linearity Error vs Digital Input Code

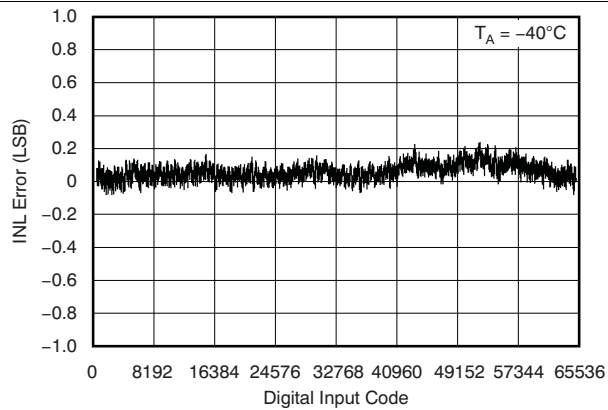


Figure 6. Linearity Error vs Digital Input Code

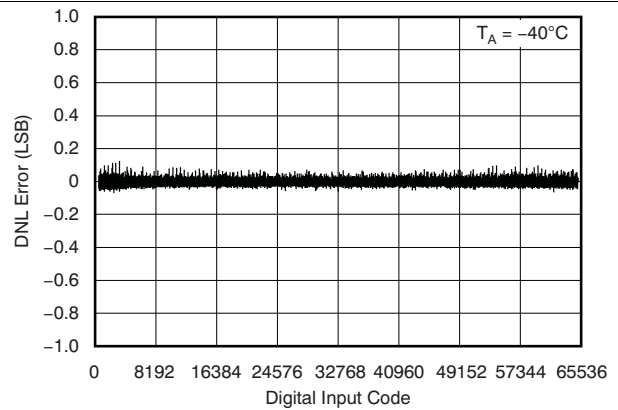


Figure 7. Differential Linearity Error vs Digital Input Code

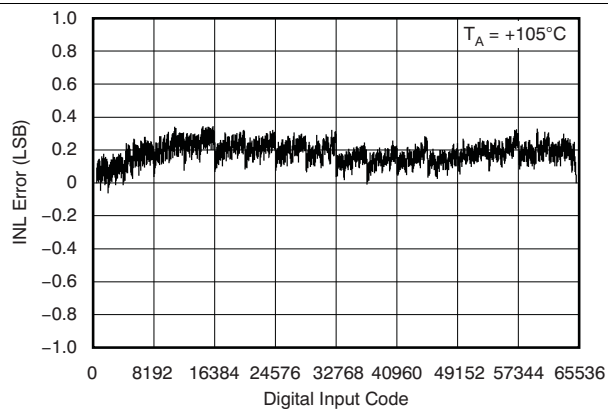


Figure 8. Linearity Error vs Digital Input Code

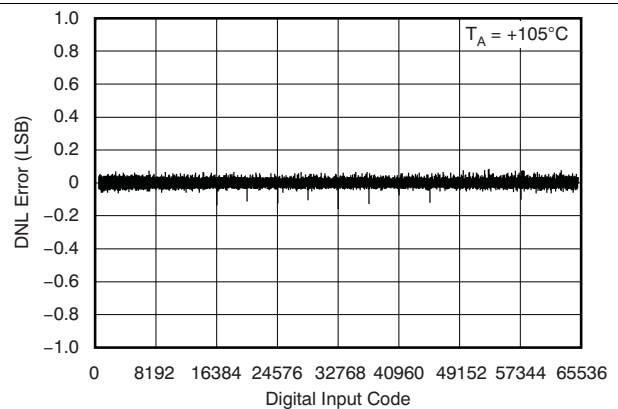
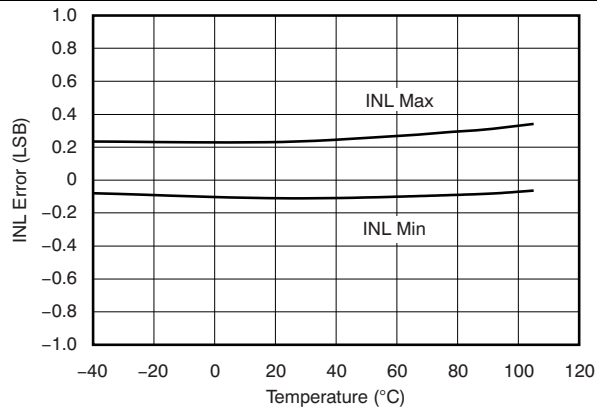
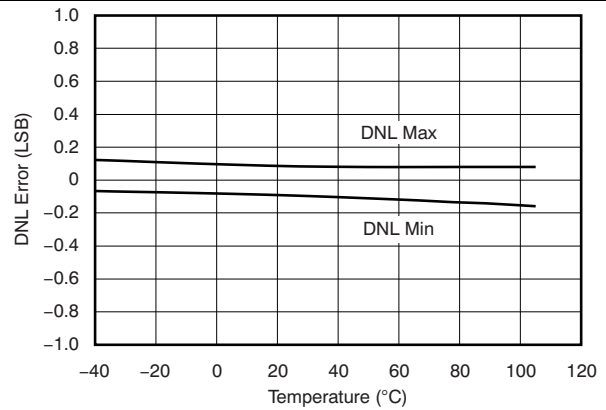


Figure 9. Differential Linearity Error vs Digital Input Code

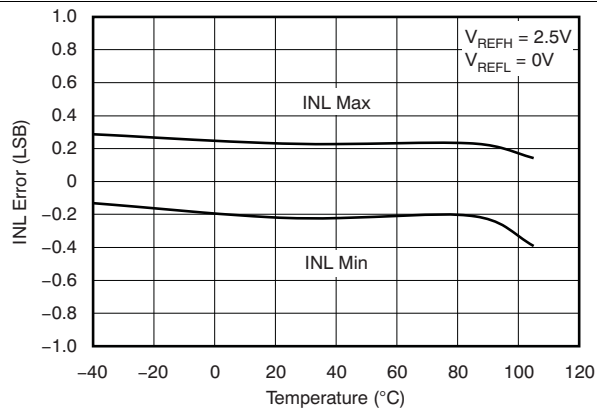
**Typical Characteristics:  $V_{DD} = +5\text{ V}$  (continued)**



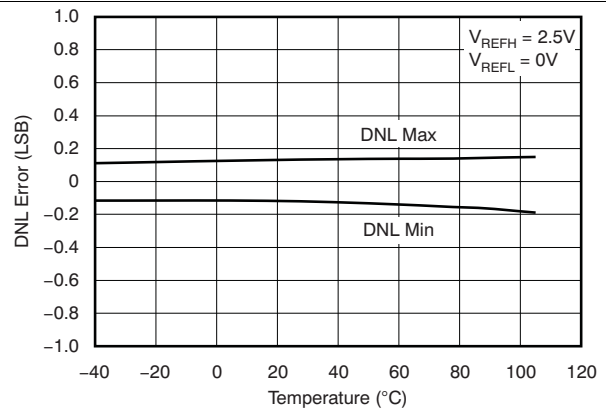
**Figure 10. Linearity Error vs Temperature**



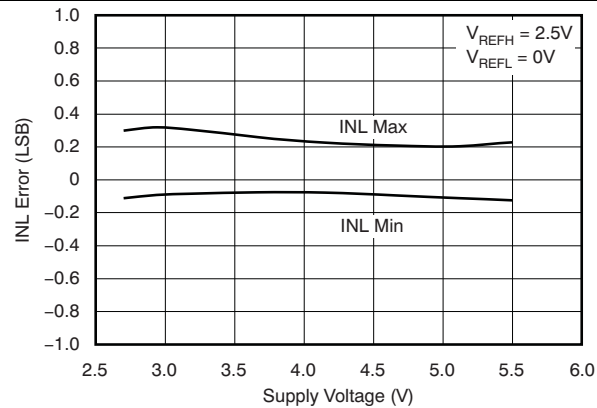
**Figure 11. Differential Linearity Error vs Temperature**



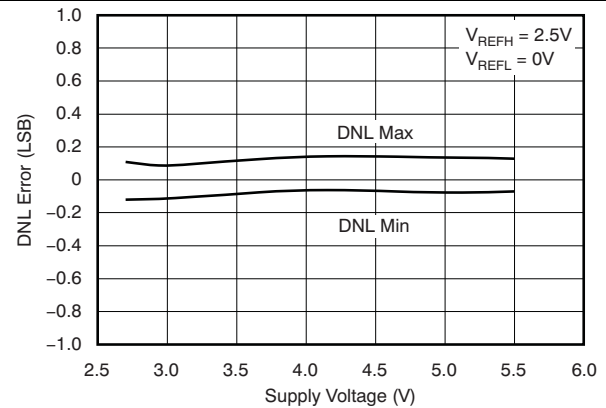
**Figure 12. Linearity Error vs Temperature  
(Gain = 2X Mode)**



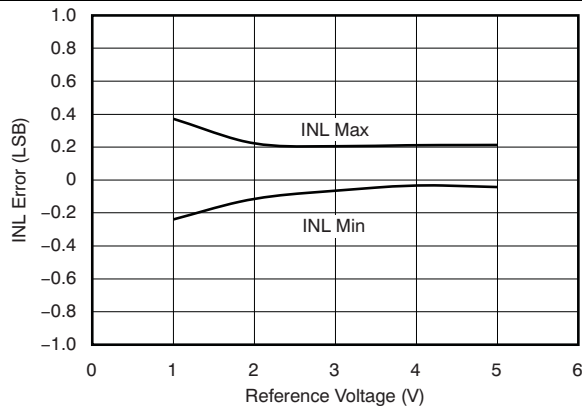
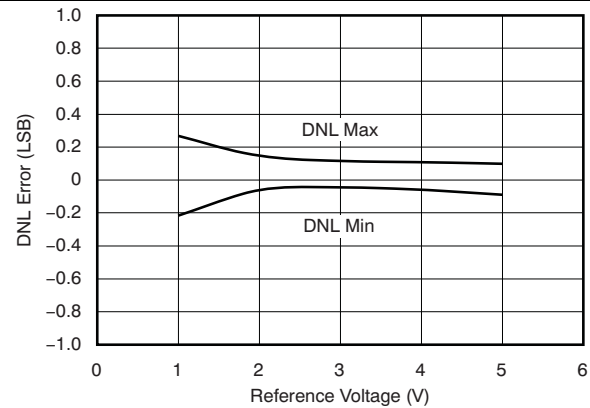
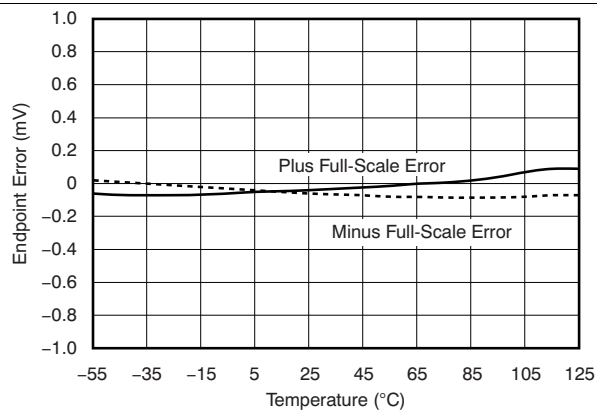
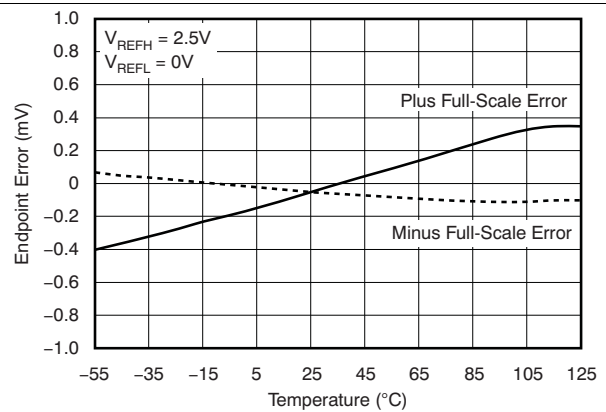
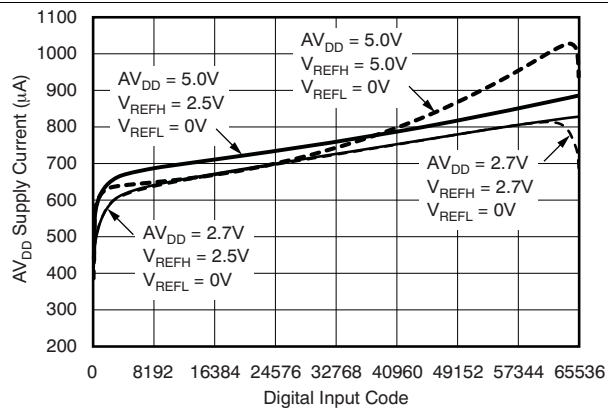
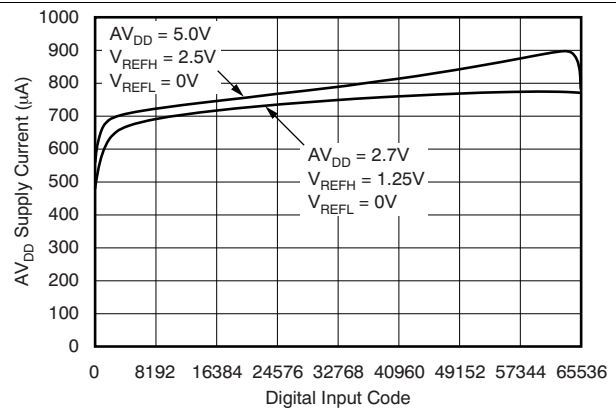
**Figure 13. Differential Linearity Error vs Temperature  
(Gain = 2X Mode)**



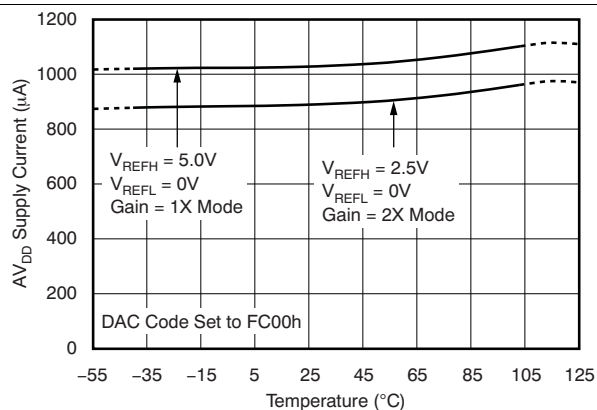
**Figure 14. Linearity Error vs Supply Voltage**



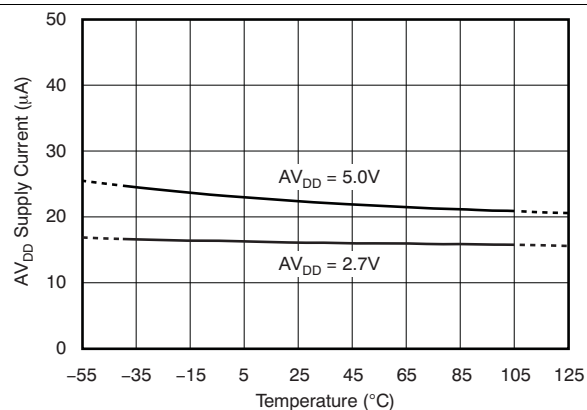
**Figure 15. Differential Linearity Error vs Supply Voltage**

**Typical Characteristics:  $V_{DD} = +5\text{ V}$  (continued)**

**Figure 16. Linearity Error vs Reference Voltage**

**Figure 17. Differential Linearity Error vs Reference Voltage**

**Figure 18. Endpoint Error vs Temperature**

**Figure 19. Endpoint Error vs Temperature  
(Gain = 2X Mode)**

**Figure 20.  $AV_{DD}$  Supply Current vs Digital Input Code**

**Figure 21.  $AV_{DD}$  Supply Current vs Digital Input Code  
(Gain = 2X Mode)**

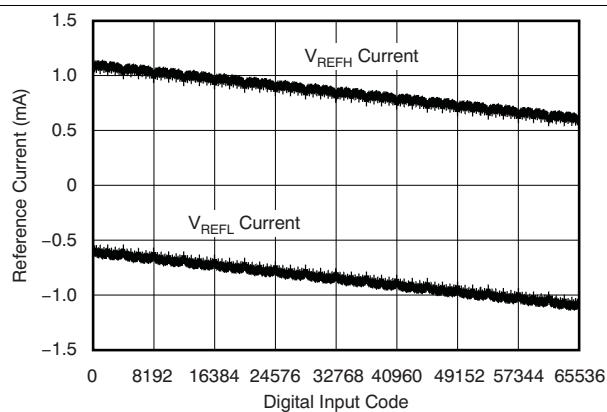
**Typical Characteristics:  $V_{DD} = +5\text{ V}$  (continued)**



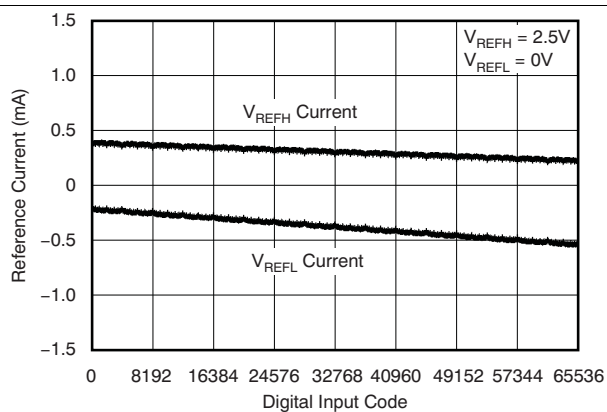
**Figure 22.  $AV_{DD}$  Supply Current vs Temperature**



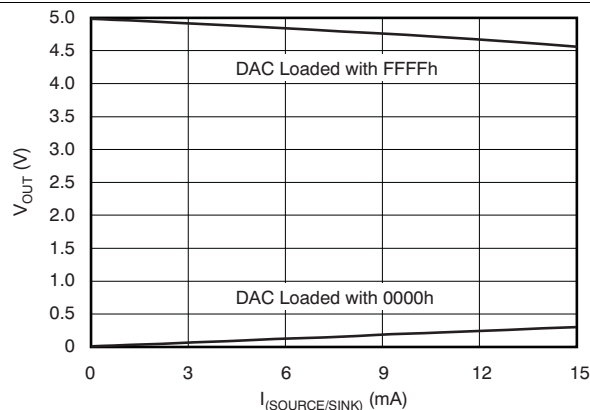
**Figure 23.  $AV_{DD}$  Power-Down Current vs Temperature**



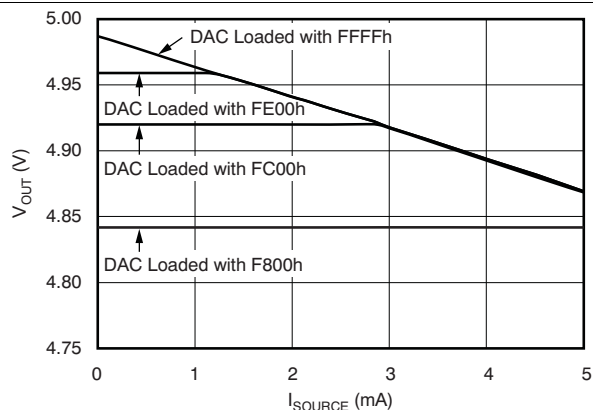
**Figure 24. Reference Current vs Digital Input Code**



**Figure 25. Reference Current vs Digital Input Code  
(Gain = 2X Mode)**

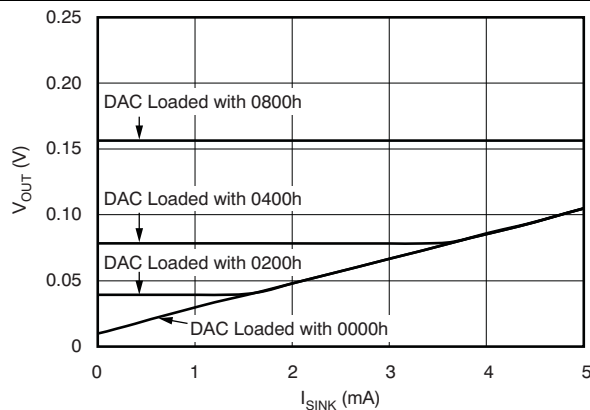


**Figure 26. Output Voltage vs Drive Current Capability**

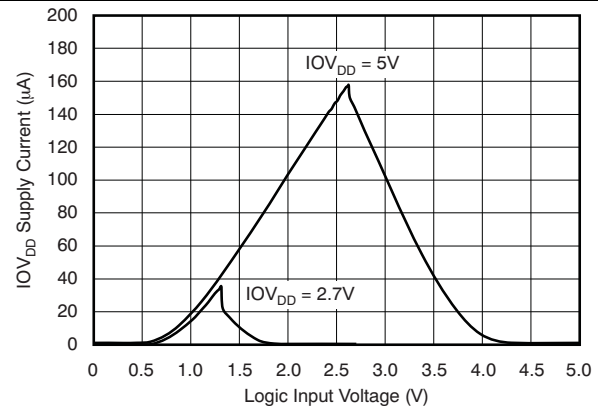


**Figure 27. Output Voltage vs Drive Current Capability  
(Operation Near  $AV_{DD}$  Rail)**

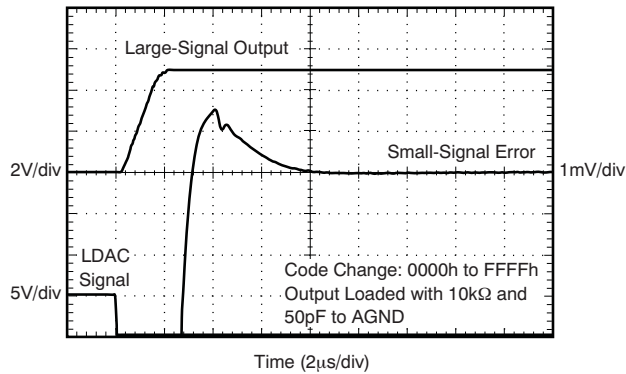
## Typical Characteristics: $V_{DD} = +5\text{ V}$ (continued)



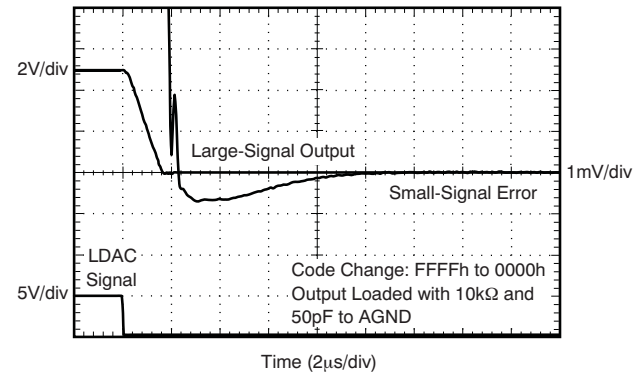
**Figure 28. Output Voltage vs Drive Current Capability (Operation Near AGND Rail)**



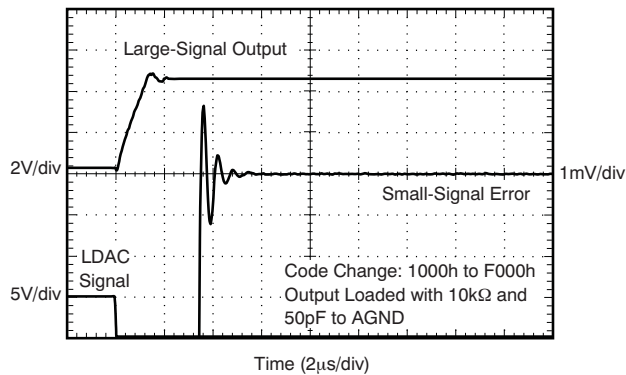
**Figure 29. IOV<sub>DD</sub> Supply Current vs Logic Input Voltage**



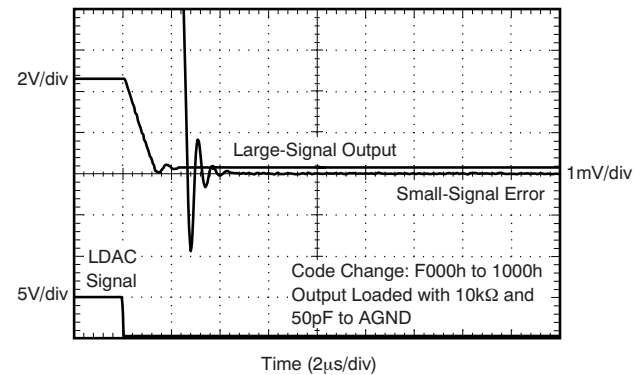
**Figure 30. Large Signal Settling Time**



**Figure 31. Large Signal Settling Time**



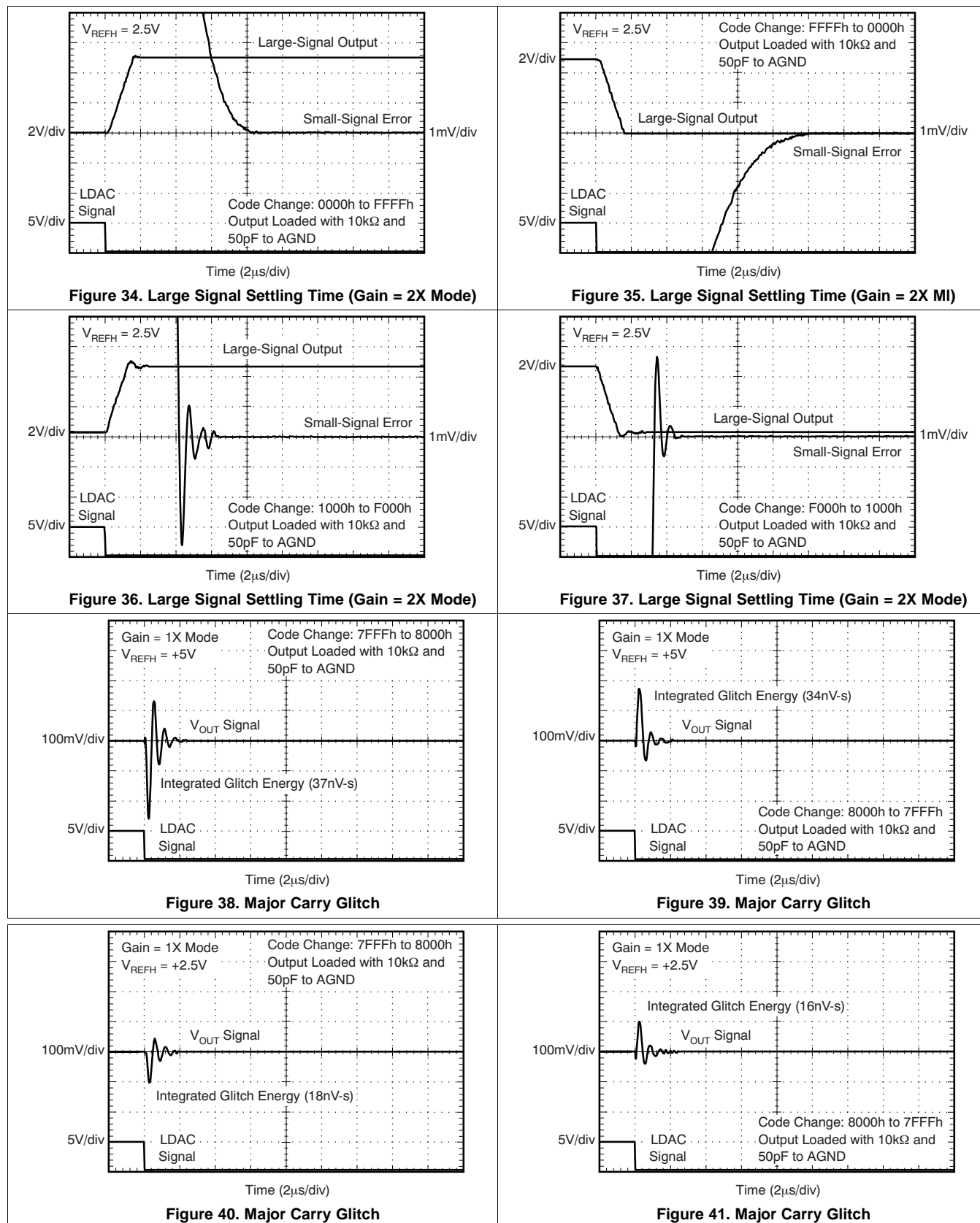
**Figure 32. Large Signal Settling Time**



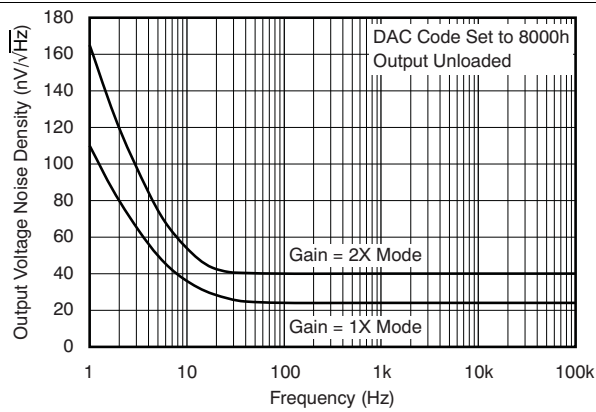
**Figure 33. Large Signal Settling Time**



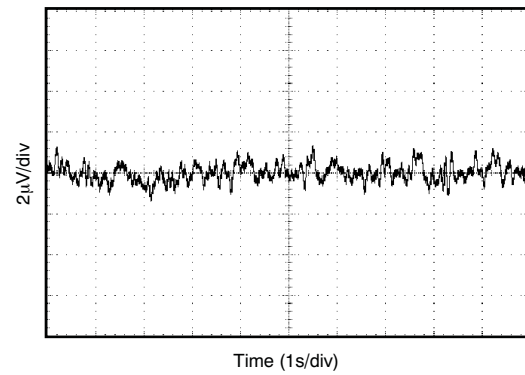
**Typical Characteristics:  $V_{DD} = +5\text{ V}$  (continued)**



**Typical Characteristics:  $V_{DD} = +5\text{ V}$  (continued)**



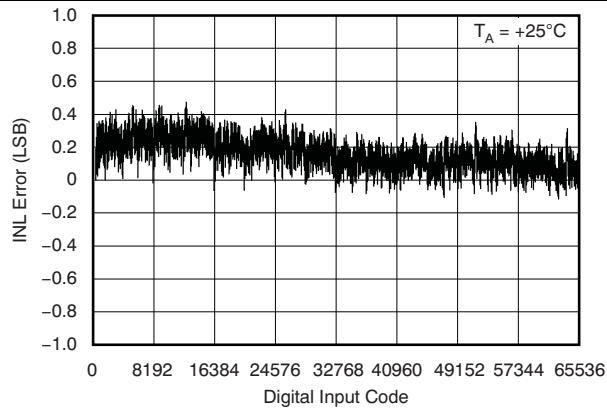
**Figure 42. Output Noise Density vs Frequency**



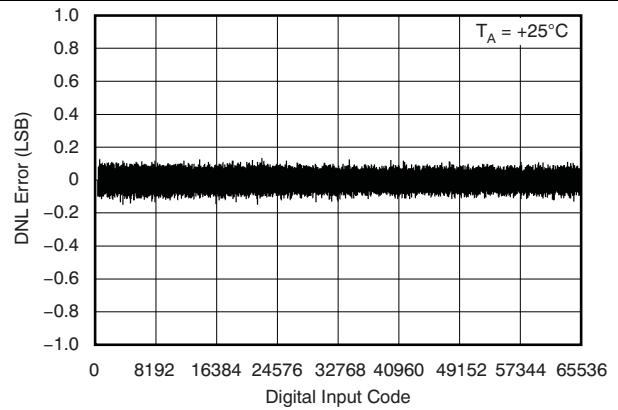
**Figure 43. Low-Frequency Output Noise (0.1Hz to 10Hz)**

## 6.9 Typical Characteristics: $V_{DD} = +2.7\text{ V}$

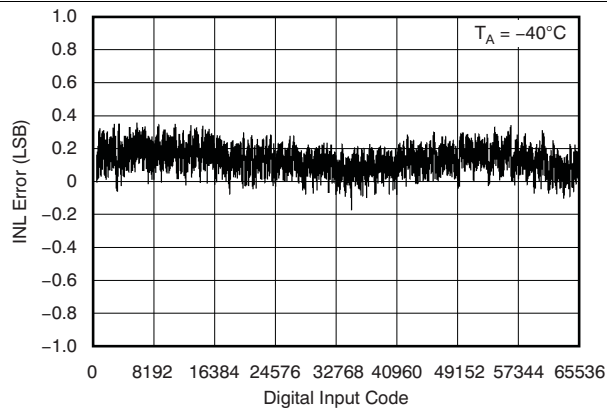
At  $T_A = +25^\circ\text{C}$ ,  $V_{REFH} = +2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , and Gain = 1X Mode, unless otherwise noted.



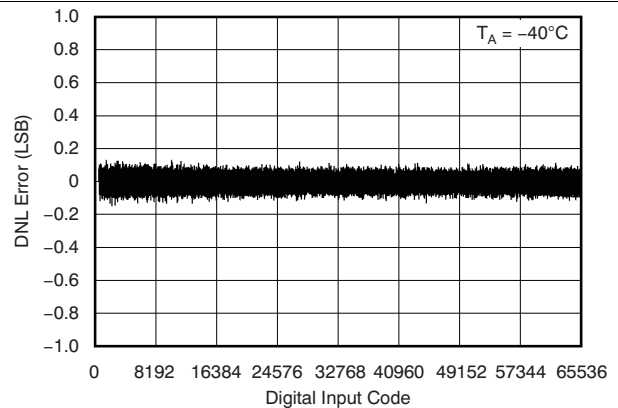
**Figure 44. Linearity Error vs Digital Input Code**



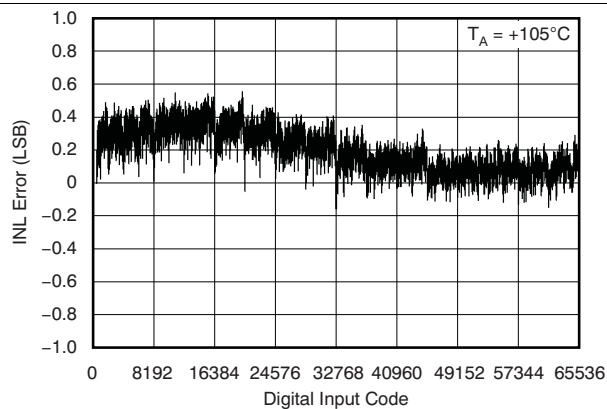
**Figure 45. Differential Linearity Error vs Digital Input Code**



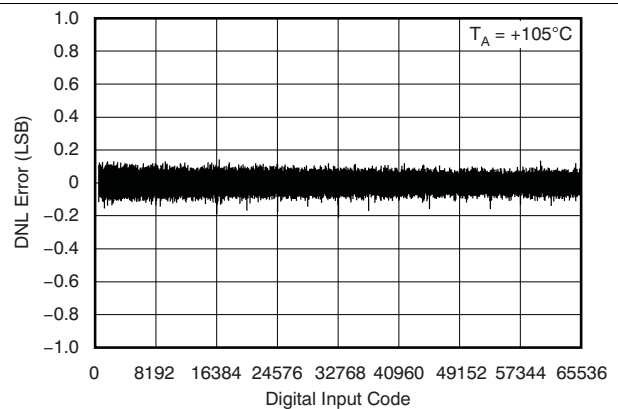
**Figure 46. Linearity Error vs Digital Input Code**



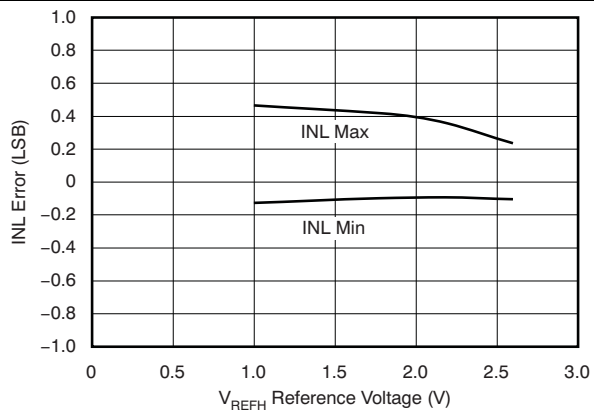
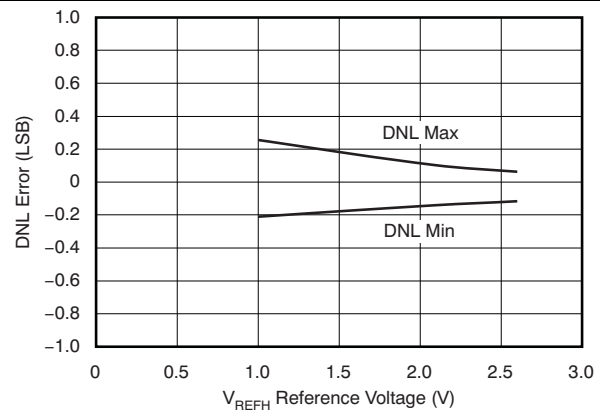
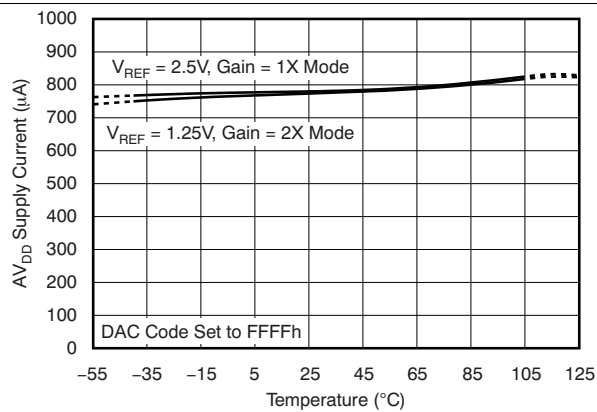
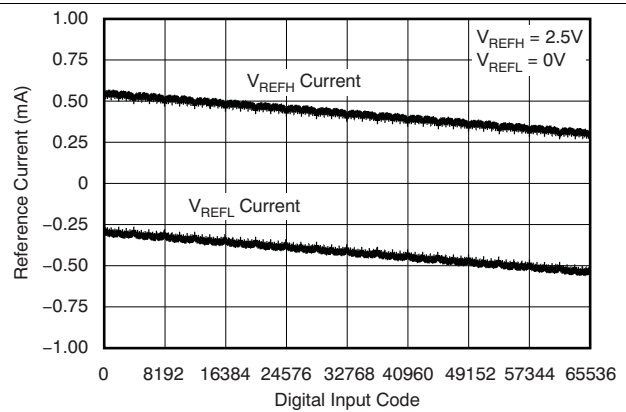
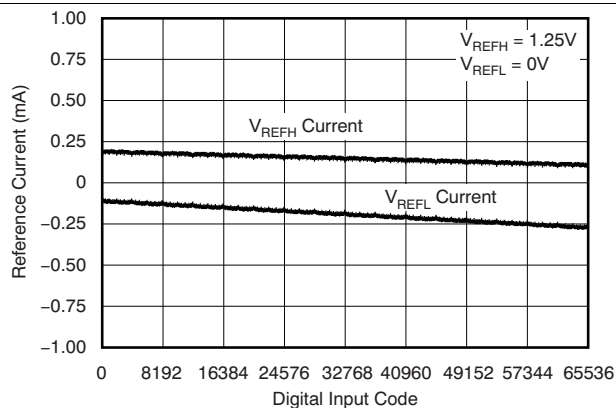
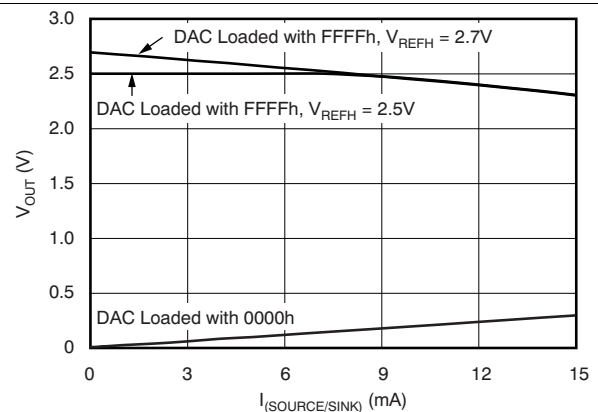
**Figure 47. Differential Linearity Error vs Digital Input Code**



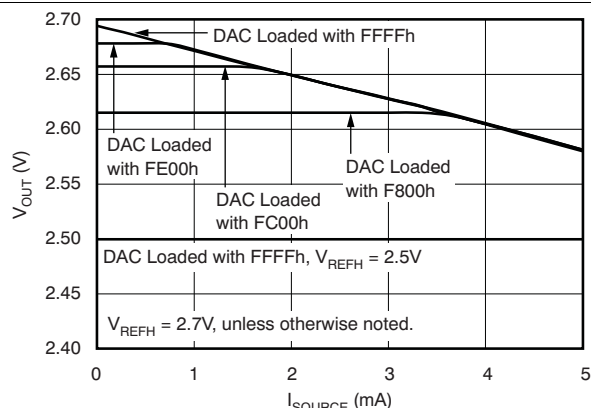
**Figure 48. Linearity Error vs Digital Input Code**



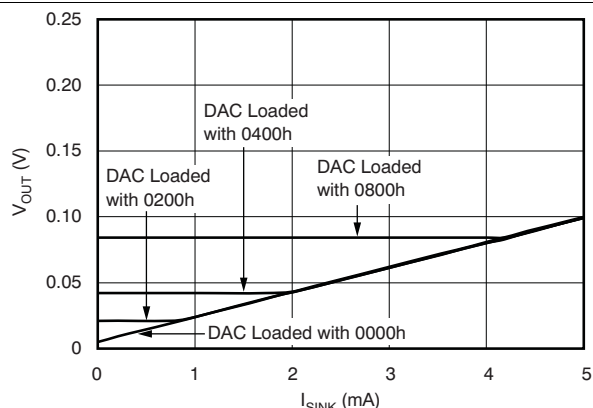
**Figure 49. Differential Linearity Error vs Digital Input Code**

**Typical Characteristics:  $V_{DD} = +2.7\text{ V}$  (continued)**

**Figure 50. Linearity Error vs**

**Figure 51. Differential Linearity Error vs Reference Voltage**

**Figure 52.  $AV_{DD}$  Supply Current vs Temperature**

**Figure 53. Reference Current vs Digital Input Code**

**Figure 54. Reference Current vs Digital Input Code  
(Gain = 2X Mode)**

**Figure 55. Output Voltage vs Drive Current Capability**

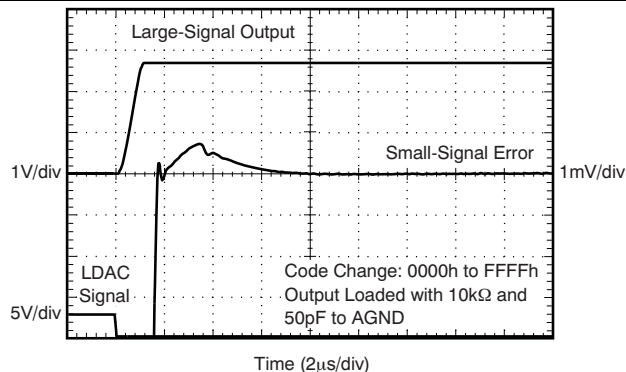
**Typical Characteristics:  $V_{DD} = +2.7\text{ V}$  (continued)**



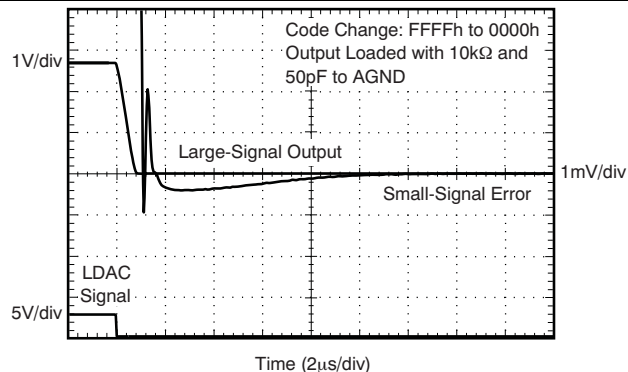
**Figure 56. Output Voltage vs Drive Current Capability (Operation Near  $AV_{DD}$  Rail)**



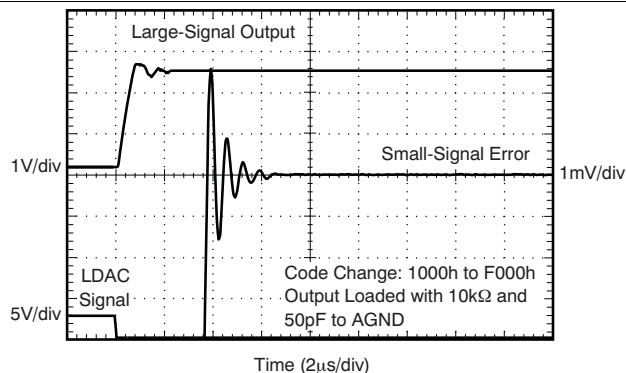
**Figure 57. Output Voltage vs Drive Current Capability (Operation Near  $AGND$  Rail)**



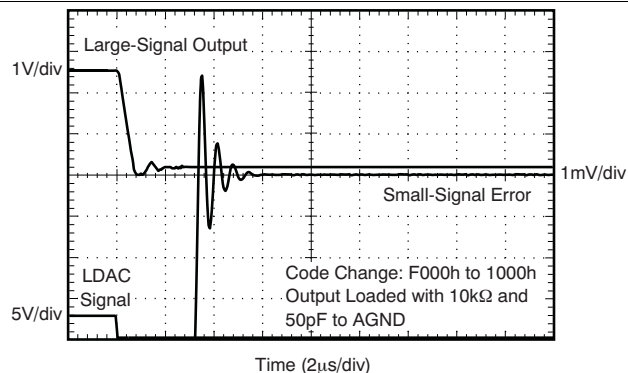
**Figure 58. Large Signal Settling Time**



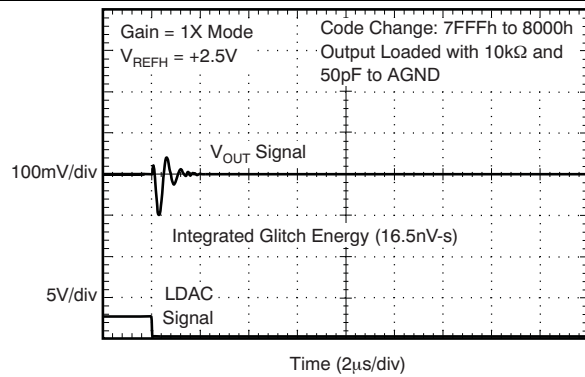
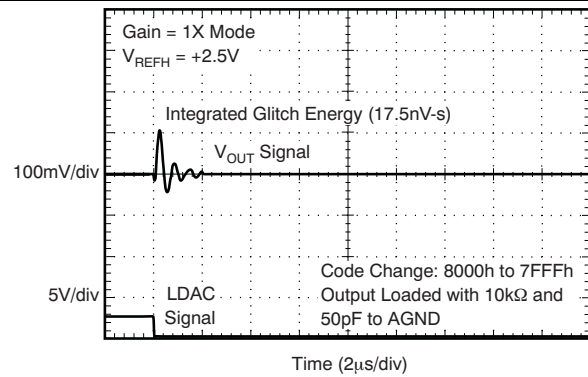
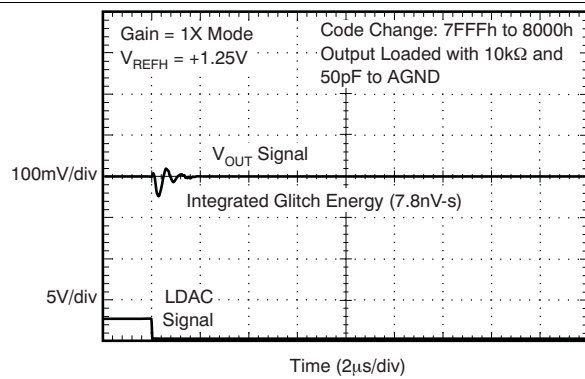
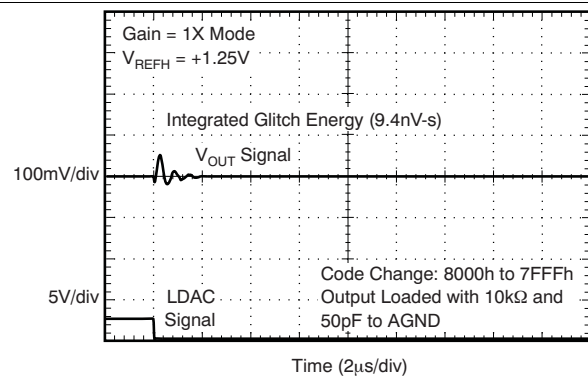
**Figure 59. Large Signal Settling Time**



**Figure 60. Large Signal Settling Time**



**Figure 61. Large Signal Settling Time**

**Typical Characteristics:  $V_{DD} = +2.7\text{ V}$  (continued)**

**Figure 62. Major Carry Glitch**

**Figure 63. Major Carry Glitch**

**Figure 64. Major Carry Glitch**

**Figure 65. Major Carry Glitch**

## 7 Detailed Description

### 7.1 Overview

The DAC8881 is a single-channel, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the four MSBs segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 66. The on-chip output buffer allows rail-to-rail output swings while providing a low output impedance to drive loads. The DAC8881 operates from a single analog power supply that ranges from 2.7 V to 5.5 V, and typically consumes 850  $\mu$ A when operating with a 3-V supply. Data are written to the device in a 16-bit word format, via an SPI serial interface. To enable compatibility with 1.8 V, 3 V, or 5 V logic families, an IOV<sub>DD</sub> supply pin is provided. This pin allows the DAC8881 input and output logic to be powered from the same logic supply used to interface signals to and from the device. Internal voltage translators are included in the DAC8881 to interface digital signals to the device core. Separate AV<sub>DD</sub> and DV<sub>DD</sub> supply pins are provided, but should be connected together. See Figure 67 for the basic configuration of the DAC8881.

To ensure a known power-up state, the DAC8881 is designed with a power-on reset function. Upon power-up, the DAC8881 is reset to either zero-scale or midscale depending on the state of the RSTSEL pin. The device can also be hardware reset by using the  $\overline{\text{RST}}$  and RSTSEL pins.

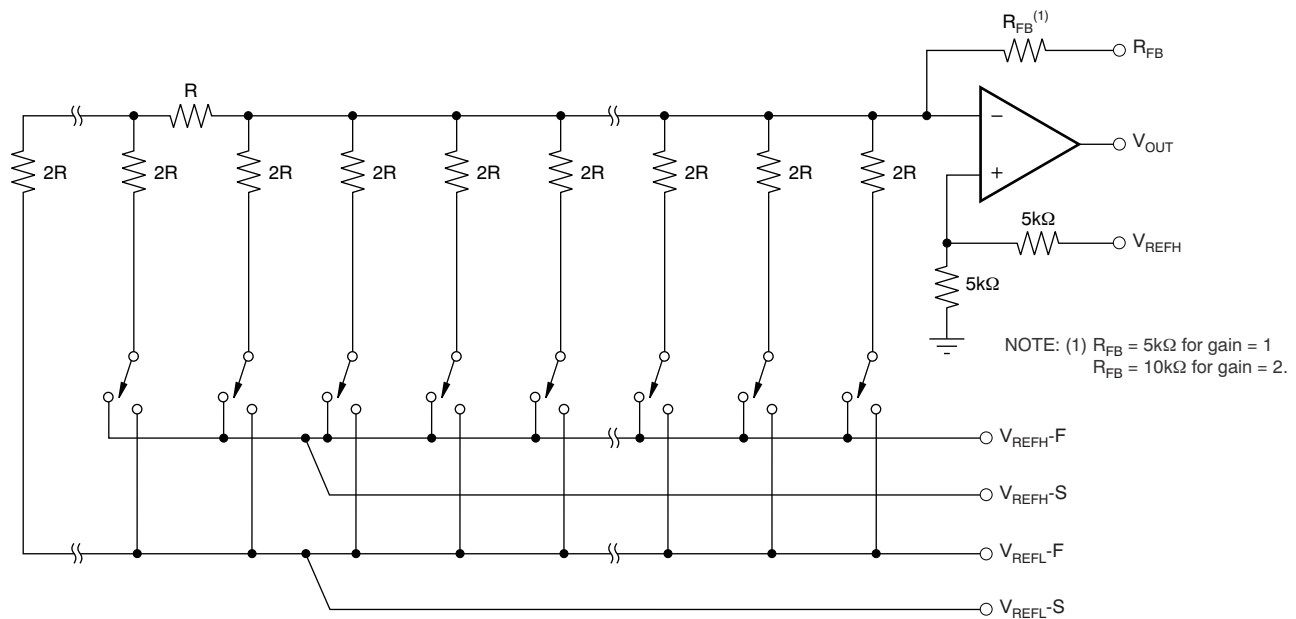


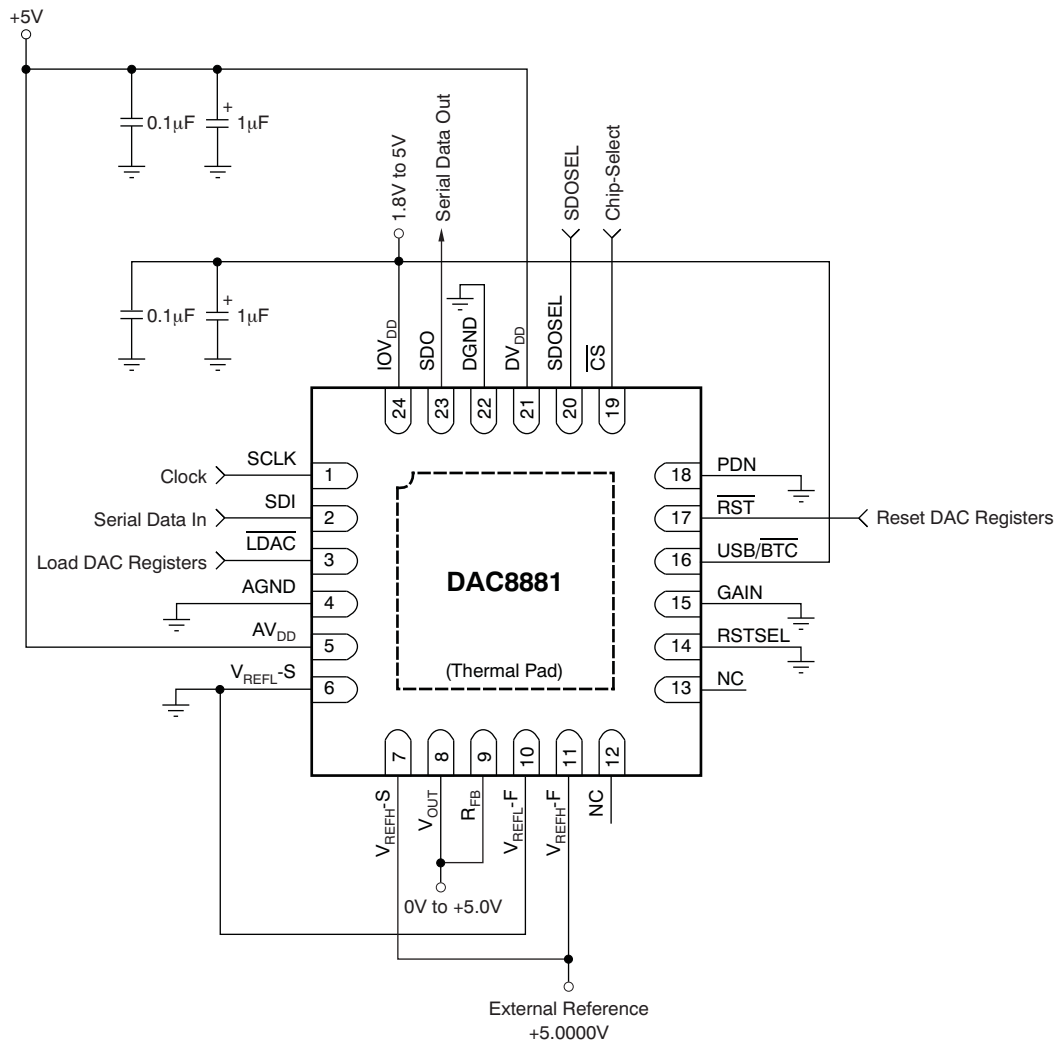
Figure 66. DAC8881 Architecture

## DAC8881

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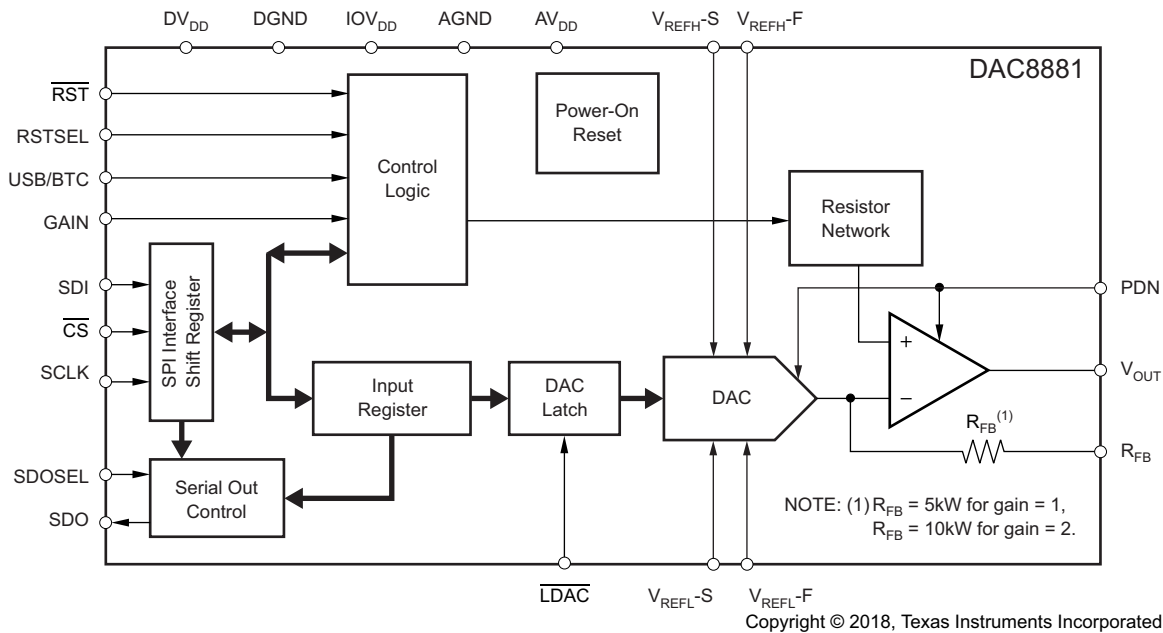
### Overview (continued)



**Figure 67. Basic Configuration**



## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Analog Output

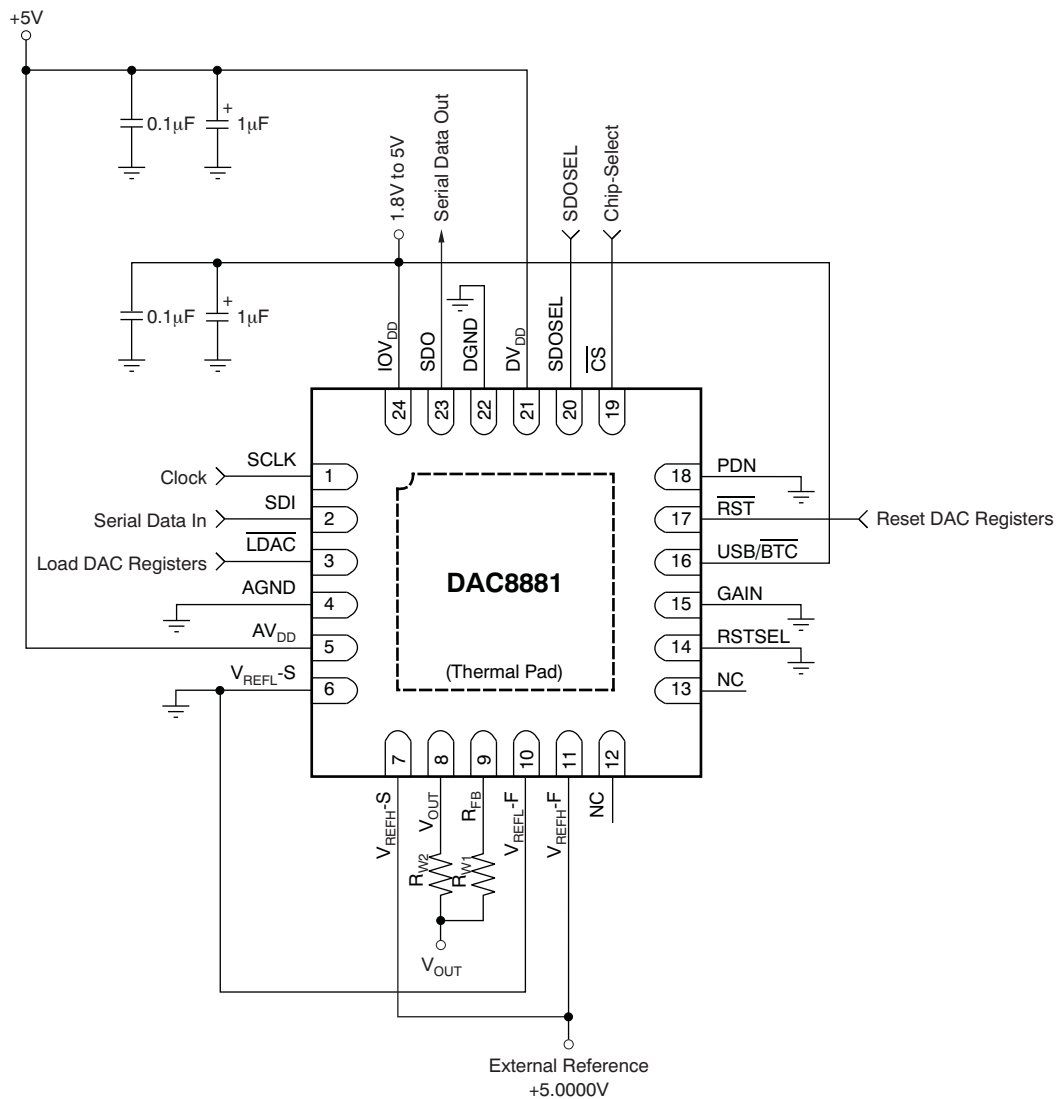
The DAC8881 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in [Figure 68](#)), thus ensuring an accurate output voltage. The output buffer V<sub>OUT</sub> and R<sub>FB</sub> pins are provided so that the output op amp buffer feedback can be connected at the load. Without a driven load, the DAC8881 output typically swings to within 15mV of the AGND and AV<sub>DD</sub> supply rails. Because of the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 5 V full-scale range has a 1 LSB value of 76 μV. With a load current of 1 mA, a series wiring and connector resistance of only 80mΩ (R<sub>W2</sub>) causes a voltage drop of 80 μV. In terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 0.5mΩ per square. For a 1mA load, a 0.25 mm wide printed circuit conductor 25 mm long results in a voltage drop of 50 μV.

## DAC8881

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### Feature Description (continued)



**Figure 68. Analog Output Closed-Loop Configuration**  
( $R_{W1}$  and  $R_{W2}$  represent wiring resistance)

## Feature Description (continued)

### 7.3.2 Reference Inputs

The reference high input,  $V_{REFH}$ , can be set to any voltage in the range of 1.25 V to  $AV_{DD}$ . The reference low input,  $V_{REFL}$ , can be set to any voltage in the range of  $-0.2$  V to  $+0.2$  V (to provide a small offset to the output of the DAC8881, if desired). The current into  $V_{REFH}$  and out of  $V_{REFL}$  depends on the DAC code, and can vary from approximately 0.5mA to 1mA in the gain = 1X mode of operation. The reference high and low inputs appear as varying loads to the external reference circuit. If the external references can source or sink the required current, and if low impedance connections are made to the  $V_{REFH}$  and  $V_{REFL}$  pins, external reference buffers are not required. Figure 67 shows a simple configuration of the DAC8881 using external references without force/sense reference buffers.

Kelvin sense connections for the reference high and low are included on the DAC8881. When properly used with external reference buffer op amps, these reference Kelvin sense pins ensure that the driven reference high and low voltages remain stable versus varying reference load currents. Figure 69 shows an example of a reference force/sense configuration of the DAC8881 operating from a single analog supply voltage. Both the  $V_{REFL}$  and  $V_{REFH}$  reference voltages are set to levels of 100 mV from the DAC8881 supply rails, and are derived from a 5-V external reference. Figure 71 and Figure 70 illustrate the effect of not using the reference force/sense buffers to drive the DAC8881  $V_{REFL}$  and  $V_{REFH}$  pins. A slight degradation in INL and DNL performance of approximately 0.1 LSB may be seen without the use of the force/sense buffer configuration.

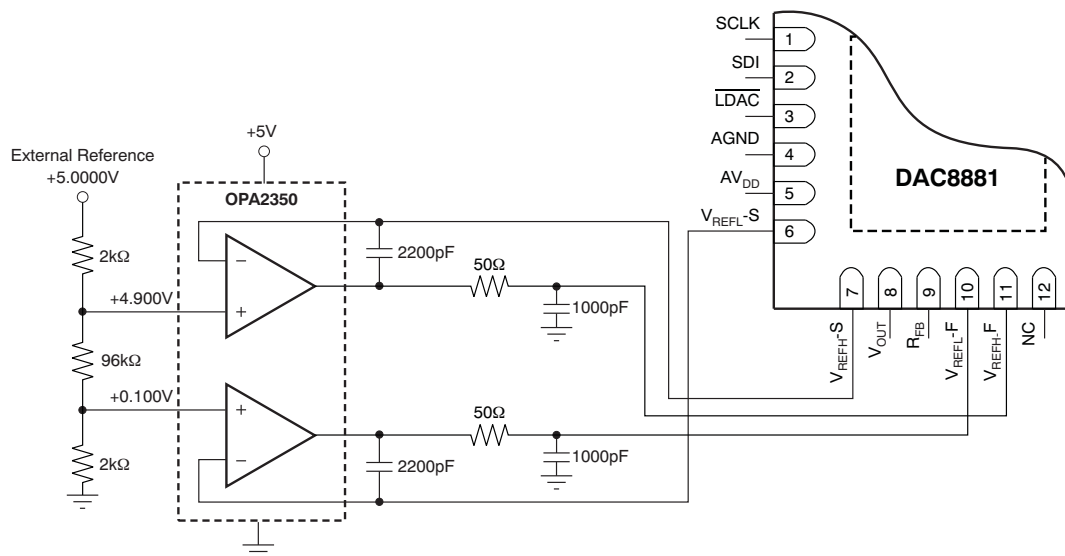


Figure 69. Buffered References ( $V_{REFH} = +4.900$  V and  $V_{REFL} = 100$  mV)

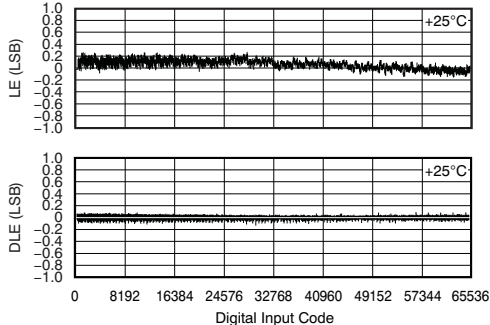


Figure 70. Linearity and Differential Linearity Error for Figure 67 without Reference Buffers

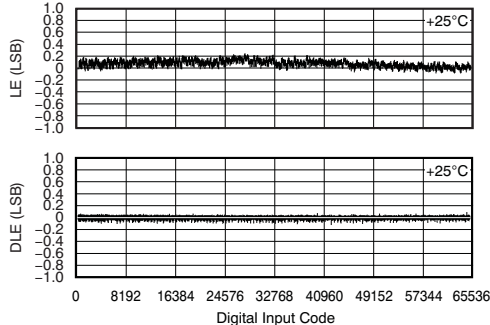


Figure 71. Linearity and Differential Linearity Error for Figure 69 with Reference Buffers

## Feature Description (continued)

### 7.3.3 Output Range

The maximum output range of the DAC8881 is  $V_{REFL}$  to  $V_{REFH} \times G$ , where  $G$  is the output buffer gain set by the GAIN pin. When the GAIN pin is connected to DGND, the output buffer gain = 1. When the GAIN pin is connected to IOV<sub>DD</sub>, the output buffer gain = 2. The output range must not be greater than AV<sub>DD</sub>; otherwise, output saturation occurs. The DAC8881 output transfer function is given in [Equation 1](#):

$$V_{OUT} = \frac{V_{REFH} - V_{REFL}}{65536} \times \text{CODE} \times \text{Buffer Gain} + V_{REFL} \quad (1)$$

Where:

CODE = 0 to 65535. This is the digital code loaded to the DAC.

Buffer Gain = 1 or 2 (set by the GAIN pin).

V<sub>REFH</sub> = reference high voltage applied to the device.

V<sub>REFL</sub> = reference low voltage applied to the device.

### 7.3.4 Input Data Format

The USB/BTC pin defines the input data format.

When this pin is connected to IOV<sub>DD</sub>, the input data format is straight binary, as shown in [Table 1](#).

When this pin is connected to DGND, the input data format is twos complement, as shown in [Table 2](#).

**Table 1. Output vs Straight Binary Code**

USB CODE	5 V RANGE	DESCRIPTION
FFFFh	+4.99992	+Full-Scale – 1LSB
C000h	+3.75000	3/4-Scale
8000h	+2.50000	Midscale
4000h	+1.25000	1/4-Scale
0000h	0.00000	Zero-Scale

**Table 2. Output vs Twos Complement Code**

BTC CODE	5 V RANGE	DESCRIPTION
7FFFh	+4.99992	+Full-Scale – 1LSB
4000h	+3.75000	3/4-Scale
0000h	+2.50000	Midscale
FFFFh	+2.49992	Midscale – 1LSB
C000h	+1.25000	1/4-Scale
8000h	0.00000	Zero-Scale

### 7.3.5 Hardware Reset

When the  $\overline{\text{RST}}$  pin is low, the device is in hardware reset mode, and the input register and DAC latch are set to the value defined by the RSTSEL pin. After  $\overline{\text{RST}}$  goes high, the device is in normal operating mode. When USB/BTC is connected to DGND, the device is in twos complement mode. In this case, the LDAC pin cannot be kept at logic level '0' or toggled when a hardware reset is issued before writing a valid DAC data.

### 7.3.6 Power-On Reset

The DAC8881 has a power-on reset function. After power-on, the value of the input register, the DAC latch, and the output from the V<sub>OUT</sub> pin are set to the value defined by the RSTSEL pin.

### 7.3.7 Program Reset Value

After a power-on reset or a hardware reset, the output voltage from the  $V_{OUT}$  pin and the values of the input register and DAC latch are determined by the status of the RSTSEL pin and the input data format, as shown in [Table 3](#).

**Table 3. Reset Value**

$\overline{LDAC}$ PIN	RSTSEL PIN	USB/ $\overline{BTC}$ PIN	INPUT FORMAT	$V_{OUT}$	VALUE OF INPUT REGISTER AND DAC LATCH
DGND or IOV <sub>DD</sub>	DGND	IOV <sub>DD</sub>	Straight Binary	0	0000h
DGND or IOV <sub>DD</sub>	IOV <sub>DD</sub>	IOV <sub>DD</sub>	Straight Binary	Midscale	8000h
IOV <sub>DD</sub>	DGND	DGND	Twos Complement	0	0000h
IOV <sub>DD</sub>	IOV <sub>DD</sub>	DGND	Twos Complement	Midscale	8000h

### 7.3.8 Power Down

The DAC8881 has a hardware power-down function. When the PDN pin is high, the device is in power-down mode. The  $V_{OUT}$  pin is connected to ground through an internal 10-k $\Omega$  resistor, but the contents of the input register and the DAC latch do not change. In power-down mode, SPI communication is still active.

### 7.3.9 Double-Buffered Interface

The DAC8881 has a double-buffered interface consisting of two register banks: the input register and the DAC latch. The input register is connected directly to the input shift register and the digital code is transferred to the input register upon completion of a valid write sequence. The DAC latch contains the digital code used by the resistor R-2R ladder. The contents of the DAC latch defines the output from the DAC.

Access to the DAC register is controlled by the  $\overline{LDAC}$  pin. When  $\overline{LDAC}$  is high, the DAC register is latched and the input register can change state without affecting the contents of the DAC latch. When  $\overline{LDAC}$  is low, however, the DAC latch becomes transparent and the contents of the input register is transferred to the DAC register.

#### 7.3.10 Load DAC Pin ( $\overline{LDAC}$ )

$\overline{LDAC}$  transfers data from the input register to the DAC register and; therefore, updates the DAC output. The contents of the DAC latch (and the output from DAC) can be changed in two ways, depending on the status of  $\overline{LDAC}$ .

##### 7.3.10.1 Synchronous Mode

When  $\overline{LDAC}$  is tied low, the DAC register updates as soon as new data are transferred into the input register after the rising edge of  $\overline{CS}$ .

##### 7.3.10.2 Asynchronous Mode

When  $\overline{LDAC}$  is high, the DAC latch is latched. The DAC latch (and DAC output) is not updated at the same time that the input register is written to. When  $\overline{LDAC}$  goes low, the DAC register updates with the contents of the input register.

### 7.3.11 1.8 V to 5.5 V Logic Interface

All digital input and output pins are compatible with any logic supply voltage between 1.8 V and 5.5 V. Connect the interface logic supply voltage to the IOV<sub>DD</sub> pin. Although timing is specified down to 2.7 V (see the [Timing Characteristics](#)), IOV<sub>DD</sub> can operate as low as 1.8 V, but with degraded timing and temperature performance. For the lowest power consumption, logic  $V_{IH}$  levels should be as close as possible to IOV<sub>DD</sub>, and logic  $V_{IL}$  levels should be as close as possible to GND. Note that the DAC8881 core internal digital logic operates from the same voltage as the 2.7V to 5.5V AV<sub>DD</sub> supply, so the DV<sub>DD</sub> pin must also be connected to the AV<sub>DD</sub> supply voltage.

## 7.4 Device Functional Modes

### 7.4.1 Serial Interface

The DAC8881 is controlled by a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP™ interface standards.

#### 7.4.1.1 Input Shift Register

Data are loaded into the device as a 16-bit word under the control of the serial clock input, SCLK. The timing diagrams for this operation are shown in the [Timing Diagram](#) section.

The  $\overline{CS}$  input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while  $\overline{CS}$  is low. To start the serial data transfer,  $\overline{CS}$  should be taken low, observing the minimum  $\overline{CS}$  falling edge to SCLK rising edge setup time,  $t_2$ . After  $\overline{CS}$  goes low, serial data are clocked into the device input shift register on the rising edges of SCLK for 16 or more clock pulses. If a frame contains less than 16 bits of data, the frame is invalid. Invalid data are not written into the input register and DAC, although the input register and DAC will continue to hold data from the preceding valid data cycle. If more than 16 bits of data are transmitted in one frame, the last 16 bits are written into the shift register and DAC.  $\overline{CS}$  may be taken high after the rising edge of the 16th SCLK pulse, observing the minimum SCLK rising edge to  $\overline{CS}$  rising edge time,  $t_7$ . The contents of the shift register are transferred into the input register on the rising edge of  $\overline{CS}$ . When data have been transferred into the input register of the DAC, the corresponding DAC register and DAC output can be updated by taking the LDAC pin low.

##### 7.4.1.1.1 Stand-Alone Mode

When the SDOSEL pin is tied to IOV<sub>DD</sub>, the interface is in Stand-Alone mode. This mode provides serial readback for diagnostic purposes. The new input data (16 bits) are clocked into the device shift register and the existing data in the input register (16 bits) are shifted out from the SDO pin. If more than 16 SCLKs are clocked when  $\overline{CS}$  is low, the contents of the input register are shifted out from the SDO pin, followed by zeroes; the last 16 bits of input data remain in the shift register. If less than 16 SCLKs are clocked while  $\overline{CS}$  is low, the data from the SDO pin are part of the data in the input register and must be ignored. Refer to [Figure 2](#) for further detail.

##### 7.4.1.1.2 Daisy-Chain Mode

When the SDOSEL pin is tied to GND, the interface is in Daisy-Chain mode. For systems that contain several DACs, the SDO pin may be used to daisy-chain several devices together.

In Daisy-Chain mode, SCLK is continuously applied to the input shift register while  $\overline{CS}$  is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. These data are clocked out on the falling edge of SCLK and are valid on the rising edge. By connecting this line to the DIN input on the next DAC in the chain, a multi-DAC interface is constructed. 16 clock pulses are required for each DAC in the system. Therefore, the total number of clock cycles must be equal to  $(16 \times N)$ , where  $N$  is the total number of devices in the chain. When the serial transfer to all devices is complete,  $\overline{CS}$  should be taken high. This action prevents any further data from being clocked into the input shift register. The contents in the shift registers are transferred into the relevant input registers on the rising edge of the  $\overline{CS}$  signal.

A continuous SCLK source may be used if  $\overline{CS}$  can be held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles can be used and  $\overline{CS}$  can be taken high some time later. When the transfer to all input registers is complete, a common LDAC signal updates all DAC registers, and all analog outputs update simultaneously.

## 8 Application and Implementation

### NOTE

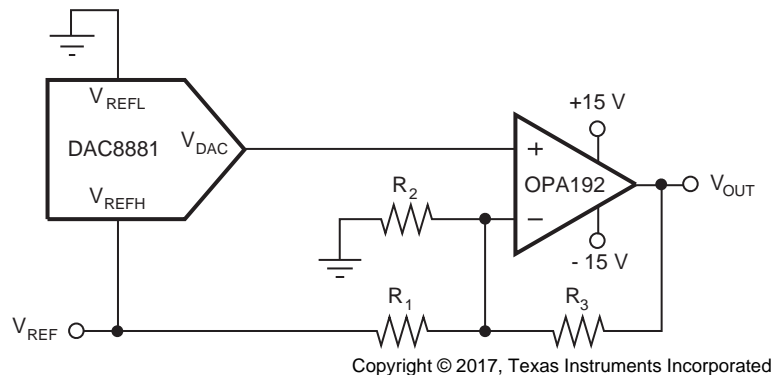
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The excellent linearity as well as low-noise and fast settling time makes the DAC8881 a strong performer in applications such as automatic test equipment, precision instrumentation and data acquisition systems. Additionally, the energy saving feature of the device, through the PDN pin, significantly reduces power dissipation -- this mode reduces current consumption, as low as 25 µA with a 5-V supply.

#### 8.1.1 Bipolar Operation Using The DAC8881

The DAC8881 is designed for single-supply operation; however, a bipolar output is also possible using the circuit shown in [Figure 72](#). This circuit gives a bipolar output voltage of  $V_{OUT}$ . When  $GAIN = 1$ ,  $V_{OUT}$  can be calculated using [Equation 2](#):



Some pins are omitted for clarity.

**Figure 72. Bipolar Operation Using the DAC8881**

$$V_{BIP}(CODE) = \left[ 1 + \frac{R_3}{R_2} + \frac{R_3}{R_1} \right] \times \frac{CODE}{65536} - \frac{R_3}{R_1} \times V_{REF} \quad (2)$$

Where:

$V_{BIP}(CODE)$  = bipolar output voltage versus CODE from the [OPA211](#).

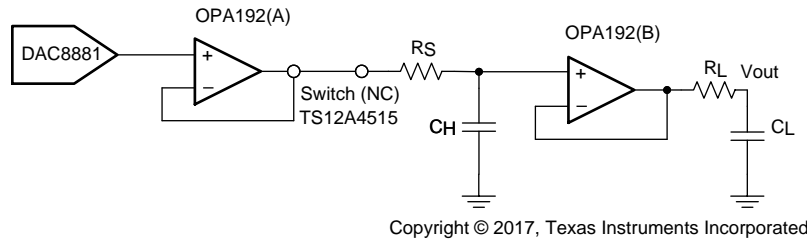
CODE = 0 to 262143. This is the digital code loaded to the DAC.

$V_{REF}$  = reference high voltage applied to the DAC8881.

As an example, a  $\pm 8$ -V output span can be achieved by using values of 5 V, 6.25 k $\Omega$ , 16.67 k $\Omega$ , and 10 k $\Omega$  for  $V_{ref}$ ,  $R_1$ ,  $R_2$ , and  $R_3$  respectively.

## 8.2 Typical Application

### 8.2.1 DAC8881 Sample Hold Circuit



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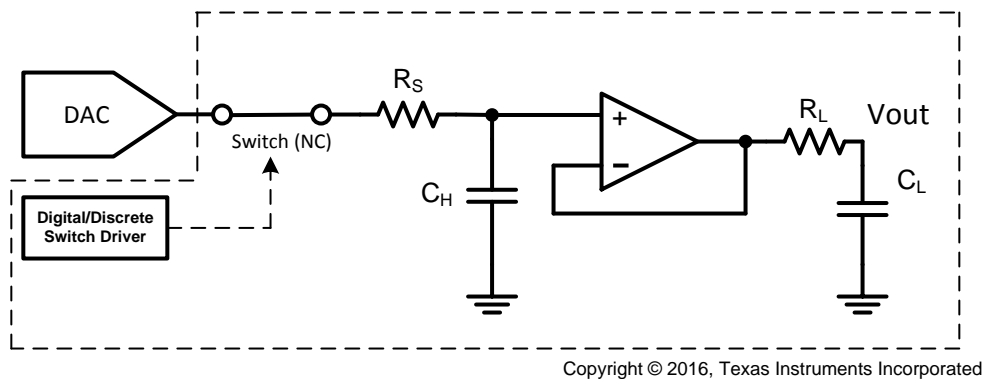
**Figure 73. DAC8881 Sample and Hold Circuit**

#### 8.2.1.1 Design Requirements

The inherent architecture of the DAC8881, which consists of an R-2R architecture, enables great performance in regards to noise and accuracy, but at a cost of large glitch area. Glitch area, also known as glitch impulse area, is defined as the area associated with the overshoot or undershoot created by a code transition, and is generally quantified in Volt-seconds. Different code-to-code transitions produce different levels of glitch impulses. DACs with R-2R architectures produce large glitches during major-carry transitions.

There are two methods that can be used to reduce this glitch area:

1. Add an external RC Filter to the output of the DAC.
  - The low-pass filter helps attenuate high-frequency glitches that would normally propagate to the DAC output. Best practice is to use a small resistor value, as large resistance develops a large potential drop and reduces the voltage seen at the load. Capacitor values can be determined from the desired cutoff frequency of the low-pass filter, as well as settling time.
2. Another technique is to employ a Sample and Hold (S&H) circuit following the DAC output.
  - In its simplest form, the sample and hold circuit can be constructed from the following components: a capacitive element, output buffer, and switch. A schematic of the simplified S&H is shown in [Figure 74](#).



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**Figure 74. Simplified Sample and Hold Circuit**

#### 8.2.1.2 Detailed Design Procedure

The Sample/Track and Hold modes of operation correspond to the state of the switch, which connects the DAC output to the hold capacitor  $C_H$ . In sample mode – also referred to as track mode -- the switch is closed, allowing the capacitor to charge or discharge to the sampled DAC output voltage. The operational amplifier is configured as a buffer, which tracks and relays the voltage seen across  $C_H$  to the output of the circuit. In hold mode, the switch opens, disconnecting  $C_H$  from the DAC output. The DAC is updated while the circuit is in hold mode, preventing any DAC major carry glitches from propagating to the S&H output. The capacitor retains the previous sampled voltage, and this value is buffered to the output of the circuit. In real circuits, switch leakage and operational amplifier input bias current must be considered as it will impact circuit performance. The switch is generally controlled by an external discrete or digital driver.



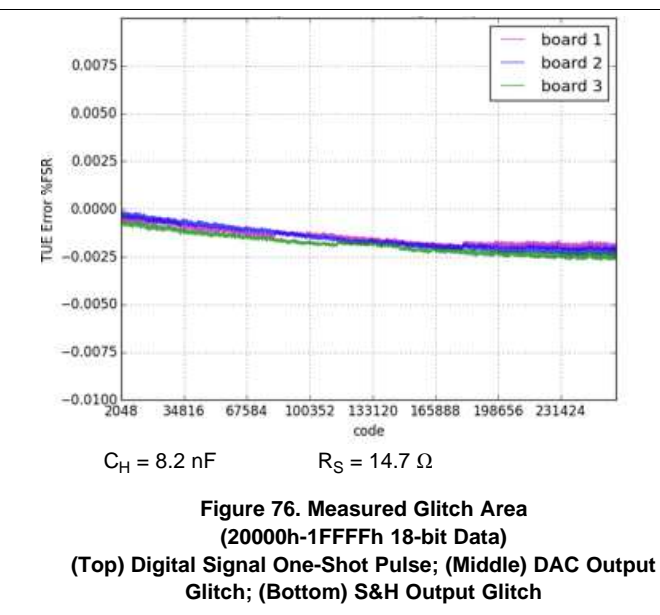
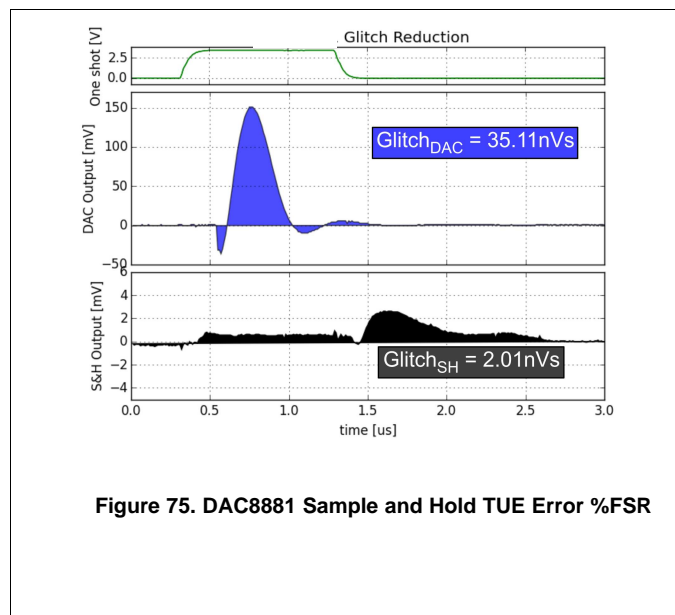
## Typical Application (continued)

Once the DAC glitch relays the switch closes and re-enters sample or track mode.

More information related to this circuit can be found in [Sample & Hold Glitch Reduction for Precision Outputs Design Guide](#) (TIDU022).

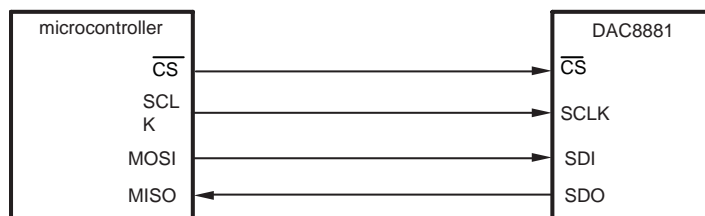
### 8.2.1.3 Application Curves

Glitch reduction and total unadjusted error (TUE) plots of the solution presented in [Sample & Hold Glitch Reduction for Precision Outputs Design Guide](#) (TIDU022) is shown in the following plots. The glitch area is reduced from 35.11 nVs to 2.01 nVs.



## 8.3 System Example

[Figure 77](#) displays a typical serial interface that may be used when connecting the DAC8881 SPI serial interface to a (master) microcontroller. The setup for the interface is as follows: The microcontroller output SPI CLK drives the SCLK pin of the DAC8881, while the DAC8881 SDI pin is driven by the MOSI pin of the microcontroller. The  $\overline{\text{CS}}$  pin of the DAC8881 can be asserted from a general program input/output pin of the microcontroller. When data are to be transmitted to the DAC8881, the  $\overline{\text{CS}}$  pin is taken low. The data from the microcontroller is then transmitted to the DAC8881, totaling 24 bits latched into the DAC8881 device through the negative edge of SCLK.  $\overline{\text{CS}}$  is then brought high after the completed write. The DAC8881 requires its data with the MSB as the first bit received.



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**Figure 77. Simplified Sample and Hold Circuit**

## 9 Power Supply Recommendations

The DAC8881 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to AVDD should be well regulated and low noise. Switching power supplies and DC-DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, a strong recommendation is to include a 1- $\mu$ F to 10- $\mu$ F capacitor and 0.1- $\mu$ F bypass capacitor. The current consumption on the AVDD pin, the short-circuit current limit, and the load current for the device is listed in [Electrical Characteristics](#). The power supply must meet the aforementioned current requirements.

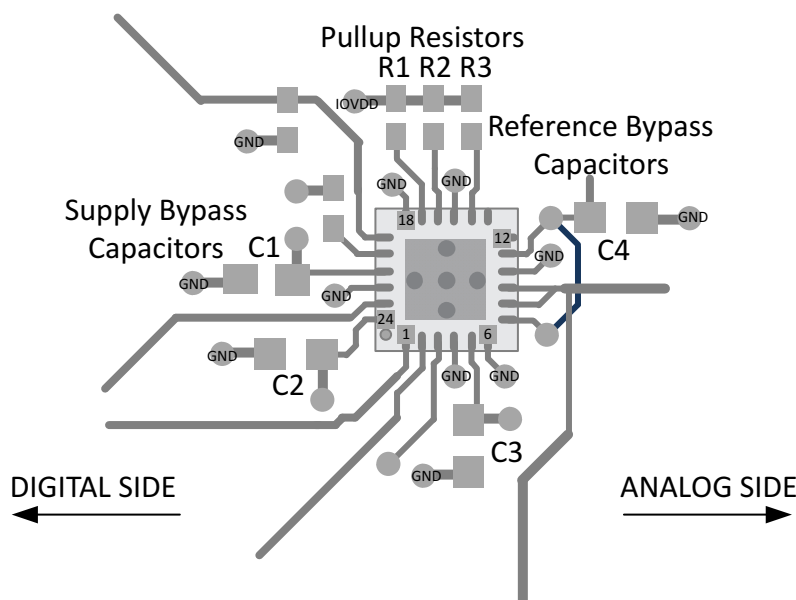
## 10 Layout

### 10.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- All Power Supply pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 to 0.22  $\mu$ F ceramic with a X7R or NP0 dielectric.
- Power supplies and VrefH/L bypass capacitors should be placed close to terminals to minimize inductance and optimize performance.
- A high-quality ceramic type NP0 or X7R is recommended for its optimal performance across temperature, and very low dissipation factor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the DAC8881 device. The separation of analog and digital blocks will allow for better design and practice as it will ensure less coupling into neighboring blocks, and will minimize the interaction between analog and digital return currents.

### 10.2 Layout Example



**Figure 78. DAC8881 Basic Layout Example**

## 11 器件和文档支持

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- [DAC8881 评估模块 \(SLAU257\)](#)
- [《通过采样和减少干扰实现高精度输出设计指南》 \(TIDU022\)](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DAC8881SRGET</a>	Active	Production	VQFN (RGE)   24	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC 8881
DAC8881SRGET.A	Active	Production	VQFN (RGE)   24	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC 8881
DAC8881SRGETG4	Active	Production	VQFN (RGE)   24	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC 8881
DAC8881SRGETG4.A	Active	Production	VQFN (RGE)   24	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC 8881

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8881SRGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
DAC8881SRGETG4	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8881SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
DAC8881SRGETG4	VQFN	RGE	24	250	210.0	185.0	35.0

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

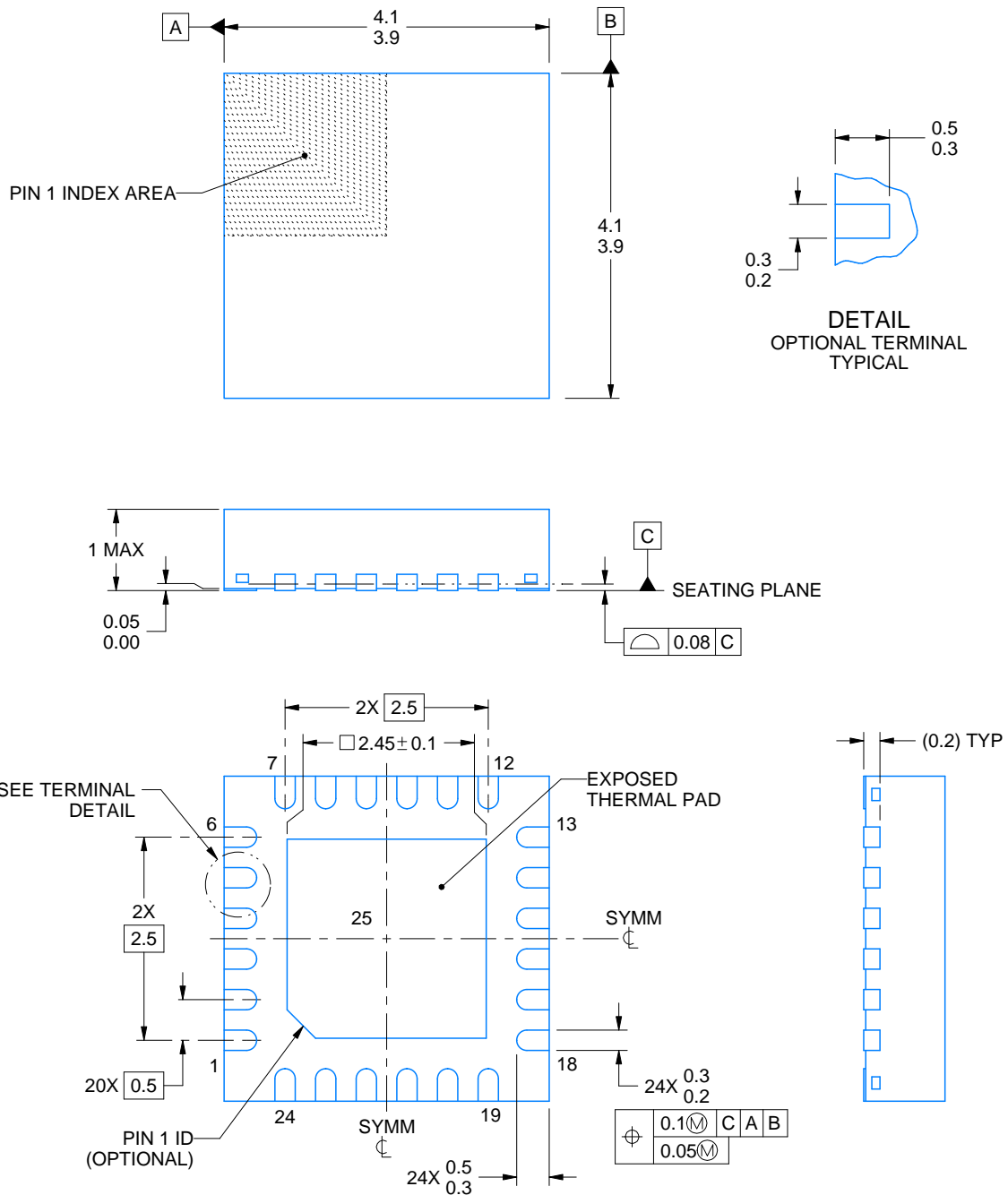
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H





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## NOTES:

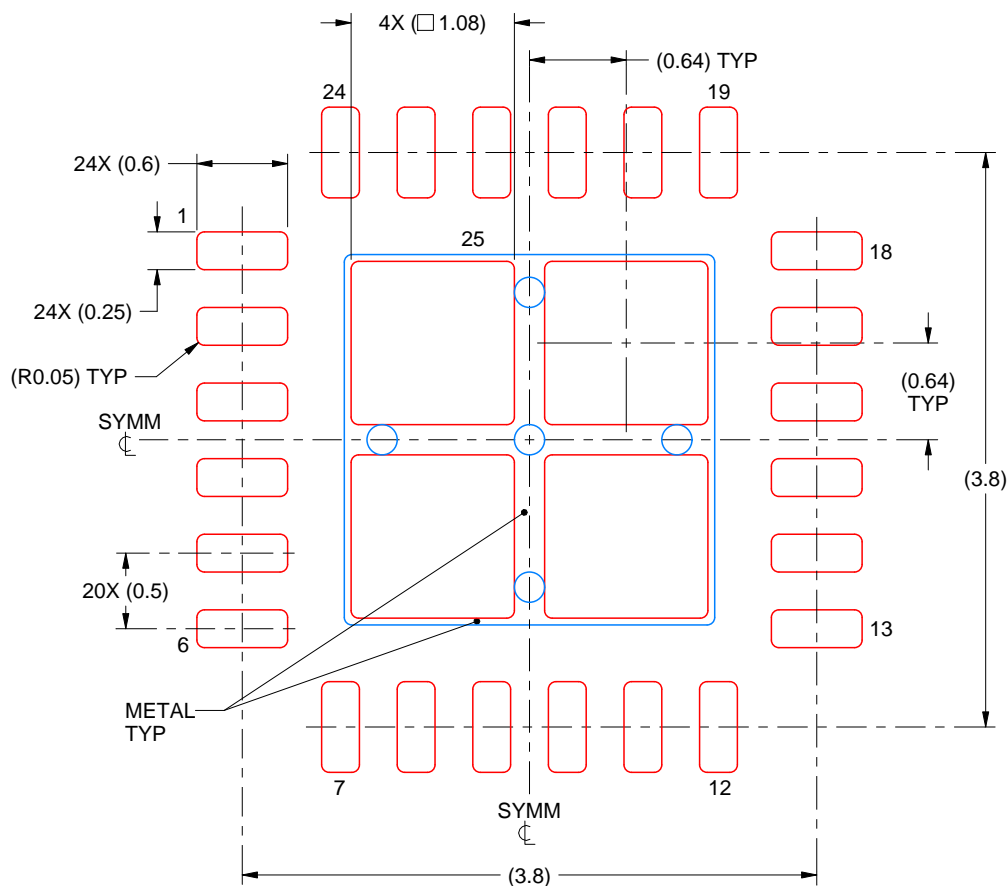
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



**RGE0024B**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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