具有集成电流检测、1/256 微步进、STEP/DIR 接口和智能调优技术的 DRV8434 步进电机驱动器

1 特性

- PWM 微步进电机驱动器
  - 简单的 STEP/DIR 接口
  - 最高 1/256 的微步进分度器
- 集成电流检测功能
  - 无需检测电阻
  - ±4% 满量程电流精度
- 智能调优、慢速和混合衰减选项
- 工作电源电压范围为 4.5V 至 48V
- 低 $R_{DS(ON)}$：24V、25°C 时为 330mΩ HS + LS
- 高电流容量：2.5A 满量程、1.8A 均方根电流
- 与以下器件引脚对引脚兼容：
  - DRV8426：33V，900mΩ HS + LS
  - DRV8436：48V，900mΩ HS + LS
  - DRV8424/25：33V，330/550mΩ HS + LS
- 可配置关断时间 PWM 斩波
  - 7μs、16μs、24μs 或 32μs
- 支持 1.8V、3.3V、5.0V 逻辑输入
- 低电流睡眠模式 (2μA)
- 展频时钟，以降低 EMI
- 小型封装和外形尺寸
- 保护特性
  - VM 欠压锁定 (UVLO)
  - 电荷泵欠压 (CPUV)
  - 过流保护 (OCP)
  - 开路负载检测 (OL)
  - 热关断 (OTSD)
  - 故障调节输出 (nFAULT)

2 应用

- 打印机和扫描仪
- ATM 和验钞机
- 纺织机
- 舞台照明设备
- 办公和家庭自动化
- 工厂自动化和机器人
- 医疗应用
- 3D 打印机

3 说明

DRV8434 是一款适用于工业和消费类应用的步进电机驱动器。该器件由两个 N 沟道功率 MOSFET H 桥驱动器、一个微步进分度器以及集成电流检测功能完全集成。DRV8434 最高可驱动 2.5A 满量程输出电流（取决于 PCB 设计）。

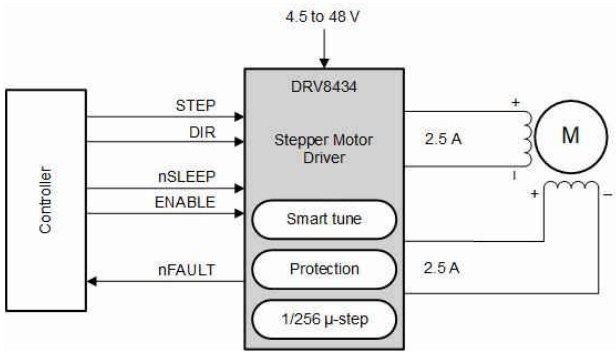
DRV8434 采用内部电流检测架构，无需再使用两个外部功率检测电阻，可缩小 PCB 面积并降低系统成本。该器件使用内部 PWM 电流调节方案，该方案能在智能调优、慢速和混合衰减选项之间进行选择。智能调优可通过自动调节实现出色的电流调节性能，并对电机变化和老化效应进行补偿和减少电机的可闻噪声。

借助简单的 STEP/DIR 接口，可通过外部控制器管理步进电机的方向和步进速率。这款器件可配置为多种步进模式，从全步进模式到 1/256 微步进模式皆可。该器件通过专用的 nSLEEP 引脚提供低功耗睡眠模式。提供的保护特性包括：电源欠压、电荷泵故障、过流、短路、开路负载和过热保护。故障状态通过 nFAULT 引脚指示。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
DRV8434PWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8434RGER	VQFN (24)	4mm x 4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2020) to Revision A (May 2022)	Page
• Updated Tri-Level and Quad-Level Input pin diagrams	27
• Updated HTSSOP and QFN layout examples	39
• Added links to Related Documents section	41

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5 Pin Configuration and Functions

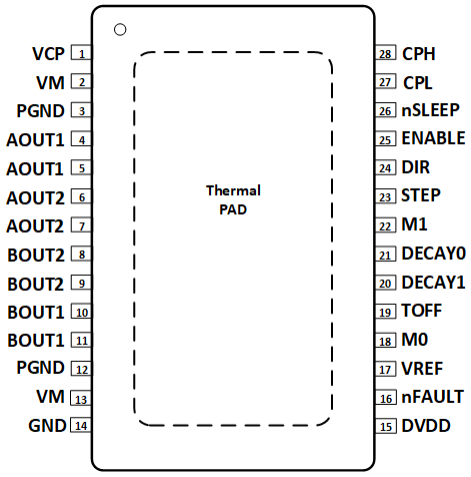

图 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View

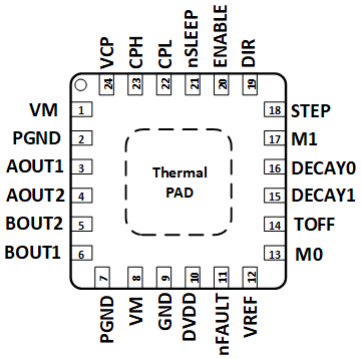

图 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View

5.1 引脚功能

引脚			I/O	类型	说明
名称	NO.				
	HTSSOP	VQFN			
AOUT1	4、5	3	O	输出	绕组 A 输出。连接到步进电机绕组。
AOUT2	6、7	4	O	输出	绕组 A 输出。连接到步进电机绕组。
PGND	3、12	2、7	—	电源	电源接地。连接到系统接地。
BOUT2	8, 9	5	O	输出	绕组 B 输出。连接到步进电机绕组。
BOUT1	10、11	6	O	输出	绕组 B 输出。连接到步进电机绕组。
CPH	28	23	—	电源	电荷泵开关节点。在 CPH 到 CPL 之间连接一个额定电压为 VM 的 X7R 0.022μF 陶瓷电容器。
CPL	27	22			
DIR	24	19	I	输入	方向输入。逻辑电平设置步进的方向；内部下拉电阻。
ENABLE	25	20	I	输入	逻辑低电平将禁用器件输出；逻辑高电平则会启用；内部上拉至 DVDD。还将决定 OCP 和 OTSD 响应的类型。
DVDD	15	10	—	电源	逻辑电源电压。通过电容为 0.47 μ F 至 1 μ F、额定电压为 6.3V 或 10V 的 X7R 陶瓷电容器连接至 GND。
GND	14	9	—	电源	器件接地。连接到系统接地。

引脚			I/O	类型	说明
名称	NO.				
	HTSSOP	VQFN			
VREF	17	12	I	输入	电流设定基准输入。最大值为 3.3V。DVDD 可用于通过电阻分压器提供 VREF。
M0	18	13	I	输入	微步进模式设置引脚。设置步进模式；内部下拉电阻。
M1	22	17			
DECAY0	21	16	I	输入	衰减模式设置引脚。设置衰减模式（请参阅节 7.3.6 部分）。
DECAY1	20	15			
STEP	23	18	I	输入	步进输入。上升沿使分度器前进一步；内部下拉电阻。
VCP	1	24	—	电源	电荷泵输出。通过一个 X7R 0.22 μF 16V 陶瓷电容器连接至 VM。
VM	2、13	1、8	—	电源	电源。连接到电机电源电压，并通过两个 0.01μF 陶瓷电容器（每个引脚一个）和一个额定电压为 VM 的大容量电容器旁路到 PGND。
TOFF	19	14	I	输入	设置电流斩波期间的衰减模式关断时间；四电平引脚。还将设置智能调优纹波控制模式中的纹波电流。
nFAULT	16	11	O	漏极开路	故障指示。故障状态下拉低逻辑低电平；开漏输出需要外部上拉电阻。
nSLEEP	26	21	I	输入	睡眠模式输入。逻辑高电平用于启用器件；逻辑低电平用于进入低功耗睡眠模式；内部下拉电阻。nSLEEP 低电平脉冲将清除故障。
PAD	-	-	-	-	散热焊盘。连接到系统接地。

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6 规格

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内（除非另有说明）[(1)]

	最小值	最大值	单位
电源电压 (VM)	–0.3	50	V
电荷泵电压（VCP、CPH）	–0.3	V_{VM} + 7	V
电荷泵负开关引脚 (CPL)	–0.3	V_{VM}	V
nSLEEP 引脚电压 (nSLEEP)	–0.3	V_{VM}	V
内部稳压器电压 (DVDD)	-0.3	5.75	V
控制引脚电压（STEP、DIR、ENABLE、nFAULT、DECAY0、DECAY1、TOFF、M0、M1）	-0.3	5.75	V
开漏输出电流 (nFAULT)	0	10	mA
基准输入引脚电压 (VREF)	-0.3	5.75	V
连续相节点引脚电压（AOUT1、AOUT2、BOUT1、BOUT2）	–1	V_{VM} + 1	V
瞬态 100ns 相节点引脚电压（AOUT1、AOUT2、BOUT1、BOUT2）	–3	V_{VM} + 3	V
峰值驱动电流（AOUT1、AOUT2、BOUT1、BOUT2）	受内部限制		A
工作环境温度，T_A	-40	125	°C
运行结温，T_J	-40	150	°C
贮存温度，T_{stg}	-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。

6.2 ESD 等级

				值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001		±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101	PWP 转角引脚（1、14、15 和 28）	±750	
			其他引脚	±500	

6.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）

		最小值	最大值	单位
V_{VM}	可确保正常（直流）运行的电源电压范围	4.5	48	V
V_I	逻辑电平输入电压	0	5.5	V
V_{VREF}	VREF 电压	0.05	3.3	V
f_{STEP}	施加的 STEP 信号 (STEP)	0	500(1)	kHz
I_{FS}	电机满量程电流 (xOUTx)	0	2.5(2)	A
I_{rms}	电机均方根电流 (xOUTx)	0	1.8(2)	A
T_A	工作环境温度	-40	125	°C
T_J	工作结温	-40	150	°C

(1) STEP 输入工作频率最高可达 500kHz，但系统带宽受电机负载限制
(2) 必须遵守功耗和热限值

6.4 热性能信息

热指标(1)		PWP (HTSSOP)	RGE (VQFN)	单位
		28 引脚	24 引脚	
$R_{\theta JA}$	结至环境热阻	29.7	39.0	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	23.0	28.9	°C/W
$R_{\theta JB}$	结至电路板热阻	9.3	16.0	°C/W
ψ_{JT}	结至顶部特征参数	0.3	0.4	°C/W
ψ_{JB}	结至电路板特征参数	9.2	15.9	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	2.4	3.4	°C/W

(1) 有关新旧热指标的更多信息，请参阅《半导体和 IC 封装热指标》应用报告。

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
t_{EN}	Enable time	ENABLE = 0/1 to output transition			5	µs
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 48V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 48 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
TRI-LEVEL INPUTS (M0, DECAY0, DECAY1, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{IL}	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	T_J = 25 °C, I_O = -1 A		165	200	mΩ
		T_J = 125 °C, I_O = -1 A		250	300	mΩ
		T_J = 150 °C, I_O = -1 A		280	350	mΩ

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 1 A		165	200	mΩ
		T_J = 125 °C, I_O = 1 A		250	300	mΩ
		T_J = 150 °C, I_O = 1 A		280	350	mΩ
t_{SR}	Output slew rate	V_{VM} = 24 V, I_O = 1 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3 V	1.254	1.32	1.386	V/A
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			8.25	µA
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	Current trip accuracy	0.25 A < I_O < 0.5 A	–12		12	%
		0.5 A < I_O < 1 A	–6		6	
		1 A < I_O < 2.5 A	–4		4	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 2.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	4			A
t_{OCP}	Overcurrent deglitch time			2		µs
t_{RETRY}	Overcurrent retry time			4		ms
t_{OL}	Open load detection time				50	ms
I_{OL}	Open load current threshold			75		mA
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.6 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500[(1)]	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or MODEx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

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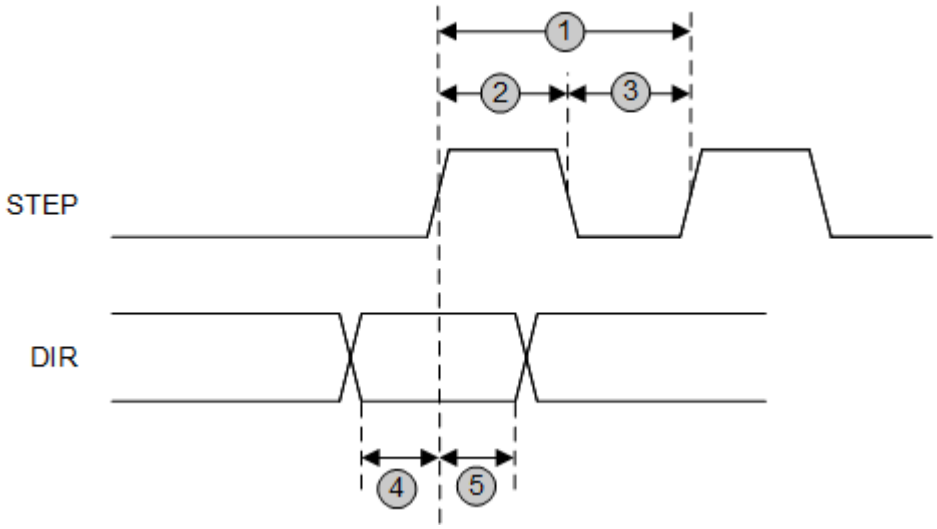

图 6-1. STEP and DIR Timing Diagram

6.6.1 典型特性

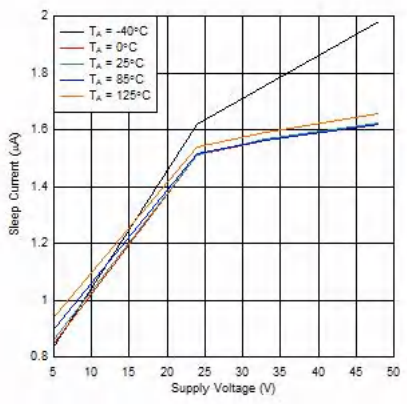

图 6-2. 睡眠电流与电源电压间的关系

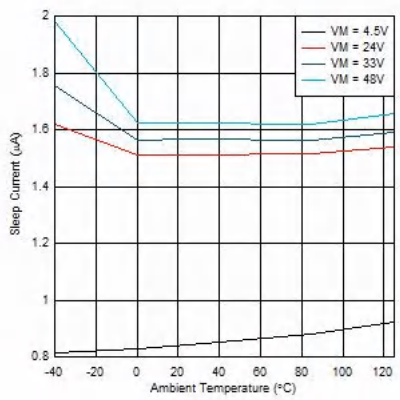

图 6-3. 睡眠电流与温度间的关系

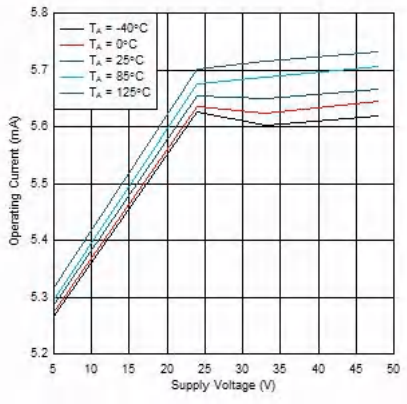

图 6-4. 工作电流与电源电压间的关系

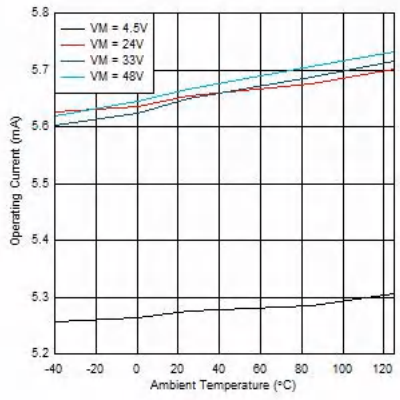

图 6-5. 工作电流与温度间的关系

6.6.1 典型特性 (continued)

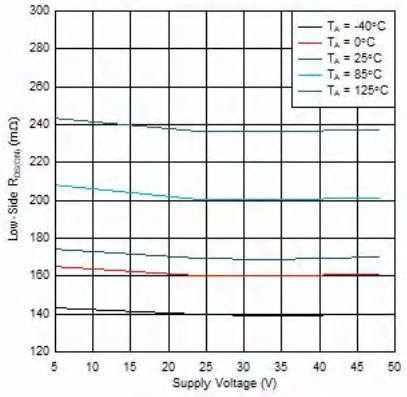

图 6-6. 低侧 $R_{DS(ON)}$ 与电源电压间的关系（MODE = 0 或 330k 至 GND）

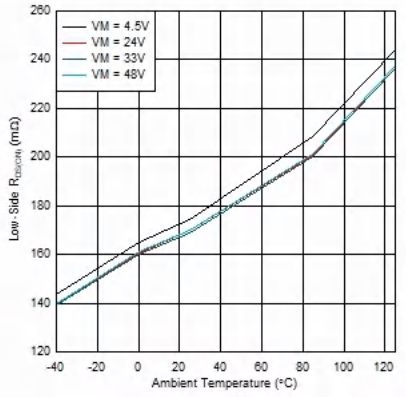

图 6-7. 低侧 $R_{DS(ON)}$ 与温度间的关系（MODE = 0 或 330k 至 GND）

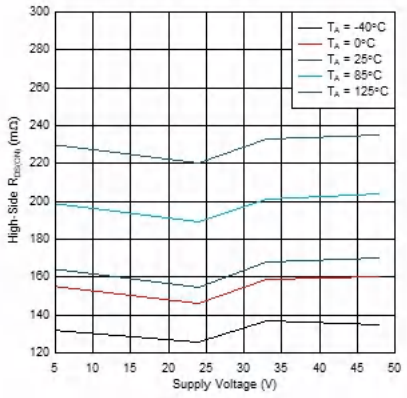

图 6-8. 高侧 $R_{DS(ON)}$ 与电源电压间的关系（MODE = 0 或 330k 至 GND）

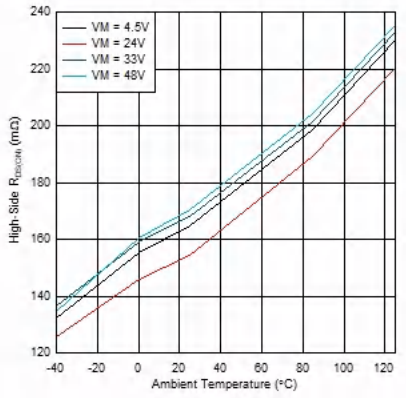

图 6-9. 高侧 $R_{DS(ON)}$ 与温度间的关系（MODE = 0 或 330k 至 GND）

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7 详细说明

7.1 概述

DRV8434 是一款用于双极步进电机的集成电机驱动器解决方案。该器件通过集成两个 N 沟道功率 MOSFET H 桥、电流检测电阻和调节电路以及一个微步进分度器，可更大程度提高集成度。DRV8434 与 DRV8426、DRV8436 和 DRV8424/25 引脚对引脚兼容。DRV8434 能够支持 4.5V 至 48V 的宽电源电压范围。DRV8434 提供高达 4A 峰值、2.5A 满量程或 1.8A 均方根 (rms) 的输出电流。实际的满量程和均方根电流取决于环境温度、电源电压和 PCB 热性能。

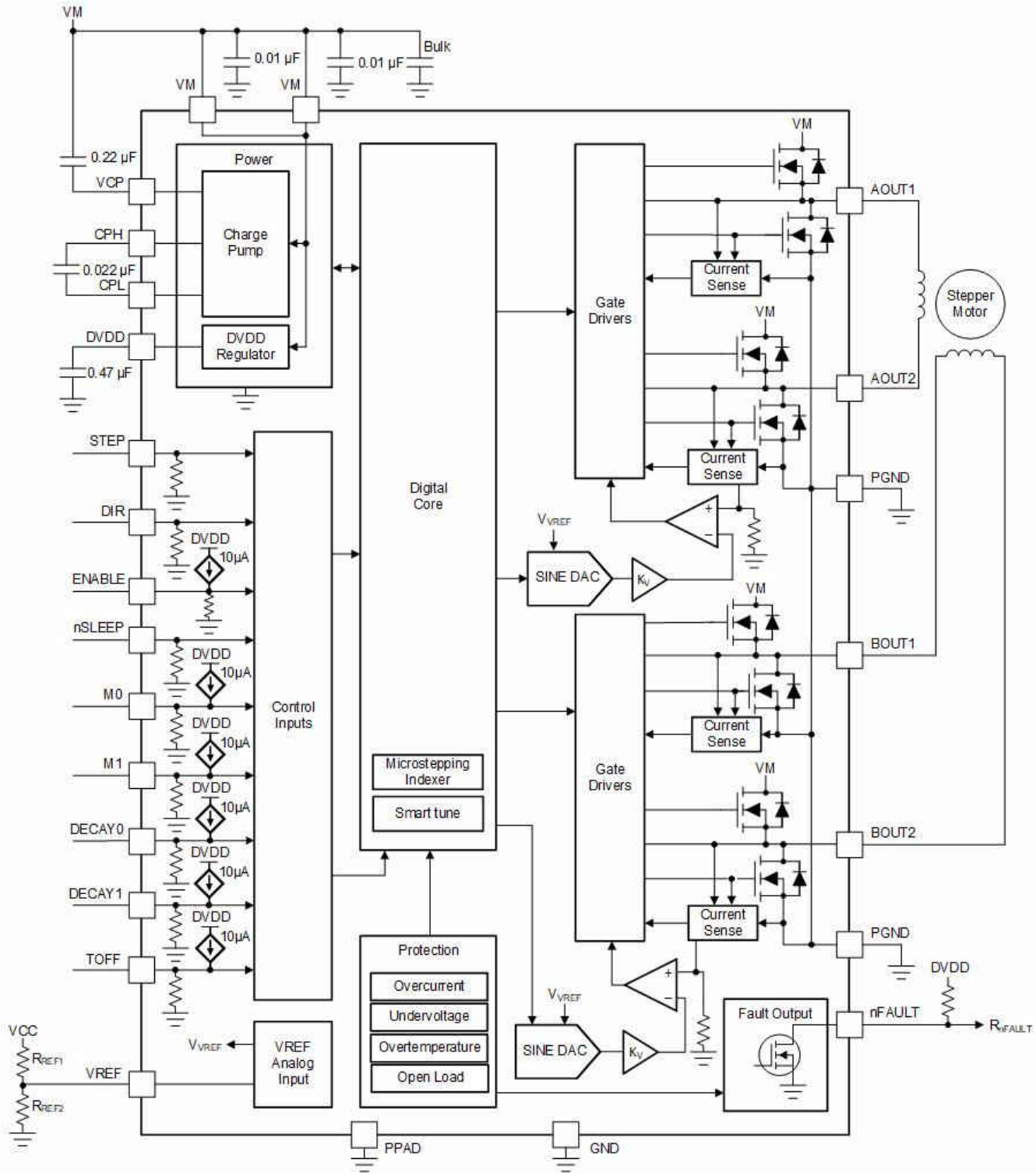
DRV8434 采用集成式电流检测架构，无需再使用两个外部功率检测电阻，从而显著节省布板空间和 BOM 成本，并减少设计工作量和降低功耗。该架构通过使用电流镜方法消除了检测电阻中的功率损耗，并使用内部功率 MOSFET 进行电流检测。通过 VREF 引脚处的电压来调节电流调节设定点。

借助简单的 STEP/DIR 接口，可通过外部控制器管理步进电机的方向和步进速率。内部微步进分度器可以执行高精度微步进，而无需外部控制器来管理绕组电流电平。分度器可实现全步进、半步进以及 1/4、1/8、1/16、1/32、1/64、1/128 和 1/256 微步进。高微步进有助于显著降低可闻噪声并实现平稳的运动。除了标准的半步进模式，非循环半步进模式可用于在较高的电机转速下增加扭矩输出。

步进电机驱动器需要通过实现多种类型的衰减模式（如慢速衰减、混合衰减和快速衰减）来再循环绕组电流。DRV8434 提供智能调优衰减模式。自动调优是一种创新的衰减机制，能够自动调节以实现出色的电流调节性能，而不受电压、电机转速、变化和老化效应的影响。自动调优纹波控制使用可变关断时间纹波电流控制方案，以更大限度地减少电机绕组电流的失真。自动调优动态衰减使用固定关断时间动态快速衰减百分比方案，以更大限度地减少电机绕组电流的失真，同时实现频率成分最小化并显著减少设计工作量。除了该无缝的轻松自动智能调优之外，DRV8434 还提供传统的衰减模式（如慢速混合衰减和混合衰减）。

该器件为内部数字振荡器和内部电荷泵集成了展频时钟特性。此特性可更大程度减少器件的辐射发射。系统包括一个低功耗睡眠模式，以便在不主动驱动电机时节省功耗。

7.2 功能模块图



7.3 特性说明

表 7-1 列出了 DRV8434 的推荐外部组件。

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表 7-1. 外部组件

组件	引脚 1	引脚 2	推荐
C_{VM1}	VM	PGND	两个额定电压为 VM 的 X7R 0.01μF 陶瓷电容器
C_{VM2}	VM	PGND	额定电压为 VM 的大容量电容器
C_{VCP}	VCP	VM	X7R 0.22μF 16V 陶瓷电容器
C_{SW}	CPH	CPL	额定电压为 VM 的 X7R 0.022μF 陶瓷电容器
C_{DVDD}	DVDD	GND	电容为 0.47μF 至 1μF 的 X7R 6.3V 陶瓷电容器
R_{nFAULT}	VCC (1)	nFAULT	>4.7kΩ 电阻
R_{REF1}	VREF	VCC	用于限制斩波电流的电阻。建议：R_{REF1} 和 R_{REF2} 的并联电阻应低于 50kΩ。
R_{REF2}（可选）	VREF	GND	

(1) VCC 不是该器件上的引脚，但开漏输出 nFAULT 需要 VCC 电源电压上拉；nFAULT 可能会被上拉到 DVDD。

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

7.3.1.1 峰值电流额定值

步进驱动器中的峰值电流受过流保护关断阈值 I_{OCP} 的限制。峰值电流表示任何瞬态持续电流脉冲，例如当对电容充电时，或当总占空比非常低时。通常，I_{OCP} 的最小值指定了步进电机驱动器的峰值电流额定值。对于 DRV8434，每个电桥的峰值电流额定值为 4A。

7.3.1.2 均方根电流额定值

均方根（平均）电流由集成电路的热特性决定。均方根电流是根据典型系统中 $R_{DS(ON)}$、上升和下降时间、PWM 频率、器件静态电流和 25°C 温度下的封装热性能计算的。实际的均方根电流可能更高或更低，具体取决于散热和环境温度。对于 DRV8434，每个电桥的均方根电流额定值为 1.8A。

7.3.1.3 Full-Scale Current Rating

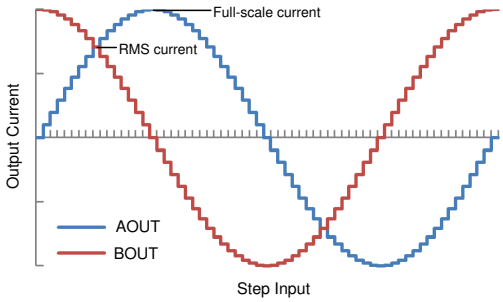

图 7-1. Full-Scale and RMS Current

7.3.2 PWM Motor Drivers

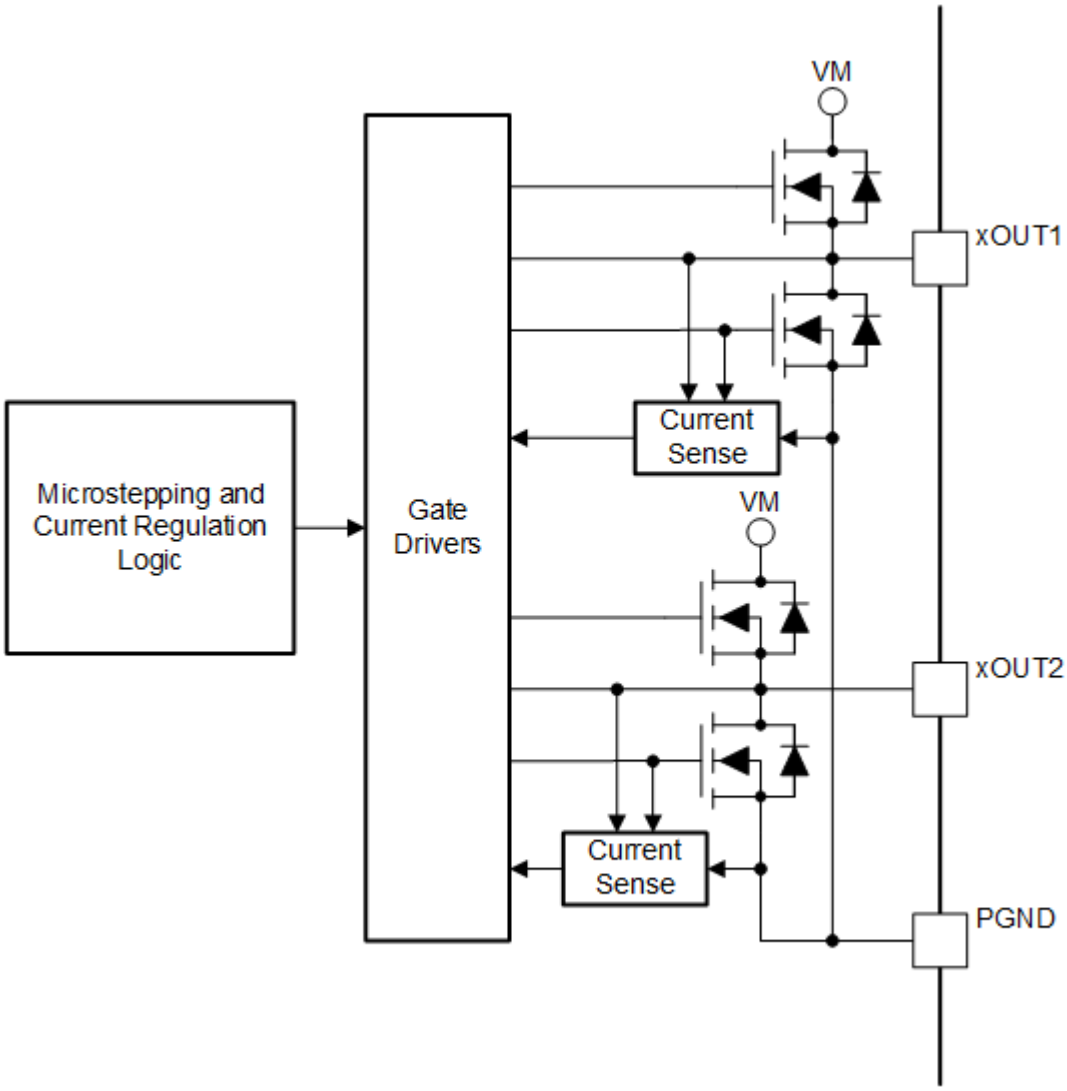

图 7-2. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the device allows a number of different step modes. The M0 and M1 pins are used to configure the step mode as shown below. The settings can be changed on the fly.

表 7-2. Microstepping Indexer Settings

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step

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表 7-2. Microstepping Indexer Settings (continued)

M0	M1	STEP MODE
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

表 7-3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer advances to the next state in the table. The direction shown is with the DIR pin logic high. If the DIR pin is logic low, the sequence table is reversed.

备注

If the step mode is changed dynamically while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered immediately after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

表 7-3. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50

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表 7-3. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

表 7-4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

表 7-4. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

表 7-5 shows the noncircular 1/2 – step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

表 7-5. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	– 100	135
5	0	– 100	180
6	– 100	– 100	225
7	– 100	0	270
8	– 100	100	315

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC must not exceed 3.3 V.

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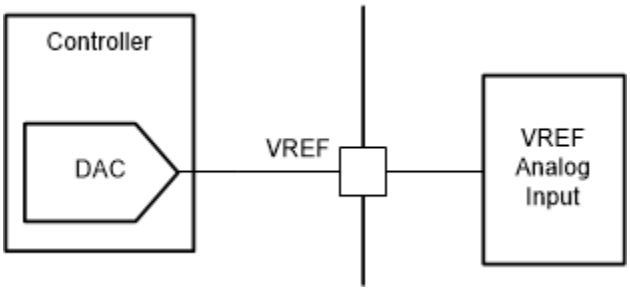

图 7-3. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

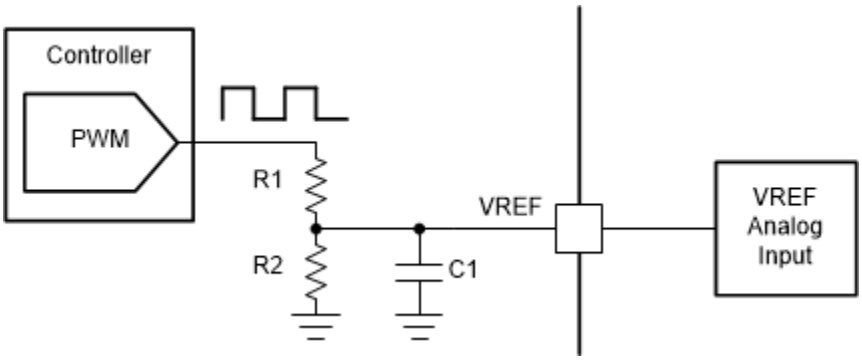

图 7-4. Controlling VREF With a PWM Resource

7.3.5 电流调节

流经电机绕组的电流由一个可调节关断时间的 PWM 电流调节电路进行调节。当 H 桥被启用时，通过绕组的电流以一定的速率上升，该速率取决于直流电压、绕组电感和存在的反电动势大小。当电流达到电流调节阈值时，电桥将进入衰减模式以减小电流，该模式的持续时间取决于 TOFF 引脚设置。关断时间结束后，将重新启用电桥，开始另一个 PWM 循环。

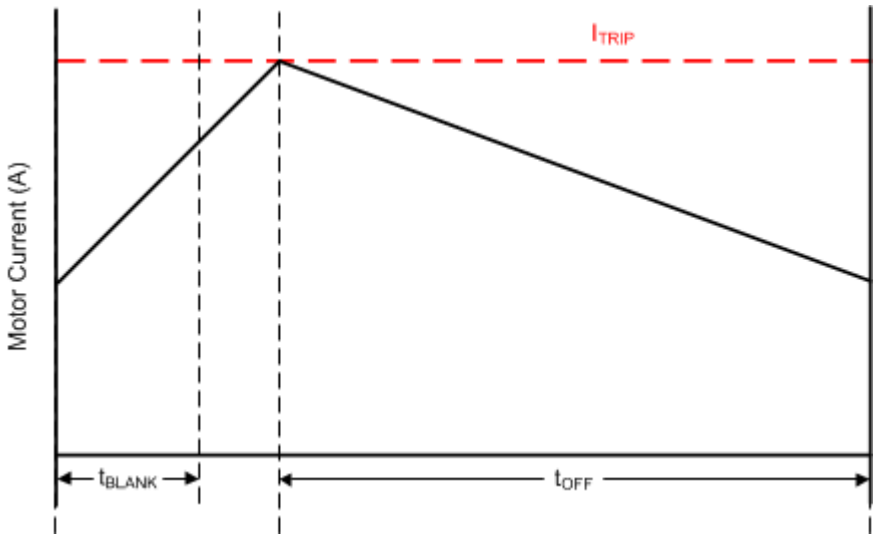

图 7-5. 电流斩波波形

PWM 调节电流由比较器设置，该比较器监测与低侧功率 MOSFET 并联的电流检测 MOSFET 两端的电压。电流检测 MOSFET 通过基准电流进行偏置，该基准电流是电流模式正弦加权 DAC 的输出，其满量程基准电流通过 VREF 引脚的电压进行设置。

您可以使用以下公式计算满量程调节电流 (I_{FS})：I_{FS} (A) = V_{REF} (V)/K_V (V/A) = V_{REF} (V)/1.32 (V/A)。

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7.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in 图 7-6, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. Fast decay mode is shown in 图 7-6, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in 图 7-6, Item 3.

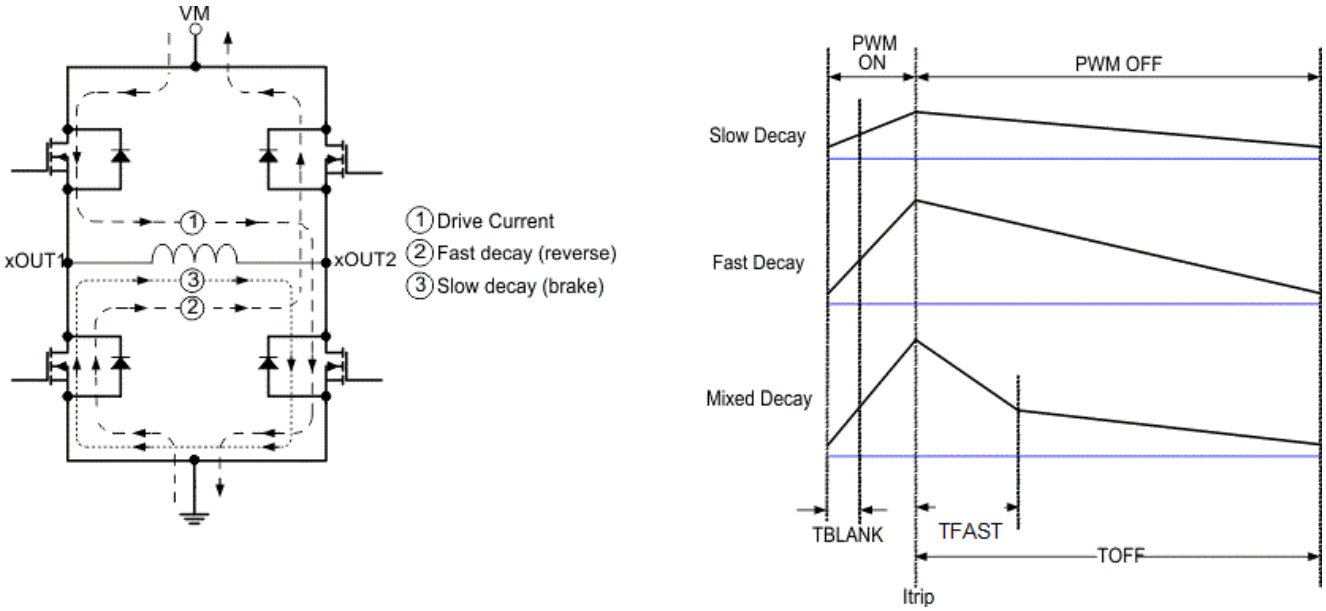

图 7-6. Decay Modes

The decay mode of the DRV8434 is selected by the DECAY0 and DECAY1 pins as shown in 表 7-6. If DECAY1 pin is Hi-Z, irrespective of the DECAY0 pin voltage, the decay mode will be smart tune dynamic decay. The decay modes can be changed on the fly. After a decay mode change, the new decay mode is applied after a 10 µs de-glitch time.

表 7-6. Decay Mode Settings

DECAY0	DECAY1	INCREASING STEPS	DECREASING STEPS
0	0	Smart tune Dynamic Decay	Smart tune Dynamic Decay
0	1	Smart tune Ripple Control	Smart tune Ripple Control
1	0	Mixed decay: 30% fast	Mixed decay: 30% fast
1	1	Slow decay	Mixed decay: 30% fast
Hi-Z	0	Mixed decay: 60% fast	Mixed decay: 60% fast
Hi-Z	1	Slow decay	Slow decay

图 7-7 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

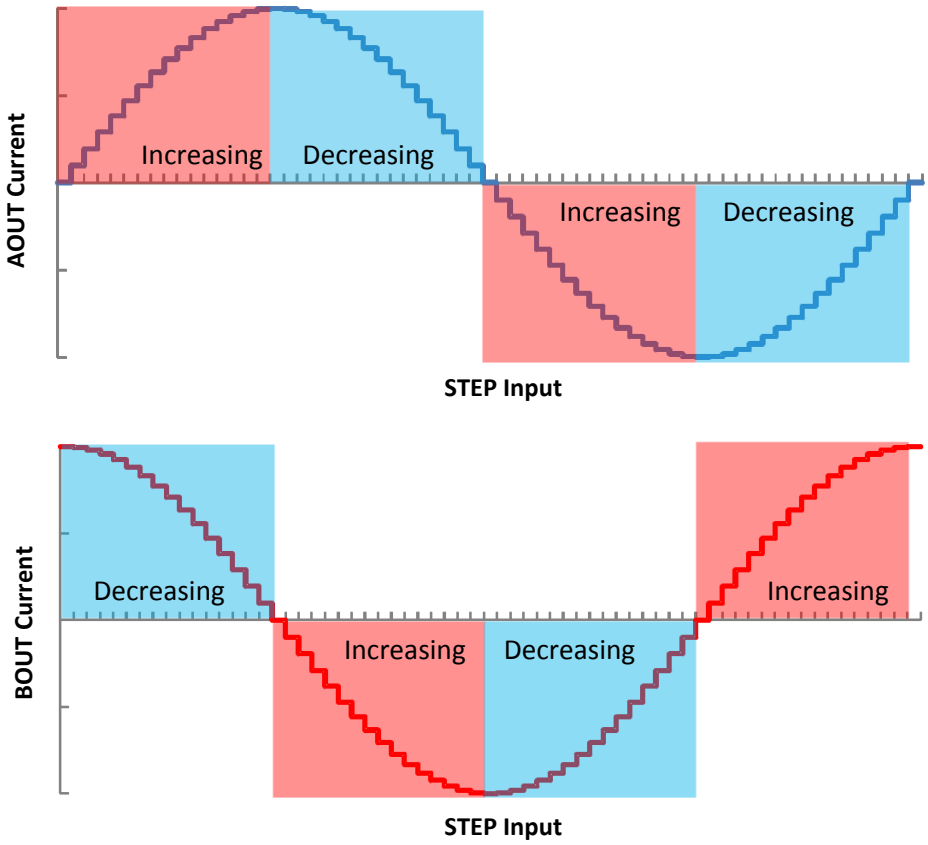

图 7-7. Definition of Increasing and Decreasing Steps

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7.3.6.1 Slow Decay for Increasing and Decreasing Current

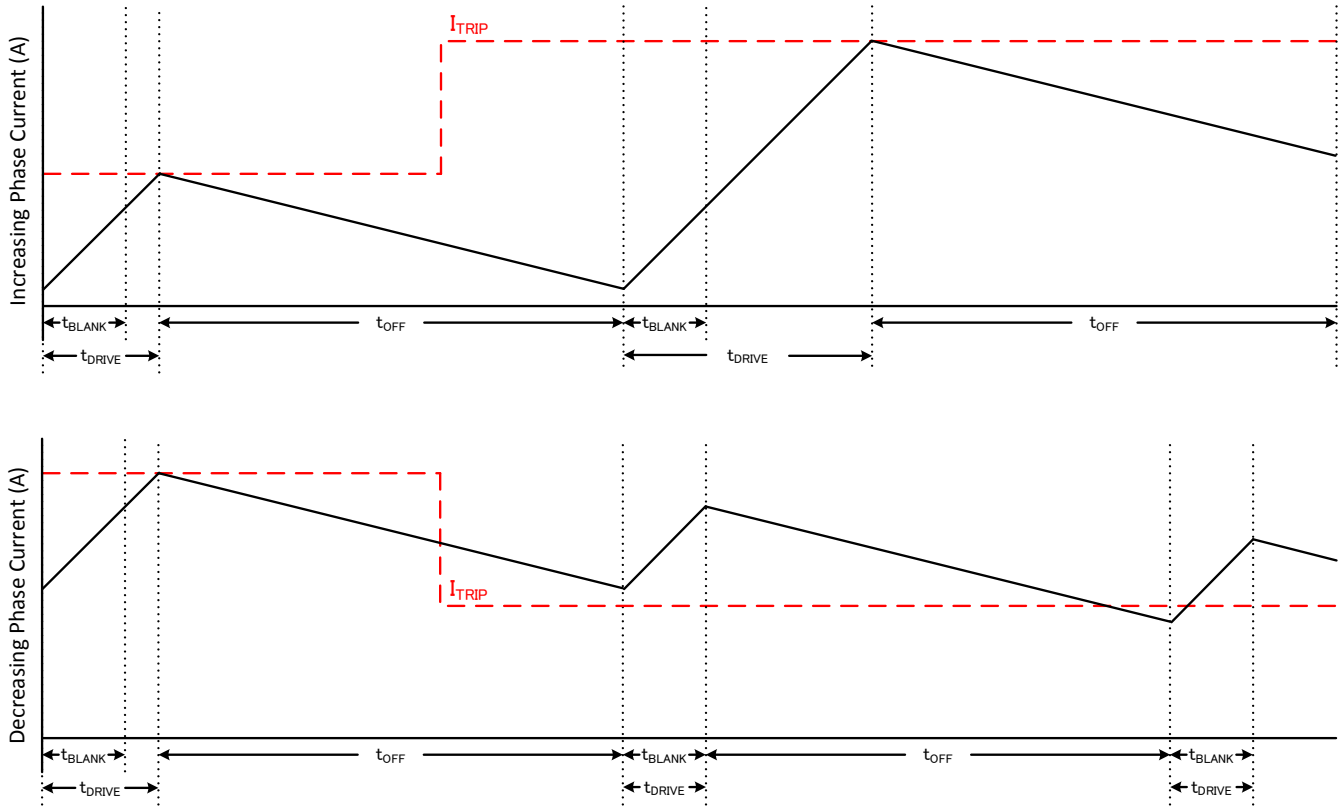

图 7-8. Slow/Slow Decay Mode

During slow decay, both low-side MOSFETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly. If the current at the end of the off time is above the I_{TRIP} level, slow decay will be extended for multiple off time duration, until the current at the end of the cumulative off time is below the I_{TRIP} level.

When the winding current is held static for a long time (for example while no STEP input is present), or at very low step rates, slow decay may not properly regulate the current because back-EMF will be small or absent across the motor windings. The motor current can rise rapidly, and may require an extremely long off-time. In some cases this could result in loss of current regulation. An aggressive decay mode is recommended in such cases.

7.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

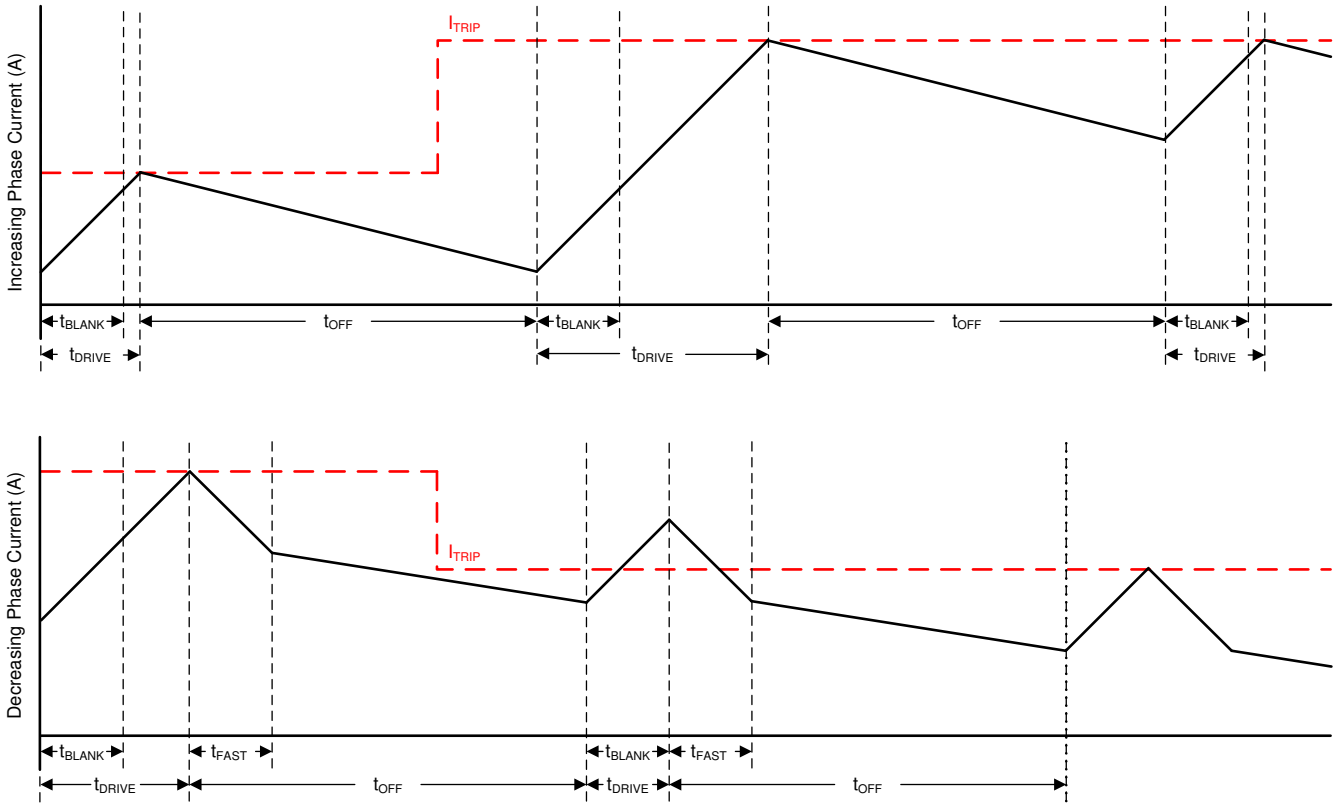

图 7-9. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF}, followed by slow decay for the remainder of the t_{OFF} time. Mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This decay mode exhibits the same current ripple as slow decay mode does for increasing current, because for increasing current, only slow decay is used in this mode. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

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7.3.6.3 上升和下降电流阶段均为混合衰减

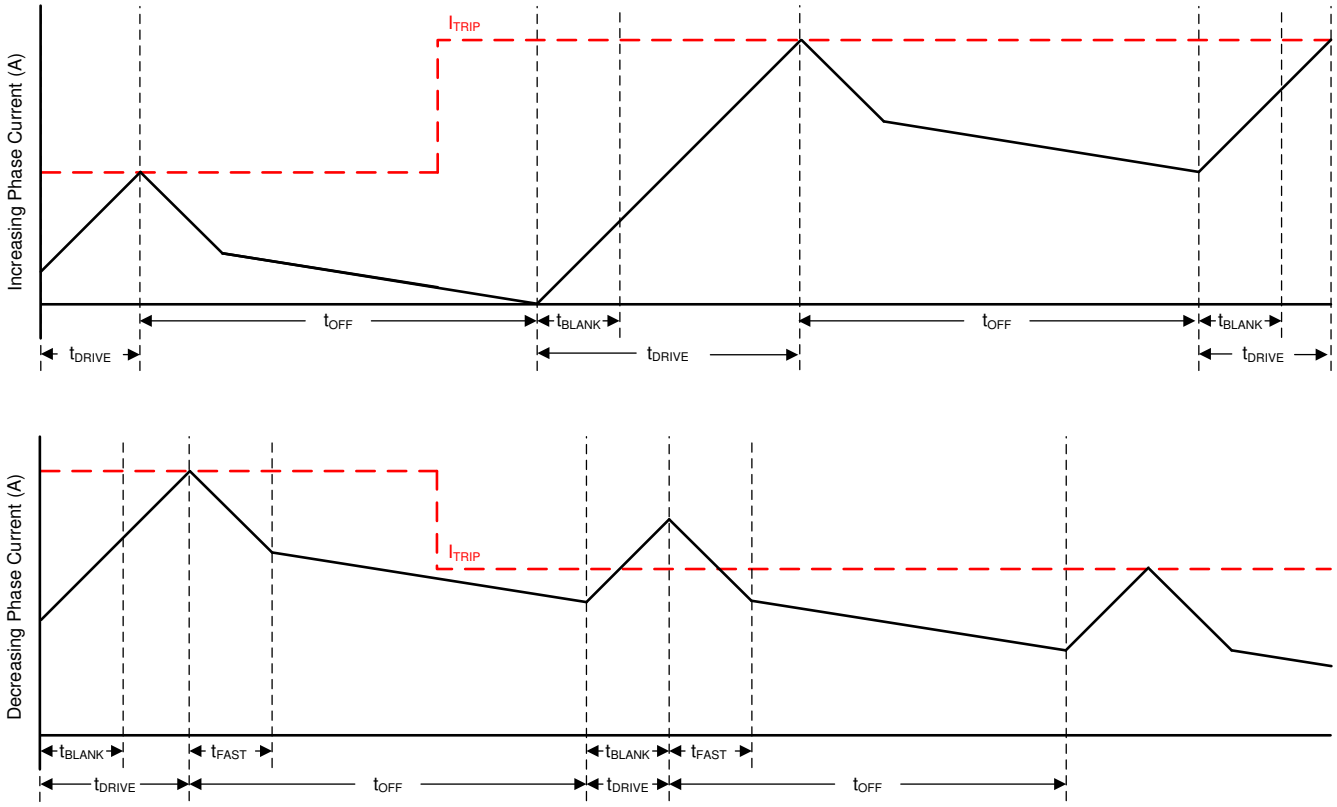

图 7-10. 混合-混合衰减模式

混合衰减下，开始的一段时间为快速衰减，然后在剩余的 t_{OFF} 内慢速衰减。在此模式下，上升和下降电流阶跃都会发生混合衰减。

该模式表现出的纹波比慢速衰减大，但比快速衰减小。在下降电流阶跃时，混合衰减可比慢速衰减更快地稳定到新的 I_{TRIP} 电平。

如果电流保持很长时间（STEP 引脚无输入）或步进速度非常慢，则慢速衰减可能无法正确调节电流，因为电机绕组上不存在反电动势。在这种状态下，电机电流上升速度会非常快，需要极长的关断时间。当电机绕组上没有反电动势时，上升或下降混合衰减模式能持续调节电流电平。

7.3.6.4 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

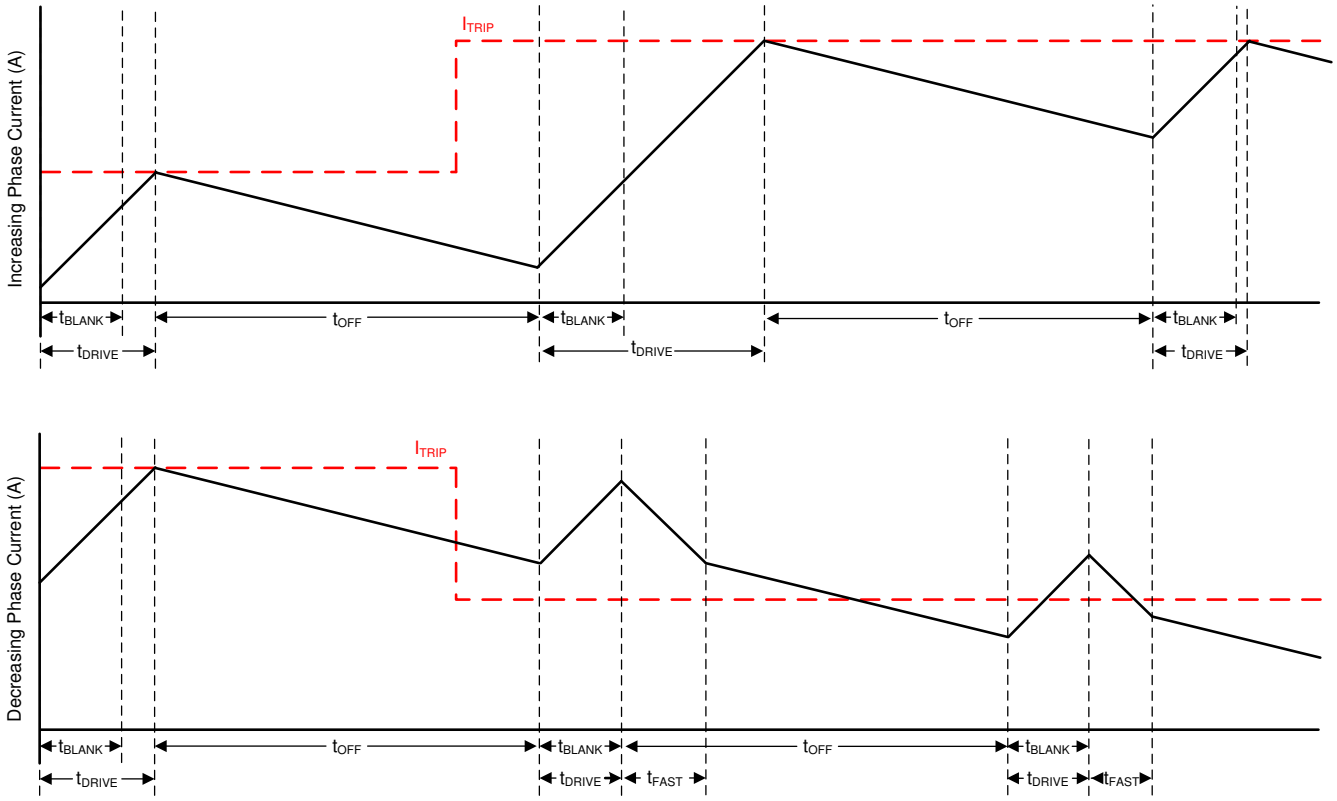

图 7-11. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

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7.3.6.5 智能调优纹波控制

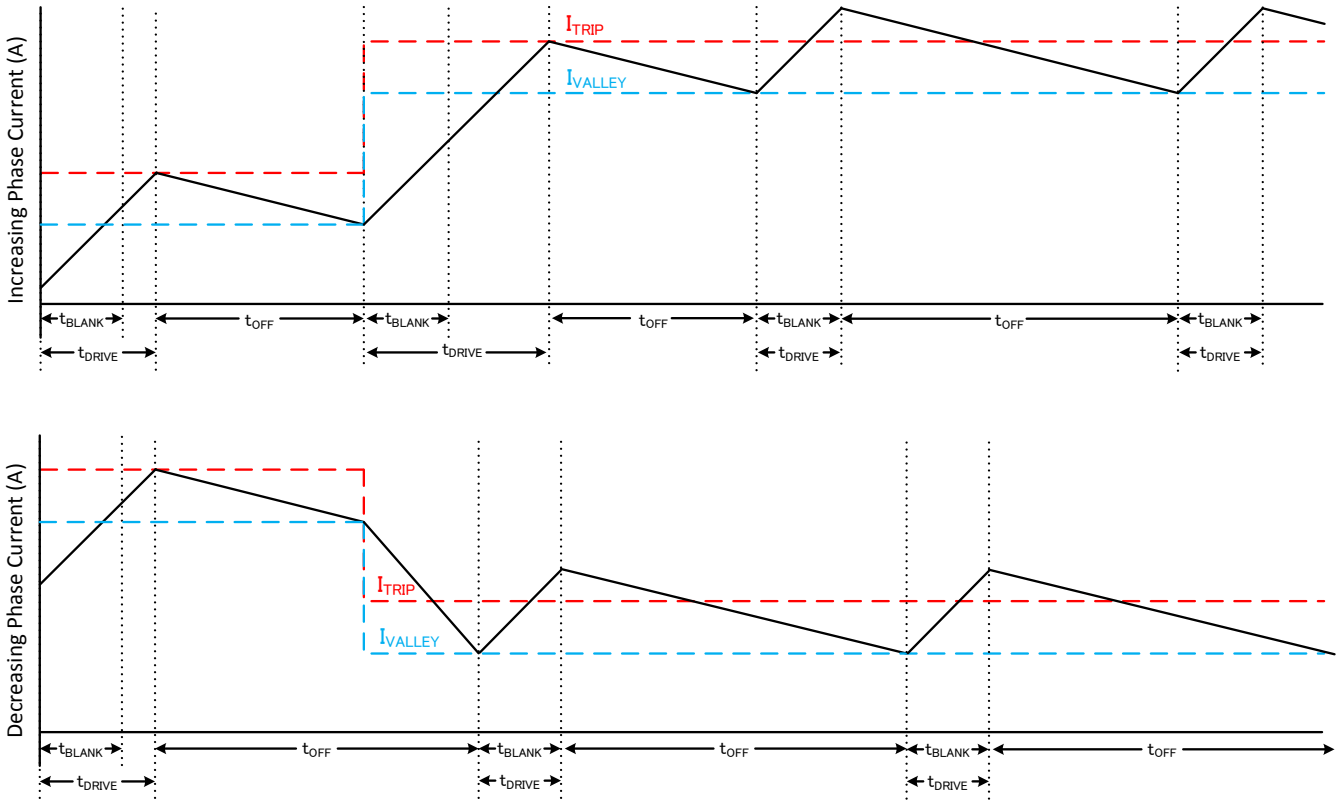

图 7-12. 智能调优纹波控制衰减模式

智能调优纹波控制通过在 I_{TRIP} 电平旁设置一个 I_{VALLEY} 电平来进行操作。当电流电平达到 I_{TRIP} 时，驱动器将进入慢速衰减，直到达到 I_{VALLEY}，而不是直到 t_{OFF} 时间结束。慢速衰减的工作原理类似于模式 1，其中两个低侧 MOSFET 都导通，允许电流再循环。在此模式下，t_{OFF} 根据电流电平和运行条件而变化。

通过 TOFF 引脚对该衰减模式下的纹波电流进行编程。纹波电流取决于特定微步进级别的 ITRIP。

表 7-7. 电流纹波设置

TOFF	特定微步进级别下的电流纹波
0	19mA + ITRIP 的 1%
1	19mA + ITRIP 的 2%
高阻态	19mA + ITRIP 的 4%
330kΩ 至 GND	19mA + ITRIP 的 6%

该纹波控制方法可以更严格地调节电流电平，从而提高电机效率和系统性能。智能调优纹波控制适用于能够承受可变关断时间调节方案的系统，以在电流调节中实现小电流纹波。选择低纹波电流设置可确保 PWM 频率不处于可闻范围之内。不过，较高的纹波电流值会降低 PWM 频率，从而降低开关损耗。

7.3.6.6 PWM 关断时间

除智能调优纹波控制模式外，TOFF 引脚将配置所有衰减模式的 PWM 关断时间，如表 7-8 所示。该器件支持动态更改关断时间。在更改关断时间设置后，新的关断时间设置将在 10μs 的抗尖峰脉冲时间之后生效。

表 7-8. 关断时间设置

TOFF	关断时间
0	7μs

表 7-8. 关断时间设置 (continued)

TOFF	关断时间
1	16μs
Hi-Z	24μs
330kΩ 至 GND	32μs

7.3.6.7 消隐时间

在 H 桥接通电流（驱动阶段开始）后，电流检测比较器将在启用电流检测电路前被忽略一段时间 (t_{BLANK})。消隐时间还将设置 PWM 的最小驱动时间。消隐时间大约为 1μs。

7.3.7 电荷泵

集成了一个电荷泵以提供高侧 N 沟道 MOSFET 栅极驱动电压。需要在 VM 和 VCP 引脚之间为电荷泵放置一个电容作为储能电容。此外，还需要在 CPH 和 CPL 引脚之间放置一个陶瓷电容作为飞跨电容。

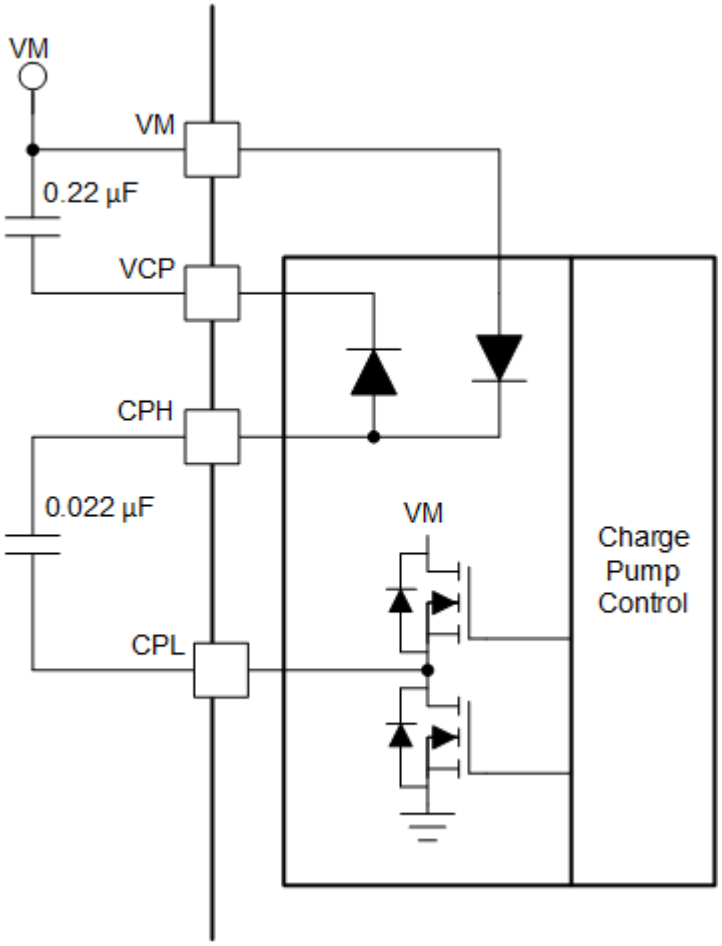

图 7-13. 电荷泵方框图

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7.3.8 线性稳压器

DVDD 器件中集成了一个线性稳压器。DVDD 稳压器可用于提供 VREF 基准电压。DVDD 最大可提供 2mA 的负载。为确保正常运行，请使用陶瓷电容器将 DVDD 引脚旁路至 GND。

DVDD 输出的标称值为 5V。当 DVDD LDO 电流负载超过 2mA 时，输出电压会显著下降。

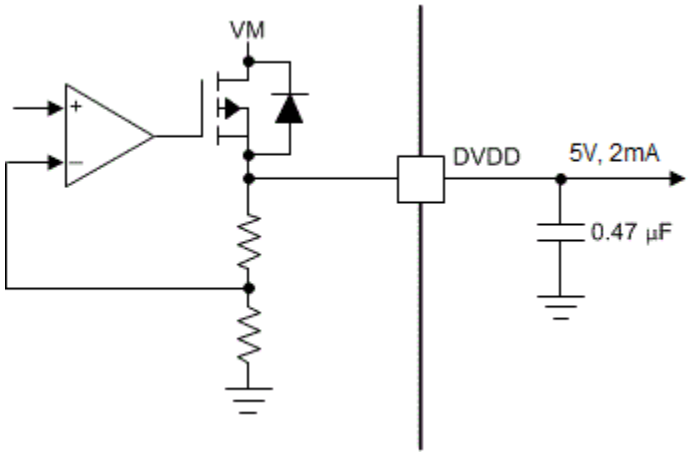

图 7-14. 线性稳压器方框图

如果数字输入必须永久连接高电平（即 Mx、DECAYx 或 TOFF），则最好将输入连接到 DVDD 引脚而不是外部稳压器。在未应用 VM 引脚或处于睡眠模式时，此方法可省电：DVDD 稳压器被禁用，电流不会流经输入下拉电阻。逻辑电平输入的典型下拉电阻为 200kΩ。

请勿将 nSLEEP 引脚连接至 DVDD，否则器件将无法退出睡眠模式。

7.3.9 Logic Level, Tri-Level and Quad-Level Pin Diagrams

图 7-15 shows the input structure for M0, DECAY0 and ENABLE pins.

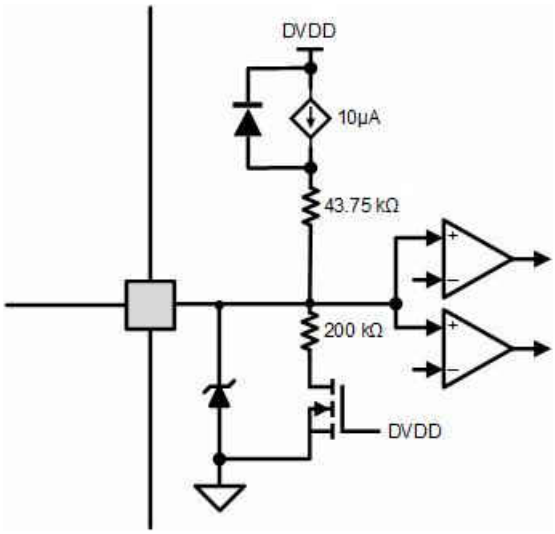

图 7-15. Tri-Level Input Pin Diagram

图 7-16 shows the input structure for DECAY1 pin.

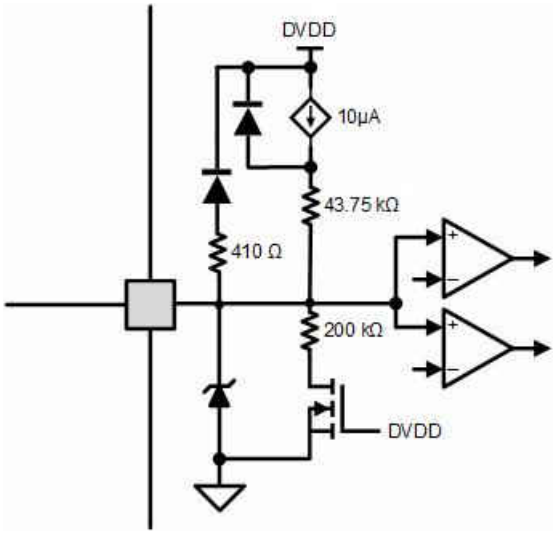

图 7-16. DECAY1 Pin Diagram

图 7-17 shows the input structure for M1 and TOFF pins.

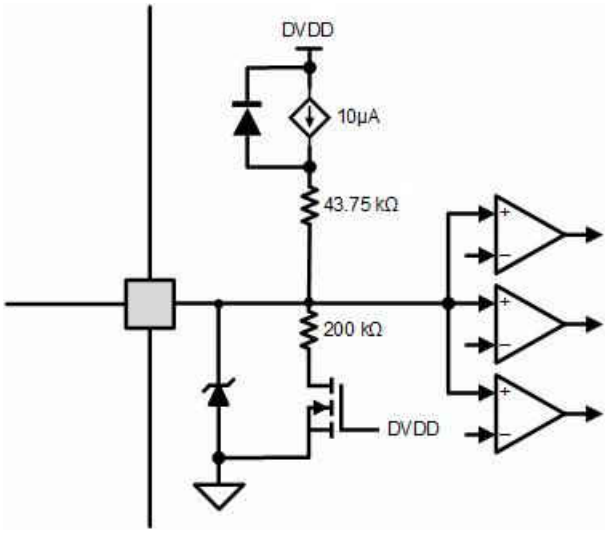

图 7-17. Quad-Level Input Pin Diagram

图 7-18 shows the input structure for STEP, DIR and nSLEEP pins.

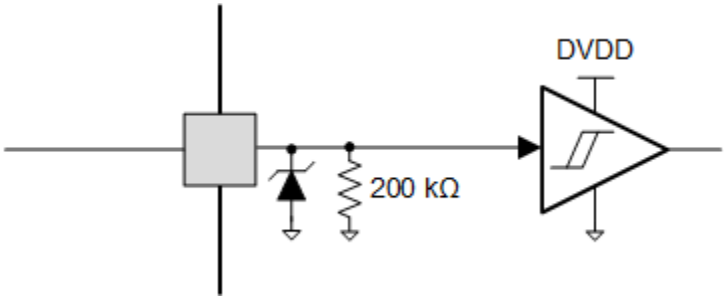

图 7-18. Logic-Level Input Pin Diagram

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7.3.9.1 nFAULT 引脚

nFAULT 引脚具有开漏输出且应上拉至 5V、3.3V 或 1.8V 电源电压。当检测到故障时，nFAULT 引脚将变成逻辑低电平；上电后，则变成高电平。对于 5V 上拉，nFAULT 引脚可通过一个电阻连接至 DVDD 引脚。对于 3.3V 或 1.8V 上拉，必须使用一个外部电源。

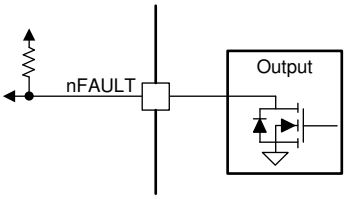

图 7-19. nFAULT 引脚

7.3.10 保护电路

DRV8434 器件可完全防止电源欠压、电荷泵欠压、输出过流、开路负载和器件过热事件。

7.3.10.1 VM 欠压锁定 (UVLO)

无论 VM 引脚电压何时降至电源电压的 UVLO 阈值电压以下，都会禁用所有输出并将 nFAULT 引脚驱动为低电平。在这种情况下，电荷泵会禁用。VM 欠压条件消失后，器件将恢复正常运行（电机驱动器运行并释放 nFAULT 引脚）。

7.3.10.2 VCP 欠压锁定 (CPUV)

无论 VCP 引脚电压何时降至 CPUV 电压以下，都会禁用所有输出并将 nFAULT 引脚驱动为低电平。在这种情况下，电荷泵将保持有效状态。VCP 欠压条件消失后，器件将恢复正常运行（电机驱动器运行且释放 nFAULT 引脚）。

7.3.10.3 过流保护 (OCP)

每个 MOSFET 上的模拟电流限制电路通过移除栅极驱动来限制通过 MOSFET 的电流。如果此电流限制的持续时间超过 t_{OCP}，则会禁用两个 H 桥中的 MOSFET 并将 nFAULT 引脚驱动为低电平。在这种情况下，电荷泵将保持运行状态。过流保护可在两种不同的模式下运行：锁存关断和自动重试。该器件支持动态更改工作模式。

7.3.10.3.1 锁存关断

必须将 ENABLE 引脚设置为高阻态，才能选择锁存关断模式。在此模式下，OCP 事件后将会禁用输出并将 nFAULT 引脚驱动为低电平。一旦 OCP 条件消除，器件会在应用 nSLEEP 复位脉冲或下电上电后恢复正常运行。

7.3.10.3.2 自动重试

必须将 ENABLE 引脚设置为高电平 (>2.7V)，才能选择自动重试模式。在此模式下，OCP 事件后将会禁用输出并将 nFAULT 引脚驱动为低电平。在经过 t_{RETRY} 时间且故障条件消失后，器件将自动恢复正常运行（电机驱动器运行且释放 nFAULT 引脚）。

7.3.10.4 开路负载检测 (OL)

如果任何线圈中的绕组电流降至开路负载电流阈值 (I_{OL}) 和分度器设置的 I_{TRIP} 电平之下，并且持续时长超过开路负载检测时间 (t_{OL})，则表明检测到开路负载条件。

ENABLE 引脚连接到 DVDD 后，如果开路负载条件消失，nFAULT 线路会被立即释放。ENABLE 引脚为高阻态时，如果开路负载条件消失，并且已应用 nSLEEP 复位脉冲，nFAULT 线路会被释放。当器件下电上电或退出睡眠模式时，该故障也会清除。

7.3.10.5 热关断 (OTSD)

如果内核温度超过热关断限值 (T_{OTSD})，则会禁用 H 桥中的所有 MOSFET 并将 nFAULT 引脚驱动为低电平。在这种情况下，电荷泵会被禁用。热关断保护可在两种不同的模式下运行：锁存关断和自动重试。该器件支持动态更改工作模式。

7.3.10.5.1 锁存关断

必须将 ENABLE 引脚设置为高阻态，才能选择锁存关断模式。在此模式下，OTSD 事件后将会禁用相关输出并将 nFAULT 引脚驱动为低电平。结温降至过热阈值限值减去迟滞 (T_{OTSD} – T_{HYS_OTSD}) 所得的值以下后，器件会在应用 nSLEEP 复位脉冲或功率循环后恢复正常运行。

7.3.10.5.2 自动重试

必须将 ENABLE 引脚设置为高电平 (>2.7V)，才能选择自动重试模式。在此模式下，OTSD 事件后将会禁用所有输出并将 nFAULT 引脚驱动为低电平。结温降至过热阈值限值减去迟滞 (T_{OTSD} – T_{HYS_OTSD}) 所得的值以下后，器件将恢复正常运行（电机驱动器运行且释放 nFAULT 线路）。

Fault Condition Summary

表 7-9. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT	Disabled	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	—	nFAULT	Disabled	Operating	Operating	Operating	Automatic: VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	ENABLE = Hi-Z	nFAULT	Disabled	Operating	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	—	nFAULT	Operating	Operating	Operating	Operating	Report only
Thermal Shutdown (OTSD)	T_J > T_{TSD}	ENABLE = Hi-Z	nFAULT	Disabled	Disabled	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 器件功能模式

7.4.1 睡眠模式 (nSLEEP = 0)

DRV8434 器件将通过 nSLEEP 引脚实现状态管理。当 nSLEEP 引脚为低电平时，DRV8434 器件将进入低功耗睡眠模式。在睡眠模式下，将会禁用所有内部 MOSFET 和电荷泵。必须在 nSLEEP 引脚触发下降沿之后再过去 t_{SLEEP} 时间后，器件才能进入睡眠模式。如果 nSLEEP 引脚变为高电平，DRV8434 器件会自动退出睡眠模式。必须在经过 t_{WAKE} 时间之后，器件才能针对输入做好准备。

7.4.2 禁用模式（nSLEEP = 1，ENABLE = 0）

ENABLE 引脚用于启用或禁用 DRV8434。当 ENABLE 引脚为低电平时，输出驱动器将在高阻态状态下被禁用。

7.4.3 工作模式（nSLEEP = 1，ENABLE = Hi-Z/1）

当 nSLEEP 引脚为高电平、ENABLE 引脚为 Hi-Z 或 1 且 VM > UVLO 时，器件将进入运行模式。必须在经过 t_{WAKE} 时间之后，器件才能针对输入做好准备。

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7.4.4 nSLEEP 复位脉冲

锁存故障可通过 nSLEEP 复位脉冲清除。该脉冲的宽度必须在 20μs 至 40μs 之间。如果 nSLEEP 在 40μs 至 120μs 的时间内保持低电平，则会清除故障，但器件有可能会关断，也有可能不关断，如时序图中所示（请参阅图 7-20）。该复位脉冲不影响电荷泵或其他功能块的状态。

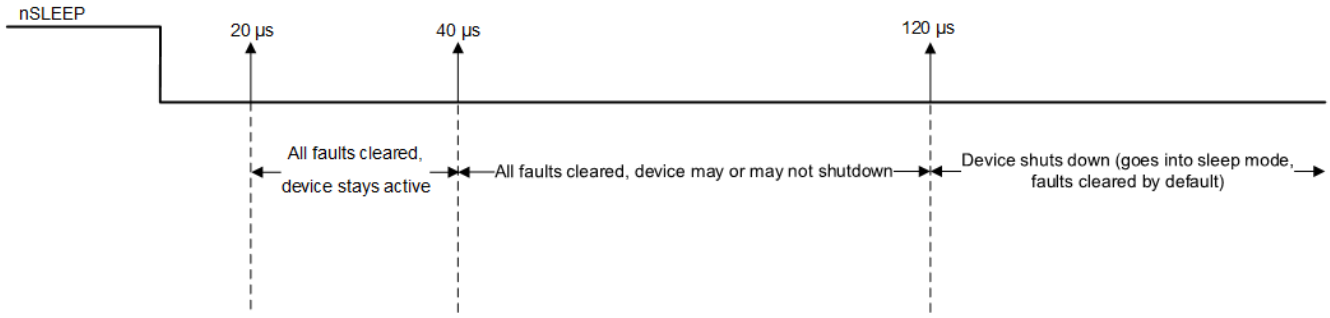

图 7-20. nSLEEP 复位脉冲

功能模式汇总

表 7-10 汇总了所有功能模式。

表 7-10. 功能模式汇总

条件		配置	H 桥	DVDD 稳压器	电荷泵	分度器	逻辑
睡眠模式	4.5V < VM < 48V	nSLEEP 引脚 = 0	禁用	禁用	禁用	禁用	禁用
工作	4.5V < VM < 48V	nSLEEP 引脚 = 1 ENABLE 引脚 = 1 或高阻态	工作	工作	工作	工作	工作
禁用	4.5V < VM < 48V	nSLEEP 引脚 = 1 ENABLE 引脚 = 0	禁用	工作	工作	工作	工作

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV8434 is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8434.

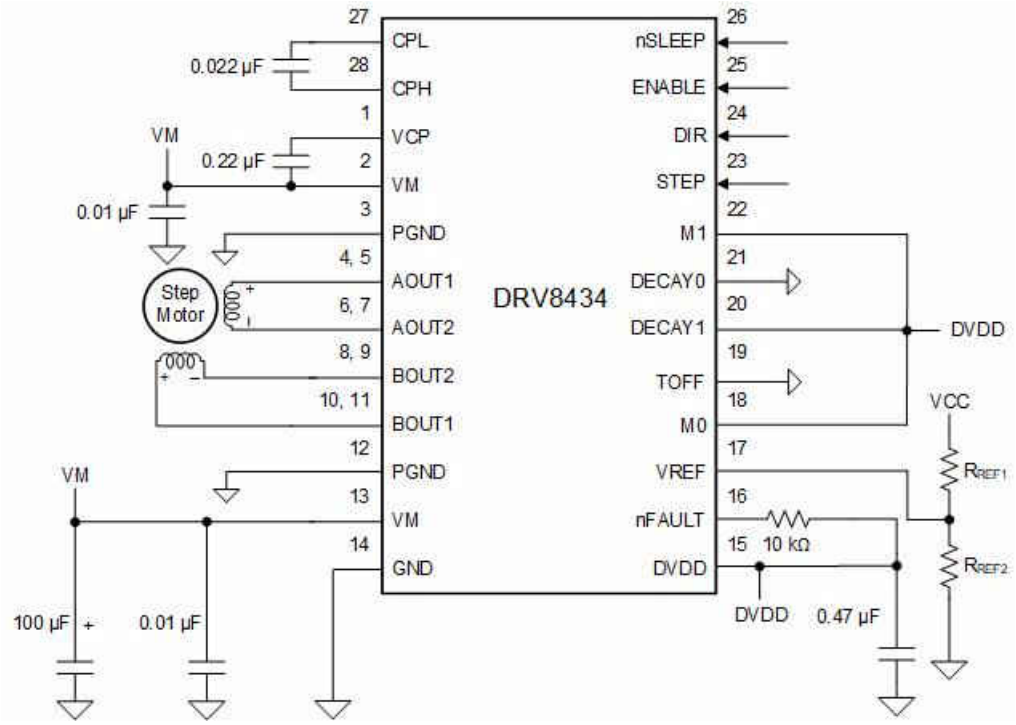

图 8-1. Typical Application Schematic (1/8 microstepping, smart tune Ripple Control Decay, HTSSOP package)

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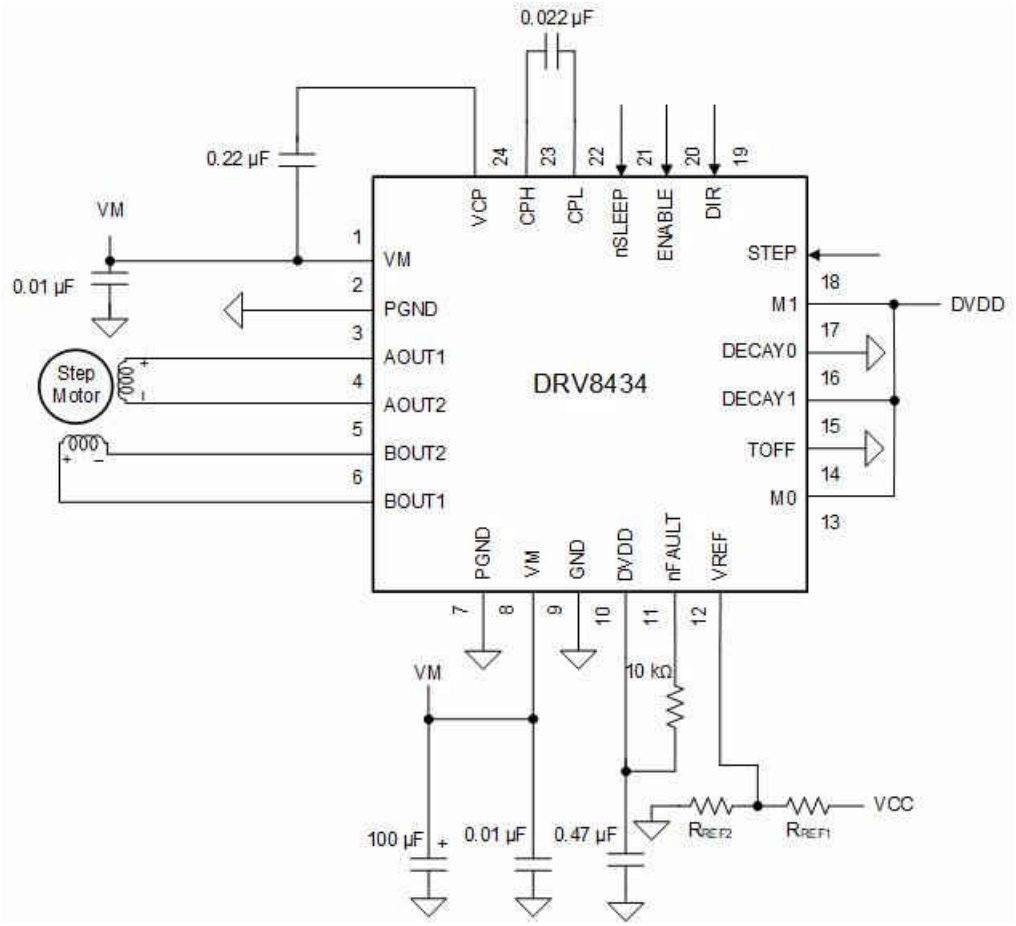

图 8-2. Typical Application Schematic (1/8 microstepping, smart tune Ripple Control Decay, VQFN package)

8.2.1 Design Requirements

表 8-1 lists the design input parameters for system design.

表 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.9 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	18.75 rpm
Target full-scale current	I_{FS}	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8434 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target

speed. Use 方程式 1 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps / s}) = \frac{v\ (\text{rpm}) \times 360\ (°/\text{rot})}{\theta_{step}\ (°/\text{step}) \times n_m\ (\text{steps / microstep}) \times 60\ (\text{s / min})} \tag{1}$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor. For example, the motor in this application is required to rotate at 1.8°/step for a target of 18.75 rpm at 1/8 microstep mode. Using 方程式 1, f_{step} can be calculated as 500 Hz.

The microstepping level is set by the M0 and M1 pins and can be any of the settings listed in 表 8-2. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed.

表 8-2. Microstepping Indexer Settings

MODE0	MODE1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

8.2.2.2 电流调节

在步进电机中，满量程电流 (I_{FS}) 是通过任一绕组的最大电流。该值大小取决于 VREF 电压和 TRQ_DAC 设置，如方程式 2 所示。

VREF 引脚上允许的最大电流为 3.3V。DVDD 可用于通过电阻分压器提供 VREF。

在步进期间，I_{FS} 定义了最大电流步进的电流斩波阈值 (I_{TRIP})。

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_V(V/A)} \times \text{TRQ_DAC}(\%) = \frac{V_{REF}(V) \times \text{TRQ_DAC}(\%)}{1.32(V/A)} \tag{2}$$

8.2.2.3 衰减模式

DRV8434A 以智能调优纹波控制衰减模式运行。当电机绕组电流达到电流斩波阈值 (I_{TRIP}) 时，DRV8434A 会将绕组置于慢速衰减模式下。

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8.2.2.4 应用曲线

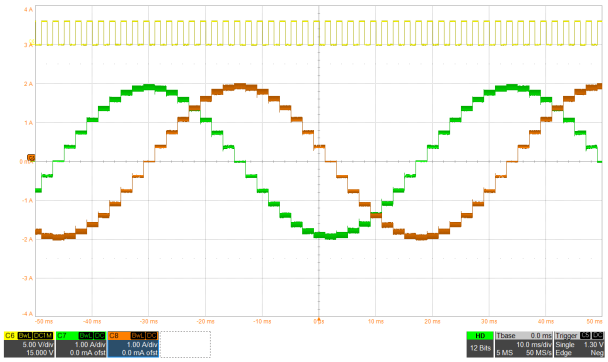

图 8-3. 智能调优纹波控制衰减下的 1/8 微步进

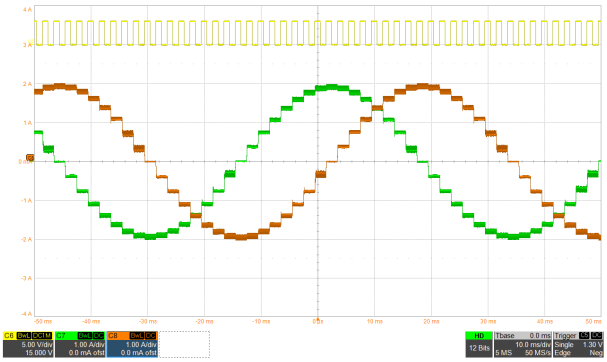

图 8-4. 智能调优动态衰减下的 1/8 微步进

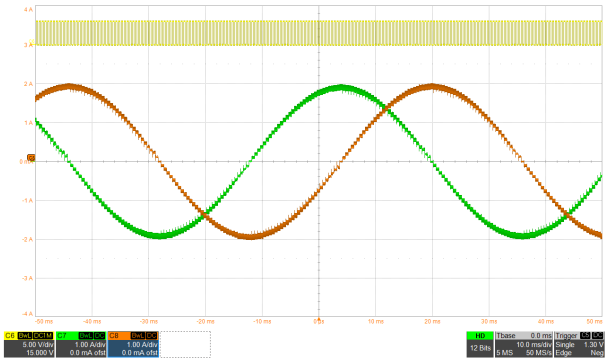

图 8-5. 智能调优纹波控制衰减下的 1/32 微步进

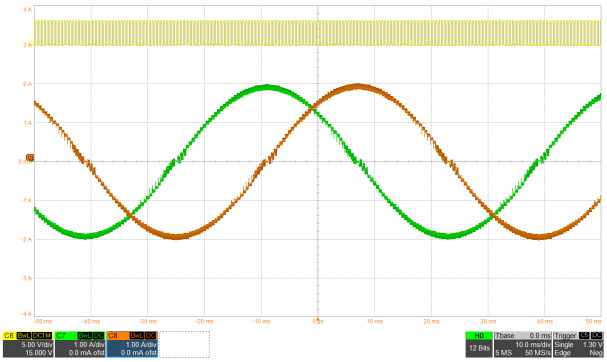

图 8-6. 智能调优动态衰减下的 1/32 微步进

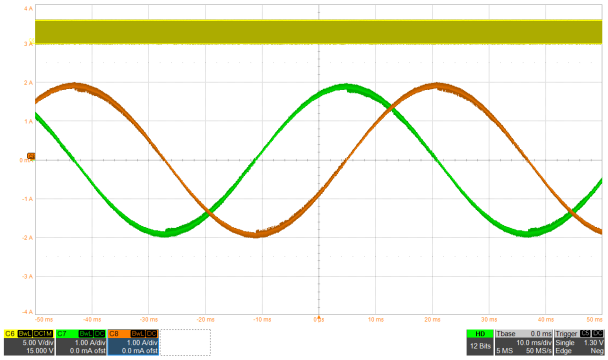

图 8-7. 智能调优纹波控制衰减下的 1/256 微步进

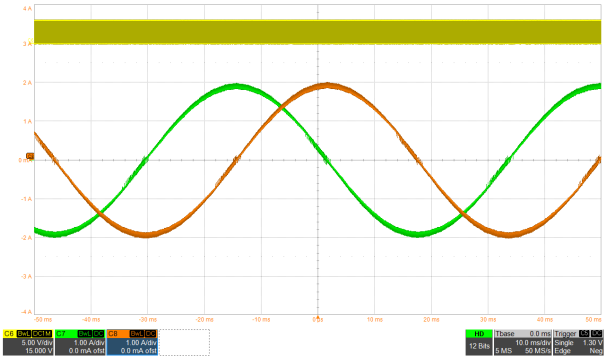

图 8-8. 智能调优动态衰减下的 1/256 微步进

8.2.2.5 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

8.2.2.5.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

8.2.2.5.2 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in 方程式 3.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (3)$$

The conduction loss for the typical application shown in 表 8-1 is calculated in 方程式 4.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (2\text{-A} / \sqrt{2})^2 \times (0.165\text{-}\Omega + 0.165\text{-}\Omega) = 1.32\text{-W} \quad (4)$$

备注

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.2.5.3 Switching Loss

The power loss due to the PWM switching frequency depends on the slew rate (t_{SR}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in 方程式 5 and 方程式 6.

$$P_{SW_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE_PWM} \times f_{PWM} \quad (5)$$

$$P_{SW_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL_PWM} \times f_{PWM} \quad (6)$$

Both t_{RISE_PWM} and t_{FALL_PWM} can be approximated as V_{VM}/ t_{SR}. After substituting the values of various parameters, and assuming 30-kHz PWM frequency, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW_RISE} = 0.5 \times 24\text{-V} \times (2\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.05\text{-W} \quad (7)$$

$$P_{SW_FALL} = 0.5 \times 24\text{-V} \times (1\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.05\text{-W} \quad (8)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW_RISE} + P_{SW_FALL}) = 2 \times (0.05\text{-W} + 0.05\text{-W}) = 0.2\text{-W} \quad (9)$$

备注

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (t_{SR}). This parameter is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.2.5.4 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (10)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (11)$$

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备注

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variation.

8.2.2.5.5 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in 方程式 12.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.32\text{-W} + 0.2\text{-W} + 0.12\text{-W} = 1.64\text{-W} \quad (12)$$

8.2.2.5.6 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 29.7 °C/W for the HTSSOP package and 39 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

$$T_J = 25°C + (1.64\text{-W} \times 29.7°C/W) = 73.71°C \quad (13)$$

The junction temperature for the VQFN package is calculated as shown below -

$$T_J = 25°C + (1.64\text{-W} \times 39°C/W) = 88.96\ °C \quad (14)$$

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-μF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 大容量电容

配备合适的局部大容量电容是电机驱动系统设计中的重要因素。使用更多的大容量电容通常是有益的，但缺点在于这会增加成本和物理尺寸。

所需的局部电容数量取决于多种因素，包括：

- 电机系统所需的最高电流
- 电源的电容和拉电流的能力
- 电源和电机系统之间的寄生电感量
- 可接受的电压纹波
- 使用的电机类型（有刷直流、无刷直流、步进电机）
- 电机制动方法

电源和电机驱动系统之间的电感将限制电流可以从电源变化的速率。如果局部大容量电容太小，系统将以电压变化的方式对电机中的电流不足或过剩电流作出响应。当使用足够多的大容量电容时，电机电压保持稳定，可以快速提供大电流。

数据表通常会给出建议值，但需要进行系统级测试来确定大小适中的大容量电容。

大容量电容的额定电压应高于工作电压，以在电机将能量传递给电源时提供裕度。

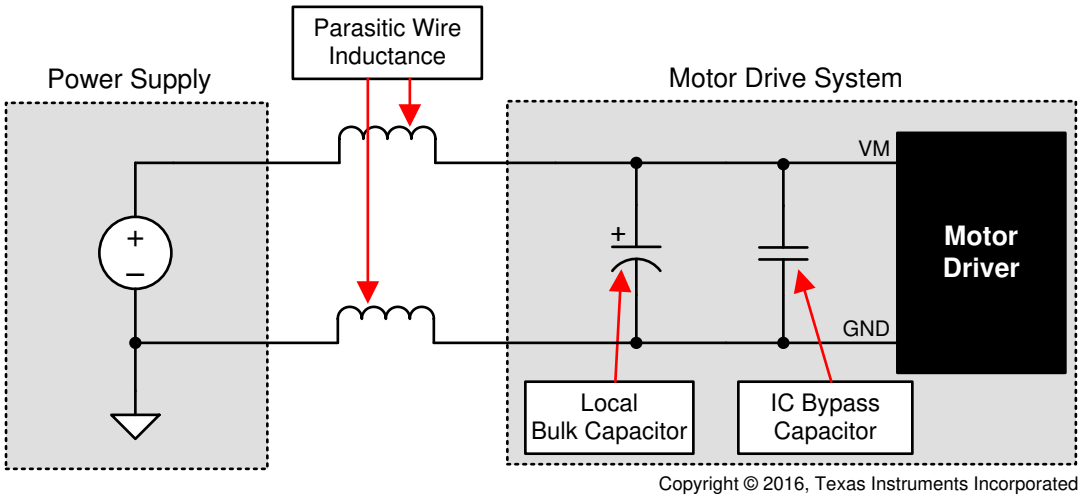

图 9-1. 带外部电源的电机驱动系统示例设置

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10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible..

10.2 Layout Example

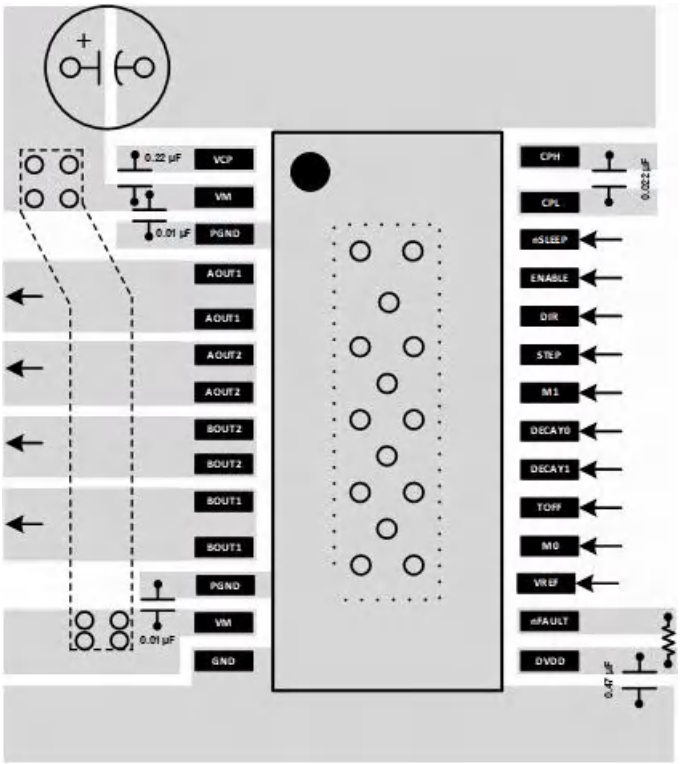

图 10-1. HTSSOP Layout Example

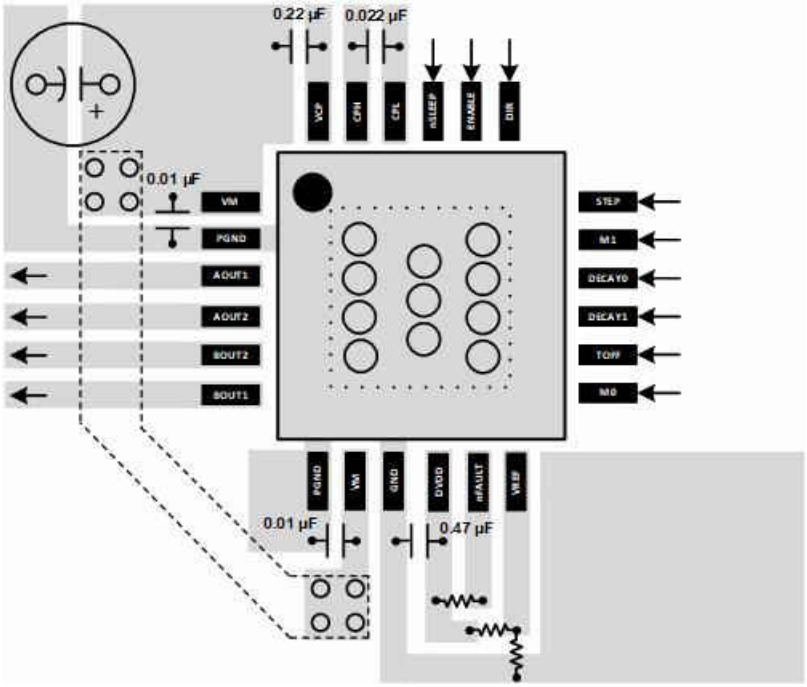

图 10-2. QFN Layout Example

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11 Device and Documentation Support

11.1 Related Documentation

- Texas Instruments, *How to Reduce Audible Noise in Stepper Motors* application report
- Texas Instruments, *How to Improve Motion Smoothness and Accuracy* application report
- Texas Instruments, *How to Drive Unipolar Stepper Motors with DRV8xxx* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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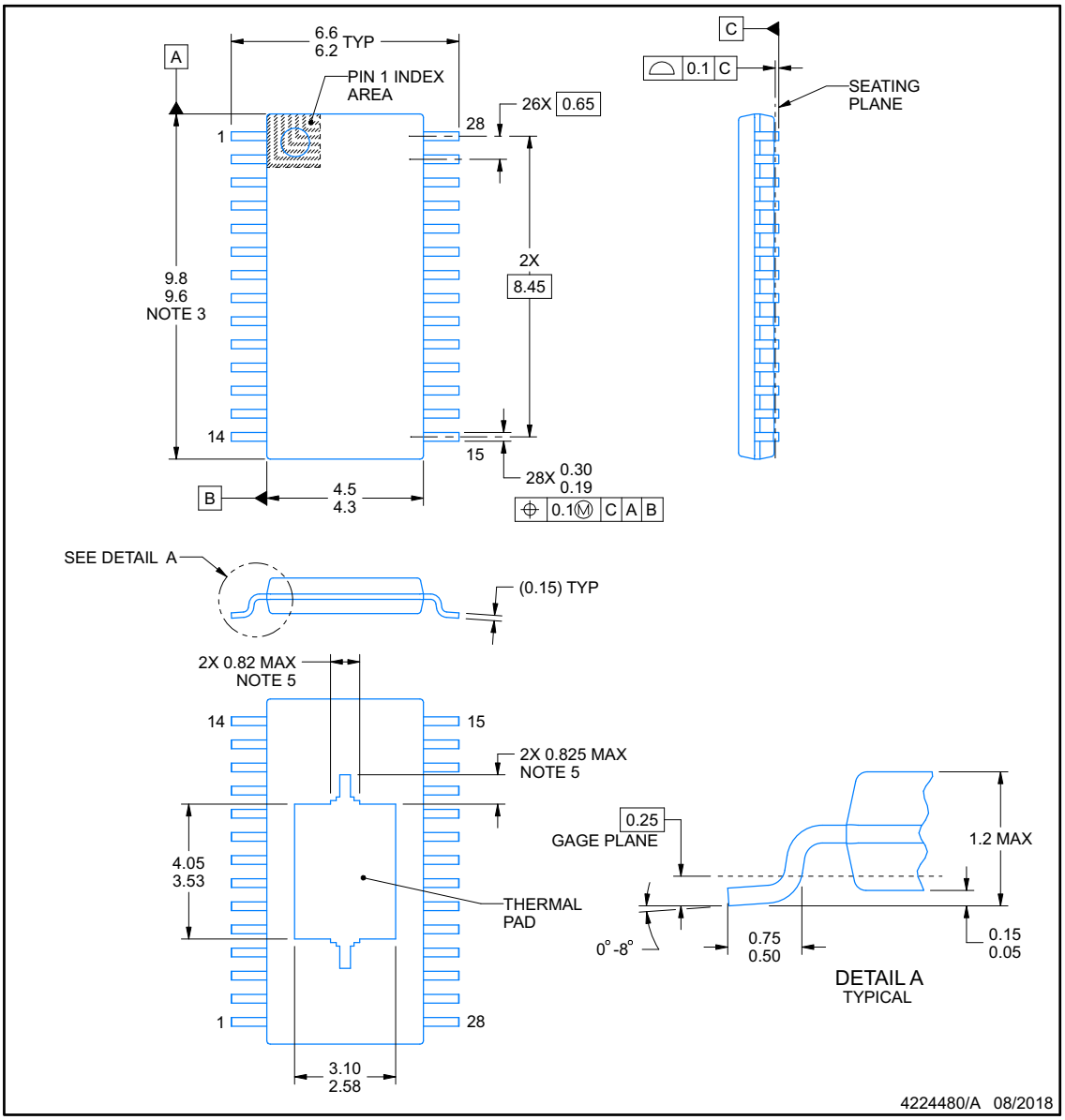
PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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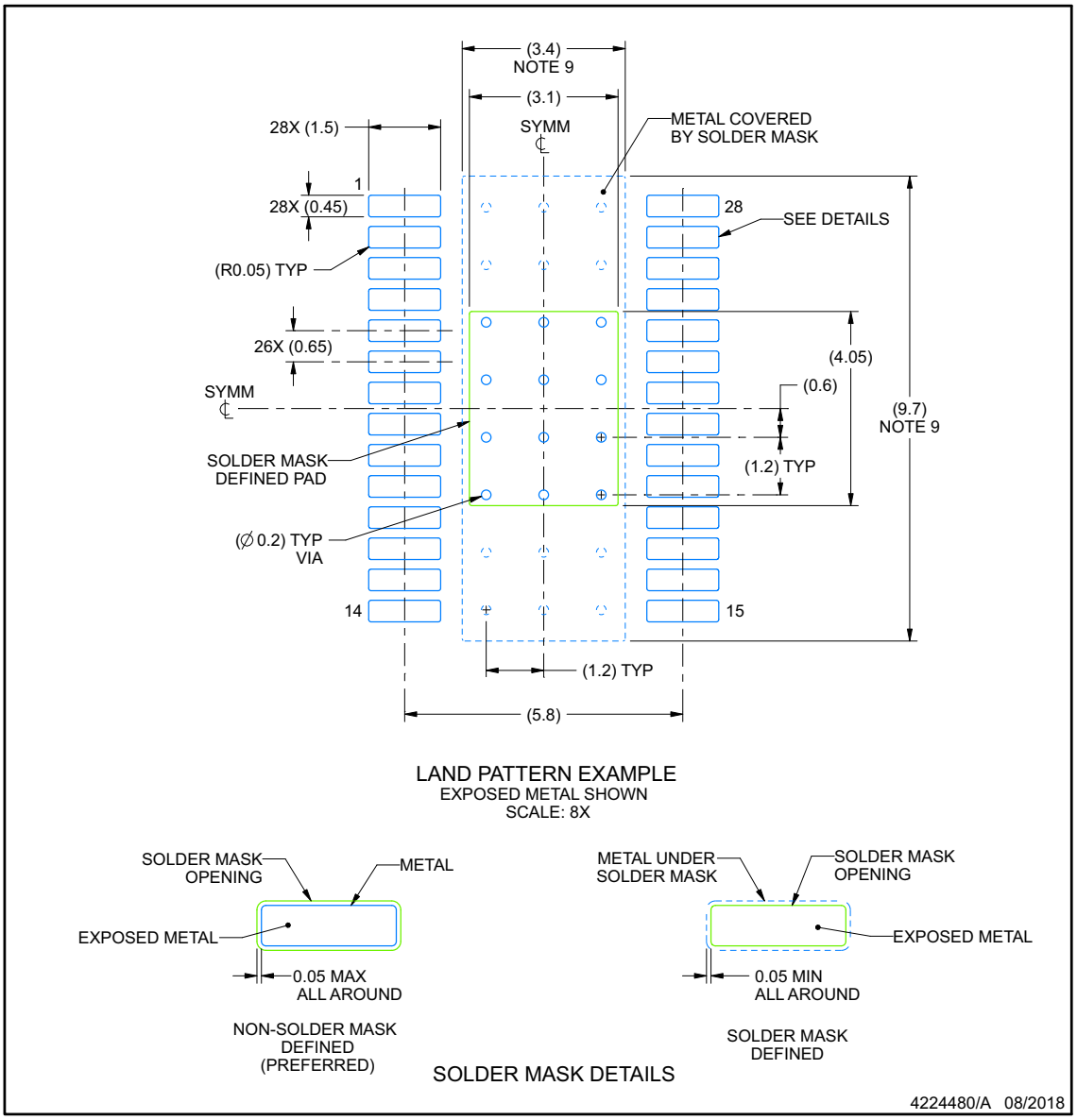
EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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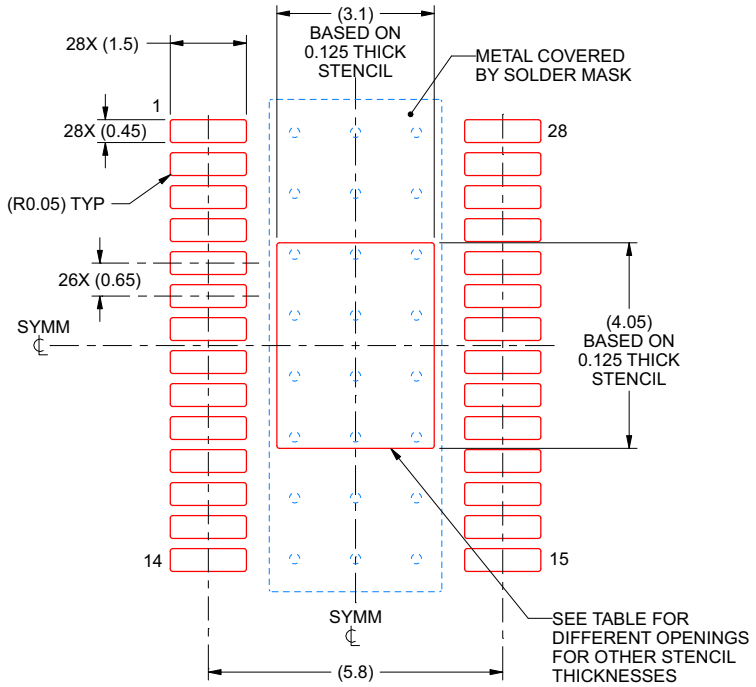
EXAMPLE STENCIL DESIGN

PWP0028M **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8434PWPR	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8434
DRV8434PWPR.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8434
DRV8434RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8434
DRV8434RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8434

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

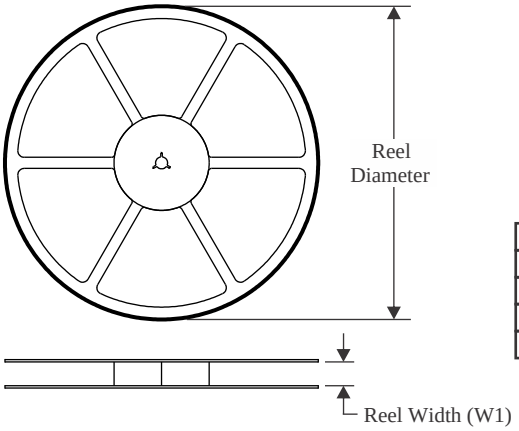
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

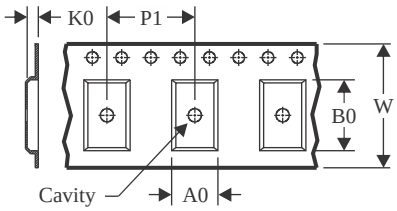
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

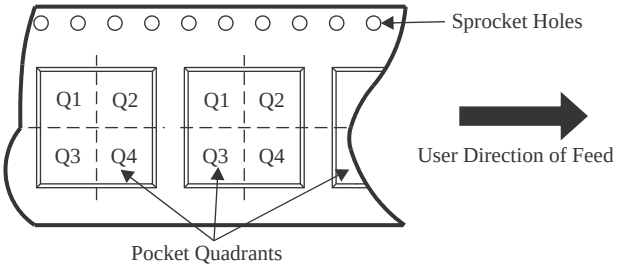


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

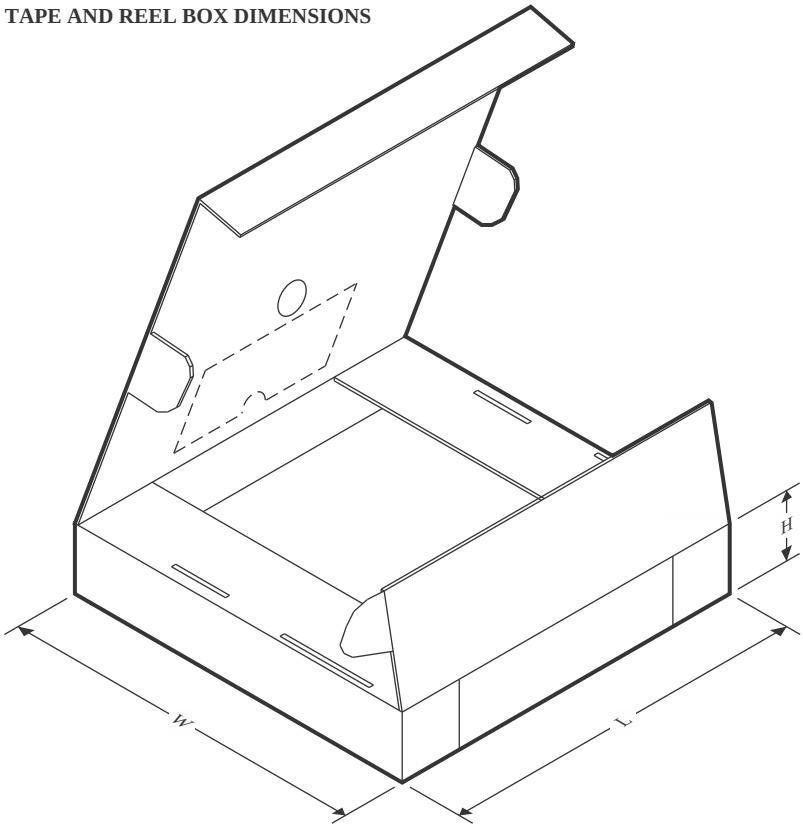
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8434PWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
DRV8434RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8434PWPR	HTSSOP	PWP	28	2500	353.0	353.0	32.0
DRV8434RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

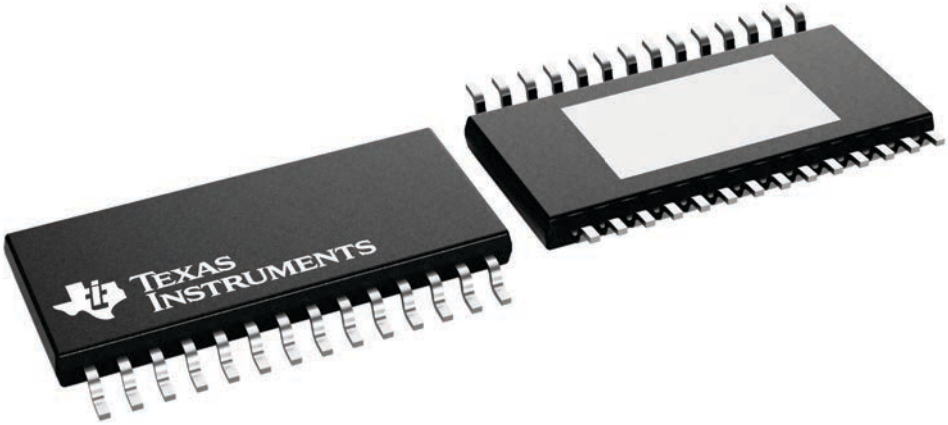
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

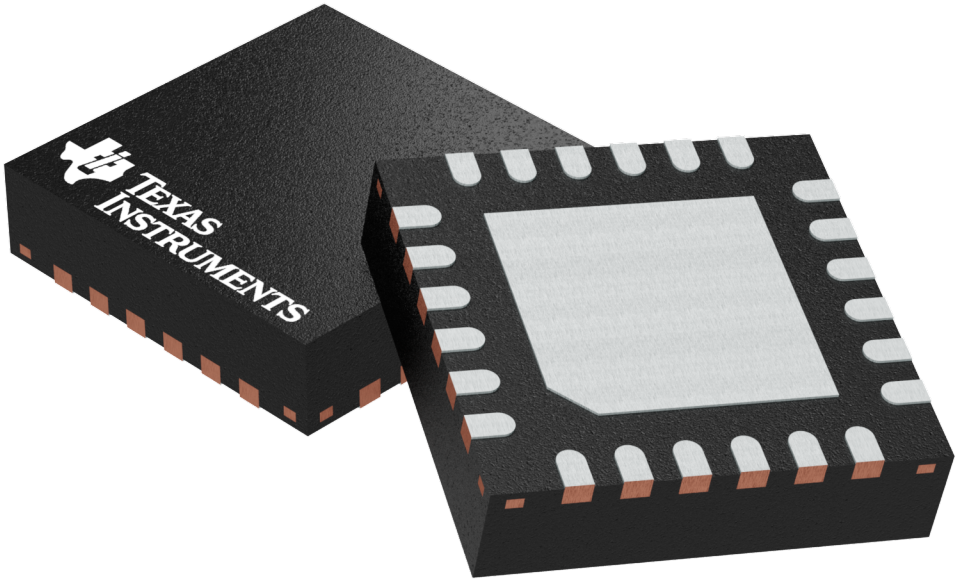
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



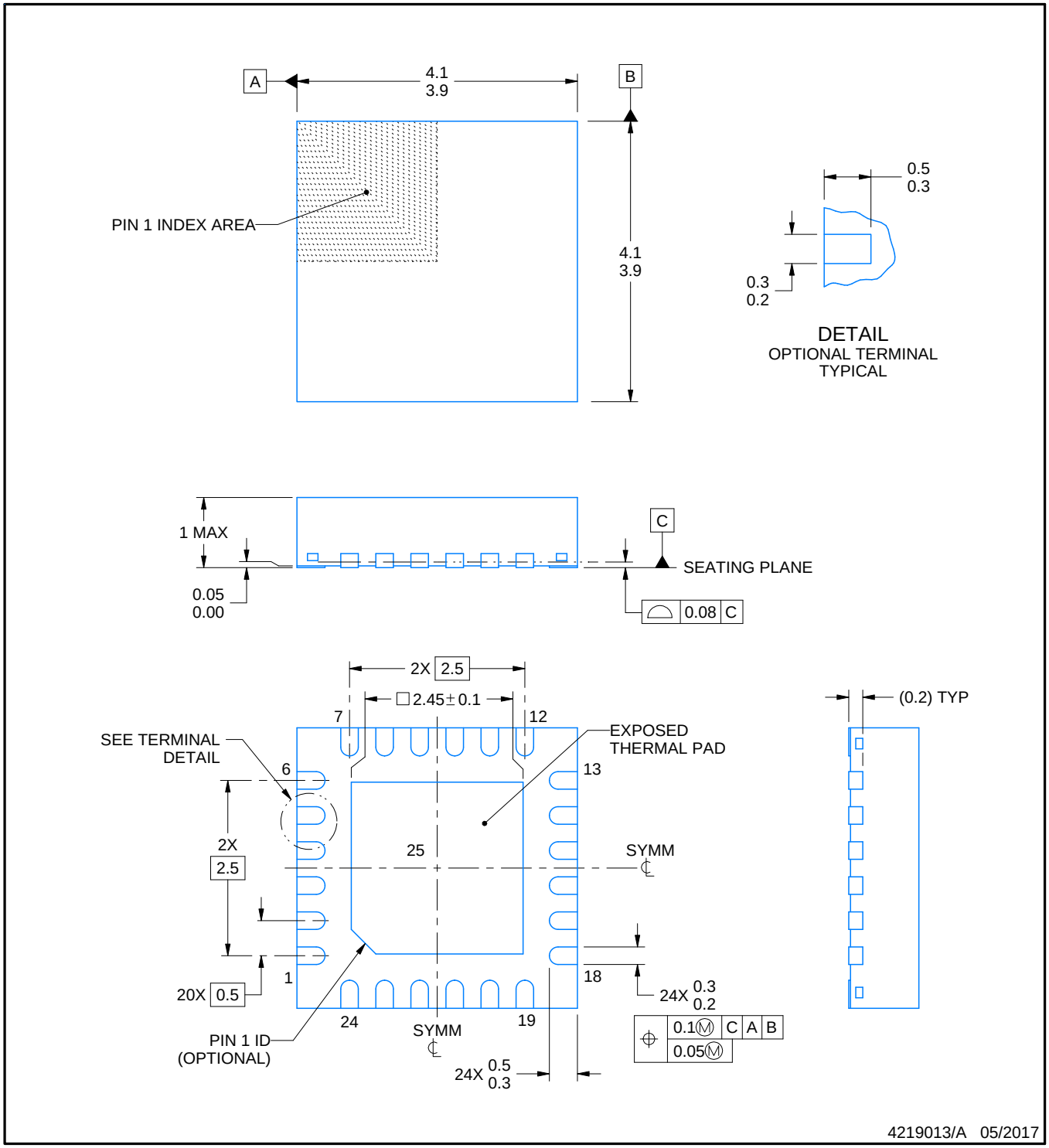
4224765/B

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

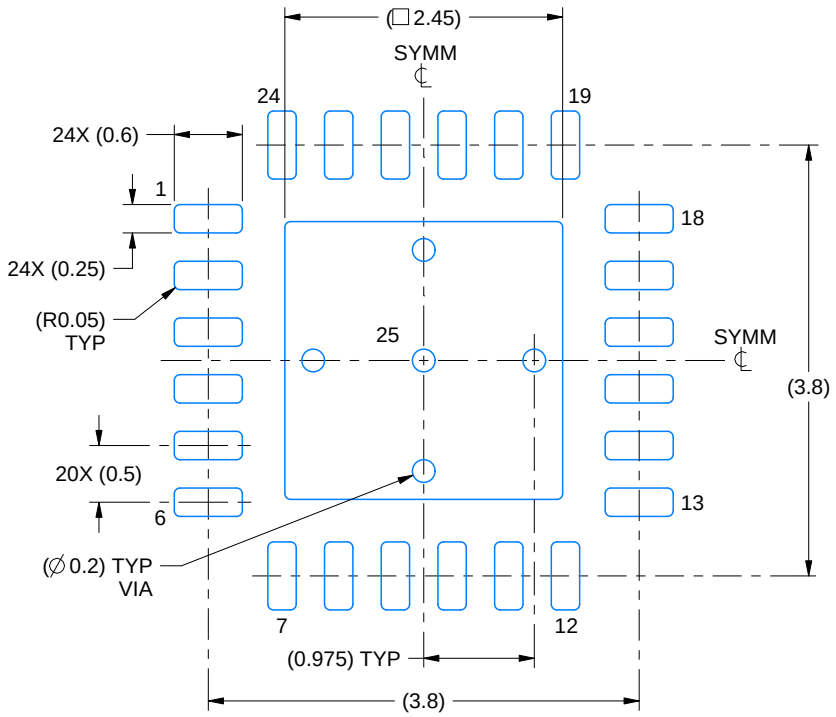


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

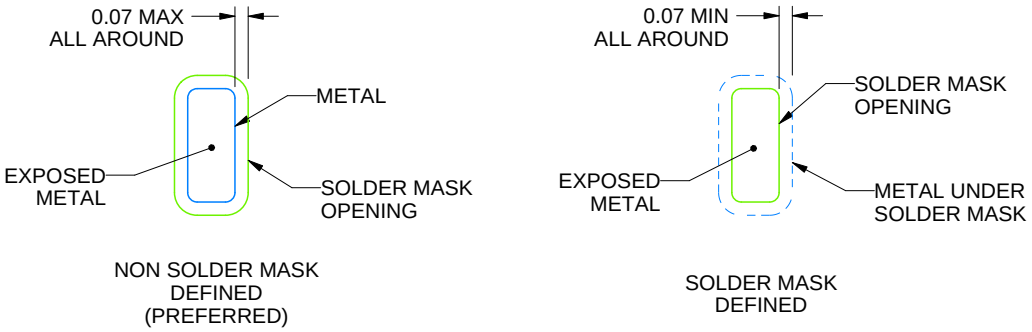


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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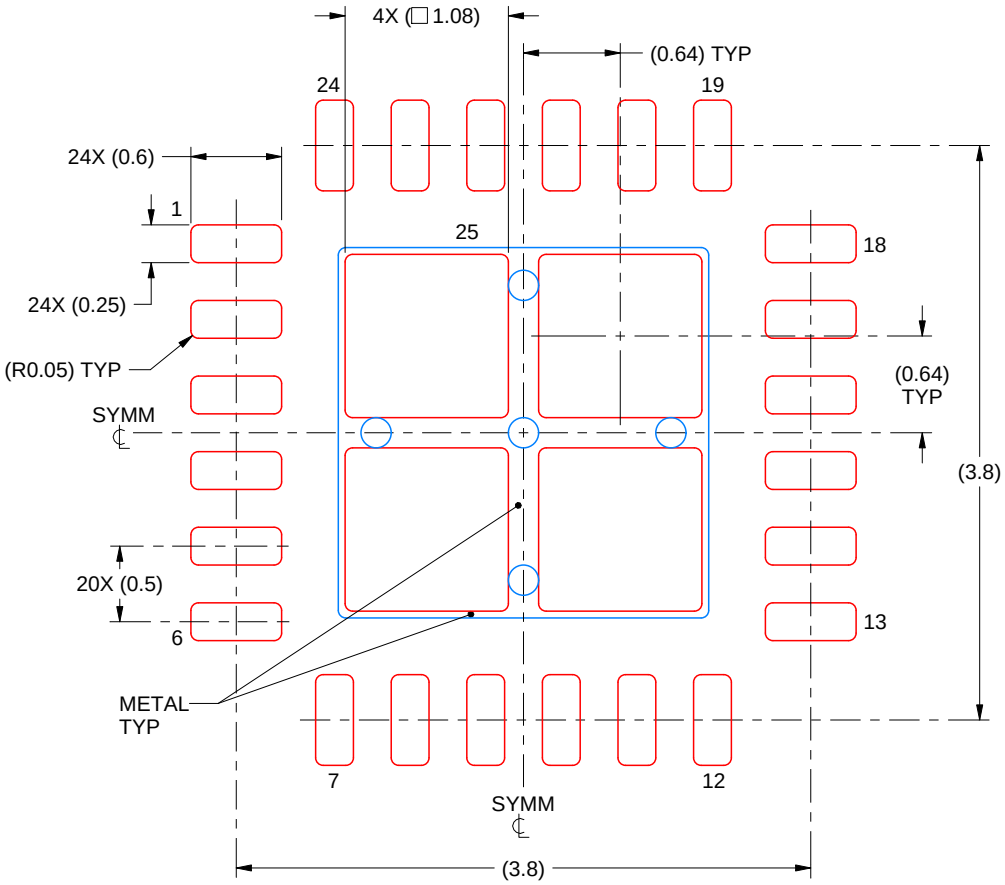
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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