4 桥接串行接口电机驱动器

查询样品: **DRV8823-Q1**

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C4B**
- 具有 **4** 个 **H** 桥的脉宽调制 **(PWM)** 电机驱动器
  - 驱动两个步进式电机、一个步进式和两个直流 **(DC)** 电机、或者四个 **DC** 电机
  - 每绕组电流高达 **1.5A**
  - 低导通电阻
  - 可编程最大绕组电流
  - **3** 位绕组电流控制支持多达 **8** 个电流级别
  - 可选缓慢或者混合衰减模式
- **8V** 至 **32V** 运行电源电压范围
- 针对栅极驱动的内部电荷泵
- 内置 **3.3V** 基准电压
- 串行数字控制接口
- 对于欠压、过热、和过流情况的完全保护
- 耐热增强型表面贴装封装

应用范围

- 车载应用

说明

DRV8823-Q1 器件为打印机和其它办公自动化设备应用提供了一个集成的电机驱动器解决方案。

此电机驱动器电路包含四个 H 桥驱动器。 每个电机驱动器块采用配置为一个 H 桥的功率 MOSFET 来驱动电机绕组。

一个简单的串行接口只借助几个数字信号即可实现对电机驱动器所有功能的控制。 还提供了一个低功耗睡眠功能。

此电机驱动器提供 PWM 电流控制功能。 根据一个外部提供的基准电压并借助一个外部电流感测电阻器，可对此电流进行编程。 此外，8 个电流级别（通过串行接口设定）可实现双极步进式电机的微步进。

还提供用于过流保护、短路保护、欠压闭锁和过热保护的内部关断功能。

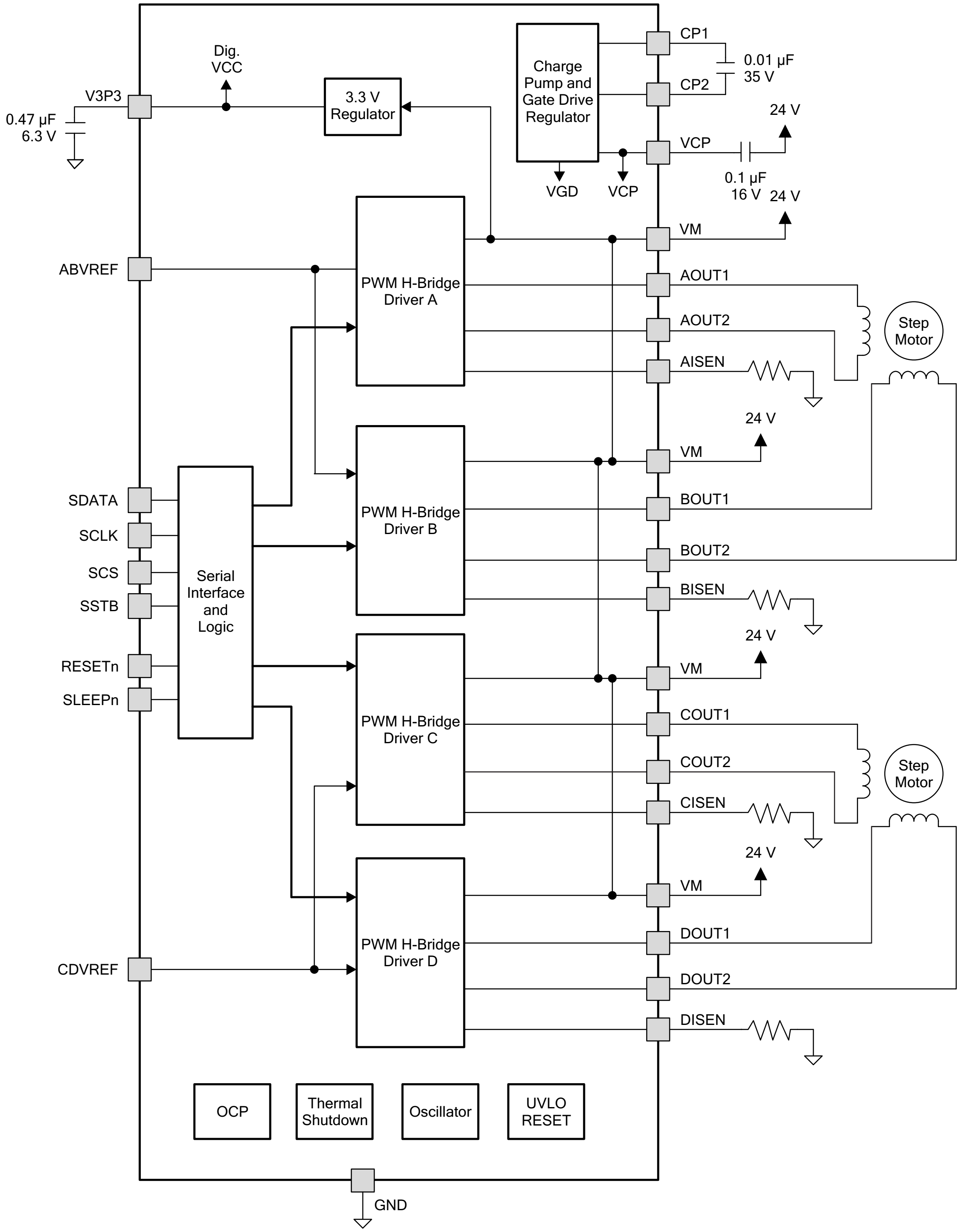
DRV8823-Q1 采用 48 引脚散热薄型小外形尺寸 (HTSSOP) 封装（环境友好型：符合 RoHS 标准并且无 Sb/Br）。

订购信息 (1)

T_A	封装 (2)		可订购部件号	正面标记
-40°C 至 125°C	PowerPAD™ (HTSSOP)-DCA	2000 卷带	DRV8823QDCARQ1	DRV8823Q

(1) 要获得最新的封装和订购信息，请参阅本文档末尾的封装选项附录，或者浏览 TI 网站www.ti.com。
(2) 封装图样、热数据和符号可从网站www.ti.com/packaging中获取。

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN FUNCTIONS

PIN		I/O (1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
VM (4 pins)	1, 2, 23, 24	-	Motor supply voltage (multiple pins)	Connect all VM pins together to motor supply voltage. Bypass to GND with several 0.1-μF, 35-V ceramic capacitors.
V3P3	16	-	3.3 V regulator output	Bypass to GND with 0.47-μF, 6.3-V ceramic capacitor.
GND	10–15, 34–39	-	Power ground (multiple pins)	Connect all PGND pins to GND and solder to copper heatsink areas.
CP1	7	IO	Charge pump flying capacitor	Connect a 0.01-μF capacitor between CP1 and CP2.
CP2	8	IO		
VCP	9	IO	Charge pump storage capacitor	Connect a 0.1-μF, 16 V ceramic capacitor to V_M.
MOTOR DRIVERS				
ABVREF	17	I	Bridge A & B current set reference voltage	Sets current trip threshold
AOUT1	5	O	Bridge A output 1	Connect to first coil of bipolar stepper motor 1, or DC motor winding.
AOUT2	3	O	Bridge A output 2	
ISENA	4	-	Bridge A current sense	Connect to current sense resistor for bridge A.
BOUT1	48	O	Bridge B output 1	Connect to second coil of bipolar stepper motor 1, or DC motor winding.
BOUT2	46	O	Bridge B output 2	
ISENB	47	-	Bridge B current sense	Connect to current sense resistor for bridge B.
CDVREF	18	I	Bridge C & D current set reference voltage	Sets current trip threshold
COUT1	27	O	Bridge C output 1	Connect to first coil of bipolar stepper motor 2, or DC motor winding.
COUT2	25	O	Bridge C output 2	
ISENC	26	-	Bridge C current sense	Connect to current sense resistor for bridge C.
DOUT1	22	O	Bridge D output 1	Connect to second coil of bipolar stepper motor 2, or DC motor winding.
DOUT2	20	O	Bridge D output 2	
ISEND	22	-	Bridge D current sense	Connect to current sense resistor for bridge D.
SERIAL INTERFACE				
SDATA	31	I	Serial data input	Data is clocked in on rising edge of SCLK.
SCLK	33	I	Serial input clock	Logic high enables serial data to be clocked in.
SCS	45	I	Serial chip select	Logic high latches serial data.
SSTB	30	I	Serial data strobe	Active low resets serial interface and disables outputs.
RESETn	43	I	Reset input	Active low input disables outputs and charge pump.
SLEEPn	42	I	Sleep input	
TEST PINS				
TEST	19, 28, 29, 32	I	Test inputs	Do not connect these pins - used for factory test only.

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output, PU = internal pullup

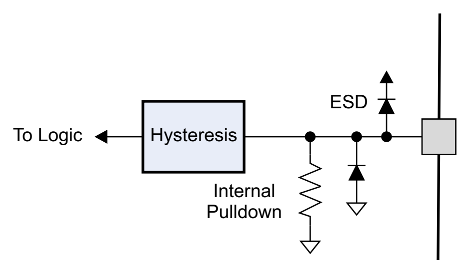
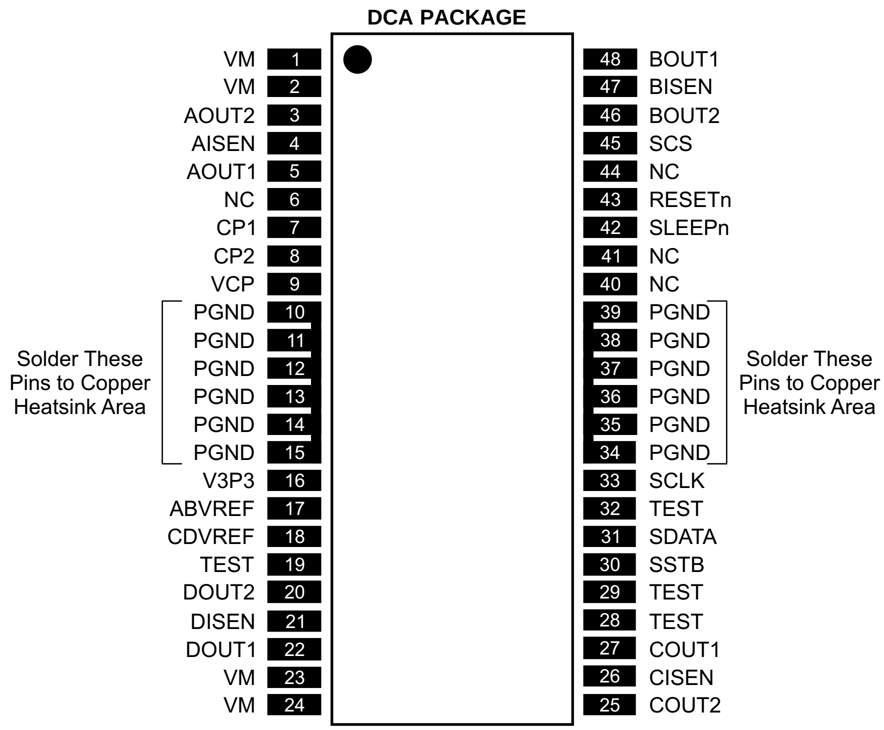


Figure 1. Logic Inputs



ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNITS
V_M	Power supply voltage range	–0.3 to 34	V
V_I	Logic input voltage range(3)	–0.5 to 5.75	V
$I_{O(peak)}$	Peak motor drive output current, t < 1 μs	Internally limited	
I_O	Motor drive output current(4)	1.5	A
P_D	Continuous total power dissipation	See Dissipation Ratings Table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_A	Operating ambient temperature range	–40 to 125	°C
T_{stg}	Storage temperature range	–60 to 150	°C
ESD rating	Human Body Model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged Device Model (CDM) AEC-Q100 750 V Classification Level C4B	750	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Input pins may be driven in this voltage range regardless of presence or absence of V_M.
(4) Power dissipation and thermal limits must be observed.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A < 25°C$	$T_A = 70°C$	$T_A = 85°C$	$T_A = 125°C$
Low-K (1)	DCA	75.7°C/W	13.2 mW/°C	1.65 W	1.06 W	0.86 W	0.332 W
Low-K (2)		32°C/W	31.3 mW/°C	3.91 W	2.50 W	2.03 W	0.778 W
High-K (3)		30.3°C/W	33 mW/°C	4.13 W	2.48 W	2.15 W	0.83 W
High-K (4)		22.3°C/W	44.8 mW/°C	5.61 W	3.59 W	2.91 W	1.118 W

(1) The JEDEC Low-K board used to derive this data was a 76-mm x 114-mm, 2-layer, 1.6-mm thick PCB with no backside copper.
(2) The JEDEC Low-K board used to derive this data was a 76-mm x 114-mm, 2-layer, 1.6-mm thick PCB with 25-cm^2 2-oz copper on back side.
(3) The JEDEC High-K board used to derive this data was a 76-mm x 114-mm, 4-layer, 1.6-mm thick PCB with no backside copper and solid 1-oz internal ground plane.
(4) The JEDEC High-K board used to derive this data was a 76-mm x 114-mm, 4-layer, 1.6-mm thick PCB with 25-cm^2 1-oz copper on back side and solid 1-oz internal ground plane.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range	8		32	V
I_{MOT}	Continuous motor drive output current(1)		1	1.5	A
V_{REF}	VREF input voltage	1		4	V

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

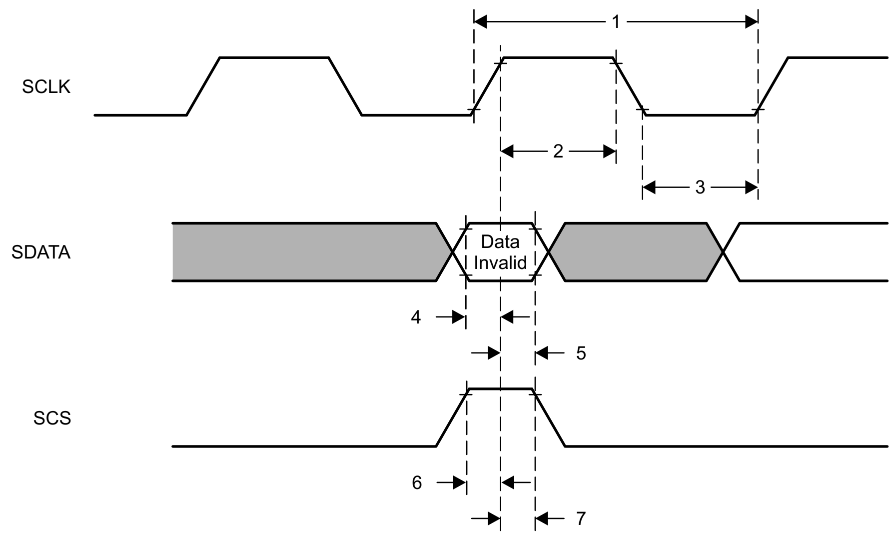
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	V_M operating supply current	V_M = 24 V, no loads		5	8	mA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.5	8	V
V_{CP}	Charge pump voltage	Relative to V_M		12		V
V_{V3P3}	V_{V3P3} output voltage		3.20	3.30	3.40	V
LOGIC-LEVEL INPUTS (INTERNAL PULLDOWNS)						
V_{IL}	Input low voltage				0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis		0.3	0.45	0.6	V
I_{IN}	Input current (internal pulldown current)	VIN = 3.3 V			100	μA
OVERTEMPERATURE PROTECTION						
T_{TSD}	Thermal shutdown temperature	Die temperature	150			°C
MOTOR DRIVERS						
$R_{DS(ON)}$	Motor number 1 FET on resistance (each individual FET)	V_M = 24 V, I_O = 0.8 A, T_A = 25°C		0.25		Ω
		V_M = 24 V, I_O = 0.8 A, T_A = 85°C		0.31	0.37	
		V_M = 24 V, I_O = 0.8 A, T_A = 85°C to 125°C		.435	.570	
$R_{DS(ON)}$	Motor number 2 FET on resistance (each individual FET)	V_M = 24 V, I_O = 0.8 A, T_A = 25°C		0.30		Ω
		V_M = 24 V, I_O = 0.8 A, T_A = 85°C		0.38	0.45	
		V_M = 24 V, I_O = 0.8 A, T_A = 85°C to 125°C		.446	.570	
I_{OFF}	Off-state leakage current				±12	μA
f_{PWM}	Motor PWM frequency(1)		42	50	57	kHz
t_{BLANK}	ITRIP blanking time(2)			3.75		μs
t_F	Output fall time		50		350	ns
t_R	Output rise time		50		350	ns
I_{OCP}	Overcurrent protect level		1.5	3	4.5	A
t_{OCP}	Overcurrent protect trip time		2.7			μs
t_{MD}	Mixed decay percentage	Measured from beginning of PWM cycle		75%		
CURRENT CONTROL						
I_{REF}	xVREF input current	xVREF = 3.3 V	–3		3	μA
$ΔI_{CHOP}$	Chopping current accuracy	xVREF = 2.5 V, derived from V3P3; 71% – 100% current	–5		5	%
		xVREF = 2.5 V, derived from V3P3; 20% – 56% current	–10		10	

(1) Factory option 100 kHz.
(2) Factory options for 2.5 μs, 5 μs or 6.25 μs.

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
1	t_{CYC}	Clock cycle time	62		ns
2	t_{CLKH}	Clock high time	25		ns
3	t_{CLKL}	Clock low time	25		ns
4	$t_{SU(SDATA)}$	Setup time, SDATA to SCLK	5		ns
5	$t_{H(DATA)}$	Hold time, SDATA to SCLK	1		ns
6	$t_{SU(SCS)}$	Setup time, SCS to SCLK	5		ns
7	$t_{H(SCS)}$	Hold time, SCS to SCLK	1		ns



FUNCTIONAL DESCRIPTION

PWM Motor Drivers

The DRV8823-Q1 device contains four H-bridge motor drivers with current-control PWM circuitry. A block diagram showing drivers A and B of the motor control circuitry (as typically used to drive a bipolar stepper motor) is shown in Figure 2. Drivers C and D are the same as A and B (though the $R_{DS(ON)}$ of the output FETs is different).

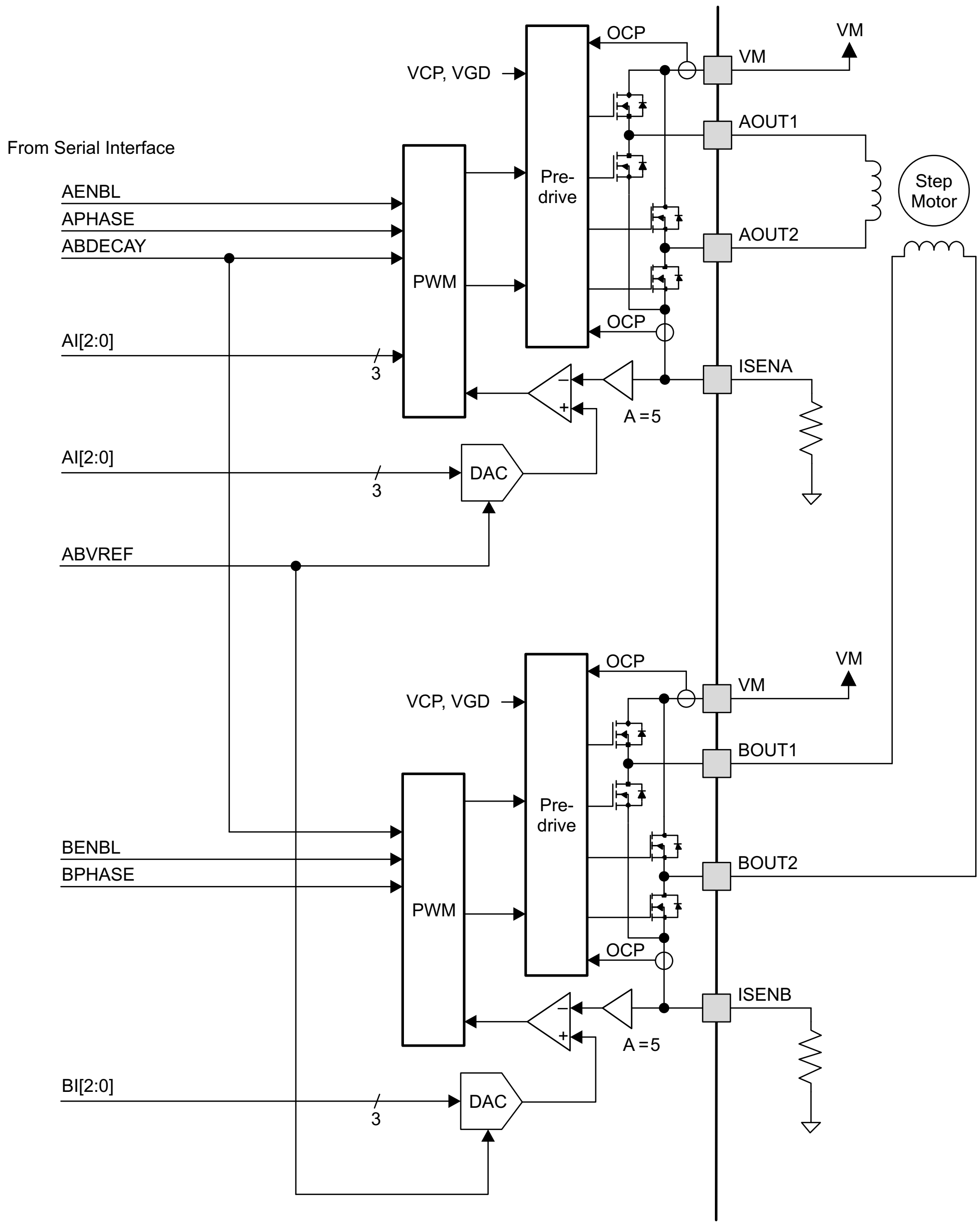


Figure 2. Block Diagram

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

Bridge Control

The xENBL bits in the serial interface registers enable current flow in each H-bridge when set to 1.

The xPHASE bits in the serial interface registers control the direction of current flow through each H-bridge. The following table shows the logic:

xPHASE	xOUT1	xOUT2
1	H	L
0	L	H

Current Regulation

The motor driver employs fixed-frequency PWM current regulation (also called current chopping). When a winding is activated, the current through it rises until it reaches a threshold, then the current is switched off until the next PWM period.

The PWM frequency is fixed at 50 kHz, but it may also be set to 100 kHz through the factory option.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the VREF pin.

The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the V_{REFx} pin is 2.5 V, the full-scale (100%) chopping current is: 2.5 V/(5 × 0.5 Ω) = 1 A.

Three serial interface register bits per H-bridge (xI2, xI1 and xI0) are used to scale the current in each bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The function of the bits is shown below:

xI2	xI1	xI0	Relative Current (% full-scale chopping current)
0	0	0	20
0	0	1	38
0	1	0	56
0	1	1	71
1	0	0	83
1	0	1	92
1	1	0	98
1	1	1	100

Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs. Note that the blanking time also sets the minimum on time of the PWM.

Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 3 as case 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 3 as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in Figure 3 as case 3.

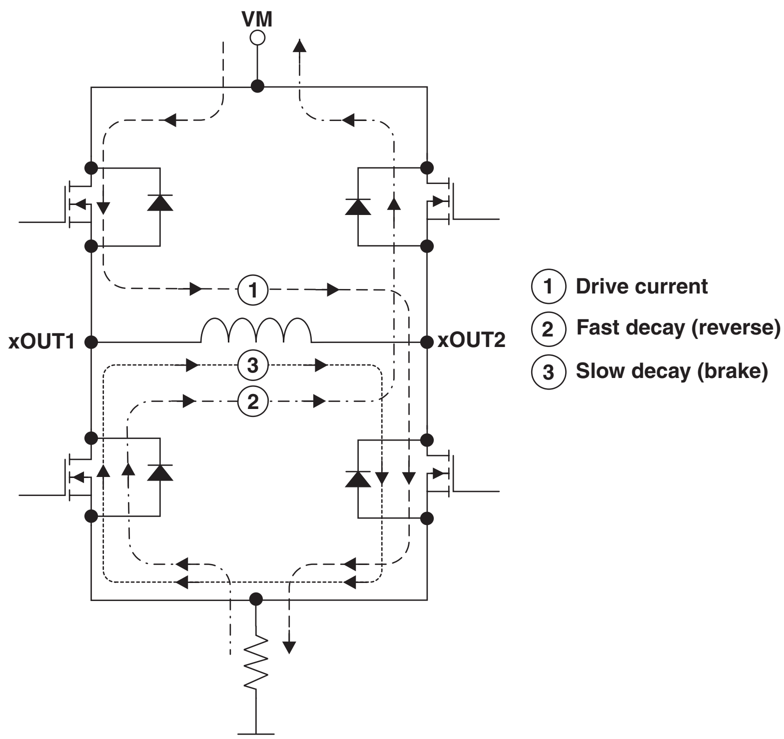


Figure 3. Decay Mode

The DRV8823-Q1 device supports slow decay and a mixed decay mode. Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

Slow or mixed decay mode is selected by the state of the xDECAY bits in the serial interface registers. If the xDECAY bit is 0, slow decay is selected. If the xDECAY bit is 1, mixed decay is selected.

Protection Circuits

The DRV8823-Q1 device is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

All of the drivers in the DRV8823-Q1 device are protected with an overcurrent protection (OCP) circuit.

The OCP circuit includes an analog current limit circuit, which acts by removing the gate drive form each output FET if the current through it exceeds a preset level. This circuit limits the current to a level that is safe to prevent damage to the FET.

A digital circuit monitors the analog current limit circuits. If any analog current limit condition exists for longer than a preset period, all drivers in the device are disabled.

The device is re-enabled upon the removal and re-application of power at the VM pins.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down.

The device remains disabled until the die temperature falls to a safe level. After the temperature falls, the device may be re-enabled upon the removal and re-application of power at the VM pin.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled. Operation resumes when VM rises above the UVLO threshold. The indexer logic is reset to its initial condition in the event of an undervoltage lockout.

Shoot-Through Current Prevention

The gate drive to each FET in the H-bridge is controlled to prevent any cross-conduction (shoot-through current) during transitions.

Serial Data Transmission

Data transfers consist of 16 bits of serial data, shifted into the SDATA pin LSB first.

On serial writes to the DRV8823-Q1 device, additional clock edges following the final data bit continues to shift data bits into the data register; therefore, the last 16 bits presented are latched and used.

One of two registers is selected by setting bits in an address field in the four upper bits in the serial data transferred (ADDR in the tables below). One 16-bit register is used to control motor number 1 (bridges A and B), and a second 16-bit register is used to control motor 2 (bridges C and D).

Data can only be transferred into the serial interface if the SCS input pin is active high.

Data is initially clocked in to a temporary holding register. This data is latched into the motor driver on the rising edge of the SSTB pin. If the SSTB pin is tied high at all times, the data will be latched in after all 16 bits have been transferred.

Data Format

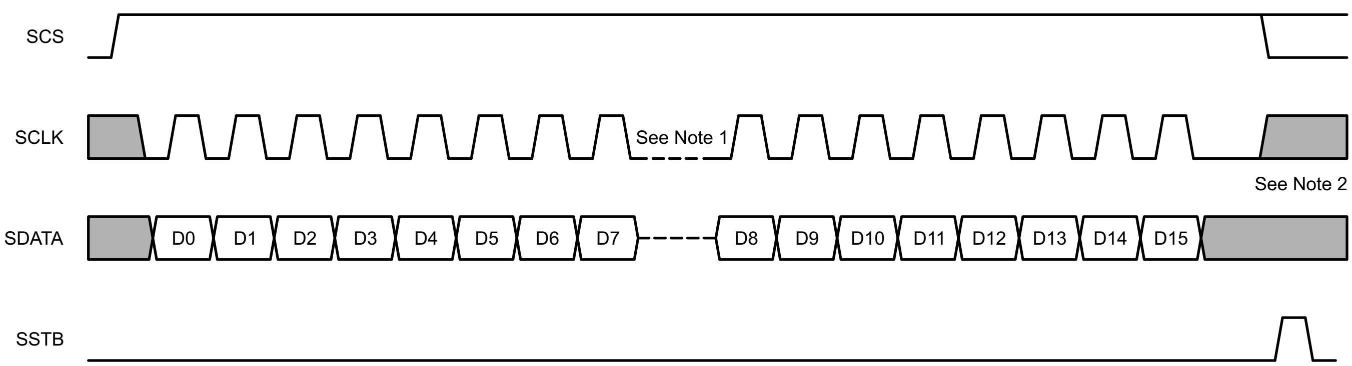
Table 1. Motor 1 Command (Bridges A and B)

Bit	D15–D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ADDR (= 0000)	BDECAY	B12	B11	B10	BPHASE	BENBL	ADECAY	A12	A11	A10	APHASE	AENBL
Reset Value	x	0	0	0	0	0	0	0	0	0	0	0	0

Table 2. Motor 2 Command (Bridges C and D)

Bit	D15–D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ADDR (= 0001)	DDECAY	D12	D11	D10	DPHASE	DENBL	CDECAY	C12	C11	C10	CPHASE	CENBL
Reset Value	x	0	0	0	0	0	0	0	0	0	0	0	0

Serial Data Timing



Note 1: Any amount of time is allowed between clocks, or groups of clocks, as long as SCS stays active. This allows 8- or 16-bit transfers.

Note 2: If more than 16 clock edges are presented while transferring data (while SCS is still high), data continues to be shifted into the data register.

Figure 4. Serial Data Timing Diagram

THERMAL INFORMATION

Thermal Protection

The DRV8823-Q1 device has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8823-Q1 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 2.

$$P_{TOT} = 4 \times R_{DS(ON)} \times (I_{OUT(RMS)})^2 \qquad (2)$$

Where: P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current applied to each winding. $I_{OUT(RMS)}$ is equal to approximately 0.7x the full-scale output current setting. The factor of 4 is derived from the two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side). The DRV8823-Q1 device has two stepper motor drivers, so the power dissipation of each must be added together to determine the total device power dissipation.

The maximum amount of power that can be dissipated in the DRV8823-Q1 device is dependent on ambient temperature and heatsinking. The thermal dissipation ratings table in the datasheet can be used to estimate the temperature rise for typical PCB constructions.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD integrated circuit package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. Figure 5 shows thermal resistance versus copper plane area for both a single-sided PCB with 2-oz copper heatsink area, and a 4-layer PCB with 1-oz copper and a solid ground plane. Both PCBs are 76 mm x 114 mm, and 1.6 mm thick. The heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

Six pins on the center of each side of the package are also connected to the device ground. A copper area can be used on the PCB that connects to the PowerPAD integrated circuit package as well as to all the ground pins on each side of the device, which is especially useful for single-layer PCB designs.

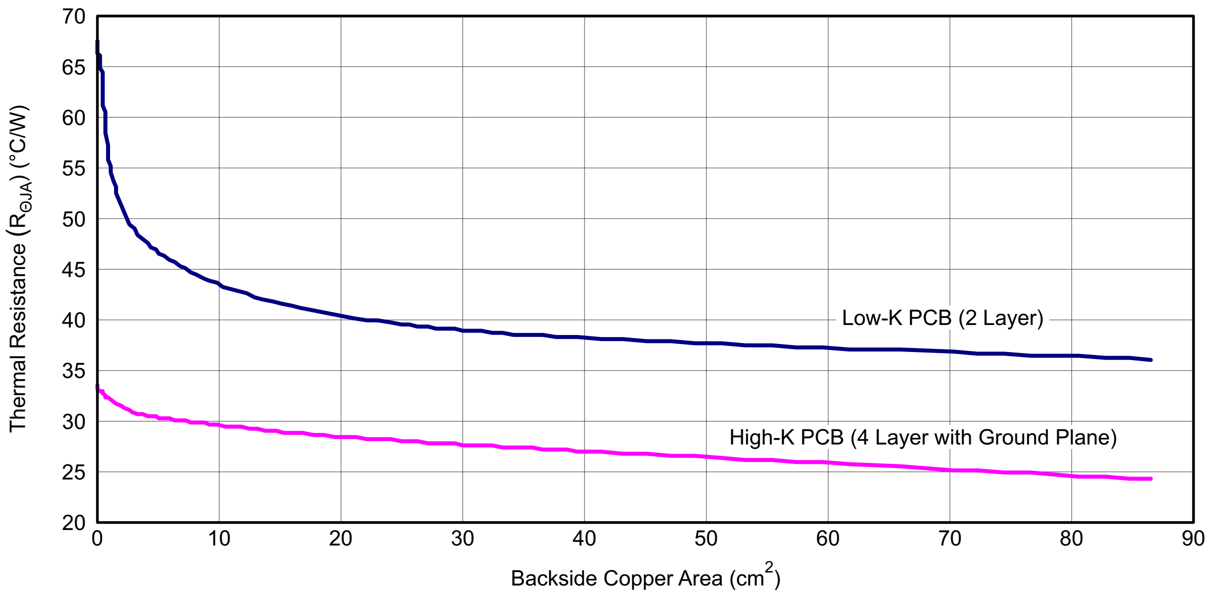


Figure 5. Thermal Resistance vs Copper Plane Area

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8823QDCARQ1	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8823Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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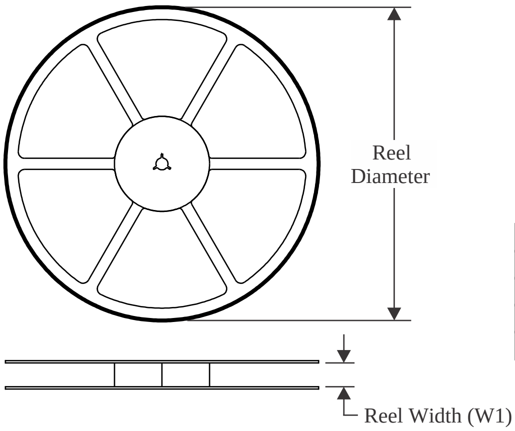
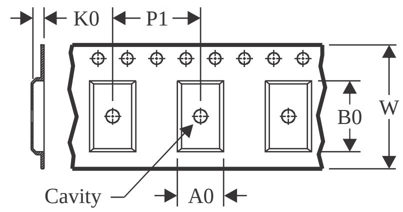
TAPE AND REEL INFORMATION

REEL DIMENSIONS

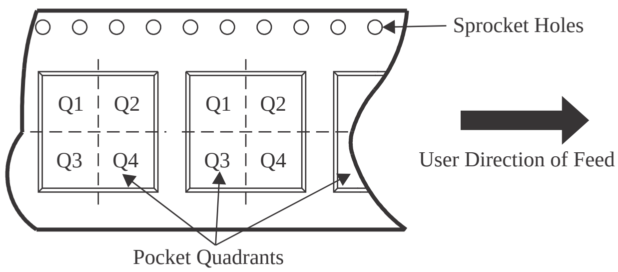


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

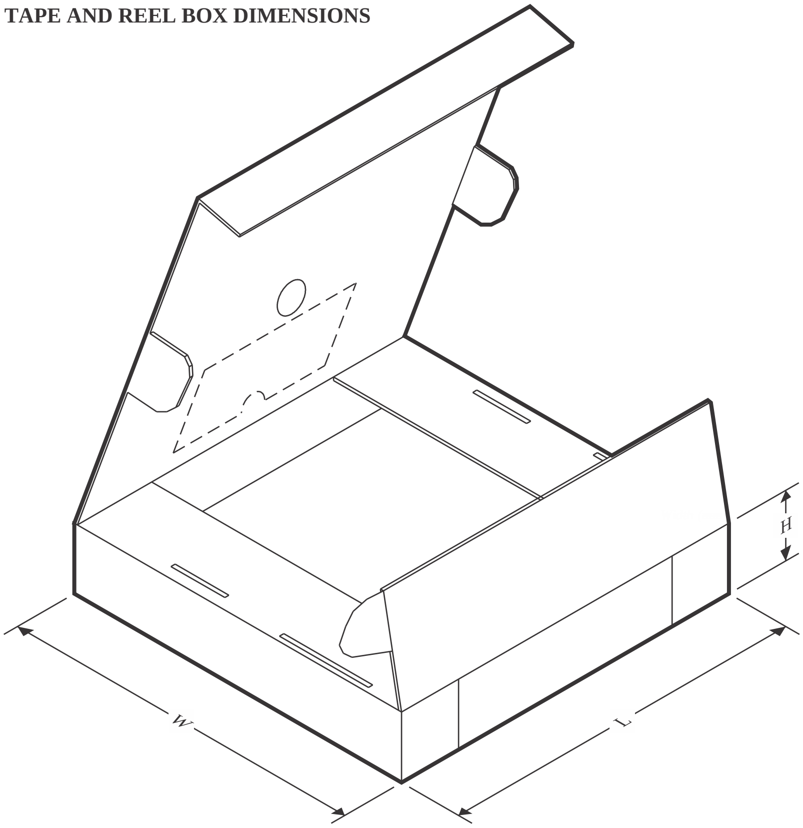
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8823QDCARQ1	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

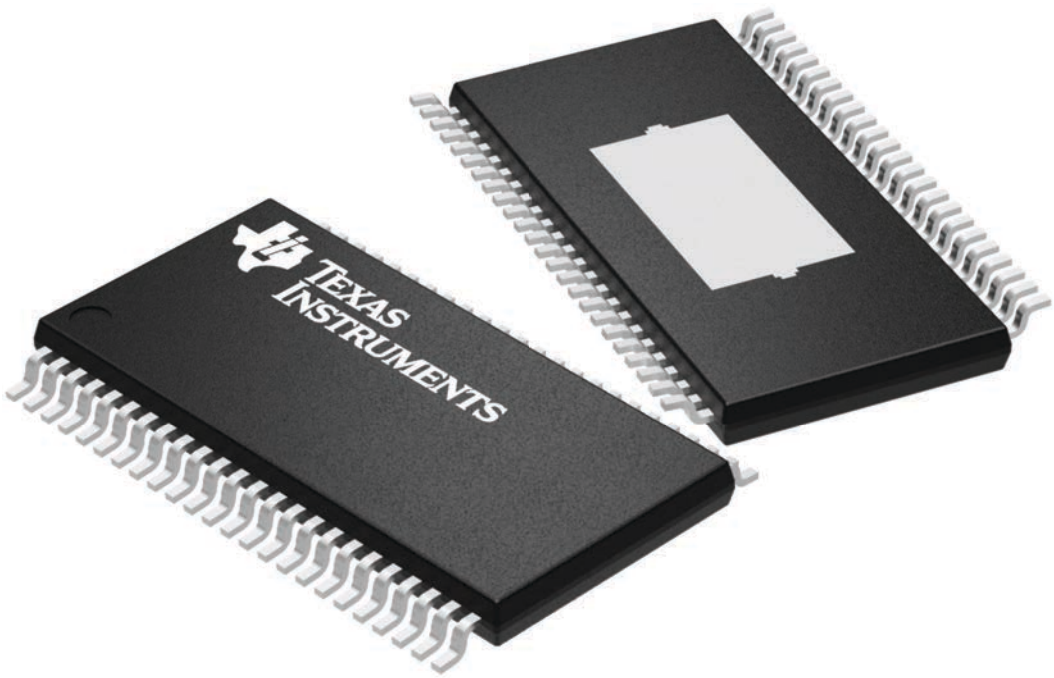
TAPE AND REEL BOX DIMENSIONS



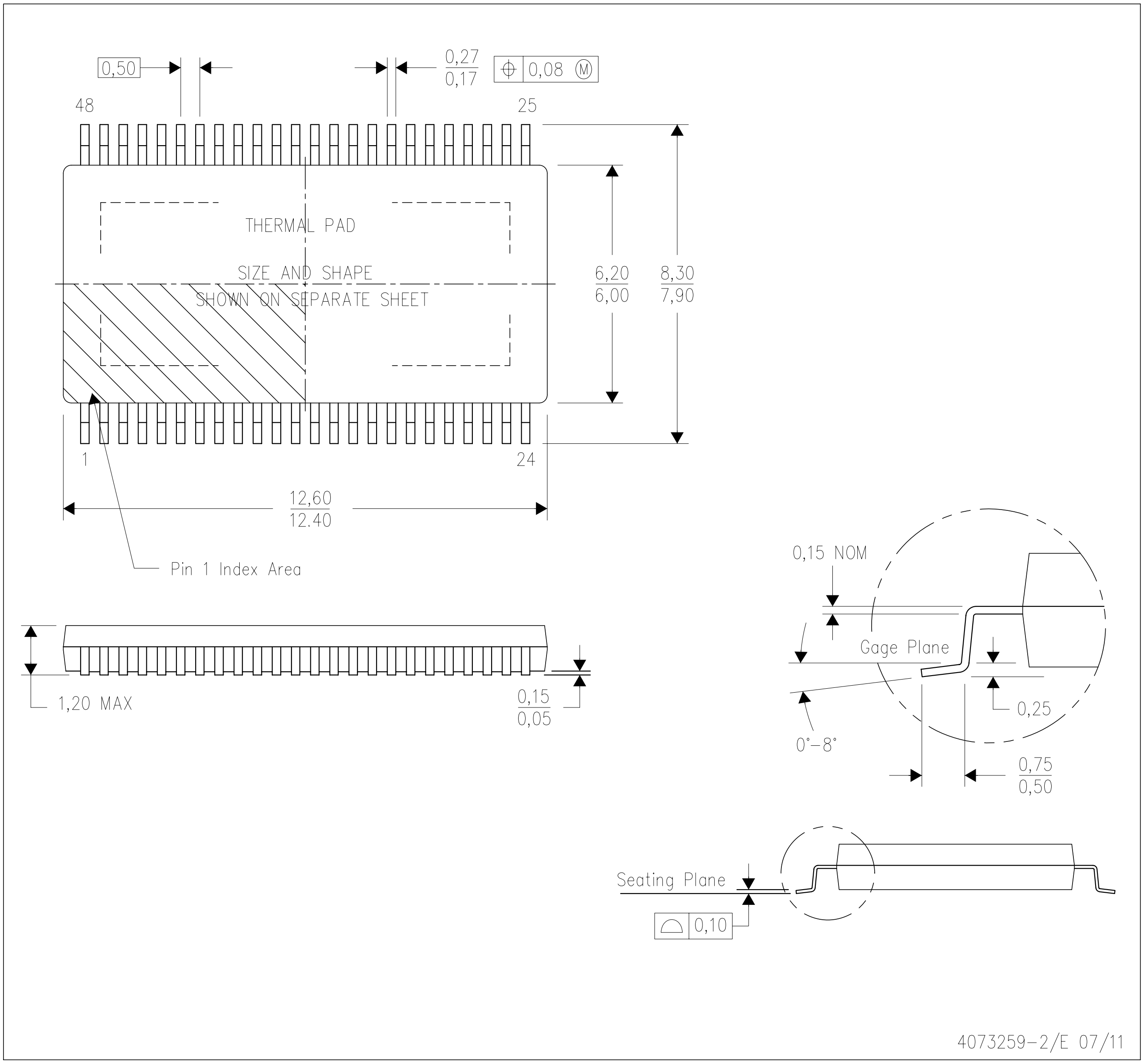
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8823QDCARQ1	HTSSOP	DCA	48	2000	350.0	350.0	43.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–153

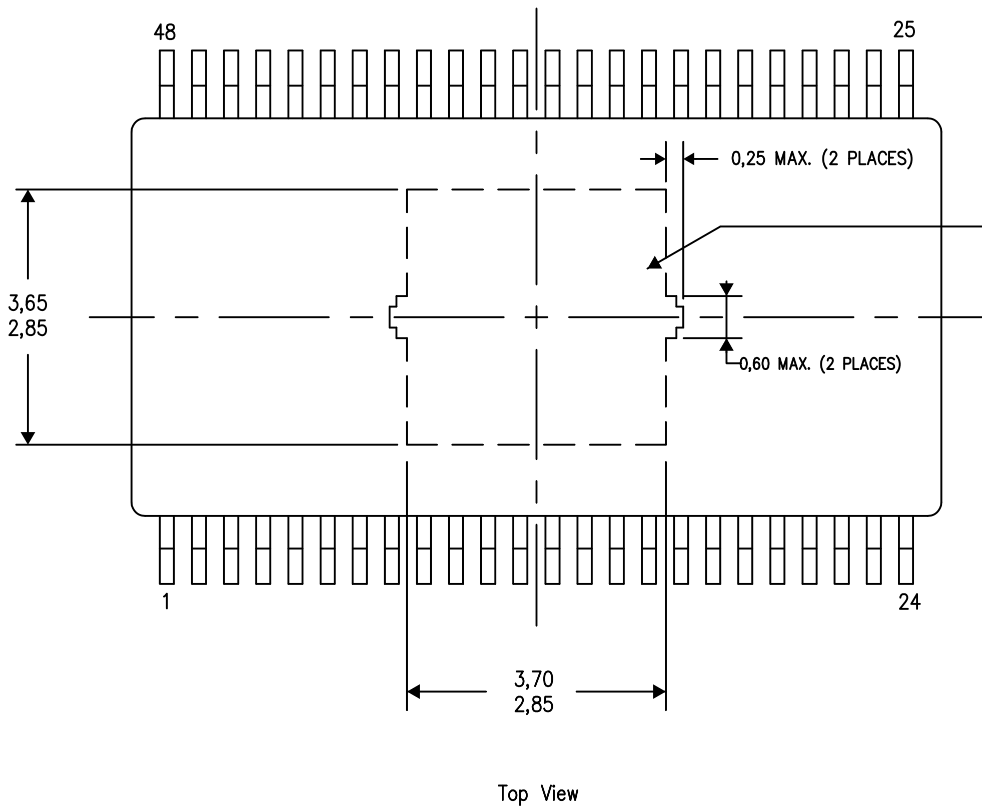
DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

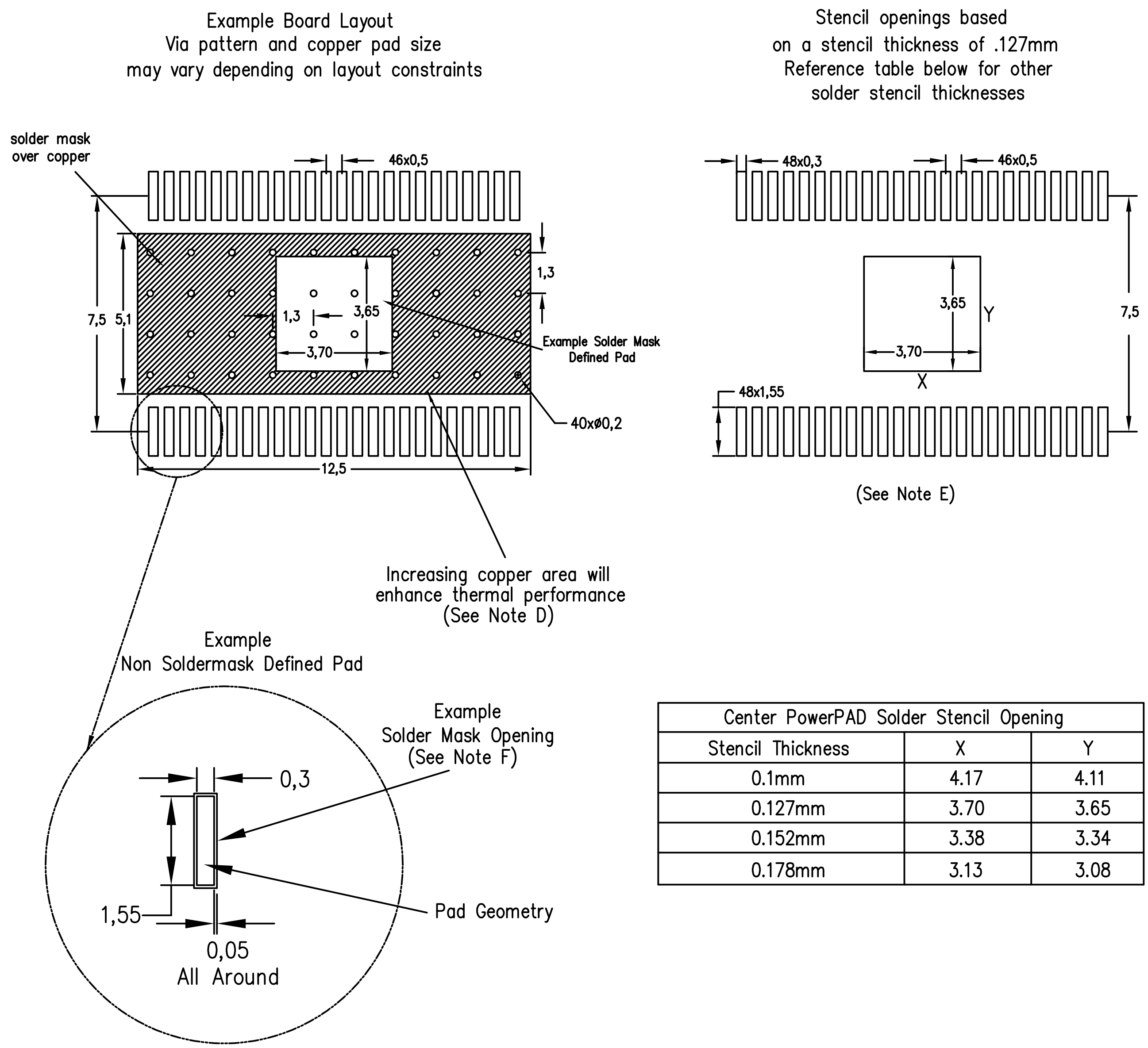


Exposed Thermal Pad Dimensions

4206320-6/S 11/14

NOTE: A. All linear dimensions are in millimeters

DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.17	4.11
0.127mm	3.70	3.65
0.152mm	3.38	3.34
0.178mm	3.13	3.08

4208546-5/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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