TEXAS INSTRUMENTS

DS160PT801
ZHCSME6A – DECEMBER 2020 – REVISED JUNE 2022

DS160PT801 PCIe® 4.0、16Gbps、8 路（16 通道）重定时器

1 特性

- 8 路（16 通道）协议感知 PCI-Express 重定时器支持 16.0、8.0、5.0 和 2.5GT/s 接口
- 芯片间通信 (ICC) 支持双芯片链路宽度扩展，从而形成 16 通道第 4 代重定时器
- 支持公共时钟、不具有展频时钟 (SSC) 的单独参考时钟和具有 SSC 的单独参考时钟
- 支持 2x4 分叉
- 自适应接收 CTLE 和 DFE 支持超高的 PCIe 第 4 代通道损耗
- 支持均衡协商
- 低延迟架构
- 片上眼图张开度监视器 (EOM) 和 PCIe 接收裕度调节功能
- 小型 8.50mm × 13.40mm BGA 封装
- 直通引脚排列可在两个信号层中实现信号分接
- 与标准 1.00mm BGA PCB 制造兼容
- 双电源：1.17 V 和 1.8 V
- 通过外部 EEPROM 或 I2C 控制器进行 I2C 配置（高达 1MHz）
- 工业温度范围：−40°C 至 85°C

2 应用

- 机架式服务器
- 微服务器和塔式服务器
- 高性能计算
- 硬件加速器

3 说明

DS160PT801 是一款高性能 8 路（16 通道）PCI-Express 协议感知重定时器，支持所有高达 16 GT/s 的标准 PCIe 数据速率。它用于扩展高速 PCIe 串行链路（从芯片至芯片主板链路到更复杂的多连接器系统拓扑）的覆盖范围并提升稳定性。

DS160PT801 支持公共时钟和独立参考时钟架构，具有/不具有展频时钟。这为定义系统时钟架构提供了较大的灵活性。

DS160PT801 中的 8 个通道可分叉为两个 x4 链路，从而支持不同的系统拓扑。

紧凑但易于制造的 BGA 封装提供了出色的热性能，同时可在空间受限的应用（如 1RU 转接卡）中实现出色布局。此功能可降低整体解决方案尺寸、PCB 布线复杂性和 BOM 成本。

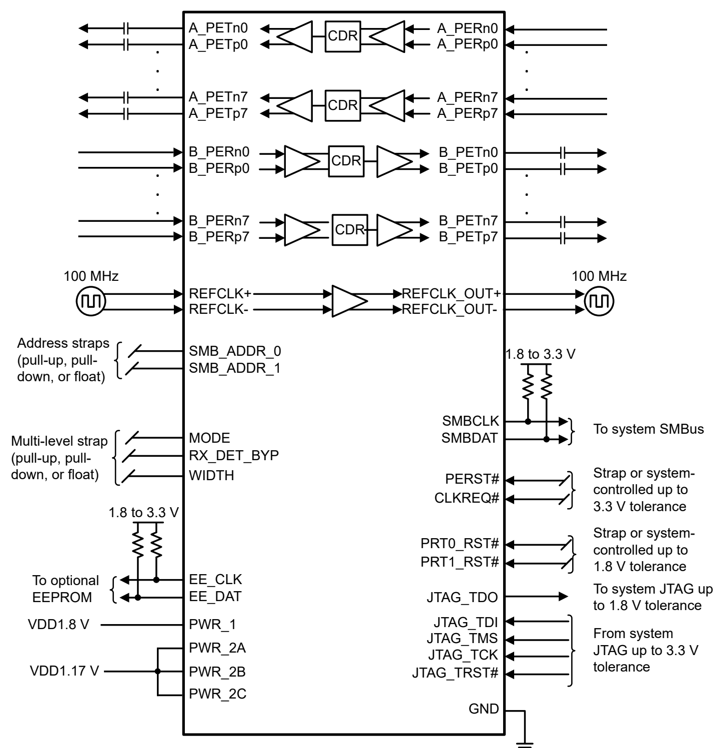
诊断功能包括带内接收器裕度调节、带外无损水平或垂直眼图裕度监视器、接收器环回、编码错误检测和片上温度传感器。这些功能有助于测量链路裕度，并可用于监测系统随时间推移的运行状况。

DS160PT801 可通过 SMBus 接口进行配置。初始配置可从外部 EEPROM 自动加载。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS160PT801	FCCSP (332)	8.50 mm x 13.40 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

English Data Sheet: SNLS592

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2020) to Revision A (June 2022)	Page
• 将数据表的状态从*预告信息* 更改为*量产数据*	1

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5 Device Comparison

PART NUMBER	LINK WIDTH	PCIe GEN	DEVICE TYPE
DS160PT801	x8	4, 3, 2, 1	Retimer

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6 Device and Documentation Support

6.1 Device Support

6.1.1 Development Support

- **IBIS-AMI model.** Simulate the DS160PT801's high-speed receiver and transmitter in tools which support IBIS-AMI simulations. Contact your local Texas Instruments sales representative for the latest status of available models.

6.1.2 12.1.2 Device Nomenclature

- **x2** – Two-lane PCI-Express Link, also referred to as by-2.
- **x4** – Four-lane PCI-Express Link, also referred to as by-4.
- **x8** – Eight-lane PCI-Express Link, also referred to as by-8.
- **x16** – Sixteen-lane PCI-Express Link, also referred to as by-16.
- **Bifurcation** – Dividing a by-M PCI-Express Link (for example, x8) into two or more separate by-N Links (for example, two x4), where N < M.
- **Stacking** – Combining multiple by-N devices (for example, two x8) to form a by-M interface (for example, x16), where M > N.

6.2 Documentation Support

6.2.1 Related Documentation

For related documentation, see the following:

- Texas Instrument, *DS160PT801 Evaluation Board* reference design

6.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

6.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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6.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS160PT801ACBR	ACTIVE	FCCSP	ACB	332	2000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	D160PT801	Samples
DS160PT801ACBT	ACTIVE	FCCSP	ACB	332	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	D160PT801	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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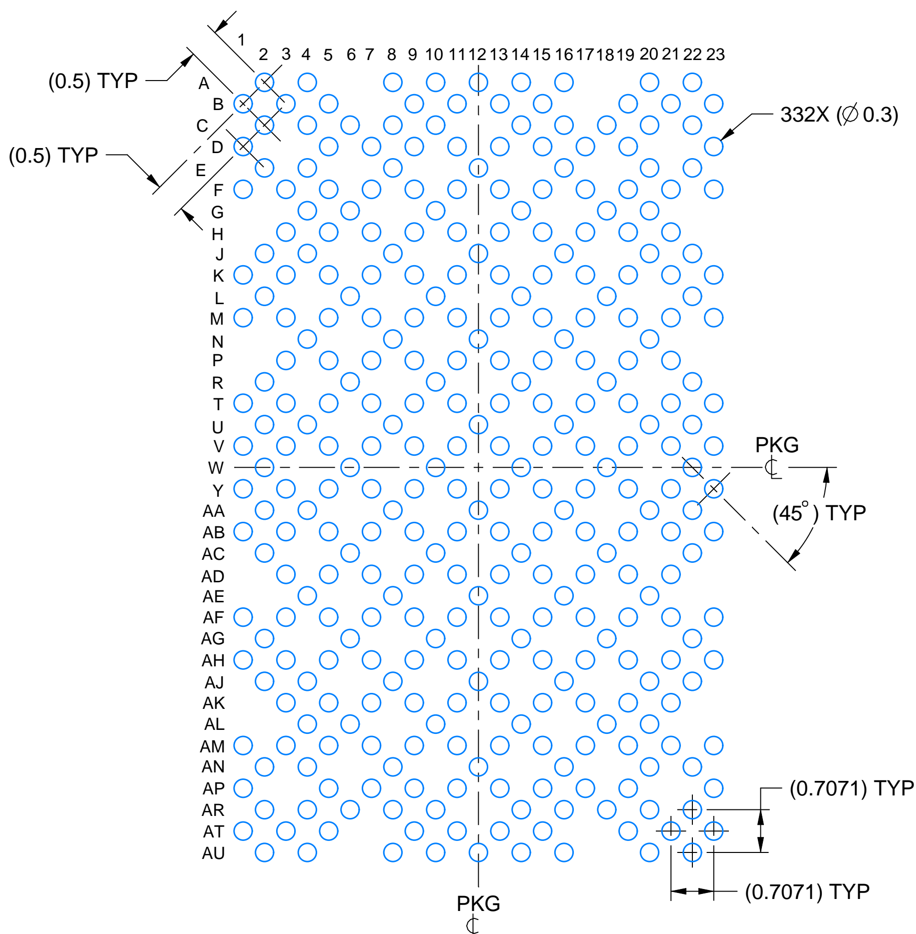
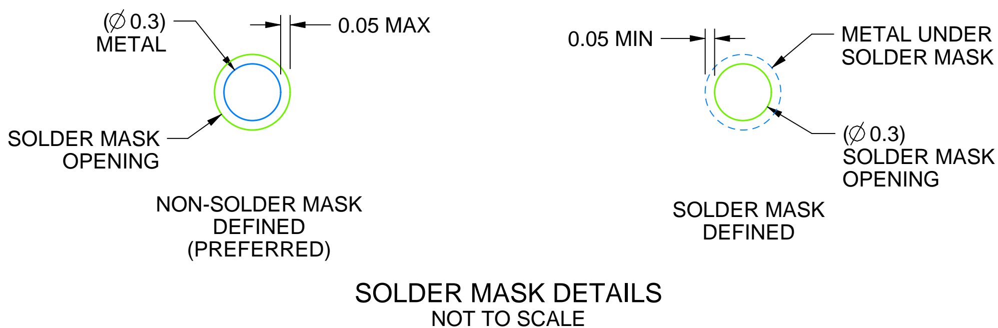
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

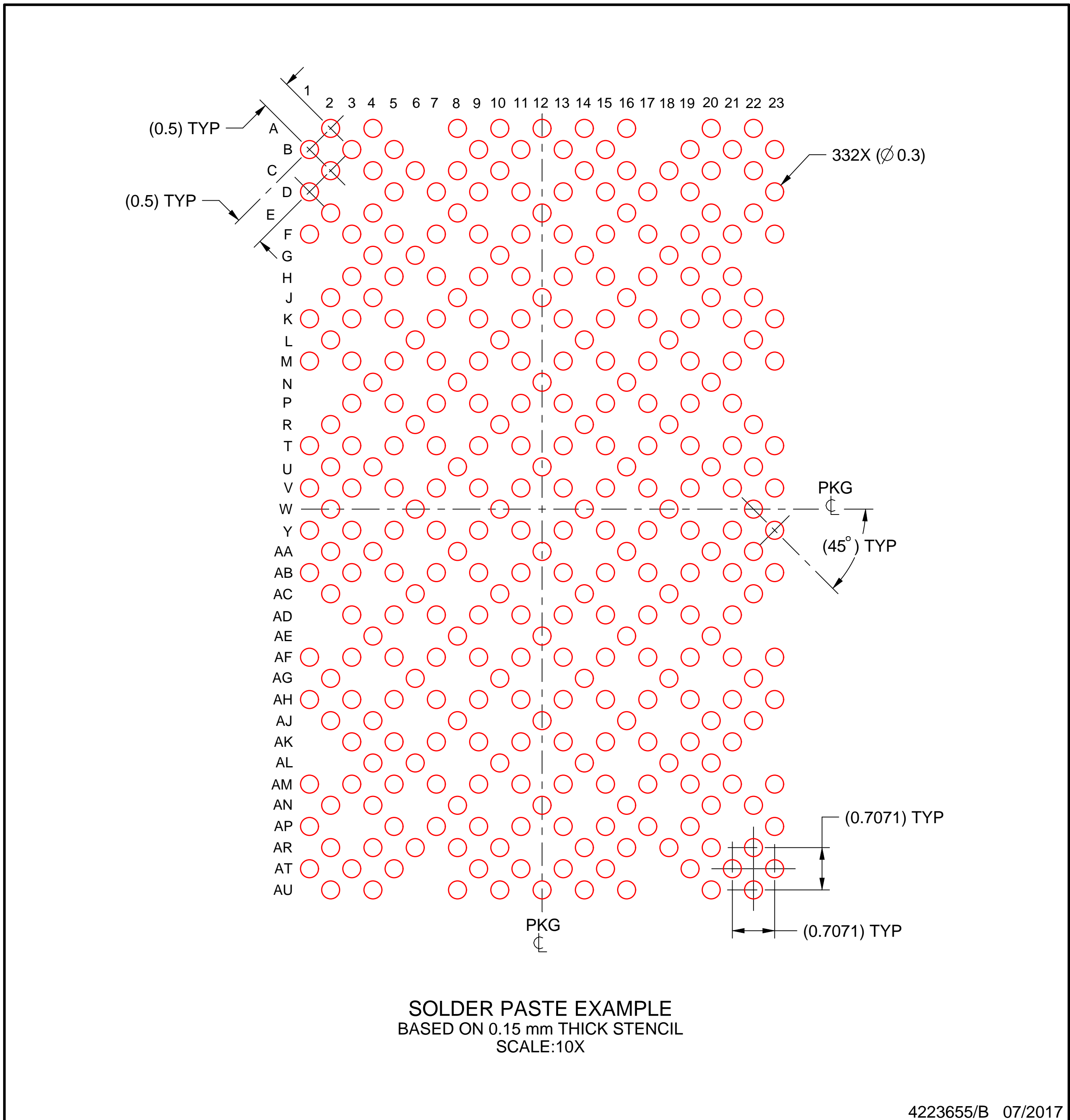
5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ACB0332A

FCBGA - 1.10 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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