

DS90UH940-Q1 支持 HDCP 的 1080p FPD-Link III 至 CSI-2 解串器

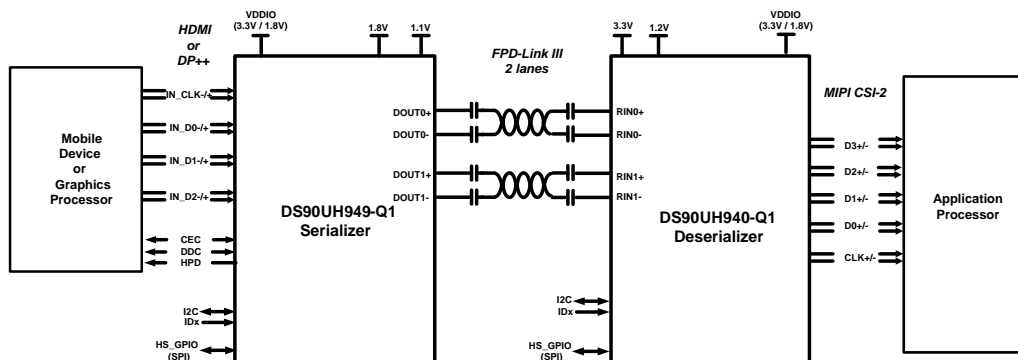
1 特性

- 支持高达 170MHz 的像素时钟频率，支持 WUXGA (1920x1200) 和 1080p60 分辨率 (24 位色深)
- 具有偏移补偿能力的单通道或双通道 FPD-Link III 接口
- MIPI D-PHY/CSI-2 发送器
 - 支持 2 通道或 4 通道两种可选操作的 CSI-2 输出端口
 - 每个 CSI-2 端口最多支持 4 个数据通道，每个通道最高 1.3Gbps
 - 视频格式: RGB888/666/565、YUV422/420 和 RAW8/10/12
 - 可编程虚拟通道标识符
- 集成具有片上密钥存储功能的高带宽数字内容保护 (HDCP) 加密引擎
- 速度高达 2.0Mbps 的通用输入输出 (GPIO)
- 具有自动温度和老化补偿功能，支持长达 15 米的电缆
- 速率高达 3.3Mbps 的串行外设接口 (SPI) 控制接口
- 具有 1Mbps 快速模式+ 的 I²C (主/从)
- 自适应接收均衡
- 支持多条 I2S (4 个数据) 通道
- 向后兼容 DS90UH925/925AQ-Q1 和 DS90UH927Q-Q1 FPD-Link III 串行器
- 汽车应用级产品: 符合 AEC-Q100 2 级要求

2 应用

- 汽车信息娱乐:
 - 中央信息显示屏
 - 后座娱乐系统
 - 数字仪表盘
- 高级驾驶员辅助系统 (ADAS) 摄像机系统

4 应用图



3 说明

DS90UH940-Q1 是一款 FPD-Link III 解串器，与 DS90UH949/947/929-Q1 串行器配合使用时可将单通道或双通道 FPD-Link III 流转换成 MIPI CSI-2 接口格式。该解串器能够在经济高效的 50Ω 单端同轴或 100Ω 差分屏蔽双绞线 (STP) 电缆上运行。它能够从单通道或双通道 FPD-Link III 串行流中恢复数据，然后将其转换为摄像机串行接口 (CSI-2) 格式，最高可支持 WUXGA 和 1080p60 视频分辨率 (24 位色深)。

FPD-Link III 接口支持通过同一条差分链路进行视频和音频数据传输以及全双工控制 (包括 I²C 和 SPI 通信)。通过两个差分对实现视频数据和控制的整合可减少互连线尺寸和重量，并简化了系统设计。通过使用低压差分信令、数据换序和随机生成最大限度地减少了电磁干扰 (EMI)。在向后兼容模式下，该器件在单一差分链路上最高可支持 WXGA 和 720p 分辨率 (24 位色深)。

该器件将自动检测 FPD-Link III 通道并提供一种时钟对齐和偏移补偿功能，无需任何特殊的训练模式。这可在互连线路 (例如，印刷电路板 (PCB) 布线) 中出现不匹配问题、电缆线对长度存在差异以及连接器不平衡时确保相位偏移在容差范围内。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|--------------|---------------------------|-----------------|
| DS90UH940-Q1 | 超薄四方扁平无引线 (WQFN) NKD (64) | 9.00mm x 9.00mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



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5 修订历史记录

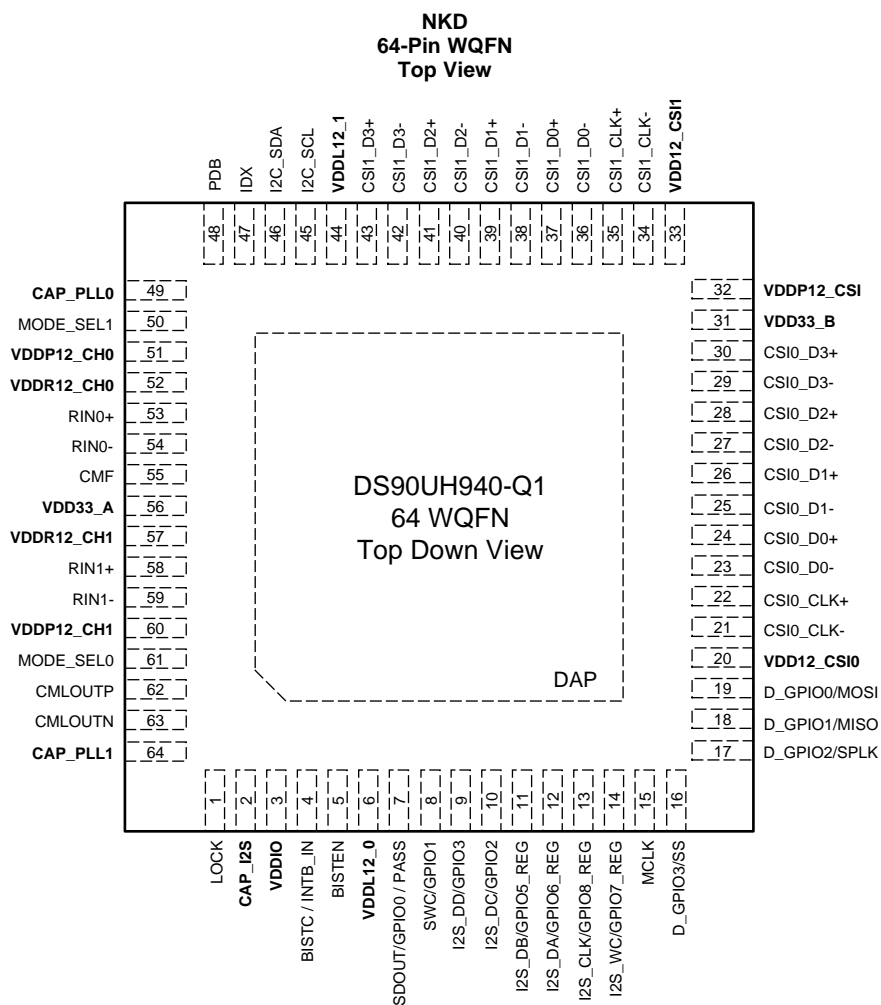
注：之前版本的页码可能与当前版本有所不同。

| Changes from Original (November 2014) to Revision A | Page |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added shared pins description on SPI pins | 5 |
| • Added shared pins description on GPIO pins | 6 |
| • Added shared pins description on D_GPIO pins | 6 |
| • Added shared pins description on register only GPIO pins. Changed "Local register control only" to "I2C register control only". | 6 |
| • Added shared pins description on slave mode I2S pins | 7 |
| • Added shared pins description on master mode I2S pins | 7 |
| • Added legend on I/O TYPE | 8 |
| • Moved Storage Temperature Range from ESD to Absolute Maximum Ratings table | 9 |
| • Added ESD Ratings table | 9 |
| • Changed IDD12Z limit from 11mA to 30mA per PE re-characterization | 12 |
| • Changed Fast Plus Mode t_{SP} maximum from 20ns to 50ns | 14 |
| • Added Power Sequence section | 22 |
| • Deleted MODE, CSI LANE, REPLICATE columns in MODE_SEL0 table | 40 |
| • Deleted MODE column. Added (CSI PORT) to CSI_SEL column in MODE_SEL1 table | 40 |
| • Changed default value from "0" to "1" in register 0x01[2] | 47 |
| • Added description to register 0x01[1] "Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table." | 47 |
| • Added to 0x02[7] in Description column "A Digital reset 0x01[0] should be asserted after toggling Output Enable bit LOW to HIGH" | 47 |
| • Added "Loaded from remote SER" in register 0x07[7:1] function column | 49 |
| • Changed signal detect bit to reserved in register 0x1C[1] | 52 |
| • Changed "0" to "0/1" in register RW column of 0x1C[1] | 52 |

修订历史记录 (接下页)

| | |
|-------------------------------------------------------------------------------------------------------|----|
| • Changed signal detect bit to reserved in register 0x1C[1] description | 52 |
| • Changed from Reserved to Rev-ID in register 0x1D Function column | 53 |
| • On register 0x22 added "(Loaded from remote SER)" | 56 |
| • Corrected in register 0x24[3] 0: Bist configured through "bit 0" to "bits 2:0" in description | 58 |
| • Added in register 0x24[2:1] additional description..... | 58 |
| • Changed in register 0x24[1] description to "internal" | 58 |
| • Changed in register 0x24[2] description to "internal" | 58 |
| • On register 0x28 added "Loaded from remote SER" | 59 |
| • Added clarification description on register 0x37 MODE_SEL | 61 |
| • Merged on 0x45 bits[7:4] and bits[3:0] default value: 0x08..... | 62 |

6 Pin Configurations and Functions



Pin Functions

| PIN | | I/O, TYPE | DESCRIPTION |
|-------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------|--------------------------|
| NAME | NUMBER | | |
| MIPI DPHY / CSI-2 OUTPUT PINS - Layout note: for unused CSI outputs, float those pins (do not connect to an external pullup or pulldown) | | | |
| CSI0_CLK- | 21 | O, DPHY | CSI0 Differential clock |
| CSI0_CLK+ | 22 | | |
| CSI0_D0- | 23 | O, DPHY | CSI0 Differential pair 0 |
| CSI0_D0+ | 24 | | |
| CSI0_D1- | 25 | O, DPHY | CSI0 Differential pair 1 |
| CSI0_D1+ | 26 | | |
| CSI0_D2- | 27 | O, DPHY | CSI0 Differential pair 2 |
| CSI0_D2+ | 28 | | |
| CSI0_D3- | 29 | O, DPHY | CSI0 Differential pair 3 |
| CSI0_D3+ | 30 | | |
| CSI1_CLK- | 34 | O, DPHY | CSI1 Differential clock |
| CSI1_CLK+ | 35 | | |
| CSI1_D0- | 36 | O, DPHY | CSI1 Differential pair 1 |
| CSI1_D0+ | 37 | | |
| CSI1_D1- | 38 | O, DPHY | CSI1 Differential pair 2 |
| CSI1_D1+ | 39 | | |

Pin Functions (continued)

| PIN | | I/O, TYPE | DESCRIPTION |
|-------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NUMBER | | |
| CSI1_D2- CSI1_D2+ | 40 41 | O, DPHY | CSI1 Differential pair 3 |
| CSI1_D3- CSI1_D3+ | 42 43 | O, DPHY | CSI1 Differential pair 3 |
| FPD-LINK III INTERFACE - Layout note: for unused FPD-LinkIII inputs, float those pins (do not connect to an external pullup or pulldown) | | | |
| RIN0- | 54 | I/O, CML | FPD-Link III Inverting Input/Output The output must be AC-coupled with a 33 nF capacitor. |
| RIN0+ | 53 | I/O, CML | FPD-Link III True Input/Output The output must be AC-coupled with a 33 nF capacitor. |
| RIN1- | 59 | I/O, CML | FPD-Link III Inverting Input/Output The output must be AC-coupled with a 33 nF capacitor. |
| RIN1+ | 58 | I/O, CML | FPD-Link III True Input/Output The output must be AC-coupled with a 33 nF capacitor. |
| CMF | 55 | I/O, CML | Common Mode Filter. Connect 0.1 μ F capacitor to GND |
| I2C PINS | | | |
| I2C_SDA | 46 | I/O, Open-Drain | I2C Data Input / Output interface Open drain. Must have an external pull-up resistor to VDDIO DO NOT FLOAT . Recommended pull-up: 4.7 k Ω . |
| I2C_SCL | 45 | I/O, Open-Drain | I2C Clock Input / Output Interface Open drain. Must have an external pull-up resistor to VDDIO DO NOT FLOAT . Recommended pull-up: 4.7 k Ω . |
| IDx | 47 | I, Analog Configuration Pin | Analog input. I2C Serial Control Bus Device ID Address. Table 11 |
| SPI PINS (Pin function programmed through register) - Layout note: for unused SPI pins, tie to an external pulldown | | | |
| MOSI (D_GPIO0) | 19 | Multi-function pin I/O, LVCMOS w/ weak internal PD | Master Out, Slave In. (Pin is shared with D_GPIO0) |
| MISO (D_GPIO1) | 18 | Multi-function pin I/O, LVCMOS w/ weak internal PD | Master In, Slave Out. (Pin is shared with D_GPIO1) |
| SPLK (D_GPIO2) | 17 | Multi-function pin I/O, LVCMOS w/ weak internal PD | Serial clock. (Pin is shared with D_GPIO2) |
| SS (D_GPIO3) | 16 | Multi-function pin I/O, LVCMOS w/ weak internal PD | Slave select. (Pin is shared with D_GPIO3) |
| CONTROL PINS | | | |
| MODE_SEL0 | 61 | I, Analog Configuration Pin | Analog input. Mode Select 0. Connect to external pull-up to VDD33 and pull-down to GND to create a voltage divider. See Table 8 |
| MODE_SEL1 | 50 | I, Analog Configuration Pin | Analog input. Mode Select 1. Connect to external pull-up to VDD33 and pull-down to GND to create a voltage divider. See Table 9 |

Pin Functions (continued)

| PIN | | I/O, TYPE | DESCRIPTION |
|--------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NUMBER | | |
| PDB | 48 | I, LVCMOS Configuration Pin w/ weak internal PD | Power-Down Mode Input Pin PDB = 1, device is enabled (normal operation) PDB = 0, device is powered down. When the device is in the POWER DOWN state, the LVCMOS outputs are in tri-state, the PLL is shutdown and IDD is minimized. Note: PDB pin requires minimum ramp time of 200us |
| BISTEN | 5 | I, LVCMOS Configuration Pin w/ weak internal PD | Bist Enable Pin 0: BIST Mode is disabled. 1: BIST Mode is enabled. See Built-In Self Test (BIST) for more information |
| BISTC (INTB_IN) | 4 | I, LVCMOS Configuration Pin w/ weak internal PD | Bist Clock Select. 0: PCLK 1: 33MHz (Pin is shared with INTB_IN) |
| INTB_IN (BISTC) | 4 | I, LVCMOS w/ weak internal PD | Interrupt input. (Pin is shared with BISTC) |
| BIDIRECTIONAL CONTROL CHANNEL (BCC) GPIO PINS (default pin function) - Layout note: for unused GPIO(s), tie to an external pulldown | | | |
| GPIO0 (SDOUT) | 7 | Multi-function pin I/O, LVCMOS | BCC GPIO0. default state: logic <i>LOW</i> (Pin is shared with SDOUT) |
| GPIO1 (SWC) | 8 | Multi-function pin I/O, LVCMOS | BCC GPIO1. default state: logic <i>LOW</i> (Pin is shared with SWC) |
| GPIO2 (I2S_DC) | 10 | Multi-function pin I/O, LVCMOS | BCC GPIO2. default state: logic <i>LOW</i> (Pin is shared with I2S_DC) |
| GPIO3 (I2S_DD) | 9 | Multi-function pin I/O, LVCMOS | BCC GPIO3. default state: logic <i>LOW</i> (Pin is shared with I2S_DD) |
| HIGH-SPEED GPIO PINS HIGH-SPEED GPIO PINS (default pin function) - Layout note: for unused D_GPIO(s), tie to an external pulldown | | | |
| D_GPIO0 (MOSI) | 19 | I/O, LVCMOS | General Purpose I/O in 2-lane FPD-Link III mode default state: <i>tri-state</i> (Pin is shared with MOSI) |
| D_GPIO1 (MISO) | 18 | I/O, LVCMOS | General Purpose I/O in 2-lane FPD-Link III mode default state: <i>tri-state</i> (Pin is shared with MISO) |
| D_GPIO2 (SPLK) | 17 | I/O, LVCMOS | General Purpose I/O in 2-lane FPD-Link III mode default state: <i>tri-state</i> (Pin is shared with SPLK) |
| D_GPIO3 (SS) | 16 | I/O, LVCMOS | General Purpose I/O in 2-lane FPD-Link III mode default state: <i>tri-state</i> (Pin is shared with SS) |
| REGISTER READ/Writes ONLY GPIO PINS (default pin function) - Layout note: for unused GPIO(s), tie to an external pulldown | | | |
| GPIO5_REG (I2S_DB) | 11 | Multi-function pin I/O, LVCMOS | General Purpose Input/Output 5 I2C register control only. default state: logic <i>LOW</i> (Pin is shared with I2S_DB) |
| GPIO6_REG (I2S_DA) | 12 | Multi-function pin I/O, LVCMOS | General Purpose Input/Output 6 I2C register control only. default state: logic <i>LOW</i> (Pin is shared with I2S_DA) |

Pin Functions (continued)

| PIN | | I/O, TYPE | DESCRIPTION |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NUMBER | | |
| GPIO7_REG (I2S_WC) | 14 | Multi-function pin I/O, LVCMOS | General Purpose Input/Output 7 I2C register control only. default state: logic <i>LOW</i> (Pin is shared with I2S_WC) |
| GPIO8_REG (I2S_CLK) | 13 | Multi-function pin I/O, LVCMOS | General Purpose Input/Output 8 I2C register control only. default state: logic <i>LOW</i> (Pin is shared with I2S_CLK) |
| SLAVE MODE LOCAL I2S CHANNEL PINS (Pin function programmed through register) - <i>Layout note: for unused I2S outputs, tie to an external pulldown</i> | | | |
| I2S_WC (GPIO7_REG) | 14 | Multi-function pin O, LVCMOS | Slave Mode I2S Word Clock Output. (Pin is shared with GPIO7_REG) |
| I2S_CLK (GPIO8_REG) | 13 | Multi-function pin O, LVCMOS | Slave Mode I2S Clock Output. (Pin is shared with GPIO8_REG) |
| I2S_DA (GPIO6_REG) | 12 | Multi-function pin O, LVCMOS | Slave Mode I2S Data Output. (Pin is shared with GPIO6_REG) |
| I2S_DB (GPIO5_REG) | 11 | Multi-function pin O, LVCMOS | Slave Mode I2S Data Output. (Pin is shared with GPIO5_REG) |
| I2S_DC (GPIO2_REG) | 10 | Multi-function pin O, LVCMOS | Slave Mode I2S Data Output. (Pin is shared with GPIO2) |
| I2S_DD (GPIO3_REG) | 9 | Multi-function pin O, LVCMOS | Slave Mode I2S Data Output. (Pin is shared with GPIO3) |
| MASTER MODE LOCAL I2S CHANNEL PINS (Pin function programmed through register) - <i>Layout note: for unused GPIO(s), tie to an external pulldown</i> | | | |
| SWC (GPIO1) | 8 | Multi-function pin O, LVCMOS | Master Mode I2S Word Clock Output. (Pin is shared with GPIO1) |
| SDOUT (GPIO0) | 7 | Multi-function pin O, LVCMOS | Master Mode I2S Data Output. (Pin is shared with GPIO0) |
| MCLK (GPIO9) | 15 | Multi-function pin O, LVCMOS | Master Mode I2S System Clock Output. (Pin is shared with GPIO9) |
| STATUS PINS - <i>Layout note: add a test point (TP) on these pins</i> | | | |
| PASS | 7 | O, LVCMOS | Normal mode status output pin (BISTEN = 0) PASS = 1: No fault detected on input display timing PASS = 0: Indicates an error condition or corruption in display timing. Fault condition occurs: <ol style="list-style-type: none"> DE length value mismatch measured once in succession VSync length value mismatch measured twice in succession BIST mode status output pin (BISTEN = 1) PASS = 1: No error detected PASS = 0: Error detected |
| POWER & GROUND ⁽¹⁾ | | | |
| VDD33_A, VDD33_B | 56 31 | Power | 3.3V (±10%) supply. Power to on-chip regulator. Requires 10 µF, 1 µF, 0.1 µF, and 0.01 µF capacitors to GND |
| VDDIO | 3 | Power | LVCMOS I/O power supply, 1.8V (±5%) OR 3.3V (±10%). Requires 10 µF, 1 µF, 0.1 µF, and 0.01 µF capacitors to GND |

(1) The VDD (VDD12, VDD33, and VDDIO) supply ramp should be faster than 1.5ms with a monotonic rise

Pin Functions (continued)

| PIN | | I/O, TYPE | DESCRIPTION |
|-------------------|--------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NUMBER | | |
| VDD12_CSI0 | 20 | Power | 1.2V (±5%) supplies. Requires 10 μ F, 1 μ F, 0.1 μ F, and 0.01 μ F capacitors to GND at each VDD pin. |
| VDDP12_CSI | 32 | | |
| VDD12_CSI1 | 33 | | |
| VDDL12_0 | 6 | | |
| VDDL12_1 | 44 | | |
| VDDP12_CH0 | 51 | | |
| VDDR12_CH0 | 52 | | |
| VDDP12_CH1 | 60 | | |
| VDDR12_CH1 | 57 | | |
| CAP_PLL0 | 49 | CAP | Decoupling capacitor connection for on-chip regulator. Each requires a 0.1 μ F decoupling capacitor to GND. |
| CAP_PLL1 | 64 | | |
| CAP_I2S | 2 | | |
| VSS | DAP | Ground | DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 32 vias. |
| OTHER PINS | | | |
| CMLOUTP | 62 | O, CML | Monitor point for equalized differential signal. Layout recommendation: 1) place 0.1 μ F series capacitor on CMLOUTP and CMLOUTN 2) place 100ohm termination between 0.1 μ F away from CMLOUTP and CMLOUTN pins 3) place test points from 0.1 μ F capacitors |
| CMLOUTN | 63 | | |

The definitions below define the functionality of the I/O cells for each pin.

I/O TYPE:

- P = Power Supply
- G = Ground
- CML = CML Interface
- DPHY = MIPI DPHY Interface
- Analog = Analog Interface
- LVCMOS = LVCMOS pin; Referenced to VDDIO IO supply
- I = Input
- O = Output
- I/O = Input/Output
- PD, PU = Internal Pull-Down/Pull-Up (All strap pins have weak internal pull-ups or pull-downs. If the default strap value is needed to be changed then an external resistor should be used.)
- Multi-function pin

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

| PARAMETER | | MIN | MAX | UNIT |
|------------------|----------------------------|------|-------------|------|
| VDD33 | Supply voltage | -0.3 | 4.0 | V |
| VDD12 | Supply voltage | -0.3 | 1.8 | V |
| VDDIO | Supply voltage | -0.3 | 4.0 | V |
| | LVC MOS I/O voltage | -0.3 | VDDIO + 0.3 | V |
| | FPD-Link III input voltage | -0.3 | 2.75 | V |
| T _J | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) For soldering specifications, see product folder at www.ti.com and [SNOA549](#)

7.2 ESD Ratings—JEDEC

| | | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±8000 |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1250 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings—IEC and ISO

| | | | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|--------|
| V _(ESD) | Electrostatic discharge | R _D = 330 Ω, C _S = 150 pF | IEC, powered-up only contact discharge (R _{IN0+} , R _{IN0-} , R _{IN1+} , R _{IN1-}) | ±8000 |
| | | | IEC, powered-up only air-gap discharge (R _{IN0+} , R _{IN0-} , R _{IN1+} , R _{IN1-}) | ±15000 |
| | | R _D = 330 Ω, C _S = 150 and 330 pF | ISO10605 contact discharge (R _{IN0+} , R _{IN0-} , R _{IN1+} , R _{IN1-}) | ±8000 |
| | | | ISO10605 air-gap discharge (R _{IN0+} , R _{IN0-} , R _{IN1+} , R _{IN1-}) | ±15000 |
| | | R _D = 2 kΩ, C _S = 150 and 330 pF | ISO10605 contact discharge (R _{IN0+} , R _{IN0-} , R _{IN1+} , R _{IN1-}) | ±8000 |
| | | | ISO10605 air-gap discharge (R _{IN0+} , R _{IN0-} , R _{IN1+} , R _{IN1-}) | ±15000 |

7.4 Recommended Operating Conditions

| | MIN | NOM | MAX | UNIT |
|--------------------------------------------------|------|-----|------|-------------------|
| Supply Voltage (VDD33) | 3.0 | 3.3 | 3.6 | V |
| Supply Voltage (VDD18) | 1.71 | 1.8 | 1.89 | V |
| Supply Voltage (VDD12) | 1.14 | 1.2 | 1.26 | V |
| Operating Free Air Temperature (T _A) | -40 | 25 | 105 | °C |
| Pixel Clock Frequency (Single Link) | 25 | | 96 | MHz |
| Pixel Clock Frequency (Dual Link) | 50 | | 170 | MHz |
| Supply Noise -- VDD33 (DC-50MHz) | | | 100 | mV _{p-p} |
| Supply Noise -- VDD18 (DC-50MHz) | | | 50 | mV _{p-p} |
| Supply Noise -- VDD12 (DC-50MHz) | | | 25 | mV _{p-p} |

7.5 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DS90UH940-Q1 | UNIT |
|-------------------------------|----------------------------------------------|--------------|------|
| | | WQFN (NKD) | |
| | | 64 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 24.8 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 6.2 | |
| R _{θJB} | Junction-to-board thermal resistance | 3.6 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.1 | |
| ψ _{JB} | Junction-to-board characterization parameter | 3.6 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.6 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------|------------------------------|--------------------------------------------|-------------------------------------------------------------|-----------------|-----|-----------------|------|
| 3.3V LVCMOS I/O (VDDIO = 3.3V ± 10%) | | | | | | | |
| V _{IH} | High Level Input Voltage | | PDB, BISTEN, BISTC, GPIO[3:0], D_GPIO[3:0], | 2.0 | | VDDIO | V |
| V _{IL} | Low Level Input Voltage | | | 0 | | 0.8 | V |
| I _{IN} | Input Current | V _{IN} = 0V or VDDIO | I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS | -10 | | 10 | μA |
| V _{OH} | High Level Output Voltage | I _{OH} = -4mA | | 2.4 | | VDDIO | V |
| V _{OL} | Low Level Output Voltage | I _{OL} = +4mA | | 0 | | 0.4 | V |
| I _{OS} | Output Short Circuit Current | V _{OUT} = 0V | | | -55 | | mA |
| I _{OZ} | Tri-state Output Current | PDB = 0V V _{OUT} = 0V or VDDIO | | -20 | | 20 | μA |
| C _{IN} | Input Capacitance | | | | | 10 | pF |
| 1.8V LVCMOS I/O (VDDIO = 1.8V ± 5%) | | | | | | | |
| V _{IH} | High Level Input Voltage | | PDB, BISTEN, BISTC, GPIO[3:0], D_GPIO[3:0], | 0.65 * VDDIO | | VDDIO | V |
| V _{IL} | Low Level Input Voltage | | | 0 | | 0.35 * VDDIO | V |
| I _{IN} | Input Current | V _{IN} = 0V or VDDIO | I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS | -10 | | 10 | μA |
| V _{OH} | High Level Output Voltage | I _{OH} = -4mA | | VDDIO- 0.45 | | VDDIO | V |
| V _{OL} | Low Level Output Voltage | I _{OL} = +4mA | | 0 | | 0.45 | V |
| I _{OS} | Output Short Circuit Current | V _{OUT} = 0V | | | -35 | | mA |
| I _{OZ} | Tri-state Output Current | PDB = 0V V _{OUT} = 0V or VDDIO | | -20 | | 20 | μA |
| C _{IN} | Input Capacitance | | | | | 10 | pF |
| SERIAL CONTROL BUS (VDDIO = 1.8V ± 5% OR 3.3V ± 10%) | | | | | | | |
| V _{IH} | Input High Level | | I2C_SDA, I2C_SCL | 0.7 * VDDIO | | VDD33 | V |
| V _{IL} | Input Low Level | | | GND | | 0.3 * VDDIO | V |
| V _{HY} | Input Hysteresis | | | | >50 | | mV |
| V _{OL} | Output Low Level | I _{OL} = +4mA | | 0 | | 0.4 | V |
| I _{IN} | Input Current | V _{IN} = 0V or VDDIO | | -10 | | 10 | μA |

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT | |
|------------------------------------|----------------------------------------------|----------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|------|-----|-----|-------------------|----------|
| FPD-LINK III CML INPUT | | | | | | | | |
| V_{TH} | Differential Threshold High Voltage | $V_{CM} = 2.1V$ (Internal V_{BIAS}) | RIN0+, RIN0- RIN1+, RIN1- | | | 50 | mV | |
| V_{TL} | Differential Threshold Low Voltage | | | | | -50 | mV | |
| V_{ID} | Input Differential Threshold | | | | | 100 | mV | |
| V_{CM} | Differential Common-mode Voltage | | | | | 2.1 | V | |
| R_T | Internal Termination Resistor - Differential | | | | | 80 | 100 | 120 |
| HSTX DRIVER | | | | | | | | |
| V_{CMTX} | HS transmit static common-mode voltage | | CS10_D3±, CS10_D2±, CS10_D1±, CS10_D0±, CS10_CLK±, CS11_D3±, CS11_D2±, CS11_D1±, CS11_D0±, CS11_CLK± | 150 | 200 | 250 | mV | |
| $ \Delta V_{CMTX(1,0)} $ | V_{CMTX} mismatch when output is 1 or 0 | | | | | 5 | mV _{P-P} | |
| $ V_{OD} $ | HS transmit differential voltage | | | | 140 | 200 | 270 | mV |
| $ \Delta V_{OD} $ | V_{OD} mismatch when output is 1 or 0 | | | | | | 14 | mV |
| V_{OHHS} | HS output high voltage | | | | | | 360 | mV |
| Z_{OS} | Single-ended output impedance | | | | 40 | 50 | 62.5 | Ω |
| ΔZ_{OS} | Mismatch in single-ended output impedance | | | | | | 10 | % |
| LPTX DRIVER | | | | | | | | |
| V_{OH} | High Level Output Voltage | $I_{OH} = -4mA$ | CS10_D3±, CS10_D2±, CS10_D1±, CS10_D0±, CS10_CLK±, CS11_D3±, CS11_D2±, CS11_D1±, CS11_D0±, CS11_CLK± | 1.05 | 1.2 | 1.3 | V | |
| V_{OL} | Low Level Output Voltage | $I_{OL} = +4mA$ | | | -50 | | 50 | mV |
| Z_{OLP} | Output impedance | | | | 110 | | | Ω |
| LOOP-THROUGH MONITOR OUTPUT | | | | | | | | |
| V_{ODP-P} | Differential Output Voltage | $R_L = 100\Omega$ | CMLOUTP, CMLOUTN | | 360 | | mV | |
| SUPPLY CURRENT | | | | | | | | |
| P_T | Total Power Consumption, Normal Operation | Checkerboard Pattern, 170MHz. See Figure 1 . 2-lane FPD-Link III Input, 2 MIPI lanes Output | VDD | | 628 | 875 | mW | |
| P_Z | Total Power Consumption, Power-Down Mode | PDB = 0V | | | 10 | 45 | mW | |
| IDD12 | Supply Current, Normal Operation | Checkerboard Pattern, 96MHz. See Figure 1 . 1-lane FPD-Link III Input, 2 MIPI lanes Output | VDD12 = 1.2 V | | 150 | 250 | mA | |
| IDD33 | | | VDD33 = 3.6 V | | 90 | 122 | mA | |
| IDDIO | | | VDDIO = 1.89 V | | 1 | 6 | mA | |
| | | | VDDIO = 3.6 V | | 1 | 6 | mA | |
| IDD12 | Supply Current, Normal Operation | Checkerboard Pattern, 96MHz. See Figure 1 . 1-lane FPD-Link III Input, 4 MIPI lanes Output | VDD12 = 1.2 V | | 125 | 225 | mA | |
| IDD33 | | | VDD33 = 3.6 V | | 90 | 122 | mA | |
| IDDIO | | | VDDIO = 1.89 V | | 1 | 6 | mA | |
| | | | VDDIO = 3.6 V | | 1 | 6 | mA | |

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT |
|-----------|----------------------------------|----------------------------------------------------------------------------------------------------------------|----------------|-----|-----|-----|------|
| IDD12 | Supply Current, Normal Operation | Checkerboard Pattern, 170MHz. See Figure 1 . 2-lane FPD-Link III Input, 2 MIPI lanes Output | VDD12 = 1.2 V | | 250 | 345 | mA |
| IDD33 | | | VDD33 = 3.6 V | | 90 | 122 | mA |
| IDDIO | | | VDDIO = 1.89 V | | 1 | 6 | mA |
| | | | VDDIO = 3.6 V | | 1 | 6 | mA |
| IDD12 | Supply Current, Normal Operation | Checkerboard Pattern, 170MHz. See Figure 1 . 2-lane FPD-Link III Input, 4 MIPI lanes Output | VDD12 = 1.2 V | | 220 | 300 | mA |
| IDD33 | | | VDD33 = 3.6 V | | 90 | 122 | mA |
| IDDIO | | | VDDIO = 1.89 V | | 1 | 6 | mA |
| | | | VDDIO = 3.6 V | | 1 | 6 | mA |
| IDD12Z | Supply Current, Power Down Mode | PDB = 0 V | VDD12 = 1.2 V | | 2 | 30 | mA |
| IDD33Z | | | VDD33 = 3.6 V | | 2 | 8 | mA |
| IDDIOZ | | | VDDIO = 1.89 V | | 0.1 | 0.3 | mA |
| | | | VDDIO = 3.6 V | | 0.1 | 0.3 | mA |

7.7 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------------------------|-------------------------------------------------------------------------------|--------------------------------|------------------------|------------------------------------|------------------|
| GPIO BIT RATE | | | | | | |
| R _{b,FC} | Forward Channel Bit Rate | PCLK = 25MHz - 170MHz ⁽¹⁾ | GPIO[3:0] | | 0.25 * PCLK | Mbps |
| R _{b,BC} | Back Channel Bit Rate | | | | 133 | kbps |
| R _{b,BC} | Back Channel Bit Rate | High Speed (2-lane Mode), 1 D_GPIO active. See Table 4 . | D_GPIO[3:0] | | 2.0 | Mbps |
| | | High Speed (2-lane Mode), 2 D_GPIO's active. See Table 4 . | | | 1.33 | Mbps |
| | | High Speed (2-lane Mode), 4 D_GPIO's active. See Table 4 . | | | 800 | kbps |
| | | Normal mode. See Table 4 . | | | 133 | kbps |
| t _{GPIO,FC} | GPIO Pulse Width, Forward Channel | | GPIO[3:0] | | >2 / PCLK ⁽¹⁾ | s |
| t _{GPIO,BC} | GPIO Pulse Width, Back Channel | | GPIO[3:0] | | 20 | μs |
| RESET | | | | | | |
| t _{LRST} | PDB Reset Low Pulse | | PDB | 2 | | ms |
| LOOP-THROUGH MONITOR OUTPUT | | | | | | |
| E _W | Differential Output Eye Opening Width | RL = 100Ω, Jitter frequency > PCLK ⁽¹⁾ / 40 | CMLOUTP, CMLOUTN | | 0.4 | UI |
| E _H | Differential Output Eye Height | See Figure 2 . | | | >300 | mV |
| FPD-LINK III CML INPUT | | | | | | |
| t _{DDL} | Lock Time | See Figure 4 . | RIN0+, RIN0-, RIN1+, RIN1- | 5 10 ⁽²⁾ | | ms |
| I2S TRANSMITTER | | | | | | |
| t _{J,I2S} | Clock Output Jitter | | I2S_CLK | | 2 | ns |
| t _{I2S} | I2S Clock Period ⁽³⁾ | See Figure 9 . | | | >2 / PCLK ⁽¹⁾ or >77 | ns |
| t _{HC,I2S} | I2S Clock High Time ⁽³⁾ | See Figure 9 . | | | 0.48 | t _{I2S} |
| t _{LC,I2S} | I2S Clock Low Time ⁽³⁾ | See Figure 9 . | | | 0.48 | t _{I2S} |
| t _{SR,I2S} | I2S Set-up Time | See Figure 9 . | I2S_DA, I2S_DB, I2S_DC, I2S_DD | | 0.4 | t _{I2S} |
| t _{HR,I2S} | I2S Hold Time | See Figure 9 . | | | 0.4 | t _{I2S} |

(1) PCLK refers to the equivalent pixel clock frequency, which is equal to the FPD-Link III line rate / 35.

(2) This parameter is specified by characterization and is not tested in production.

(3) I2S specifications for t_{LC,I2S} and t_{HC,I2S} pulses must each be greater than 1 PCLK period to ensure sampling and supersedes the 0.35*t_{I2S} requirement. t_{LC,I2S} and t_{HC,I2S} must be longer than the greater of either 0.35*t_{I2S} or 2 * PCLK.

7.8 Timing Requirements for the Serial Control Bus

Over I²C supply and temperature ranges unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|-----------------------------------------------------------------------------------|-----------------|------|-----|---------------------|------|
| f _{SCL} | SCL Clock Frequency | Standard Mode | >0 | | 100 | kHz |
| | | Fast Mode | >0 | | 400 | kHz |
| | | Fast Plus Mode | >0 | | 1 | MHz |
| t _{LOW} | SCL Low Period | Standard Mode | 4.7 | | | μs |
| | | Fast Mode | 1.3 | | | μs |
| | | Fast Plus Mode | 0.5 | | | μs |
| t _{HIGH} | SCL High Period | Standard Mode | 4.0 | | | μs |
| | | Fast Mode | 0.6 | | | μs |
| | | Fast Plus Mode | 0.26 | | | μs |
| t _{HD;STA} | Hold time for a start or a repeated start condition Figure 8 | Standard Mode | 4.0 | | | μs |
| | | Fast Mode | 0.6 | | | μs |
| | | Fast Plus Mode | 0.26 | | | μs |
| t _{SU;STA} | Set Up time for a start or a repeated start condition Figure 8 | Standard Mode | 4.7 | | | μs |
| | | Fast Mode | 0.6 | | | μs |
| | | Fast Plus Mode | 0.26 | | | μs |
| t _{HD;DAT} | Data Hold Time Figure 8 | Standard Mode | 0 | | | μs |
| | | Fast Mode | 0 | | | μs |
| | | Fast Plus Mode | 0 | | | μs |
| t _{SU;DAT} | Data Set Up Time Figure 8 | Standard Mode | 250 | | | ns |
| | | Fast Mode | 100 | | | ns |
| | | Fast Plus Mode | 50 | | | ns |
| t _{SU;STO} | Set Up Time for STOP Condition Figure 8 | Standard Mode | 4.0 | | | μs |
| | | Fast Mode | 0.6 | | | μs |
| | | Fast Plus Mode | 0.26 | | | μs |
| t _{BUF} | Bus Free Time Between STOP and START Figure 8 | Standard Mode | 4.7 | | | μs |
| | | Fast Mode | 1.3 | | | μs |
| | | Fast Plus Mode | 0.5 | | | μs |
| t _r | SCL & SDA Rise Time, Figure 8 | Standard Mode | | | 1000 ⁽¹⁾ | ns |
| | | Fast Mode | | | 300 ⁽¹⁾ | ns |
| | | Fast Plus Mode | | | 120 ⁽¹⁾ | ns |
| t _f | SCL & SDA Fall Time, Figure 8 | Standard Mode | | | 300 ⁽¹⁾ | ns |
| | | Fast mode | | | 300 ⁽¹⁾ | ns |
| | | Fast Plus Mode | | | 120 ⁽¹⁾ | ns |
| C _b | Capacitive Load for Each Bus Line | Standard Mode | | | 400 | pF |
| | | Fast Mode | | | 400 | pF |
| | | Fast Plus Mode | | | 550 | pF |
| t _{SP} | Input Filter | Fast Mode | | | 50 | ns |
| | | Fast Plus Mode | | | 50 | ns |

(1) Parameter is specified by bench characterization and is not tested in production.

7.9 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT | |
|--------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----------|------|----------------------------------------|------|-------------------|-------|
| HSTX DRIVER | | | | | | | | |
| HSTX _{DBR} | Data bit rate ⁽¹⁾ | MIPI 2 Lanes | CSI0_D0± | 350 | | 1344 | Mbps | |
| | | MIPI 4 Lanes | CSI0_D1± | 175 | | 1190 | | |
| f _{CLK} | DDR Clock frequency ⁽¹⁾ | MIPI 2 Lanes | CSI0_D2± | 175 | | 672 | MHz | |
| | | MIPI 4 Lanes | CSI0_D3± | 87.5 | | 595 | | |
| ΔV _{CMTX(HF)} | Common mode voltage variations HF ⁽¹⁾ | Above 450MHz | CSI1_D1± | | | 15 | mV _{RMS} | |
| ΔV _{CMTX(LF)} | Common mode voltage variations LF ⁽¹⁾ | Between 50 and 450MHz | CSI1_D2± | | | 25 | mV _{RMS} | |
| t _{RHS} t _{FHS} | 20% to 80% Rise and Fall HS ⁽¹⁾ | HS bit rates ≤ 1 Gbps (UI ≥ 1 ns) | CSI1_D3± | | | 0.3 | UI | |
| | | HS bit rates > 1 Gbps (UI < 1 ns) | CSI0_CLK± | | | 0.35 | UI | |
| | | Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps | | | 100 | | | ps |
| SDD _{TX} | TX differential return loss ⁽¹⁾ | f _{LP} MAX | | | | -18 | dB | |
| | | f _H | | | | | | |
| | | f _{MAX} | | | | -9 | dB | |
| LPTX DRIVER | | | | | | | | |
| t _{RLP} | Rise Time LP ⁽²⁾ (3) | 15% to 85% rise time | CSI0_D0± | | | 25 | ns | |
| t _{FLP} | Fall Time LP ⁽²⁾ (3) | 15% to 85% fall time | CSI0_D1± | | | 25 | ns | |
| t _{REOT} | Rise Time Post-EoT ⁽¹⁾ (3) | 30%-85% rise time | CSI0_D2± | | | 35 | ns | |
| t _{LP-PULSE-TX} | Pulse width of the LP exclusive-OR clock ⁽¹⁾ (3) | First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state | CSI0_D3± | | | | | |
| | | All other pulses | CSI1_D0± | 40 | | | ns | |
| t _{LP-PER-TX} | Period of the LP exclusive-OR clock ⁽¹⁾ | | CSI1_D1± | | | | | |
| | | | CSI1_D2± | 20 | | | ns | |
| DV/DtSR | Slew rate ⁽²⁾ (3) | Load = 0pF | CSI0_CLK± | | | 500 | mV/ns | |
| | | Load = 5pF | CSI1_CLK± | | | 300 | mV/ns | |
| | | Load = 20pF | | | | 250 | mV/ns | |
| | | Load = 70pF | | | | 150 | mV/ns | |
| | | Load = 0 to 70pF (Falling Edge Only) | | | 30 | | | mV/ns |
| | | Load = 0 to 70pF (Rising Edge Only) | | | 30 | | | mV/ns |
| | | Load = 0 to 70pF (Rising Edge Only) | | | 30 - 0.075*(V _{O,INST} - 700) | | | mV/ns |
| C _{LOAD} | Load capacitance ⁽³⁾ | | | 0 | | 70 | pF | |

(1) Specification is ensured by design and is not tested in production.

(2) This parameter is specified by characterization and is not tested in production.

(3) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2ns delay.

Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|----------------------------------|------------------------------------------------------------|---------------|-----|----------------|-------------------|
| DATA-CLOCK TIMING SPECIFICATIONS ⁽¹⁾ (Figure 10) | | | | | | | |
| U _{INST} | UI instantaneous | fCLK = CSI-2 DDR Clock frequency | CSI0_D0± CSI0_D1± | 1/(fCLK * 2) | | | UI |
| ΔUI | UI variation PCLK = 25 - 96MHz | UI ≥ 1ns | CSI0_D2± CSI0_D3± | -10% | | 10% | UI |
| | | UI < 1ns | CSI1_D0± | -5% | | 5% | UI |
| t _{SKEW(TX)} | Data to Clock Skew (measured at transmitter) Skew between clock and data from ideal center | Data rate ≤ 1 Gbps | CSI1_D1± | -0.15 | | 0.15 | U _{INST} |
| | | Data rate > 1 Gbps | CSI1_D2± CSI1_D3± CSI0_CLK± CSI1_CLK± | -0.2 | | 0.2 | U _{INST} |
| CSI-2 TIMING SPECIFICATIONS ⁽¹⁾ (Figure 11, Figure 12) | | | | | | | |
| t _{CLK-MISS} | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX | | CSI0_D0± CSI0_D1± CSI0_D2± | 60 | | | ns |
| t _{CLK-POST} | HS exit | | CSI0_D3± CSI1_D0± | 60 + 52*UI | | | ns |
| t _{CLK-PRE} | Time HS clock shall be driver prior to any associated Data Lane beginning the transition from LP to HS mode | | CSI1_D1± CSI1_D2± CSI1_D3± CSI0_CLK± CSI1_CLK± | 8 | | | UI |
| t _{CLK-PREPARE} | Clock Lane HS Entry | | | 38 | | 95 | ns |
| t _{CLK-SETTLE} | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions | | | 95 | | 300 | ns |
| t _{CLK-TERM-EN} | Time-out at Clock Lane Display Module to enable HS Termination | | | | | 38 | ns |
| t _{CLK-TRAIL} | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst | | | 60 | | | ns |
| t _{CLK-PREPARE + t_{CLK-ZERO}} | TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock | | | 300 | | | ns |
| t _{D-TERM-EN} | Time for the Data Lane receiver to enable the HS line termination | | | | | 35 + 4*UI | ns |
| t _{EOT} | Transmitted time interval from the start of t _{HS-TRAIL} to the start of the LP-11 state following a HS burst | see ⁽⁴⁾ | | | | 105 + 12*UI | ns |
| t _{HS-EXIT} | Time that the transmitter drives LP=11 following a HS burst | | | 100 | | | ns |
| t _{HS-PREPARE} | Data Lane HS Entry | | | 40 + 4*UI | | 85 + 6*UI | ns |

(4) (a) 1280x720p60; PCLK = 74.25MHz; 4 MIPI lanes reg0x6c=0x02; reg0x6d=0x84
 (b) 1280x720p60; PCLK = 74.25MHz; 2 MIPI lanes reg0x6c=0x02; reg0x6d=0x89
 (c) 640x480p60; PCLK = 25MHz; 4 MIPI lanes reg0x6c=0x02; reg0x6d=0x82
 (d) 640x480p60; PCLK = 25MHz; 2 MIPI lanes reg0x6c=0x02; reg0x6d=0x83
 (e) Other video formats may require additional register configuration.

Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER | TEST CONDITIONS | PIN/FREQ. | MIN | TYP | MAX | UNIT |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|---------------------|-----|---------------------|------|
| $t_{HS-PREPARE} + t_{HS-ZERO}$ | $t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence | | 145 + $10 \cdot UI$ | | | ns |
| $t_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $t_{HS-SETTLE}$ | | 85 + $6 \cdot UI$ | | 145 + $10 \cdot UI$ | ns |
| $t_{HS-SKIP}$ | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | | 40 | | 55 + $4 \cdot UI$ | ns |
| $t_{HS-TRAIL}$ | Data Lane HS Exit | | 60 + $4 \cdot UI$ | | | ns |
| t_{LPX} | Transmitted length of LP state | | 50 | | | ns |
| t_{WAKEUP} | Recovery Time from Ultra Low Power State (ULPS) | | 1 | | | ms |

7.10 Timing Diagrams and Test Circuits

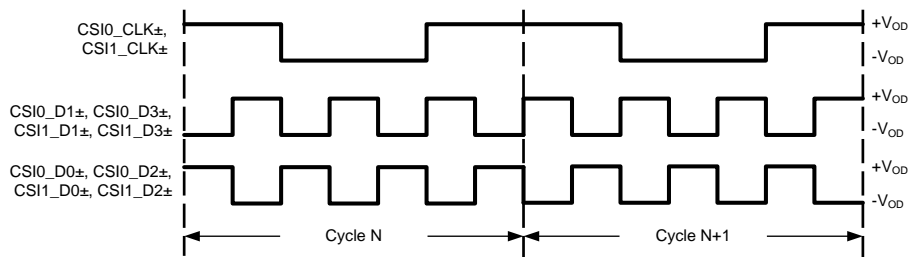


Figure 1. Checkerboard Data Pattern

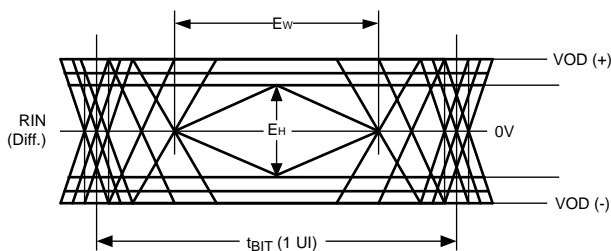


Figure 2. CML Output Driver



Figure 3. LVCMOS Transition Times

Timing Diagrams and Test Circuits (continued)

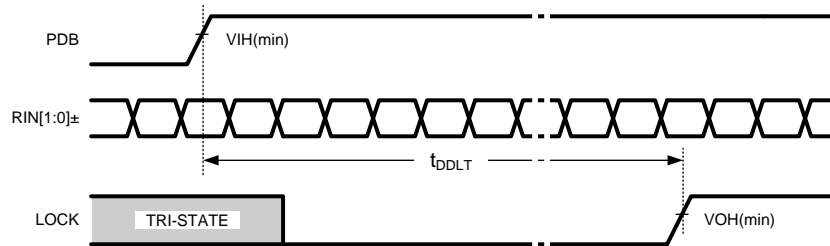


Figure 4. CML PLL Lock Time

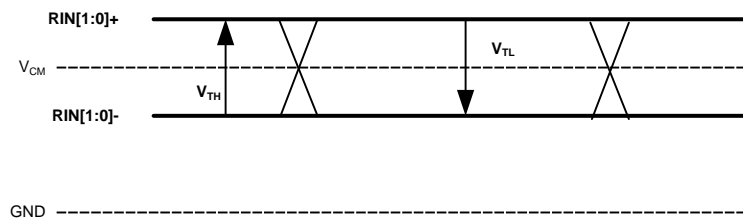


Figure 5. FPD-Link III Receiver DC V_{TH}/V_{TL} Definition

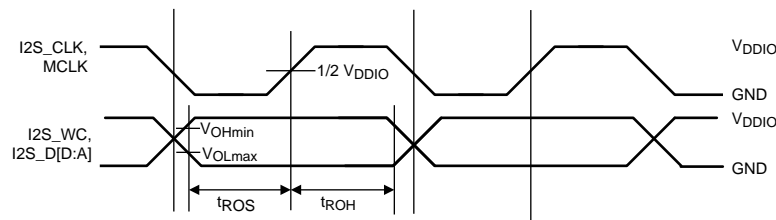


Figure 6. Output Data Valid (Setup and Hold) Times

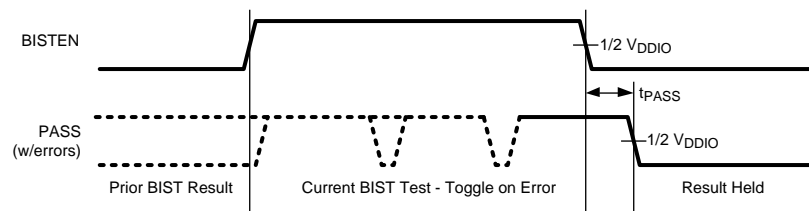


Figure 7. BIST PASS Waveform

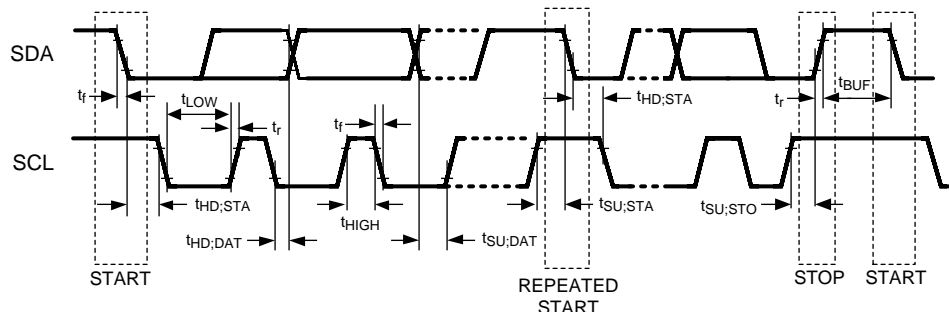


Figure 8. Serial Control Bus Timing Diagram

Timing Diagrams and Test Circuits (continued)

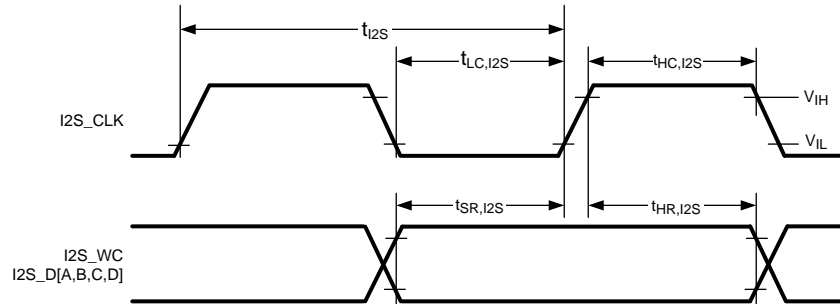


Figure 9. I2S Timing

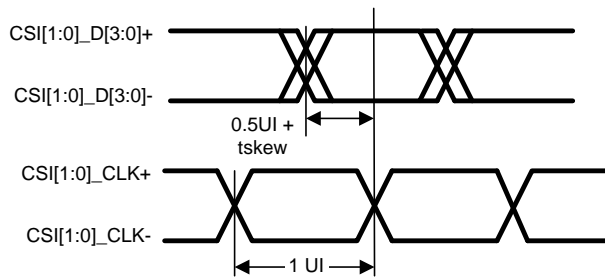


Figure 10. Clock and Data Timing in HS Transmission

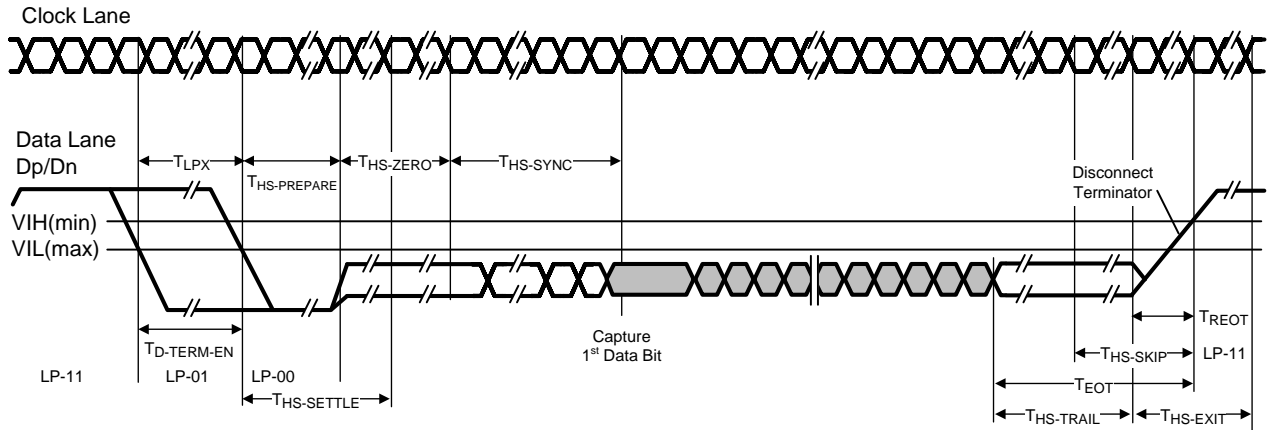


Figure 11. High Speed Data Transmission Burst

Timing Diagrams and Test Circuits (continued)

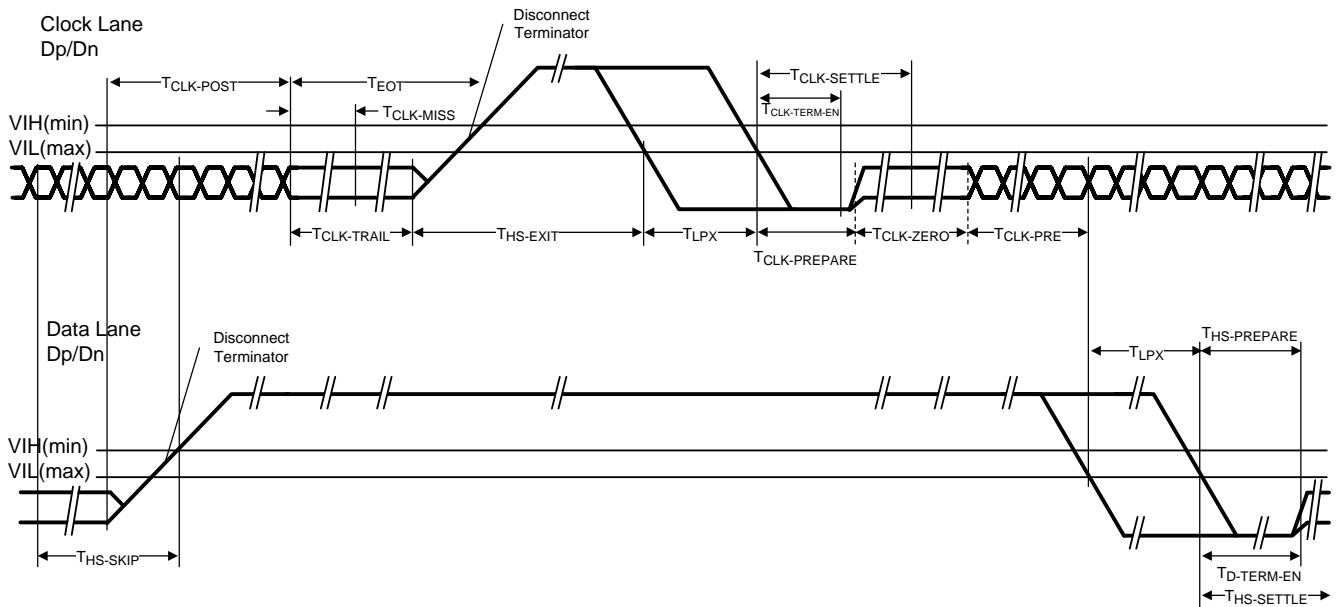


Figure 12. Switching the Clock Lane between Clock Transmission and Low-Power Mode

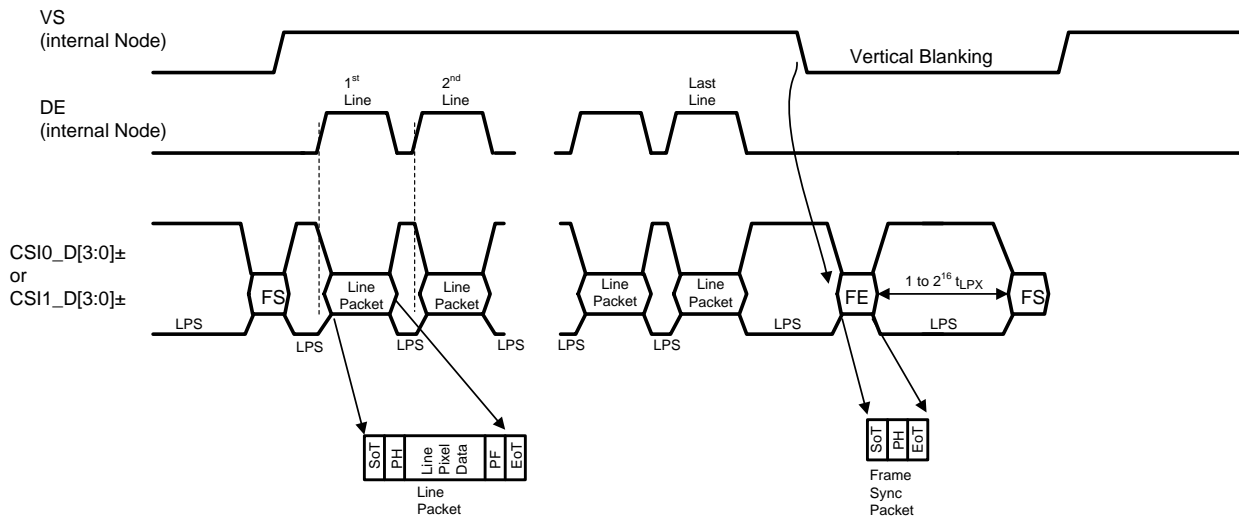


Figure 13. Long Line Packets and Short Frame Sync Packets

Timing Diagrams and Test Circuits (continued)

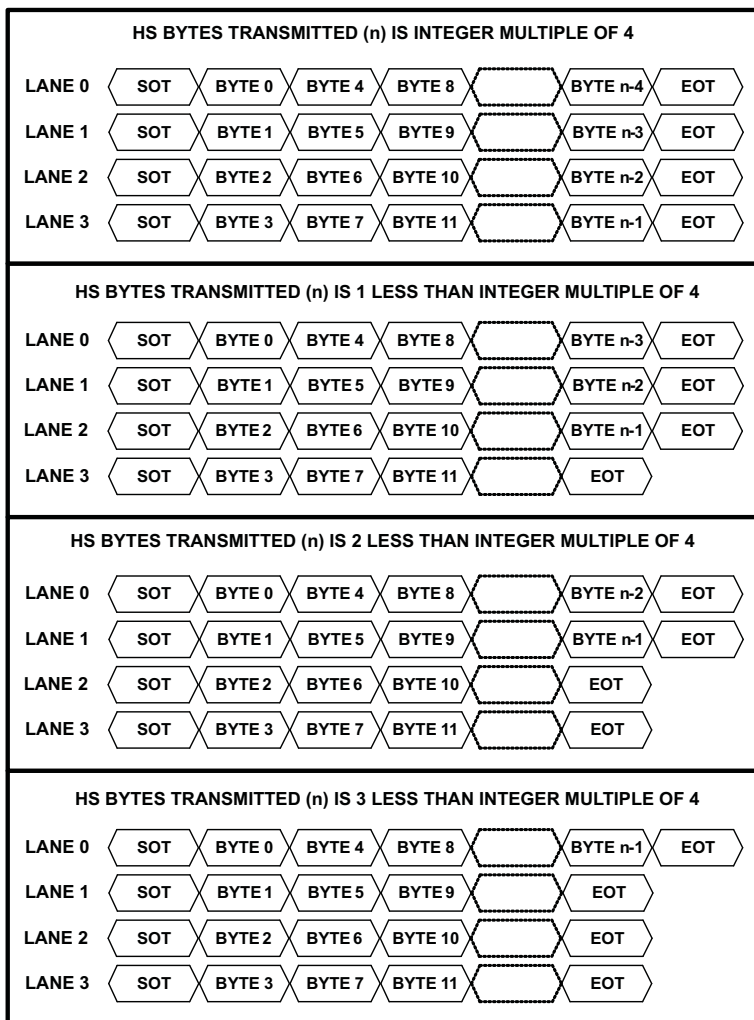


Figure 14. 4 MIPI Data Lane Configuration

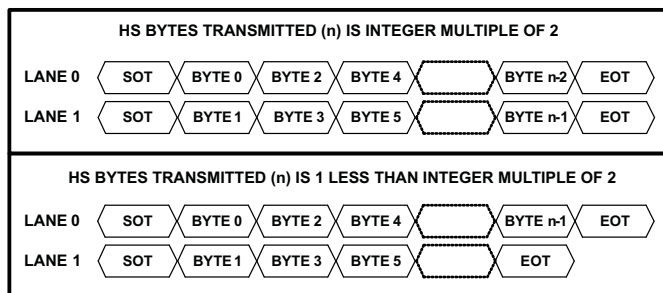
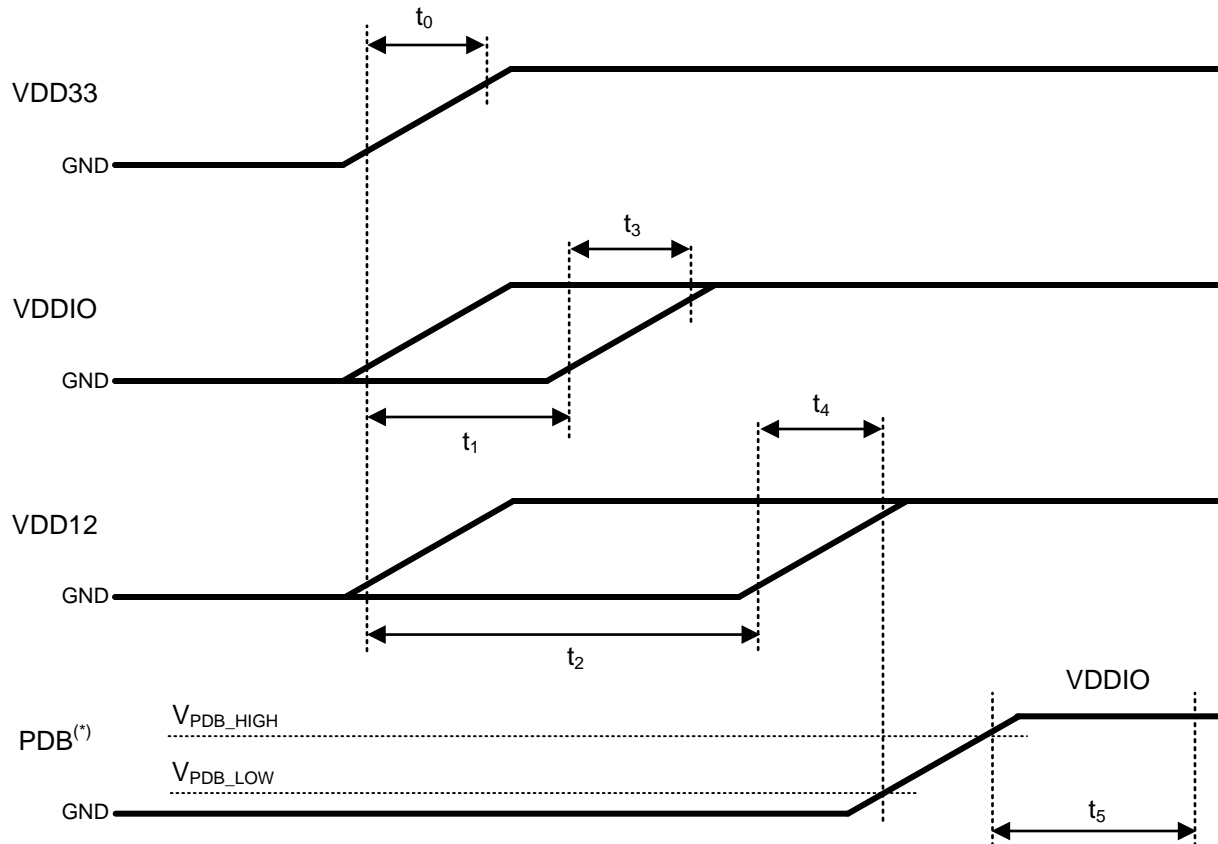


Figure 15. 2 MIPI Data Lane Configuration

7.11 Power Sequence



(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

Figure 16. Power Sequence

Table 1. Power-Up Sequencing Constraints

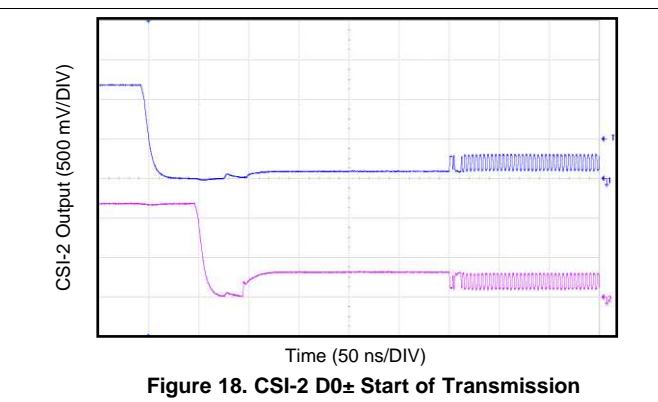
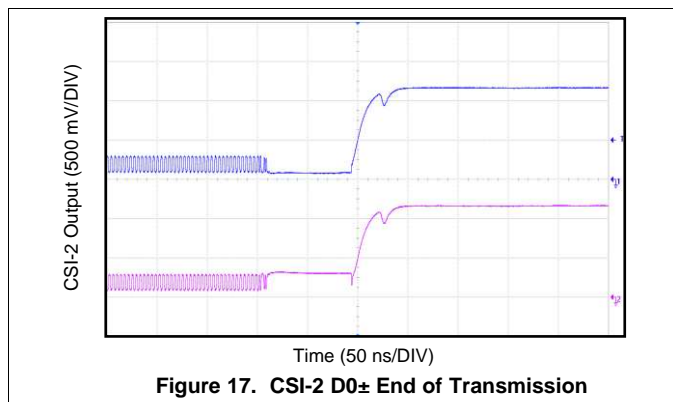
| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|-----------------|---------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|--------------|-----|--------------|-------|
| VDDIO | VDDIO voltage range | | 3.0 | | 3.6 | V |
| | | | 1.71 | | 1.89 | V |
| VDD33 | VDD33 voltage range | | 3.0 | | 3.6 | V |
| VDD12 | VDD12 voltage range | | 1.14 | | 1.26 | V |
| V_{PDB_LOW} | PDB LOW threshold Note: V_{PDB} should not exceed limit for respective I/O voltage before 90% voltage of VDD12 | VDDIO = 3.3V ± 10% | 0.8 | | | V |
| | | VDDIO = 1.8V ± 5% | 0.35 * VDDIO | | | |
| V_{PDB_HIGH} | PDB HIGH threshold | VDDIO = 3.3V ± 10% | | | 2.0 | V |
| | | VDDIO = 1.8V ± 5% | | | 0.65 * VDDIO | |
| t_0 | VDD33 rise time | These time constants are specified for rise time of power supply voltage ramp (10% - 90%) | | | <1.5 | ms |
| t_3 | VDDIO rise time | These time constants are specified for rise time of power supply voltage ramp (10% - 90%) | | | <1.5 | ms |

Power Sequence (continued)

Table 1. Power-Up Sequencing Constraints (continued)

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|----------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|-------|
| t ₄ | VDD12 rise time | These time constants are specified for rise time of power supply voltage ramp (10% - 90%) | | | <1.5 | ms |
| t ₁ | VDDIO delay time | V _{IL} of rising edge (VDDIO) to V _{IL} of rising edge (VDD_N) The power supplies may be ramped simultaneously. If sequenced, VDD33 should be first, either by itself or with VDDIO (1.8V or 3.3V) or VDD12, with the other rail(s) following in any order. | >0 | | | ms |
| t ₂ | VDD12 delay time | | | | | |
| t ₅ | Startup time | The part is powered up after the startup time has elapsed from the moment PDB goes HIGH. Local I2C is available to read/write 948/940 registers after this time. | | | <1 | ms |

7.12 Typical Characteristics



8 Detailed Description

8.1 Overview

The DS90UH940-Q1 receives a 35-bit symbol over single or dual serial FPD-Link III pairs operating at up to 3.36 Gbps line rate in 1-lane FPD-Link III mode and 2.975 Gbps per lane in 2-lane FPD-Link III mode. The DS90UH940-Q1 converts this stream into a CSI-2 MIPI Interface (4 data channels + 1 clock, or 8 data channels + 2 clocks in replicate mode). The FPD-Link III serial stream contains an embedded clock, video control signals, audio, GPIOs, I2C, and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

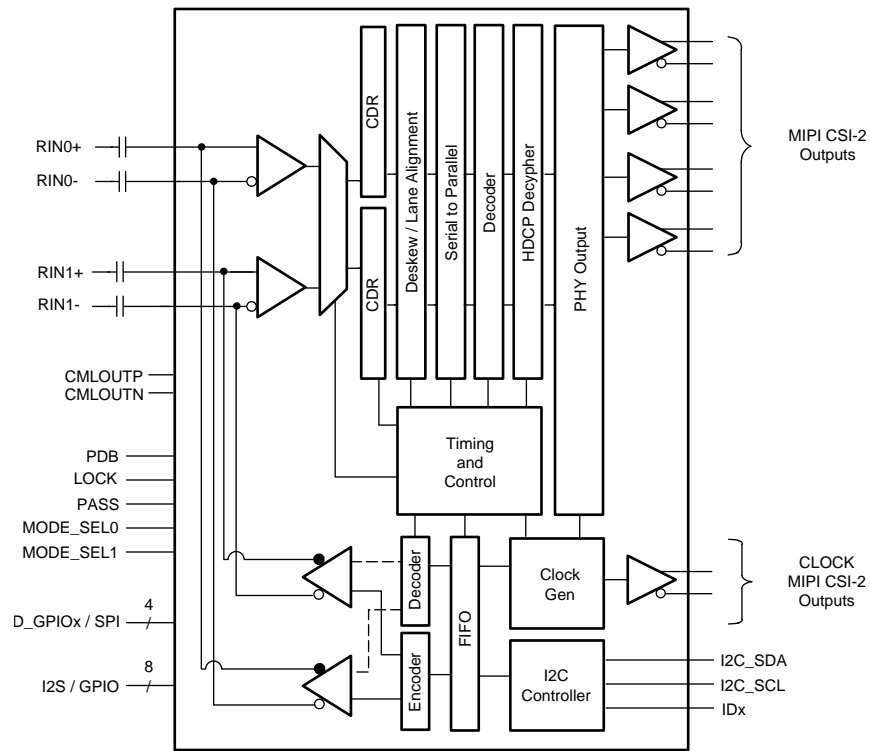
The DS90UH940-Q1 is intended for use with the DS90UH949-Q1 or DS90UH947-Q1 Serializers, but is also backward compatible to the DS90UH925Q-Q1, DS90UH925AQ-Q1, and DS90UH927Q-Q1 FPD-Link III Serializers.

The DS90UH940-Q1 deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream. It also applies decryption through a High-Bandwidth Digital Content Protection (HDCP) Cipher to this video and audio data stream following reception of the data from the FPD-Link III decoder. On-chip non-volatile memory stores the HDCP keys. All key exchange is done through the FPD-Link III bidirectional control interface. The decrypted MIPI CSI-2 interface is provided to the processor.

The DS90UH940-Q1 deserializer incorporates an I2C compatible interface. The I2C compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C compatible masters at either side of the serial link.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 High Speed Forward Channel Data Transfer

The High Speed Forward Channel is composed of 35 bits of data containing RGB data, sync signals, HDCP, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. Figure 19 illustrates the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.



Figure 19. FPD-Link III Serial Stream

The DS90UH940-Q1 supports clocks in the range of 25 MHz to 96 MHz over a 1-lane, or 50MHz to 170MHz over 2-lanes. The FPD-Link III serial stream rate is 3.36 Gbps maximum (875 Mbps minimum) or 2.975 Gbps maximum per lane (875 Mbps minimum) respectively.

8.3.2 Low Speed Back Channel Data Transfer

The Low-Speed Backward Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel contains the I2C, HDCP, CRC and 4 bits of standard GPIO information with 5 or 20 Mbps line rate (configured by MODE_SEL1).

8.3.3 FPD-Link III Port Register Access

Since the DS90UH940-Q1 contains two ports, some registers need to be duplicated to allow control and monitoring of the two ports. To facilitate this, PORT1_SEL and PORT0_SEL bits (0x34[1:0]) register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) will be available independent of the settings in the PORT_SEL register.

Feature Description (continued)

Setting the PORT1_SEL and PORT0_SEL bit will allow a read of the register for the selected port. If both bits are set, port1 registers will be returned. Writes will occur to ports for which the select bit is set, allowing simultaneous writes to both ports if both select bits are set.

8.3.4 Clock and Output Status

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is tri-state or LOW (depending on the value of the OUTPUT ENABLE setting). After the deserializer completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the LVCMOS and LVDS outputs. The State of the outputs is based on the OUTPUT ENABLE and OUTPUT SLEEP STATE SELECT register settings. See register 0x02 in [Table 12](#).

Table 2. Output State Table

| Inputs | | | | Outputs | | | |
|--------------|-----|-------------------------------|----------------------------------------------|---------|-----------------|------------------------------|--------------|
| Serial Input | PDB | OUTPUT ENABLE Reg 0x02 [7] | OUTPUT SLEEP STATE SELECT Reg 0x02 [4] | LOCK | PASS | Data GPIO / D_GPIO I2S | CSI-2 Output |
| X | L | X | X | Z | Z | Z | Z |
| X | H | L | L | L or H | L | L | HS0 |
| X | H | L | H | L or H | Z | Z | Z |
| Static | H | H | L | L | L | L | HS0 |
| Static | H | H | H | L | Previous Status | L | HS0 |
| Active | H | H | L | L | L | L | HS0 |
| Active | H | H | H | H | Valid | Valid | Valid |

8.3.5 LVCMOS VDDIO Option

The 1.8V or 3.3V Inputs and Outputs are powered from a separate VDDIO supply to offer compatibility with external system interface signals.

NOTE

When configuring the VDDIO power supplies, all the single-ended data and control input pins for device need to scale together with the same operating VDDIO levels.

8.3.6 Power Down (PDB)

The deserializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the VDDIO, where VDDIO = 3.0 V to 3.6 V or VDD33. To save power, disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after VDD33 and VDDIO have reached final levels; no external components are required. In the case of driven by the VDDIO = 3.0 V to 3.6 V or VDD33 directly, a 10kΩ resistor to the VDDIO = 3.0 V to 3.6 V or VDD33, and a >10 μF capacitor to the GND are required (see [Figure 37](#) Typical Connection Diagram).

8.3.7 Interrupt Pin — Functional Description and Usage (INTB_IN)

The INTB_IN pin is an active low interrupt input pin. This interrupt signal, when configured, will propagate to the paired serializer. Consult the appropriate Serializer datasheet for details of how to configure this interrupt functionality.

1. On the Serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN (pin 4) is set LOW by some downstream device.
3. Serializer pulls INTB pin LOW. The signal is active LOW, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read HDCP_ISR register.
5. A read to HDCP_ISR will clear the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTB_IN. This would be when the downstream device

releases the INTB_IN (pin 4) on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

8.3.8 General-purpose I/O

8.3.8.1 GPIO[3:0] and D_GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general purpose I/Os in either forward channel (outputs) or back channel (inputs) mode. GPIO and D_GPIO modes may be configured from the registers (Table 11). The same registers configure either GPIO or D_GPIO, depending on the status of PORT1_SEL and PORT0_SEL bits (0x34[1:0]). D_GPIO operation requires 2-lane FPD-Link III mode. Consult the appropriate Serializer datasheet for details on D_GPIO configuration. Note: if paired with a DS90UH925Q-Q1 serializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the serializer. To enable 18-bit mode, set serializer register 0x12[2] = 1. 18-bit mode will be auto-loaded into the deserializer from the serializer. See Table 3 for GPIO enable and configuration.

Table 3. GPIO Enable and Configuration

| Description | Device | Forward Channel | Back Channel |
|-----------------|--------------|-----------------|-----------------|
| GPIO3 / D_GPIO3 | Serializer | 0x0F[3:0] = 0x3 | 0x0F[3:0] = 0x5 |
| | Deserializer | 0x1F[3:0] = 0x5 | 0x1F[3:0] = 0x3 |
| GPIO2 / D_GPIO2 | Serializer | 0x0E[7:4] = 0x3 | 0x0E[7:4] = 0x5 |
| | Deserializer | 0x1E[7:4] = 0x5 | 0x1E[7:4] = 0x3 |
| GPIO1 / D_GPIO1 | Serializer | 0x0E[3:0] = 0x3 | 0x0E[3:0] = 0x5 |
| | Deserializer | 0x1E[3:0] = 0x5 | 0x1E[3:0] = 0x3 |
| GPIO0 / D_GPIO0 | Serializer | 0x0D[3:0] = 0x3 | 0x0D[3:0] = 0x5 |
| | Deserializer | 0x1D[3:0] = 0x5 | 0x1D[3:0] = 0x3 |

The input value present on GPIO[3:0] or D_GPIO[3:0] may also be read from register, or configured to local output mode (Table 11).

8.3.8.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. The mode is controlled by register 0x43 (Table 11). The back channel frequency can be controlled several ways:

- Register 0x23[6] sets the divider that controls the back channel frequency based on the internal oscillator. 0x23[6] = 0 sets the divider to 4 and 0x23[6] = 1 sets the divider to 2. As long as BC_HS_CTL (0x23[4]) is set to 0, the back channel frequency would be either 5 Mbps or 10Mbps based on this bit.
- Register 0x23[4] enables the high-speed back channel. This can also be pin-strapped via MODE_SEL1 (See Table 4). This bit overrides 0x23[6], and sets the divider for the back channel frequency to 1. Setting this bit to 1 sets the back channel frequency to 20 Mbps.

The back channel frequency has variation of $\pm 20\%$. Note: The back channel frequency must be set to 5 Mbps when paired with a DS90UH925Q-Q1, DS90UH925AQ-Q1, or DS90UH927Q-Q1. See Table 4 for details about configuring the D_GPIOs in various modes.

Table 4. Back Channel D_GPIO Effective Frequency

| HSCC_MODE (0x43[2:0]) | Mode | Number of D_GPIOs | Samples per Frame | D_GPIO Effective Frequency ⁽¹⁾ (kHz) | | | D_GPIOs Allowed |
|--------------------------|--------|----------------------|----------------------|-------------------------------------------------|---------------------------|---------------------------|--------------------|
| | | | | 5 Mbps BC ⁽²⁾ | 10 Mbps BC ⁽³⁾ | 20 Mbps BC ⁽⁴⁾ | |
| 000 | Normal | 4 | 1 | 33 | 66 | 133 | D_GPIO[3:0] |
| 011 | Fast | 4 | 6 | 200 | 400 | 800 | D_GPIO[3:0] |
| 010 | Fast | 2 | 10 | 333 | 666 | 1333 | D_GPIO[1:0] |
| 001 | Fast | 1 | 15 | 500 | 1000 | 2000 | D_GPIO0 |

(1) The effective frequency assumes the worst case back channel frequency (-20%) and a 4X sampling rate.

(2) 5 Mbps corresponds to BC_FREQ_SELECT = 0 & BC_HS_CTL = 0

(3) 10 Mbps corresponds to BC_FREQ_SELECT = 1 & BC_HS_CTL = 0

(4) 20 Mbps corresponds to BC_FREQ_SELECT = X & BC_HS_CTL = 1

8.3.8.3 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode. See [Table 5](#) for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Low-Speed Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 5. GPIO_REG and GPIO Local Enable and Configuration

| Description | Register Configuration | Function |
|-------------|------------------------|----------------------|
| GPIO_REG8 | 0x21[7:4] = 0x1 | Output, L |
| | 0x21[7:4] = 0x9 | Output, H |
| | 0x21[7:4] = 0x3 | Input, Read: 0x6F[0] |
| GPIO_REG7 | 0x21[3:0] = 0x1 | Output, L |
| | 0x21[3:0] = 0x9 | Output, H |
| | 0x21[3:0] = 0x3 | Input, Read: 0x6E[7] |
| GPIO_REG6 | 0x20[7:4] = 0x1 | Output, L |
| | 0x20[7:4] = 0x9 | Output, H |
| | 0x20[7:4] = 0x3 | Input, Read: 0x6E[6] |
| GPIO_REG5 | 0x20[3:0] = 0x1 | Output, L |
| | 0x20[3:0] = 0x9 | Output, H |
| | 0x20[3:0] = 0x3 | Input, Read: 0x6E[5] |
| GPIO3 | 0x1F[3:0] = 0x1 | Output, L |
| | 0x1F[3:0] = 0x9 | Output, H |
| | 0x1F[3:0] = 0x3 | Input, Read: 0x6E[3] |
| GPIO2 | 0x1E[7:4] = 0x1 | Output, L |
| | 0x1E[7:4] = 0x9 | Output, H |
| | 0x1E[7:4] = 0x3 | Input, Read: 0x6E[2] |
| GPIO1 | 0x1E[3:0] = 0x1 | Output, L |
| | 0x1E[3:0] = 0x9 | Output, H |
| | 0x1E[3:0] = 0x3 | Input, Read: 0x6E[1] |
| GPIO0 | 0x1D[3:0] = 0x1 | Output, L |
| | 0x1D[3:0] = 0x9 | Output, H |
| | 0x1D[3:0] = 0x3 | Input, Read: 0x6E[0] |

8.3.9 SPI Communication

The SPI Control Channel utilizes the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available, Forward Channel and Reverse Channel modes. In Forward Channel mode, the SPI Master is located at the Serializer, such that the direction of sending SPI data is in the same direction as the video data. In Reverse Channel mode, the SPI Master is located at the Deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI Control Channel can operate in a high speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the slave to the master on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies where the MISO pin can be ignored by the master.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

Note: SPI cannot be used to access Serializer / Deserializer registers.

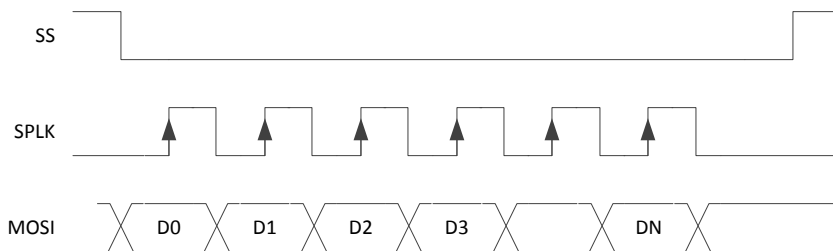
8.3.9.1 SPI Mode Configuration

SPI is configured over I2C using the High-Speed Control Channel Configuration (HSCC_CONTROL) register, 0x43 (Table 12). HSCC_MODE (0x43[2:0]) must be configured for either High-Speed, Forward Channel SPI mode (110) or High-Speed, Reverse Channel SPI mode (111).

8.3.9.2 Forward Channel SPI Operation

In Forward Channel SPI operation, the SPI master located at the Serializer generates the SPI Clock (SPLK), Master Out / Slave In data (MOSI), and active low Slave Select (SS). The Serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, MOSI, and SS are each sent on data bits in the forward channel frame. At the Deserializer, the SPI signals are regenerated using the pixel clock. In order to preserve setup and hold time, the Deserializer will hold MOSI data while the SPLK signal is high. In addition, it delays SPLK by one pixel clock relative to the MOSI data, increasing setup by one pixel clock.

SERIALIZER



DESERIALIZER

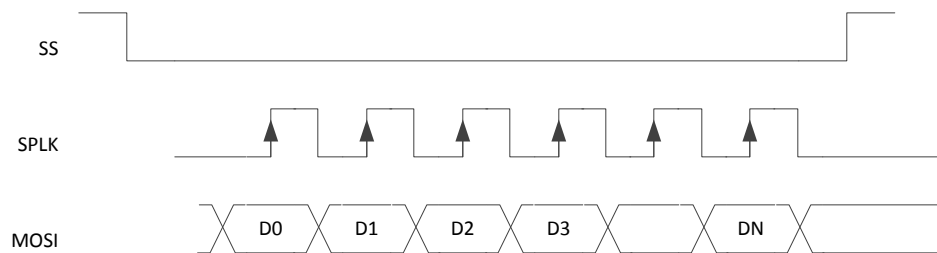


Figure 20. Forward Channel SPI Write

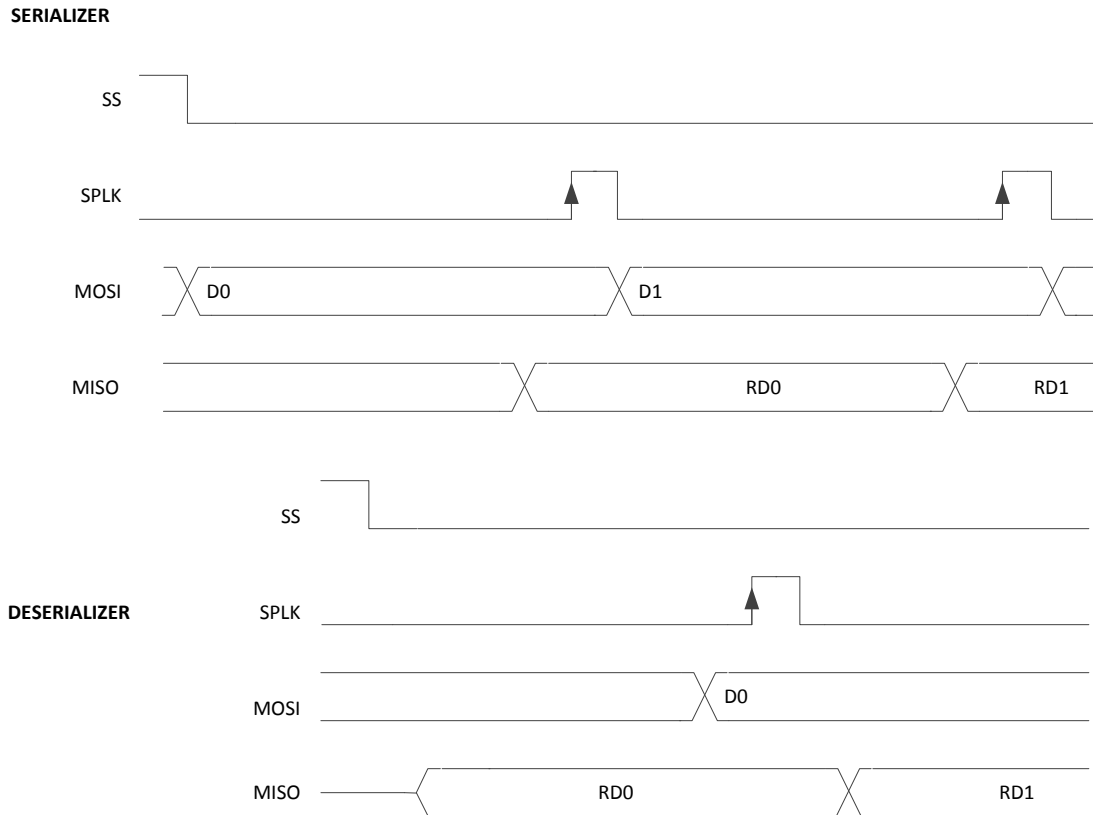


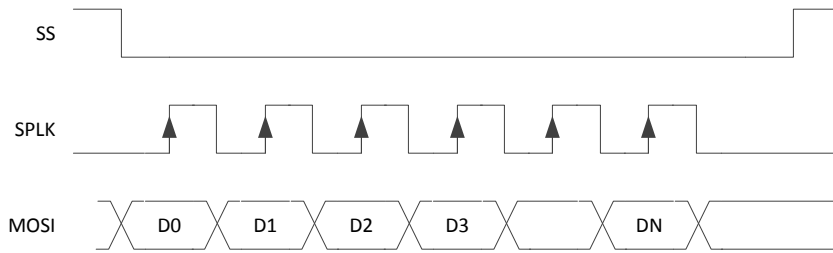
Figure 21. Forward Channel SPI Read

8.3.9.3 Reverse Channel SPI Operation

In Reverse Channel SPI operation, the Deserializer samples the Slave Select (SS), SPI clock (SCLK) into the internal oscillator clock domain. In addition, upon detection of the active SPI clock edge, the Deserializer samples the SPI data (MOSI). The SPI data samples are stored in a buffer to be passed to the Serializer over the back channel. The Deserializer sends SPI information in a back channel frame to the Serializer. In each back channel frame, the Deserializer sends an indication of the Slave Select value. The Slave Select should be inactive (high) for at least one back-channel frame period to ensure propagation to the Serializer.

Because data is delivered in separate back channel frames and buffered, the data may be regenerated in bursts. The following figure (Figure 22) shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the SS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

DESERIALIZER



SERIALIZER

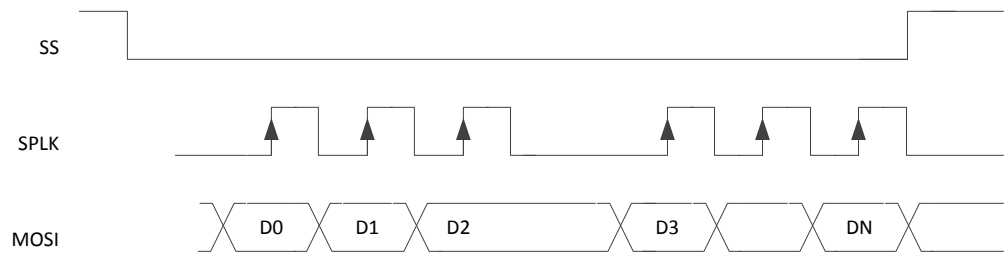
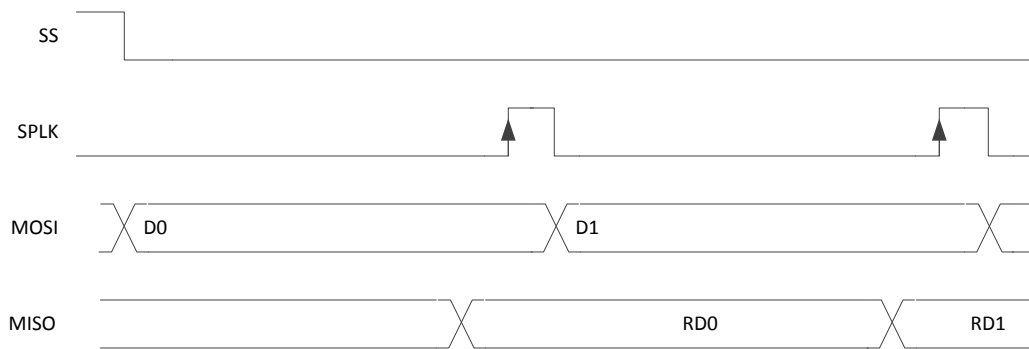


Figure 22. Reverse Channel SPI Write

For Reverse Channel SPI reads, the SPI master must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in Forward channel mode. Note that at most one data/clock sample will be sent per back channel frame.

DESERIALIZER



SERIALIZER

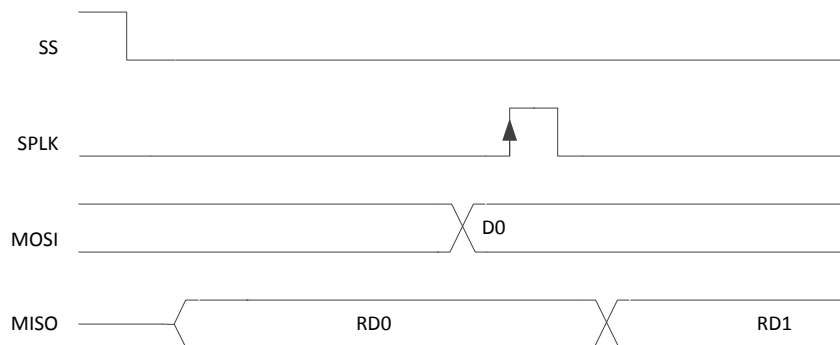


Figure 23. Reverse Channel SPI Read

For both Reverse Channel SPI writes and reads, the SPI_SS signal should be deasserted for at least one back channel frame period.

Table 6. SPI SS Deassertion Requirement

| Back Channel Frequency | Deassertion Requirement |
|------------------------|-------------------------|
| 5 Mbps | 7.5 μ s |
| 10 Mbps | 3.75 μ s |
| 20 Mbps | 1.875 μ s |

8.3.10 Backward Compatibility

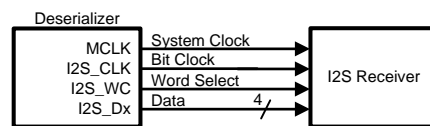
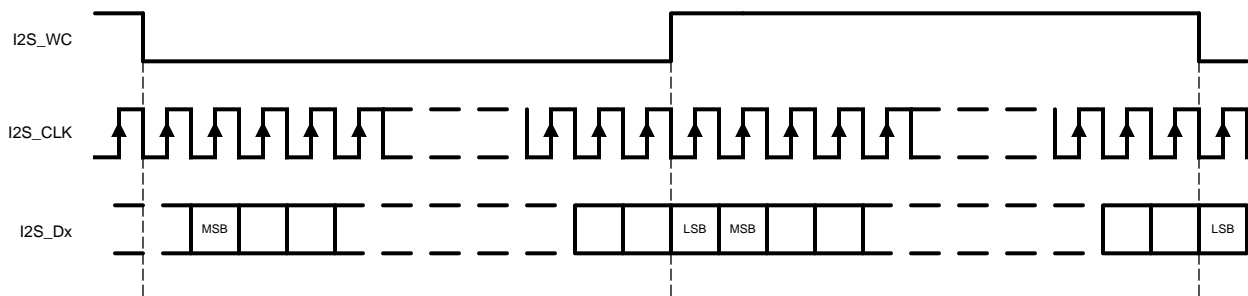
The DS90UH940-Q1 is also backward compatible to the DS90UH925Q-Q1, DS90UH925AQ-Q1, and DS90UH927Q-Q1 for PCLK frequencies ranging from 25MHz to 85MHz. Backward compatibility does not need to be enabled. When paired with a backward compatible device, the Deserializer will auto-detect to 1-lane FPD-Link III on the primary channel (RIN0 \pm).

8.3.11 Input Equalization

An FPD-Link III input adaptive equalizer provides compensation for transmission medium losses and reduces medium-induced deterministic jitter. It equalizes up to 15m STP or 50 Ω Coaxial cables with 3 connection breaks at maximum serializer stream payload of 3.36 Gbps.

8.3.12 I2S Audio Interface

This Deserializer features six I2S output pins that, when paired with a compatible serializer, supports surround sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1MHz and the smaller of <PCLK/2 or <13MHz. Four I2S data outputs carry two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input.


Figure 24. I2S Connection Diagram

Figure 25. I2S Frame Timing Diagram

When paired with a DS90UH925Q, the Deserializer I2S interface supports a single I2S data output through I2S_DA (24-bit video mode), or two I2S data outputs through I2S_DA and I2S_DB (18-bit video mode).

8.3.12.1 I2S Transport Modes

By default, packetized audio is received during video blanking periods in dedicated Data Island Transport frames. The transport mode is set in the serializer and auto-loaded into the deserializer by default. The audio configuration may be disabled from control registers if Forward Channel Frame Transport of I2S data is desired. In frame transport, only I2S_DA is received to the Deserializer. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[D:A]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UH927Q, DS90UH949-Q1, DS90UH947-Q1, or DS90UH929-Q1 serializer. If connected to a DS90UH925Q serializer, only I2S_DA and I2S_DB may be received.

8.3.12.2 I2S Jitter Cleaning

This device features a standalone PLL to clean the I2S data jitter, supporting high-end car audio systems. If I2S_CLK frequency is less than 1MHz, this feature must be disabled through register 0x2B[7]. See [Table 12](#).

8.3.12.3 MCLK

The deserializer has an I2S Master Clock Output (MCLK). It supports x1, x2, or x4 of I2S CLK Frequency. When the I2S PLL is disabled, the MCLK output is off. [Table 7](#) covers the range of I2S sample rates and MCLK frequencies. By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bits 0x3A[6:4] (I2S_DIVSEL), shown in [Table 12](#). To select desired MCLK frequency, write 0x3A[7], then write to bit [6:4] accordingly.

Table 7. Audio Interface Frequencies

| Sample Rate (kHz) | I2S Data Word Size (bits) | I2S_CLK (MHz) | MCLK Output (MHz) | Register 0x3A[6:4] |
|-------------------|---------------------------|---------------|-------------------|--------------------|
| 32 | 16 | 1.024 | I2S_CLK x1 | 000 |
| | | | I2S_CLK x2 | 001 |
| | | | I2S_CLK x4 | 010 |
| 44.1 | | 1.4112 | I2S_CLK x1 | 000 |
| | | | I2S_CLK x2 | 001 |
| | | | I2S_CLK x4 | 010 |
| 48 | | 1.536 | I2S_CLK x1 | 000 |
| | | | I2S_CLK x2 | 001 |
| | | | I2S_CLK x4 | 010 |
| 96 | | 3.072 | I2S_CLK x1 | 001 |
| | | | I2S_CLK x2 | 010 |
| | | | I2S_CLK x4 | 011 |
| 192 | 6.144 | I2S_CLK x1 | 010 | |
| | | I2S_CLK x2 | 011 | |
| | | I2S_CLK x4 | 100 | |

Table 7. Audio Interface Frequencies (continued)

| Sample Rate (kHz) | I2S Data Word Size (bits) | I2S_CLK (MHz) | MCLK Output (MHz) | Register 0x3A[6:4] |
|-------------------|---------------------------|---------------|-------------------|--------------------|
| 32 | 24 | 1.536 | I2S_CLK x1 | 000 |
| | | | I2S_CLK x2 | 001 |
| | | | I2S_CLK x4 | 010 |
| 44.1 | | 2.117 | I2S_CLK x1 | 001 |
| | | | I2S_CLK x2 | 010 |
| | | | I2S_CLK x4 | 011 |
| 48 | | 2.304 | I2S_CLK x1 | 001 |
| | | | I2S_CLK x2 | 010 |
| | | | I2S_CLK x4 | 011 |
| 96 | | 4.608 | I2S_CLK x1 | 010 |
| | | | I2S_CLK x2 | 011 |
| | | | I2S_CLK x4 | 100 |
| 192 | 9.216 | I2S_CLK x1 | 011 | |
| | | I2S_CLK x2 | 100 | |
| | | I2S_CLK x4 | 101 | |
| 32 | 32 | 2.048 | I2S_CLK x1 | 001 |
| | | | I2S_CLK x2 | 010 |
| | | | I2S_CLK x4 | 011 |
| 44.1 | | 2.8224 | I2S_CLK x1 | 001 |
| | | | I2S_CLK x2 | 010 |
| | | | I2S_CLK x4 | 011 |
| 48 | | 3.072 | I2S_CLK x1 | 001 |
| | | | I2S_CLK x2 | 010 |
| | | | I2S_CLK x4 | 011 |
| 96 | | 6.144 | I2S_CLK x1 | 010 |
| | | | I2S_CLK x2 | 011 |
| | | | I2S_CLK x4 | 100 |
| 192 | 12.288 | I2S_CLK x1 | 011 | |
| | | I2S_CLK x2 | 100 | |
| | | I2S_CLK x4 | 110 | |

8.3.13 HDCP

The HDCP Cipher function is implemented in the deserializer per HDCP v1.4 specification. The DS90UH940-Q1 provides HDCP decryption of audiovisual content when connected to an HDCP capable FPD-Link III serializer. HDCP authentication and shared key generation is performed using the HDCP Control Channel, which is embedded in the forward and backward channels of the serial link. On-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

8.3.13.1 HDCP I2S Audio Encryption

Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. When HDCP is active, packetized Data Island Transport audio is also encrypted along with the video data per HDCP v1.4. I2S audio transmitted in Forward Channel Frame Transport mode is not encrypted. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

8.3.14 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

8.3.14.1 BIST Configuration And Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33 MHz internal Oscillator clock (OSC) frequency in the Serializer. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK status is valid throughout the entire duration of BIST.

See [Figure 26](#) for the BIST mode flow diagram.

8.3.14.1.1 Sample BIST Sequence

Note: Before BIST can be enabled, D_GPIO0 (pin 19) must be strapped HIGH and D_GPIO[3:1] (pins 16, 17, and 18) must be strapped LOW.

1. BIST Mode is enabled via the BISTEN pin of Deserializer. The desired clock source is selected through the deserializer BISTC pin.
2. The serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires LOCK, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate per 35 bits.
3. To Stop BIST mode, set the BISTEN pin LOW. The deserializer stops checking the data, and the final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. [Figure 27](#) shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

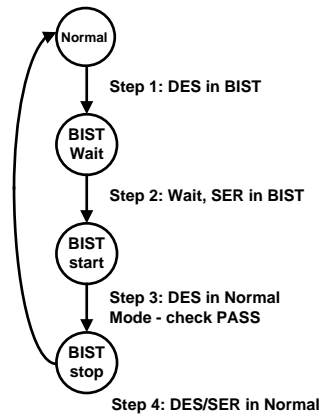


Figure 26. BIST Mode Flow Diagram

8.3.14.2 Forward Channel and Back Channel Error Checking

The Deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer. Forward channel errors may also be read from register 0x25 (Table 12).

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 12). CRC errors are recorded in an 8-bit register in the serializer. The register is cleared when the serializer enters the BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of the last BIST run until cleared or the serializer enters BIST mode again.

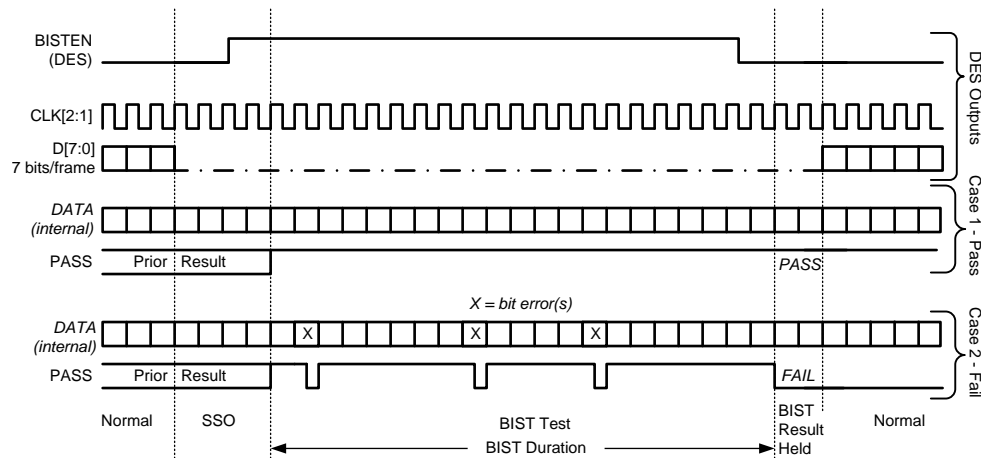


Figure 27. BIST Waveforms

8.3.15 Internal Pattern Generation

The deserializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note AN-2198 (SNLA132).

8.4 Device Functional Modes

8.4.1 Configuration Select

The DS90UH940-Q1 can be configured for several different operating modes via the MODE_SEL[1:0] input pins, or via the register bits 0x23 [4:3] (MODE_SEL1) and 0x6A [5:4] (MODE_SEL0). A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] input and VDD33 to select one of the possible selected modes.

The DS90UH940-Q1 is capable of operating in either in 1-lane or 2-lane modes for FPD-Link III. By default, the FPD-Link III receiver automatically configures the input based on 1- or 2-lane mode operation. Programming register 0x34 [4:3] settings will override the automatic detection. For each FPD-Link III pair, the serial datastream is composed of a 35-bit symbol.

The DS90UH940-Q1 recovers the FPD-Link III serial datastream(s) and produces CSI-2 TX data driven to the MIPI DPHY interface. There are two CSI-2 ports (CSI0_Dn and CSI1_Dn) and each consist of one clock lane and four data lanes. The DS90UH940-Q1 supports two CSI-2 TX ports, and each may be configured to support either two or four CSI-2 data lanes. Unused CSI-2 outputs are driven to LP11 states. The MIPI DPHY transmission operates in both differential (HS) and single-ended (LP) modes. During HS transmission, the pair of outputs operates in differential mode; and in LP mode, the pair operates as two independent single-ended traces. Both the data and clock lanes enter LP mode during the horizontal and vertical blanking periods.

The configurations outlined in ([1-lane FPD-Link III Input, 4 MIPI lanes Output](#), [1-lane FPD-Link III Input, 2 MIPI lanes Output](#), [1- or 2-lane FPD-Link III Input, 2 or 4 MIPI lanes Output in Replicate](#)) will apply to DS90UH949-Q1, DS90UH947-Q1, DS90UH929-Q1, DS90UH925Q-Q1, DS90UH925AQ-Q1, and DS90UH927Q-Q1 FPD-Link III Serializers.

The configurations outlined in ([2-lane FPD-Link III Input, 4 MIPI lanes Output](#), [2-lane FPD-Link III Input, 2 MIPI lanes Output](#), [1- or 2-lane FPD-Link III Input, 2 or 4 MIPI lanes Output in Replicate](#)) will apply to DS90UH949-Q1 and DS90UH947-Q1 FPD-Link III Serializers.

The device can be configured in following modes:

- 1-lane FPD-Link III Input, 4 MIPI lanes Output
- 1-lane FPD-Link III Input, 2 MIPI lanes Output
- 2-lane FPD-Link III Input, 4 MIPI lanes Output
- 2-lane FPD-Link III Input, 4 MIPI lanes Output
- 1- or 2-lane FPD-Link III Input, 2 or 4 MIPI lanes Output (Replicate)

8.4.1.1 1-lane FPD-Link III Input, 4 MIPI lanes Output

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 25 MHz to 96 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 3.36 Gbps (35 bit * 96 MHz). Each MIPI data lane will operate at a speed of 7 * PCLK frequency; resulting in a data rate of 175 Mbps to 672 Mbps. The corresponding MIPI transmit clock rate will operate between 87.5 MHz to 336 MHz.

8.4.1.2 1-lane FPD-Link III Input, 2 MIPI lanes Output

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 25 MHz to 96 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 3.36 Gbps (35 bit * 96 MHz). Each MIPI data lane will operate at a speed of 14 * PCLK frequency; resulting in a data rate of 350 Mbps to 1344 Mbps. The corresponding MIPI transmit clock rate will operate between 175 MHz to 672 MHz.

8.4.1.3 2-lane FPD-Link III Input, 4 MIPI lanes Output

In this configuration the PCLK rate embedded is split into 2-lane FPD-Link III frame and can range from 50 MHz to 170 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 2.975 Gbps (35 bit * 85 MHz). The embedded datastreams from the received FPD-Link III inputs are merged in HS mode to form packets that carry the video stream. Each MIPI data lane will operate at a speed of 7 * PCLK frequency, resulting in a data rate of 350 Mbps to 1190 Mbps. The corresponding MIPI transmit clock rate will operate between 175 MHz to 595 MHz.

Device Functional Modes (continued)

8.4.1.4 2-lane FPD-Link III Input, 2 MIPI lanes Output

In this configuration the PCLK rate embedded is split into 2-lane FPD-Link III frame and can range from 25 MHz to 48 MHz, resulting in a link rate of 875 Mbps (35 bit * 25 MHz) to 1.680 Gbps (35 bit * 48 MHz). The embedded datastreams from the received FPD-Link III inputs are merged in HS mode to form packets that carry the video stream. Each MIPI data lane will operate at a speed of 14 * PCLK frequency, resulting in a data rate of 700 Mbps to 1344 Mbps. The corresponding MIPI transmit clock rate will operate between 350 MHz to 672 MHz.

8.4.1.5 1- or 2-lane FPD-Link III Input, 2 or 4 MIPI lanes Output in Replicate

Same as 1- or 2-lane FPD-Link III Input(s), duplicates the MIPI CSI-2 lanes on CSI1_D[3:0] and CSI1_CLK outputs.

8.4.2 MODE_SEL[1:0]

Configuration of the device may be done via the MODE_SEL[1:0] input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs (V_{R4}) and VDD33 to select one of the other 8 possible selected modes. See [Table 8](#) and [Table 9](#). Possible configurations are shown in [Figure 28](#).

Device Functional Modes (continued)

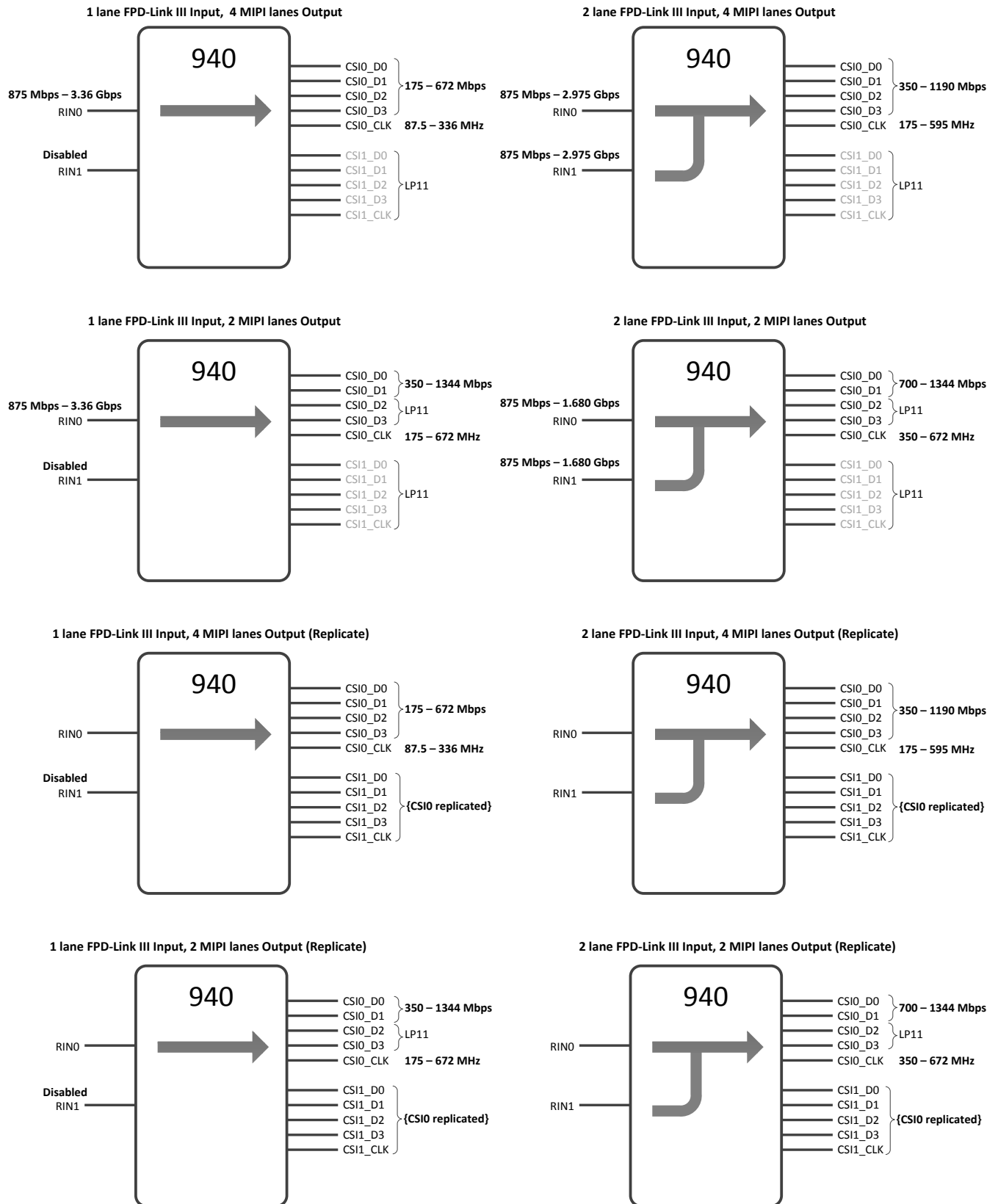


Figure 28. Datapath Configurations

Device Functional Modes (continued)

Configuration of the device may be done via the MODE_SEL[1:0] input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs (V_{R1}) and VDD33 to select one of the other 8 possible selected modes. See [Table 8](#) and [Table 9](#).

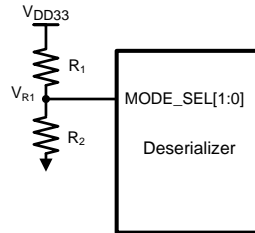


Figure 29. MODE_SEL[1:0] Connection Diagram

Table 8. Configuration Select (MODE_SEL0)

| # | Ideal Ratio V_{R1}/V_{DD33} | Target V_{R1} (V) | Suggested Resistor R1 k Ω (1% tol) | Suggested Resistor R2 k Ω (1% tol) | Output Mode |
|---|-------------------------------|---------------------|-------------------------------------------|-------------------------------------------|----------------------------------------------------------------------------------|
| 1 | 0 | 0 | Open | 40.2 or Any | 4 data lanes 1 CSI port active (determined by MODE_SEL1 CSI_SEL bit) |
| 2 | 0.169 | 0.559 | 232 | 47.5 | 4 data lanes both CSI ports active (overrides MODE_SEL1) |
| 3 | 0.230 | 0.757 | 107 | 31.6 | 2 data lanes 1 CSI port active (determined by MODE_SEL1 CSI_SEL bit) |
| 4 | 0.295 | 0.974 | 113 | 47.5 | 2 data lanes both CSI ports active (overrides MODE_SEL1) |
| 5 | 0.376 | 1.241 | 113 | 68.1 | RESERVED |
| 6 | 0.466 | 1.538 | 107 | 93.1 | RESERVED |
| 7 | 0.556 | 1.835 | 90.9 | 113 | RESERVED |
| 8 | 0.801 | 2.642 | 45.3 | 182 | RESERVED |

Table 9. Configuration Select (MODE_SEL1)

| # | Ideal Ratio V_{R1}/V_{DD33} | Target V_{R1} (V) | Suggested Resistor R1 k Ω (1% tol) | Suggested Resistor R2 k Ω (1% tol) | CSI_SEL (CSI PORT) | High Speed Back Channel | Input Mode |
|---|-------------------------------|---------------------|-------------------------------------------|-------------------------------------------|--------------------|-------------------------|------------|
| 1 | 0 | 0 | Open | 40.2 or Any | CSI0 | 5 Mbps | STP |
| 2 | 0.169 | 0.559 | 232 | 47.5 | CSI0 | 5 Mbps | Coax |
| 3 | 0.230 | 0.757 | 107 | 31.6 | CSI0 | 20 Mbps | STP |
| 4 | 0.295 | 0.974 | 113 | 47.5 | CSI0 | 20 Mbps | Coax |
| 5 | 0.376 | 1.241 | 113 | 68.1 | CSI1 | 5 Mbps | STP |
| 6 | 0.466 | 1.538 | 107 | 93.1 | CSI1 | 5 Mbps | Coax |
| 7 | 0.556 | 1.835 | 90.9 | 113 | CSI1 | 20 Mbps | STP |
| 8 | 0.801 | 2.642 | 45.3 | 182 | CSI1 | 20 Mbps | Coax |

8.4.3 CSI-2 Interface

The DS90UH940-Q1 (in default mode) takes RGB 24-bpp data bits defined in the serializer and directly maps to the pixel color space in the data frame. The DS90UH940-Q1 follows the general frame format as described per the CSI-2 standard (Figure 30). Upon the end of the vertical sync pulse (VS), the DS90UH940-Q1 generates the Frame End and Frame Start synchronization packets within the vertical blanking period. The timing of the Frame Start will not reflect the timing of the VS signal.

Upon the rising edge of the DE signal, each active line is output in a long data packet with the defined data format (Figure 13). At the end of each packet, the data lanes $Dn\pm$ return to the LP-11 state, while the clock lane $CLK\pm$ continue outputting the high speed clock.

The DS90UH940-Q1 CSI-2 transmitter consists of a high speed clock ($CLK\pm$) and data ($Dn\pm$) outputs based on a source synchronous interface. The half rate clock at $CLK\pm$ is derived from the pixel clock sourced by the clock/data recovery circuit of the DS90UH940-Q1. The CSI-2 clock frequency is 3.5 times (4 MIPI lanes) or 7 times (2 MIPI lanes) the recovered pixel clock frequency. The MIPI DPHY outputs either 2 or 4 high speed data lanes ($Dn\pm$) according to the CSI-2 protocol. The data rate of each lane is 7 times (4 MIPI lanes) or 14 times (2 MIPI lanes) the pixel clock. As an example in a 4 MIPI lane configuration, at a pixel clock of 150 MHz, the $CLK\pm$ runs at 525 MHz, and each data lane runs at 1050 Mbps.

The half-rate clock maintains a quadrature phase relationship to the data signals and allows receiver to sample data at the rising and falling edges of the clock (DDR). Figure 10 shows the timing relationship of the clock and data lines. The DS90UH940-Q1 supports continuous high speed clock. High speed data are sent out at data lanes $Dn\pm$ in bursts. In between data bursts, the data lanes return to Low Power (LP) States in according to protocol defined in D-PHY standard. The rising edge of the differential clock ($CSI_CLK+ - CSI_CLK-$) is sent during the first payload bit of a transmission burst in the data lanes.

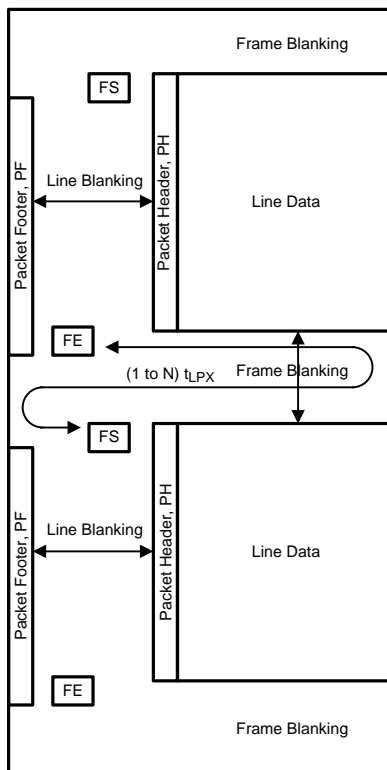


Figure 30. CSI-2 General Frame Format

8.4.4 Input Display Timing

The DS90UH940-Q1 has built-in support to detect the incoming video format extracted from the FPD-Link III datastream(s) and automatically generate CSI-2 output timing parameters accordingly. The input video format detection is derived from progressive display resolutions based on the CEA-861D specification. The video data rate and frame rate is determined by measuring internal VS and DE signals.

8.4.5 MIPI CSI-2 Output Data Formats

The DS90UH940-Q1 CSI-2 Tx supports multiple data types. These can be seen in [Table 10](#).

Table 10. CSI-2 Output Data Formats⁽¹⁾

| Data Format | CSI-2 Data Type [5:0] | Reg0x6B [3:2] IFMT | Reg0x6B [7:4] OFMT | Description |
|---------------------|-----------------------|--------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------|
| RGB888 | 0x24 | 00 | 0000 | RGB888 image data – using 24-bit container for RGB 24-bpp |
| RGB666 | 0x23 | 00 | 0001 | RGB666 image data |
| RGB565 | 0x22 | 00 | 0010 | RGB565 image data |
| YUV420 | 0x1A | 00 | 0011 | YUV4:2:0 image data, Legacy YUV420 8-bit |
| YUV420 8-bit | 0x18 | 00 | 0100 | YUV4:2:0 image data |
| YUV422 8-bit | 0x1E | 00 | 0101 | YUV4:2:2 image data |
| RAW8 | 0x2A | 11 | 0110 | RAW Bayer, 8-bit image data D[0:7] of Serializer inputs are used as RAW data; Alignment is configured with CSIIA_{0x6C}_0x09 [4] |
| RAW10 | 0x2B | 11 | 0111 | RAW Bayer, 10-bit image data D[0:9] of Serializer inputs are used as RAW data; Alignment is configured with CSIIA_{0x6C}_0x09 [4] |
| RAW12 | 0x2C | 11 | 1000 | RAW Bayer, 12-bit image data D[0:11] of Serializer inputs are used as RAW data; Alignment is configured with CSIIA_{0x6C}_0x09 [4] |
| YUV420 8-bit (CSPS) | 0x1C | 00 | 1001 | YUV4:2:0 image data, YUV420 Chroma Shifted Pixel Sampling |

(1) Note: Color space conversion is only available from RGB to YUV.

8.4.6 Non-Continuous / Continuous Clock

DS90UH940-Q1 D-PHY supports Continuous clock mode and Non-Continuous clock mode on the CSI-2 interface. Default mode is Non-Continuous Clock mode, where the Clock Lane enters in LP mode between the transmissions of data packets. Non-continuous clock mode will only be non-continuous during the vertical blanking period for lower PCLK rates. For higher PCLK rates, the clock will be non-continuous between line and frame packets. Operating modes are configurable through 0x6A [1].

Clock lane enters LP11 during horizontal blanking if the horizontal blanking period is longer than the overhead time to start/stop the clock lane. There is auto-detection of the length of the horizontal blank period. The fixed threshold is 96 PCLK cycles.

8.4.7 Ultra Low Power State (ULPS)

The DS90UH940-Q1 supports the MIPI defined Ultra-Low Power State (ULPS). DS90UH940-Q1 D-PHY lanes will enter ULPS mode upon software standby mode through 0x6A [2] generated by the processor. When ULPS is issued, all active CSI-2 lanes including the clock and data lanes of the enabled CSI-2 port are put in ULPS according to the MIPI DPHY protocol. D-PHY can reduce power consumption by entering ULPS mode. Ultra Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

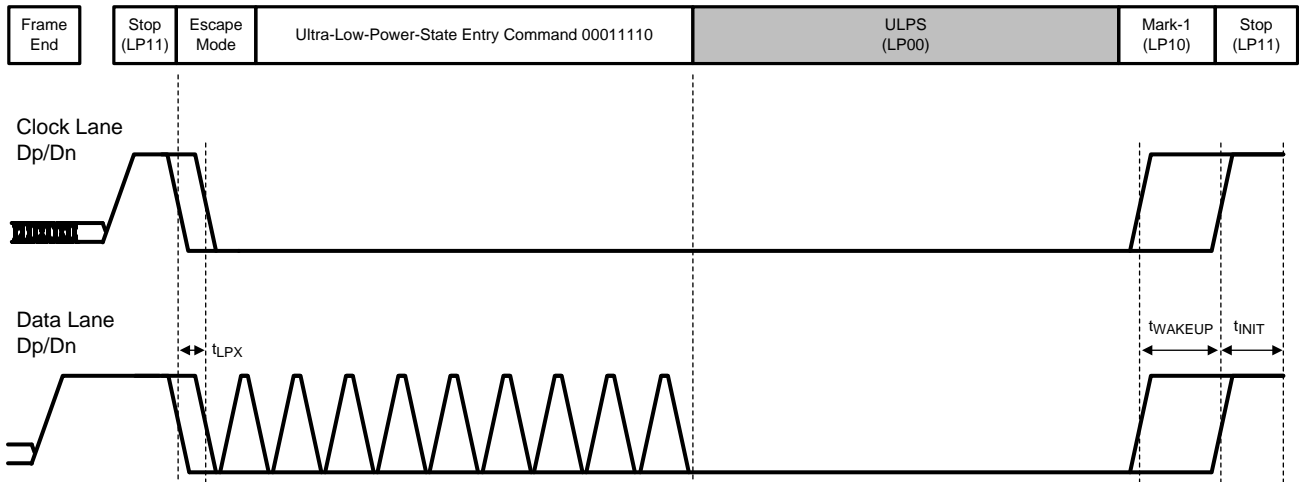


Figure 31. Ultra Low Power State

8.4.8 CSI-2 Data Identifier

The DS90UH940-Q1 MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in Figure 32. The virtual channel ID is contained in the 2 MSBs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSBs of the data identifier byte.

- CSIIA_{0x6C}_0x2E[7:6] CSI_VC_ID: Configures the virtual ID linked to the current context.
- CSICFG1_0x6B[7:4] OFMT: Configures the data format linked to the current context.

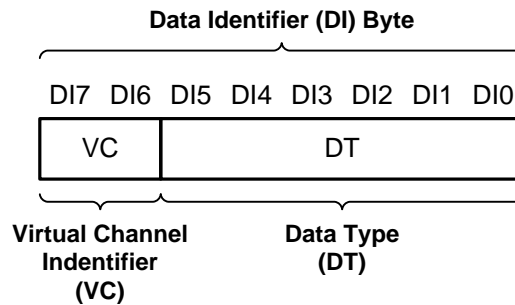


Figure 32. CSI-2 Data Identifier Structure

8.5 Programming

8.5.1 Serial Control Bus

The device may also be configured by the use of a I2C compatible serial control bus. Multiple devices may share the serial control bus (up to 8 device addresses supported). The device address is set via a resistor divider (R1 and R2 — see Figure 33 below) connected to the IDx pin.

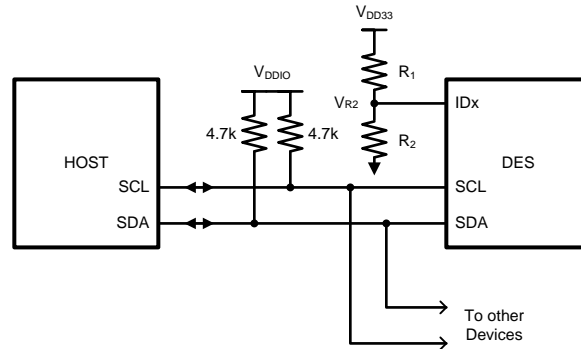


Figure 33. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to 1.8 V or 3.3 V VDDIO. For most applications, a 4.7kΩ pull-up resistor to VDD33 is recommended. However, the pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 8 possible device addresses. A pull-up resistor and a pull-down resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{R2}) and VDD33, each ratio corresponding to a specific device address. See Table 11 below.

Table 11. Serial Control Bus Addresses for IDx

| # | Ideal Ratio V_{R2} / V_{DD33} | Ideal V_{R2} (V) | Suggested Resistor R1 kΩ (1% tol) | Suggested Resistor R2 kΩ (1% tol) | 7-bit Address | 8-bit Address |
|---|---------------------------------|--------------------|-----------------------------------|-----------------------------------|---------------|---------------|
| 1 | 0 | 0 | Open | 40.2 or >10 | 0x2C | 0x58 |
| 2 | 0.169 | 0.559 | 232 | 47.5 | 0x2E | 0x5C |
| 3 | 0.230 | 0.757 | 107 | 31.6 | 0x30 | 0x60 |
| 4 | 0.295 | 0.974 | 113 | 47.5 | 0x32 | 0x64 |
| 5 | 0.376 | 1.241 | 113 | 68.1 | 0x34 | 0x68 |
| 6 | 0.466 | 1.538 | 107 | 93.1 | 0x36 | 0x6C |
| 7 | 0.556 | 1.835 | 90.9 | 113 | 0x38 | 0x70 |
| 8 | 0.801 | 2.642 | 45.3 | 182 | 0x3C | 0x78 |

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 34

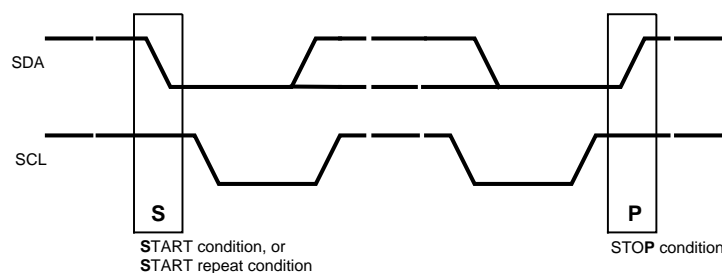


Figure 34. START and STOP Conditions

8.5.5 Multi-Master Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices (in backward compatible), simultaneous access to serializer or deserializer registers from both local and remote I2C masters may cause incorrect operation, thus restrictions should be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in an errored read or write.

Two basic options are recommended. The first is to allow device register access only from one controller. In a Display mode system, this would allow only the Host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer (local to the Display) would not be allowed to access the deserializer or serializer registers.

The second basic option is to allow local register access only with no access to remote serializer or deserializer registers. The Host controller would be allowed to access the serializer registers while a controller at the deserializer could access those register only. Access to remote I2C slaves would still be allowed in one direction (Camera or Display mode).

In a very limited case, remote and local access could be allowed to the deserializer registers at the same time. Register access is ensured to work correctly if both local and remote masters are accessing the same deserializer register. This allows a simple method of passing control of the Bidirectional Control Channel from one master to another.

8.5.6 Restrictions on Control Channel Direction for Multi-Master Operation

Only Display or Camera mode operation should be active at any time across the Bidirectional Control Channel. If both directions are required, some method of transferring control between I2C masters should be implemented.

8.6 Register Maps

Table 12. Serial Control Bus Registers

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|-------------------------|--------|-----------------------------------------|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x00 | I2C Device ID | 7:1 | DEVICE ID | RW | Strap | 7-bit address of Deserializer; Defaults to the address configured by the IDx strap pin. See Table 11 . |
| | | 0 | DES ID | RW | 0 | 0: Device ID is from IDx strap 1: Register I2C Device ID overrides IDx strap |
| 0x01 | Reset | 7:3 | RESERVED | RW | 0 | Reserved |
| | | 2 | RESERVED | R | 1 | Reserved |
| | | 1 | DIGITAL RESET0 | RW | 0 | Digital Reset. Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation. Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table. |
| | | 0 | DIGITAL RESET1 | RW | 0 | Digital Reset. Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation |
| 0x02 | General Configuration 0 | 7 | OUTPUT ENABLE | RW | 1 | Output Enable Override Value (in conjunction with Output Sleep State Select) If the Override control is not set, the Output Enable will be set to 1. A Digital reset 0x01[0] should be asserted after toggling Output Enable bit <i>LOW</i> to <i>HIGH</i> |
| | | 6 | OUTPUT ENABLE OVERRIDE | RW | 0 | Overrides Output Enable and Output Sleep State default 0: Disable override 1: Enable override |
| | | 5 | OSC CLOCK OUTPUT ENABLE (AUTO_CLOCK_EN) | RW | 0 | OSC clock output enable If loss of lock OSC clock is output onto PCLK. The frequency is selected in register 0x24. 1: Enable 0: Disable |
| | | 4 | OUTPUT SLEEP STATE SELECT | RW | 0 | OSS Select Override value to control output state when LOCK is low (used in conjunction with Output Enable) If the Override control is not set, the Output Sleep State Select will be set to 1. |
| | | 3:0 | RESERVED | RW | 0 | Reserved |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|-------------------------|--------|----------------------------|------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x03 | General Configuration 1 | 7 | RESERVED | RW | 1 | Reserved |
| | | 6 | BC CRC GENERATOR ENABLE | RW | 1 | Back Channel CRC Generator Enable 0: Enable 1: Disable (Default) |
| | | 5 | FAILSAFE LOW | RW | 1 | Controls the pull direction for undriven LVCMOS inputs 1: Pull down 0: Pull up |
| | | 4 | FILTER ENABLE | RW | 1 | HS,VS,DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected. 1: Filtering enable 0: Filtering disable |
| | | 3 | I2C PASS-THROUGH | RW | 0 | I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled |
| | | 2 | AUTO ACK | RW | 0 | Automatically Acknowledge I2C writes independent of the forward channel lock state 1: Enable 0: Disable |
| | | 1 | DE GATE RGB | RW | 0 | Gate RGB data with DE signal. RGB data is gated with DE in order to allow packetized audio and block unencrypted data when paired with a serializer that supports HDCP. When paired with a serializer that does not support HDCP, RGB data is not gated with DE by default. However, to enable packetized audio this bit must be set. 1: Gate RGB data with DE (has no effect when paired with a serializer that supports HDCP) 0: Pass RGB data independent of DE (has no effect when paired with a serializer that does not support HDCP) |
| | | 0 | RESERVED | RW | 0 | Reserved |
| 0x04 | BCC Watchdog Control | 7:1 | BCC WATCHDOG TIMER | RW | 0x7F | The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0. |
| | | 0 | BCC WATCHDOG TIMER DISABLE | RW | 0 | Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation |
| 0x05 | I2C Control 1 | 7 | I2C PASS THROUGH ALL | RW | 0 | I2C Pass-Through All Transactions 0: Disabled 1: Enabled |
| | | 6:4 | I2C SDA HOLD | RW | 0x1 | Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds. |
| | | 3:0 | I2C FILTER DEPTH | RW | 0xE | I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|------------------------------------|------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x06 | I2C Control 2 | 7 | FORWARD CHANNEL SEQUENCE ERROR | R | 0 | Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. If this bit is set, an error may have occurred in the control channel operation. |
| | | 6 | CLEAR SEQUENCE ERROR | RW | 0 | Clears the Sequence Error Detect bit |
| | | 5 | RESERVED | R | 0 | Reserved. |
| | | 4:3 | SDA Output Delay | RW | 0 | SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00 : 250ns 01: 300ns 10: 350ns 11: 400ns |
| | | 2 | LOCAL WRITE DISABLE | RW | 0 | Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer. |
| | | 1 | I2C BUS TIMER SPEEDUP | RW | 0 | Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second. |
| 0x07 | REMOTE ID | 7:1 | REMOTE ID (Loaded from remote SER) | RW | 0x00 | 7-bit Serializer Device ID Configures the I2C Slave ID of the remote Serializer. A value of 0 in this field disables I2C access to the remote Serializer. This field is automatically loaded from the Serializer once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel. |
| | | 0 | FREEZE DEVICE ID | RW | 0 | Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written. |
| 0x08 | SlaveID[0] | 7:1 | SLAVE ID0 | RW | 0 | 7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x09 | SlaveID[1] | 7:01 | SLAVE ID1 | RW | 0 | 7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|-----------------|------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0A | SlaveID[2] | 7:1 | SLAVE ID2 | RW | 0 | 7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x0B | SlaveID[3] | 7:1 | SLAVE ID3 | RW | 0 | 7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x0C | SlaveID[4] | 7:1 | SLAVE ID4 | RW | 0 | 7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x0D | SlaveID[5] | 7:1 | SLAVE ID5 | RW | 0 | 7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x0E | SlaveID[6] | 7:1 | SLAVE ID6 | RW | 0 | 7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x0F | SlaveID[7] | 7:1 | SLAVE ID7 | RW | 0 | 7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer. |
| | | 0 | RESERVED | RW | 0 | Reserved. |
| 0x10 | SlaveAlias[0] | 7:1 | SLAVE ALIAS ID0 | RW | 0 | 7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |
| 0x11 | SlaveAlias[1] | 7:1 | SLAVE ALIAS ID1 | RW | 0 | 7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|-----------------|------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x12 | SlaveAlias[2] | 7:1 | SLAVE ALIAS ID2 | RW | 0 | 7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |
| 0x13 | SlaveAlias[3] | 7:1 | SLAVE ALIAS ID3 | RW | 0 | 7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |
| 0x14 | SlaveAlias[4] | 7:1 | SLAVE ALIAS ID4 | RW | 0 | 7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |
| 0x15 | SlaveAlias[5] | 7:1 | SLAVE ALIAS ID5 | RW | 0 | 7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved |
| 0x16 | SlaveAlias[6] | 7:1 | SLAVE ALIAS ID6 | RW | 0 | 7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |
| 0x17 | SlaveAlias[7] | 7:1 | SLAVE ALIAS ID7 | RW | 0 | 7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave. |
| | | 0 | RESERVED | | 0 | Reserved. |
| 0x18 | MAILBOX_18 | 7:0 | MAILBOX_18 | RW | 0 | Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link. |
| 0x19 | MAILBOX_19 | 7:0 | MAILBOX_19 | RW | 0x01 | Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|--------------------------------|--------|--------------------------|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1A | GPIO[9] and Global GPIO Config | 7 | GLOBAL GPIO OUTPUT VALUE | RW | 0 | Global GPIO Output Value This value is output on each GPIO pin when the individual pin is not otherwise enabled as a GPIO and the global GPIO direction is Output |
| | | 6 | RESERVED | RW | 0 | Reserved |
| | | 5 | GLOBAL GPIO FORCE DIR | RW | 0 | The GLOBAL GPIO DIR and GLOBAL GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. The GLOBAL bits are overridden by the individual GPIO DIR and GPIO EN bits. {GLOBAL GPIO DIR, GLOBAL GPIO EN} 00: Functional mode; output 10: Tri-state 01: Force mode; output 11: Force mode; input |
| | | 4 | GLOBAL GPIO FORCE EN | RW | 0 | |
| | | 3 | GPIO9 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 2 | RESERVED | RW | 0 | Reserved |
| | | 1 | GPIO9 DIR | RW | 0 | The GPIO DIR and GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 0 | GPIO9 EN | RW | 0 | |
| 0x1B | Frequency Counter | 7:0 | Frequency Count | RW | 0 | Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 50ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency. |
| 0x1C | General Status | 7:5 | RESERVED | R | 0 | Reserved. |
| | | 4 | DUAL_RX_STS | R | 0 | Receiver Dual Link Status: This bit indicates the current operating mode of the FPD-Link III Receive port 1: 2-lane mode active 0: 1-lane mode active |
| | | 3 | I2S LOCKED | R | 0 | I2S LOCK STATUS 0: I2S PLL controller not locked 1: I2S PLL controller locked to input I2S clock |
| | | 2 | RESERVED | R | 0 | Reserved. |
| | | 1 | RESERVED | R | 0/1 | Reserved. |
| | | 0 | LOCK | R | 0 | De-Serializer CDR, PLL's clock to recovered clock frequency 1: De-Serializer locked to recovered clock 0: De-Serializer not locked In Dual Link mode, this indicates both channels are locked. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|----------------|--------|----------------------------------------------|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1D | GPIO0 Config | | | | | GPIO0 and D_GPIO0 Configuration If PORT1_SEL is set, this register controls the D_GPIO0 pin |
| | | 7:4 | Rev-ID | R | | Revision ID |
| | | 3 | GPIO0 OUTPUT VALUE D_GPIO0 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 2 | GPIO0 REMOTE ENABLE D_GPIO0 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 1 | GPIO0 DIR D_GPIO0 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 0 | GPIO0 EN D_GPIO0 EN | RW | 0 | |
| 0x1E | GPIO1_2 Config | | | | | GPIO1/GPIO2 and D_GPIO1/D_GPIO2 Configuration If PORT1_SEL is set, this register controls the D_GPIO1 and D_GPIO2 pins |
| | | 7 | GPIO2 OUTPUT VALUE D_GPIO2 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 6 | GPIO2 REMOTE ENABLE D_GPIO2 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 5 | GPIO2 DIR D_GPIO2 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 4 | GPIO2 EN D_GPIO2 EN | RW | 0 | |
| | | 3 | GPIO1 OUTPUT VALUE D_GPIO1 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 2 | GPIO1 REMOTE ENABLE D_GPIO1 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 1 | GPIO1 DIR D_GPIO1 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 0 | GPIO1 EN D_GPIO1 EN | RW | 0 | |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|----------------|--------|----------------------------------------------|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1F | GPIO3 Config | | | | | GPIO3 and D_GPIO3 Configuration If PORT1_SEL is set, this register controls the D_GPIO3 pin |
| | | 7:4 | RESERVED | RW | 0 | Reserved (No GPIO 4) |
| | | 3 | GPIO3 OUTPUT VALUE D_GPIO3 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 2 | GPIO3 REMOTE ENABLE D_GPIO3 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 1 | GPIO3 DIR D_GPIO3 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 0 | GPIO3 EN D_GPIO3 EN | RW | 0 | |
| 0x20 | GPIO5_6 Config | 7 | GPIO6 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 6 | GPIO6 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 5 | GPIO6 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 4 | GPIO6 EN | RW | 0 | |
| | | 3 | GPIO5 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 2 | GPIO5 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 1 | GPIO5 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 0 | GPIO5 EN | RW | 0 | |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|----------------|--------|---------------------|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x21 | GPIO7_8 Config | 7 | GPIO8 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 6 | GPIO8 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 5 | GPIO8 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 4 | GPIO8 EN | RW | 0 | |
| | | 3 | GPIO7 OUTPUT VALUE | RW | 0 | Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. |
| | | 2 | GPIO7 REMOTE ENABLE | RW | 0 | Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer. |
| | | 1 | GPIO7 DIR | RW | 0 | The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input |
| | | 0 | GPIO7 EN | RW | 0 | |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|------------------|--------|--------------------------------------------------------|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x22 | Datapath Control | 7 | OVERRIDE FC CONFIG | RW | 0 | 1: Disable loading of this register from the forward channel, keeping locally written values intact 0: Allow forward channel loading of this register |
| | | 6 | PASS RGB (Loaded from remote SER) | RW | 0 | Setting this bit causes RGB data to be sent independent of DE. This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that this bit prevents HDCP operation and blocks packetized audio. This bit has no effect when paired with a serializer that does not support HDCP. 1: Pass RGB independent of DE 0: Normal operation Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |
| | | 5 | DE POLARITY (Loaded from remote SER) | RW | 0 | This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low) Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |
| | | 4 | I2S_RPTR_REG EN (Loaded from remote SER) | RW | 0 | Regenerate I2S Data from Repeater I2S pins. 1: Don't output packetized audio data on RGB video output pins 0: Output packetized audio on RGB video output pins (Default). Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |
| | | 3 | I2S 4-CHANNEL ENABLE OVERRIDE (Loaded from remote SER) | RW | 0 | 1: Set I2S 4-Channel Enable from bit of this register 0: Set I2S 4-Channel disabled Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |
| | | 2 | 18-BIT VIDEO SELECT (Loaded from remote SER) | RW | 0 | 1: Select 18-bit video mode 0: Select 24-bit video mode Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |
| | | 1 | I2S TRANSPORT SELECT (Loaded from remote SER) | RW | 0 | 1: Enable I2S In-Band Transport 0: Enable I2S Data Island Transport Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |
| | | 0 | I2S 4-CHANNEL ENABLE (Loaded from remote SER) | RW | 0 | I2S 4-Channel Enable 1: Enable I2S 4-Channel 0: Disable I2S 4-Channel Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|----------------|--------|-----------------|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x23 | RX Mode Status | 7 | RX RGB CHECKSUM | RW | 0 | RX RGB Checksum Enable Setting this bit enables the Receiver to validate a one-byte checksum following each video line. Checksum failures are reported in the HDCP_STS register. |
| | | 6 | BC_FREQ_SELECT | RW | 0 | Back Channel Frequency Select 0: Divide-by-4 frequency based on the internal oscillator 1: Divide-by-2 frequency based on the internal oscillator This bit will be ignored if BC_HIGH_SPEED is set to a 1. Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer. |
| | | 5 | AUTO_I2S | RW | 1 | Auto I2S Determine I2S mode from the AUX data codes. |
| | | 4 | BC_HS_CTL | RW | Strap | Back-Channel High-Speed control Enables high-speed back-channel at 20Mbps. This bit will override the BC_FREQ_SELECT setting. Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer. BC_HIGH_SPEED is loaded from the MODE_SEL1 pin strap options. |
| | | 3 | COAX_MODE | RW | Strap | Coax Mode Configures the FPD3 Receiver for operation over Coax or STP cabling: 0 : Shielded Twisted pair (STP) 1 : Coax Coax Mode is loaded from the MODE_SEL1 pin strap options. |
| | | 2 | REPEATER_MODE | RW | Strap | Repeater Mode Indicates device is strapped to repeater mode. Repeater Mode is loaded from the MODE_SEL1 pin strap options. |
| | | 1 | RESERVED | RW | 0 | Reserved |
| | | 0 | RESERVED | RW | 0 | Reserved |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|------------------|--------|-------------------|------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x24 | BIST Control | 7:6 | BIST_OUT_MODE | RW | 0 | BIST Output Mode 00 : No toggling 01 : Alternating 1/0 toggling 1x : Toggle based on BIST data |
| | | 5:4 | AUTO_OSC_FREQ | RW | 0 | When register 0x02 bit 5 (AUTO)CLOCK_EN is set, this field controls the nominal frequency of the oscillator-based receive clock. 00: 50 MHz 01: 25 MHz 10: 10 MHz 11: Reserved |
| | | 3 | BIST_PIN_CONFIG | RW | 1 | Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register |
| | | 2:1 | BIST_CLOCK_SOURCE | RW | 0 | BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK_SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details. 00: External Pixel Clock 01: Internal Pixel Clock 1x: Internal Pixel Clock |
| | | 0 | BIST_EN | RW | 0 | BIST Control 1: Enabled 0: Disabled |
| 0x25 | BIST ERROR COUNT | 7:0 | BIST ERROR COUNT | R | 0 | Bist Error Count Returns BIST error count for selected port. Port selected is based on the PORT_SEL control in the DUAL_RX_CTL register 0x34 [1:0]. |
| 0x26 | SCL High Time | 7:0 | SCL HIGH TIME | RW | 0x83 | I2C Master SCL High Time This field configures the high pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz. |
| 0x27 | SCL Low Time | 7:0 | SCL LOW TIME | RW | 0x84 | I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|--------------------|--------|-----------------------------------------------|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x28 | Datapath Control 2 | 7 | OVERRIDE FC CONFIG | RW | 0 | 1: Disable loading of this register from the forward channel, keeping locally written values intact 0: Allow forward channel loading of this register |
| | | 6 | RESERVED | RW | 0 | Reserved |
| | | 5 | VIDEO_DISABLED (Loaded from remote SER) | RW | 0 | Forward channel video disabled 0 : Normal operation 1 : Video is disabled, control channel is enabled This is a status bit only, indicating the forward channel is not sending active video. In this mode, the control channel and GPIO functions are enabled. Setting OVERRIDE_FC_CONFIG will prevent this bit from changing. |
| | | 4 | DUAL_LINK (Loaded from remote SER) | R | | 1: Dual Link mode enabled 0: Single Link mode enabled This bit will always be loaded from forward channel and cannot be written locally. To force DUAL_LINK receive mode, use the RX_PORT_SEL register (address 0x34) |
| | | 3 | ALTERNATE I2S ENABLE (Loaded from remote SER) | RW | 0 | 1: Enable alternate I2S output on GPIO1 (word clock) and GPIO0 (data) 0: Normal Operation |
| | | 2 | I2S DISABLED (Loaded from remote SER) | RW | 0 | 1: I2S DISABLED 0: Normal Operation |
| | | 1 | 28BIT VIDEO (Loaded from remote SER) | RW | 0 | 1: 28 bit Video enable. i.e. HS, VS, DE are present in forward channel. 0: Normal Operation |
| | | 0 | I2S SURROUND (Loaded from remote SER) | RW | 0 | 1: I2S Surround enabled 0: I2S Surround disabled |
| 0x2B | I2S Control | 7:4 | RESERVED | RW | 0 | Reserved |
| | | 3 | I2S FIFO OVERRUN STATUS | R | 0 | I2S FIFO Overrun Status |
| | | 2 | I2S FIFO UNDERRUN STATUS | R | 0 | I2S FIFO Underrun Status |
| | | 1 | I2S FIFO ERROR RESET | RW | 0 | I2S Fifo Error Reset 1: Clears FIFO Error |
| | | 0 | I2S DATA FALLING EDGE | RW | 0 | I2S Clock Edge Select 1: I2S Data is strobed on the Rising Clock Edge. 0: I2S Data is strobed on the Falling Clock Edge. |
| 0x2E | PCLK Test Mode | 7 | EXTERNAL PCLK | RW | 0 | Select pixel clock from BISTC input |
| | | 6:0 | RESERVED | RW | 0 | Reserved |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|-----------------------|------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x34 | DUAL_RX_CTL | 7 | RESERVED | R | 0 | Reserved |
| | | 6 | RX_LOCK_MODE | RW | 0 | RX Lock Mode: Determines operating conditions for indication of RX_LOCK and generation of video data. 0 : RX_LOCK asserted only when receiving active video (Forward channel VIDEO_DISABLED bit is 0) 1 : RX_LOCK asserted when device is linked to a Serializer even if active video is not being sent. This allows indication of valid link where Bidirectional Control Channel is enabled, but Deserializer is not receiving Audio/Video data. |
| | | 5 | RAW_2ND_BC | RW | 0 | Enable Raw Secondary Back channel If this bit is set to a 1, the secondary back channel will operate in a raw mode, passing D_GPIO0 from the Deserializer to the Serializer, without any oversampling or filtering. |
| | | 4:3 | FPD3 INPUT MODE | RW | 0 | FPD-Link III Input Mode Determines operating mode of FPD-Link III Receive interface 00: Auto-detect based on received data 01: Forced Mode: 2-lane 10: Forced Mode: 1-lane, primary input 11: Forced Mode: 1-lane, secondary input |
| | | 2 | RESERVED | RW | 0 | Reserved |
| | | 1 | PORT1_SEL | RW | 0 | Selects Port 1 for Register Access from primary I2C Address For writes, port1 registers and shared registers will both be written. For reads, port1 registers and shared registers will be read. This bit must be cleared to read port0 registers. |
| | | 0 | PORT0_SEL | RW | 1 | Selects Port 0 for Register Access from primary I2C Address For writes, port0 registers and shared registers will both be written. For reads, port0 registers and shared registers will both be read. Note that if PORT1_SEL is also set, then port1 registers will be read. |
| 0x35 | AEQ TEST | | | | | AEQ Test register If PORT1_SEL is set, this register sets port1 AEQ controls |
| | | 7 | RESERVED | RW | 0 | Reserved |
| | | 6 | AEQ_RESTART | RW | 0 | Set high to restart AEQ adaptation from initial value. Method is write HIGH then write LOW - not self clearing. Adaption will be restarted on both ports. |
| | | 5 | OVERVERRIDE_AEQ_FLOOR | RW | 0 | Enable operation of SET_AEQ_FLOOR |
| | | 4 | SET_AEQ_FLOOR | RW | 0 | AEQ adaptation starts from a pre-set floor value rather than from zero - recommended for long cable situations |
| | | 3:0 | RESERVED | RW | 0x0 | Reserved |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|----------------|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x37 | MODE_SEL | 7 | MODE_SEL1 DONE | RW | 0 | MODE_SEL1 Done: 0: indicates the MODE_SEL1 decode has not been latched into the MODE_SEL1 status bits. 1: indicates the MODE_SEL1 decode has completed and latched into the MODE_SEL1 status bits. |
| | | 6:4 | MODE_SEL1 | RW | 0 | MODE_SEL1 Decode 3-bit decode from MODE_SEL1 pin, see MODE_SEL1 table first column "#" for mode selection: 000: CSIO / 5 Mbps / STP (#1 on MODE_SEL1) 001: CSIO / 5 Mbps / coax (#2 on MODE_SEL1) 010: CSIO / 20 Mbps / STP (#3 on MODE_SEL1) 011: CSIO / 20 Mbps / coax (#4 on MODE_SEL1) 100: CSI1 / 5 Mbps / STP (#5 on MODE_SEL1) 101: CSI1 / 5 Mbps / coax (#6 on MODE_SEL1) 110: CSI1 / 20 Mbps / STP (#7 on MODE_SEL1) 111: CSI1 / 20 Mbps / coax (#8 on MODE_SEL1) <i>Note: 0x37[6] is the MSB; 0x37[4] is the LSB</i> |
| | | 3 | MODE_SELO DONE | RW | 0 | MODE_SELO Done: 0: indicates the MODE_SELO decode has not been latched into the MODE_SELO status bits. 1: indicates the MODE_SELO decode has completed and latched into the MODE_SELO status bits. |
| | | 2:0 | MODE_SELO | RW | 0 | MODE_SELO Decode 3-bit decode from MODE_SELO pin, see MODE_SELO table first column "#" for mode selection: 000: 4 data lanes, 1 CSI port activeActive CSI port determined by MODE_SEL1 CSI_SEL bit. (#1 on MODE_SELO) 001: 4 data lanes, both CSI ports activeoverrides MODE_SEL1. (#2 on MODE_SELO) 010: 2 data lanes, 1 CSI port activeActive CSI port determined by MODE_SEL1 CSI_SEL bit. (#3 on MODE_SELO) 011: 2 data lanes, both CSI port activeoverrides MODE_SEL1. (#4 on MODE_SELO) 100: RESERVED (#5 on MODE_SELO) 101: RESERVED (#6 on MODE_SELO) 110: RESERVED (#7 on MODE_SELO) 111: RESERVED (#8 on MODE_SELO) <i>Note: 0x37[2] is the MSB; 0x37[0] is the LSB</i> |
| 0x3A | I2S_DIVSEL | 7 | reg_ov_mdiv | RW | 0x0 | 0: No override for MCLK divider 1: Override divider select for MCLK |
| | | 6:4 | reg_mdiv | RW | 0x0 | Divide ratio select for VCO output (32*REF/M) 000: Divide by 32 (=REF/M) 001: Divide by 16 (=2*REF/M) 010: Divide by 8 (=4*REF/M) 011: Divide by 4 (=8*REF/M) 100: Reserved 101: Divide by 2 (=16*REF/M) 110: Reserved 111: Divide by 1 (32*REF/M) |
| | | 3 | RESERVED | R | 0x0 | |
| | | 2 | reg_ov_mselect | RW | 0x0 | 0: Divide ratio of reference clock VCO selected by PLL-SM 1: Override divide ratio of clock to VCO |
| | | 1:0 | reg_mselect | RW | 0x0 | Divide ratio select for VCO input (M) 00: Divide by 1 01: Divide by 2 10: Divide by 4 11: Divide by 8 |
| | | | | | | |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------------|--------|-------------------------|------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x41 | LINK ERROR COUNT | 7:5 | RESERVED | RW | 0 | Reserved |
| | | 4 | LINK ERROR COUNT ENABLE | RW | 0 | Enable serial link data integrity error count 1: Enable error count 0: DISABLE |
| | | 3:0 | LINK ERROR COUNT | RW | 0x3 | Link error count threshold. Counter is pixel clock based. clk0, clk1 and DCA are monitored for link errors, if error count is enabled, deserializer loose lock once error count reaches threshold. If disabled deserializer loose lock with one error. |
| 0x43 | HSCC_CONTROL | 7:5 | RESERVED | RW | 0 | Reserved |
| | | 4 | SPI_MISO_MODE | RW | 0 | SPI MISO pin mode during Reverse SPI mode During Reverse SPI mode, SPI_MISO is typically an output signal. For bused SPI applications, it may be necessary to tri-state the SPI_MISO output if the device is not selected (SPI_SS = 0). 0 : Always enable SPI_MISO output driver 1 : Tri-state SPI_MISO output if SPI_SS is not asserted (low) |
| | | 3 | SPI_CPOL | RW | 0 | SPI Clock Polarity Control 0 : SPI Data driven on Falling clock edge, sampled on Rising clock edge 1 : SPI Data driven on Rising clock edge, sampled on Falling clock edge |
| | | 2:0 | HSCC_MODE | RW | 0 | High-Speed Control Channel Mode Enables high-speed modes for the secondary link back-channel, allowing higher speed signaling of GPIOs or SPI interface: These bits indicates the High Speed Control Channel mode of operation: 000: Normal frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode |
| 0x44 | ADAPTIVE EQ BYPASS | | | | | Adaptive Equalizer Bypass register If PORT1_SEL is set, this register sets port1 AEQ controls |
| | | 7:5 | EQ STAGE 1 SELECT VALUE | RW | 0x3 | EQ select value[5:3] - Used if adaptive EQ is bypassed. |
| | | 4 | RESERVED | RW | 0 | Reserved |
| | | 3:1 | EQ STAGE 2 SELECT VALUE | RW | 0 | EQ select value [2:0] - Used if adaptive EQ is bypassed. |
| | | 0 | ADAPTIVE EQ BYPASS | RW | 0 | 1: Disable adaptive EQ 0: Enable adaptive EQ |
| 0x45 | ADAPTIVE EQ MIN MAX | | | | | Adaptive Equalizer Configuration If PORT1_SEL is set, this register sets port1 AEQ configuration |
| | | 7:4 | RESERVED | RW | 0x08 | Reserved |
| | | 3:0 | ADAPTIVE EQ FLOOR VALUE | RW | | When AEQ floor is enabled by mode-sel pin or register (reg_35[5:4]) the starting setting is given by this register. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|-------------------|--------|----------------------|------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x52 | CML OUTPUT CTL1 | 7 | CML CHANNEL SELECT 1 | RW | 0 | Selects between PORT0 and PORT1 to output onto CMLOUT±. 0: Recovered forward channel data from RIN0± is output on CMLOUT± 1: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This bit must match 0x57[2:1] setting for PORT0 or PORT1. |
| | | 6:0 | RESERVED | RW | 0 | Reserved |
| 0x56 | CML OUTPUT ENABLE | 7:4 | RESERVED | RW | 0 | Reserved |
| | | 3 | CMLOUT ENABLE | RW | 0 | Enable CMLOUT± Loop-through Driver 0: Disabled (Default) 1: Enabled |
| | | 2:0 | RESERVED | RW | 0 | Reserved |
| 0x57 | CML OUTPUT CTL2 | 7:3 | RESERVED | RW | 0 | Reserved |
| | | 2:1 | CML CHANNEL SELECT 2 | RW | 0 | Selects between PORT0 and PORT1 to output onto CMLOUT±. 01: Recovered forward channel data from RIN0± is output on CMLOUT± 10: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This must match 0x52[7] setting for PORT0 or PORT1. |
| | | 0 | RESERVED | RW | 0 | Reserved |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|-----------------|------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x64 | PGCTL | 7:4 | PATGEN_SEL | RW | 1 | Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode: 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/White to Cyan 1000: Horizontally Scaled Black to Green/White to Magenta 1001: Horizontally Scaled Black to Blue/White to Yellow 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertically Scaled Black to Green/White to Magenta 1101: Vertically Scaled Black to Blue/White to Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved See TI App Note AN-2198 |
| | | 3 | PATGEN_UNH | RW | 0 | Enables the UNH-IOL compliance test pattern: 0: Pattern type selected by PATGEN_SEL 1: Compliance test pattern is selected. Value of PATGEN_SEL is ignored. |
| | | 2 | PATGEN_COLOR | RW | 0 | Enable Color Bars Pattern 0: Color Bars disabled (default) 1: Color bars enabled Overrides the selection from bits [7:4] |
| | | 1 | PATGEN_VCOM_REV | RW | 0 | Reverse the order of color bands in VCOM pattern 0: Color sequence from top left is (YCBR) (default) 1: Color sequence from top left is (RBCY) |
| | | 0 | PATGEN_EN | RW | 0 | Pattern Generator Enable: 1: Enable Pattern Generator 0: Disable Pattern Generator |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|-----------------|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x65 | PGCFG | 7:5 | RESERVED | R | 0 | Reserved |
| | | 4 | PATGEN_18B | RW | 0 | 18-bit Mode Select: 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. This bit has no effect in external timing mode (PATGEN_TSEL = 0). |
| | | 3 | PATGEN_EXTCLK | RW | 0 | Select PCLK of Pattern generator 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0). |
| | | 2 | PATGEN_TSEL | RW | 0 | Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. |
| | | 1 | PATGEN_INV | RW | 0 | Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output. |
| | | 0 | PATGEN_ASCRL | RW | 0 | Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern. |
| 0x66 | PGIA | 7:0 | PATGEN_IA | RW | 0 | Indirect Address: This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198 . |
| 0x67 | PGID | 7:0 | PATGEN_ID | RW | 0 | Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value. See TI App Note AN-2198 . |
| 0x68 | PGDBG | 7:4 | RESERVED | RW | 0 | Reserved |
| | | 3 | PATGEN_BIST_EN | RW | 0 | Pattern Generator BIST Enable: Enables Pattern Generator in BIST mode. Pattern Generator will compare received video data with local generator pattern. Upstream device must be programmed to the same pattern. |
| | | 2:0 | RESERVED | RW | 0 | Reserved |
| 0x69 | PGTSTDAT | 7 | PATGEN_BIST_ERR | R | 0 | Pattern Generator BIST Error Flag During Pattern Generator BIST mode, this bit indicates if the BIST engine has detected errors. If the BIST Error Count (available in the Pattern Generator indirect registers) is non-zero, this flag will be set. |
| | | 6:0 | RESERVED | R | 0 | |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|------------------|--------|-----------------|------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x6A | CSICFG0 | 7:6 | RESERVED | RW | 00 | Reserved |
| | | 5:4 | LANE_CNT | RW | 00 | Setup number of data lanes for the CSI ports. 00/01: 4 data lanes 10: 2 data lanes |
| | | 3 | ULPM | RW | 0 | When set, put the data lanes in ultra-low power mode (LP00) by sending out a LP signalling sequence. |
| | | 2 | ULPS | RW | 0 | When set with ULPM, put the clock lane into ultra-low power mode. No effect if ULPM is not set. |
| | | 1 | CONTS_CLK | RW | 0 | When set, keep the clock lane running (in HS mode) during line blank (DE=0) and frame black (VS not active) |
| | | 0 | CSI_DIS | RW | 0 | When set, disable the CSI state machine. Function as a soft reset. |
| 0x6B | CSICFG1 | 7:4 | OFMT | RW | 0000 | Program the output CSI data formats 0000: RGB888 0001: RGB666 0010: RGB565 0011: YUV420 Legacy 0100: YUV420 0101: YUV422_8 0110: RAW8 0111: RAW10 1000: RAW12 1001: YUV420 (CSPS) |
| | | 3:2 | IFMT | RW | 00 | Program the input data format in HDMI terminology 00: RGB444 01: YUV422 10: YUV444 11: RAW |
| | | 1 | INV_VS | RW | 0 | When set, the VS received from the digital receiver will be inverted. Because the CSI logic works on active-high VS, this bit is typically set when the VS from the data source is active-low. |
| | | 0 | INV_DE | RW | 0 | When set, the DE received from the digital receiver will be inverted. Because the CSI logic works on active-high DE, this bit is typically set when the DE from the data source is active-low. |
| | | 7:0 | CSI_IA | RW | 0 | Indirect address port for accessing CSI registers. Refer to Table 13 |
| 0x6C | CSIIA | 7:0 | CSI_ID | RW | 0 | Indirect data port for accessing CSI registers. Refer to Table 13 |
| 0x6D | CSIID | 7:0 | CSI_ID | RW | 0 | Indirect data port for accessing CSI registers. Refer to Table 13 |
| 0x6E | GPI Pin Status 1 | 7 | GPI7 Pin Status | R | 0 | GPI7/I2S_WC pin status |
| | | 6 | GPI6 Pin Status | R | 0 | GPI6/I2S_DA pin status |
| | | 5 | GPI5 Pin Status | R | 0 | GPI5/I2S_DB pin status |
| | | 4 | RESERVED | R | 0 | Reserved for future use |
| | | 3 | GPI3 Pin Status | R | 0 | GPI3 / I2S_DD pin status |
| | | 2 | GPI2 Pin Status | R | 0 | GPI2 / I2S_DC pin status |
| | | 1 | GPI1 Pin Status | R | 0 | GPI1 pin status |
| | | 0 | GPI0 Pin Status | R | 0 | GPI0 pin status |
| 0x6F | GPI Pin Status 2 | 7:1 | RESERVED | R | 0 | Reserved for future use |
| | | 0 | GPI8 Pin Status | R | 0 | GPI8/I2S_CLK pin status |
| 0x80 | RX_BKSV0 | 7:0 | BKSV0 | R | 0 | BKSV0: Value of byte0 of the Receiver KSV. |
| 0x81 | RX_BKSV1 | 7:0 | BKSV1 | R | 0 | BKSV1: Value of byte1 of the Receiver KSV. |
| 0x82 | RX_BKSV2 | 7:0 | BKSV2 | R | 0 | BKSV2: Value of byte2 of the Receiver KSV. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|------------------|------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x83 | RX_BKSV3 | 7:0 | BKSV3 | R | 0 | BKSV3: Value of byte3 of the Receiver KSV. |
| 0x84 | RX_BKSV4 | 7:0 | BKSV4 | R | 0 | BKSV4: Value of byte4 of the Receiver KSV. |
| 0x90 | TX_KSV0 | 7:0 | TX_KSV0 | R | 0 | TX_KSV0: Value of byte0 of the Transmitter KSV. |
| 0x91 | TX_KSV1 | 7:0 | TX_KSV1 | R | 0 | TX_KSV1: Value of byte1 of the Transmitter KSV. |
| 0x92 | TX_KSV2 | 7:0 | TX_KSV2 | R | 0 | TX_KSV2: Value of byte2 of the Transmitter KSV. |
| 0x93 | TX_KSV3 | 7:0 | TX_KSV3 | R | 0 | TX_KSV3: Value of byte3 of the Transmitter KSV. |
| 0x94 | TX_KSV4 | 7:0 | TX_KSV4 | R | 0 | TX_KSV4: Value of byte4 of the Transmitter KSV. |
| 0xC0 | HDCCP_DBG | 7 | RESERVED | R | 0 | Reserved |
| | | 6 | HDCCP_I2C_TO_DIS | R | 0 | HDCCP I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the HDCCP I2C master. When enabled, the bus timeout function allows the I2C master to assume the bus is free if no signaling occurs for more than 1 second. Set via the HDCCP_DBG register in the HDCCP Transmitter. |
| | | 5:4 | RESERVED | R | 0 | Reserved |
| | | 3 | RGB_CHKSUM_EN | R | 0 | Enable RGB video line checksum: Enables sending of ones-complement checksum for each 8-bit RGB data channel following end of each video data line. Set via the HDCCP_DBG register in the HDCCP Transmitter. |
| | | 2 | FAST_LV | R | 0 | Fast Link Verification: HDCCP periodically verifies that the HDCCP Receiver is correctly synchronized. Setting this bit will increase the rate at which synchronization is verified. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames. Set via the HDCCP_DBG register in the HDCCP Transmitter. |
| | | 1 | TMR_SPEEDUP | R | 0 | Timer Speedup: Speed up HDCCP authentication timers. Set via the HDCCP_DBG register in the HDCCP Transmitter. |
| | | 0 | HDCCP_I2C_FAST | R | 0 | HDCCP I2C Fast mode Enable: Setting this bit to a 1 will enable the HDCCP I2C Master in the HDCCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Master will operation with Standard mode timing. Set via the HDCCP_DBG register in the HDCCP Transmitter. |
| 0xC1 | HDCCP_DBG 2 | 7:2 | RESERVED | RW | 0 | Reserved |
| | | 1 | NO_DECRYPT | RW | 0 | No Decrypt: When set to a 1, the HDCCP Receiver will output the encrypted data on the RGB pins. All other functions will work normally. This provides a simple way of showing that the link is encrypted. |
| | | 0 | HDCCP_EN_MODE | RW | 0 | HDCCP Enable Mode: This bit controls whether the HDCCP Repeater function will enable HDCCP in attached HDCCP Transmitters if it detects HDCCP is already enabled. 1 : Don't re-enable HDCCP if already enabled. 0 : Re-enable HDCCP at start of authentication, even if HDCCP Transmitter already has HDCCP enabled. |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|----------------|--------|----------------|------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xC4 | HDCP_STS | 7:2 | RESERVED | R | 0 | Reserved |
| | | 1 | RGB_CHKSUM_ERR | R | 0 | RGB Checksum Error Detected: If RGB Checksum is enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected. This register may be cleared by writing any value to this register |
| | | 0 | AUTHED | R | 0 | HDCP Authenticated: Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication. |
| 0xC9 | KSV_FIFO_DATA | 7:0 | KSV_FIFO_DATA | RW | 0x00 | KSV_FIFO_DATA: During External Repeater Control mode, the External HDCP controller writes KSV data to the KSV FIFO through this register. A byte written to this register location will write one byte of KSV data to the KSV FIFO at the location indicated by the KSV_FIFO_ADDR registers. |
| 0xCA | KSV_FIFO_ADDR0 | 7:0 | KSV_FIFO_ADDR0 | RW | 0x00 | KSV FIFO Address Register 0: This register contains the lower 8 bits of the KSF FIFO Address. This value should be set to 0 before writing the first byte of KSV data to the KSV FIFO. The KSV FIFO Address will automatically increment for each write to the KSV_FIFO_DATA register. |
| 0xCB | KSV_FIFO_ADDR1 | 7:0 | KSV_FIFO_ADDR1 | RW | 0x00 | KSV FIFO Address Register 1: This register contains the most significant bit of the KSF FIFO Address. This value should be set to 0 before writing the first byte of KSV data to the KSV FIFO. The KSV FIFO Address will automatically increment for each write to the KSV_FIFO_DATA register. |
| 0xE0 | RPTR_TX0 | | | | | HDCP Repeater Transmit Port 0 Register |
| | | 7:1 | PORT0_ADDR | R | 0 | Transmit Port 0 I2C Address Indicates the I2C address for the Repeater Transmit Port. |
| | | 0 | PORT0_VALID | R | 0 | Transmit Port 0 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register |
| 0xE1 | RPTR_TX1 | | | | | HDCP Repeater Transmit Port 1 Register |
| | | 7:1 | PORT1_ADDR | R | 0 | Transmit Port 1 I2C Address Indicates the I2C address for the Repeater Transmit Port. |
| | | 0 | PORT1_VALID | R | 0 | Transmit Port 1 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register |
| 0xE2 | RPTR_TX2 | | | | | HDCP Repeater Transmit Port 2 Register |
| | | 7:1 | PORT2_ADDR | R | 0 | Transmit Port 2 I2C Address Indicates the I2C address for the Repeater Transmit Port. |
| | | 0 | PORT2_VALID | R | 0 | Transmit Port 2 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register |
| 0xE3 | RPTR_TX3 | | | | | HDCP Repeater Transmit Port 3 Register |
| | | 7:1 | PORT3_ADDR | R | 0 | Transmit Port 3 I2C Address Indicates the I2C address for the Repeater Transmit Port. |
| | | 0 | PORT3_VALID | R | 0 | Transmit Port 3 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register |
| 0xF0 | HDCP_RX_ID0 | 7:0 | HDCP_RX_ID0 | R | 0x5F | HDCP_RX_ID0: First byte ID code, '_' |

Register Maps (continued)
Table 12. Serial Control Bus Registers (continued)

| ADD (hex) | Register Name | Bit(s) | Function | Type | Default Value (hex) | Description |
|-----------|---------------|--------|-------------|------|---------------------|----------------------------------------------------------------------------------------------------------|
| 0xF1 | HDCP_RX_ID1 | 7:0 | HDCP_RX_ID1 | R | 0x55 | HDCP_RX_ID1: 2nd byte of ID code, 'U' |
| 0xF2 | HDCP_RX_ID2 | 7:0 | HDCP_RX_ID2 | R | 0x48 | HDCP_RX_ID2: 3rd byte of ID code. Value will be either 'B' or 'H'. 'H' indicates an HDCP capable device. |
| 0xF3 | HDCP_RX_ID3 | 7:0 | HDCP_RX_ID3 | R | 0x39 | HDCP_RX_ID3: 4th byte of ID code: '9' |
| 0xF4 | HDCP_RX_ID4 | 7:0 | HDCP_RX_ID4 | R | 0x34 | HDCP_RX_ID4: 5th byte of ID code: '4' |
| 0xF5 | HDCP_RX_ID5 | 7:0 | HDCP_RX_ID5 | R | 0x30 | HDCP_RX_ID5: 6th byte of ID code: '0' |

Table 13. CSI Indirect Register Table

| Offset (hex) | Register Name | Bit(s) | Default Value (hex) | Function |
|--------------|---------------|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x09 | RAW_ALIGN | 7:5 | 0x00 | Reserved |
| | | 4 | | Raw Align. 0: RAW Output onto LSB's of RGB Bus 1: RAW Output onto MSB's of RGB Bus |
| | | 3:0 | | Reserved |
| 0x13 | CSI_EN_PORT0 | 7 | 0 | Register Control 0 = Disable 1 = Enable |
| | | 6 | 0 | Reserved |
| | | 5:0 | 0x3F | 0x00 = Disable CSI Port 0 0x3F = Enable CSI Port 0 |
| 0x14 | CSI_EN_PORT1 | 7 | 0 | Register Control 0 = Disable 1 = Enable |
| | | 6 | 0 | Reserved |
| | | 5:0 | 0x00 | 0x00 = Disable CSI Port 1 0x3F = Enable CSI Port 1 |
| 0x16 | CSIPASS | 7:3 | 0x02 | Reserved |
| | | 2 | | CSI_PASS to GPIO3. Configures GPIO3 to output the PASS signal when this bit is set HIGH. |
| | | 1 | | CSI_PASS to GPIO0. Configures GPIO0 to output the PASS signal when this bit is set HIGH. This is the default. |
| | | 0 | | CSI_PASS. This bit reflects the status of the PASS signal. |
| 0x2E | CSI_VC_ID | 7:6 | 0x00 | CSI Virtual Channel identifier. 00: CSI-2 outputs with ID as virtual channel 0. 01: CSI-2 outputs with ID as virtual channel 1. 10: CSI-2 outputs with ID as virtual channel 2. 11: CSI-2 outputs with ID as virtual channel 3. |
| | | 5:0 | | Reserved |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UH940-Q1 is a FPD-Link III Deserializer which, in conjunction with the DS90UH949/947-Q1 Serializers, converts 1-lane or 2-lane FPD-Link III streams into a MIPI CSI-2 interface. The Deserializer is capable of operating over cost-effective 50Ω single-ended coaxial or 100Ω differential shielded twisted-pair (STP) cables. It recovers the data from two FPD-Link III serial streams and translates it into a Camera Serial Interface (CSI-2) format compatible with MIPI DPHY/CSI-2 supporting video resolutions up to WUXGA and 1080p60 with 24-bit color depth.

9.2 Typical Applications

Bypass capacitors should be placed near the power supply pins. At a minimum, four (4) 10μF capacitors should be used for local device bypassing. Ferrite beads are placed on the two sets of supply pins (VDD33 and VDDIO) for effective noise suppression. The interface to the graphics source is LVDS. The VDDIO pins may be connected to 3.3V or 1.8V. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable. See [Figure 37](#) for a typical STP connection diagram and for a typical coax connection diagram.

Typical Applications (continued)

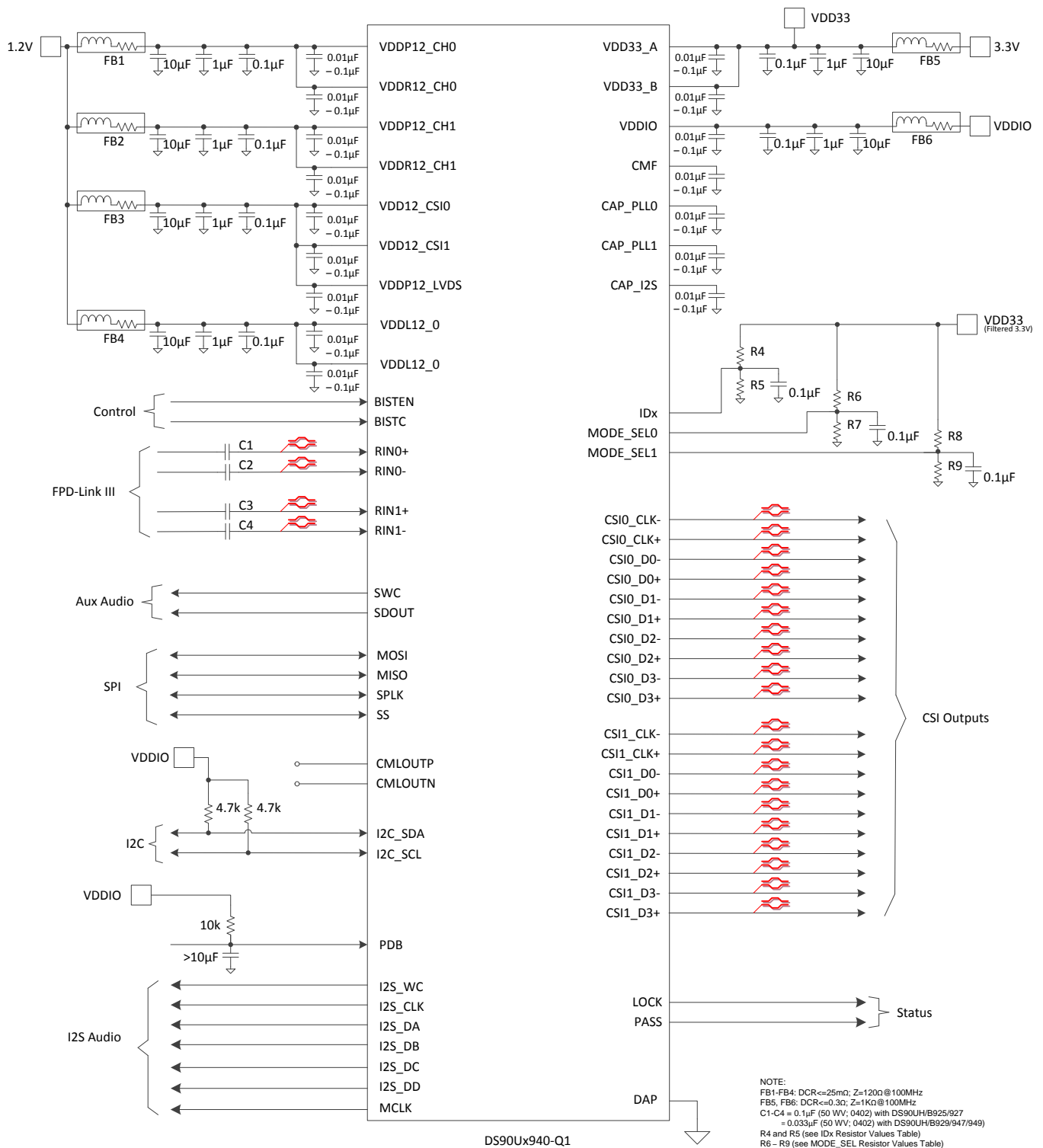


Figure 37. Typical Connection Diagram (STP)

Typical Applications (continued)

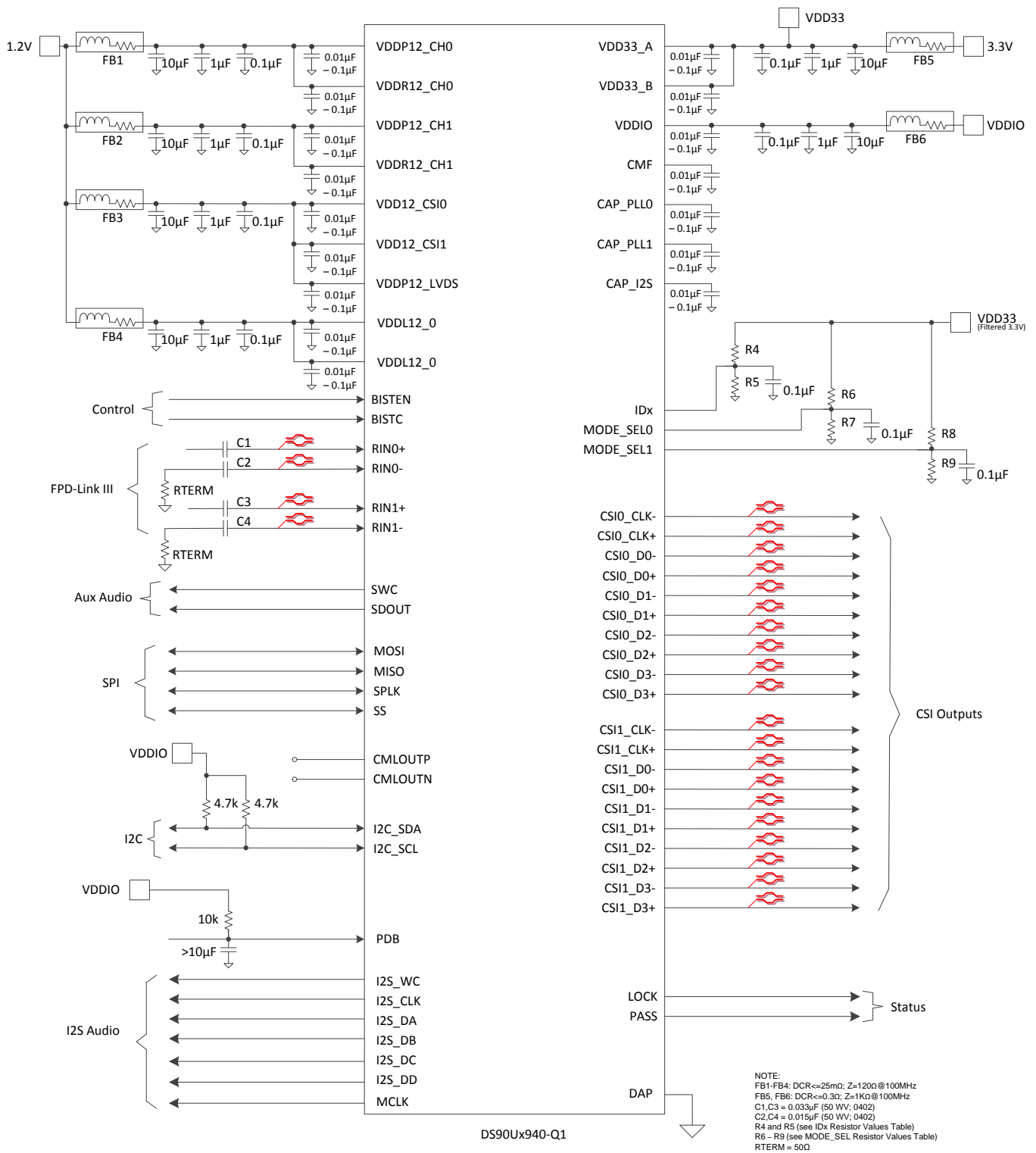
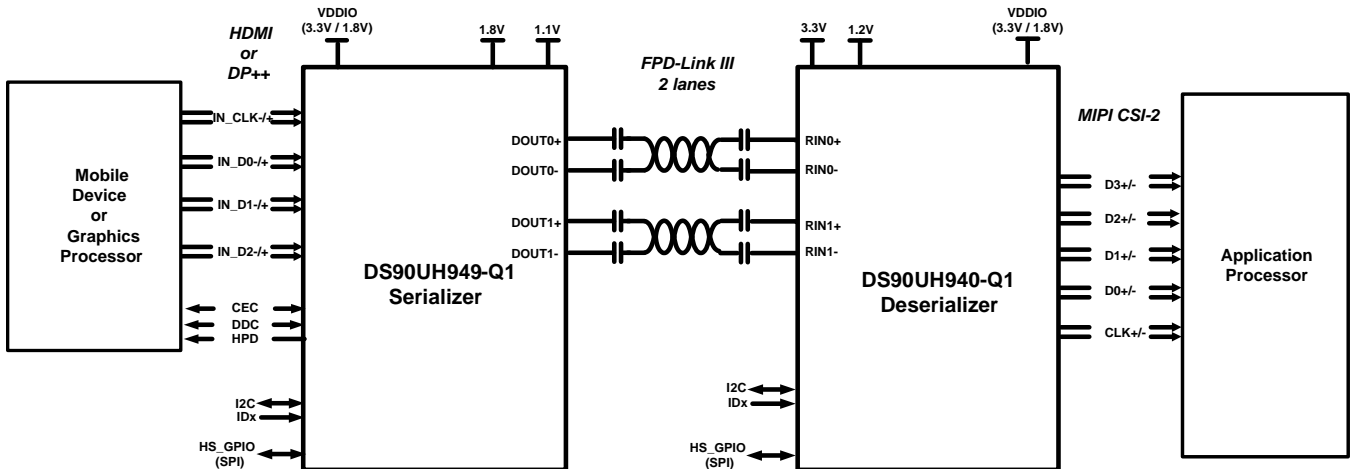


Figure 38. Typical Connection Diagram (Coax)



9.2.1 Design Requirements

For the typical design application, use the following as input parameters.

Table 14. Design Parameters

| Design Parameter | Example Value |
|-------------------------------------------|---------------|
| VDDIO | 1.8V or 3.3V |
| VDD12 | 1.2V |
| VDD33 | 3.3V |
| AC Coupling Capacitor for RIN0± and RIN1± | 33 nF |

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 39. For applications utilizing single-ended 50 Ω coaxial cable, the unused data pins (RIN0-, RIN1-) should utilize a 15 nF capacitor and should be terminated with a 50 Ω resistor.

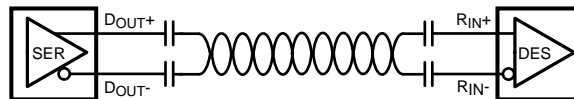


Figure 39. AC-Coupled Connection (STP)

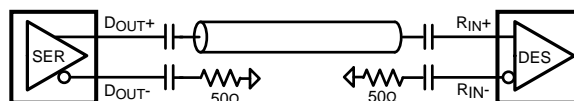


Figure 40. AC-Coupled Connection (Coaxial)

For high-speed FPD-Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O's require 33 nF AC coupling capacitors to the line.

9.2.2 Detailed Design Procedure

9.2.2.1 PCB Layout and Power System Considerations

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μF to 10 μF . Tantalum capacitors may be in the 2.2 μF to 10 μF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 μF to 100 μF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20MHz-30MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 32 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the WQFN style package, including PCB design and manufacturing requirements, is provided in TI Application Note: AN-1187.

9.2.2.2 CML Interconnect Guidelines

See AN-1108 and AN-905 for full details.

- Use 100 Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
 - S = space between the pair
 - 2S = space between pairs
 - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: [SNLA187](#)

9.2.3 Application Performance Plots

The plots below correspond to 1080p60 video application with 2-lane FPD-Link III input and MIPI 4 lanes output.

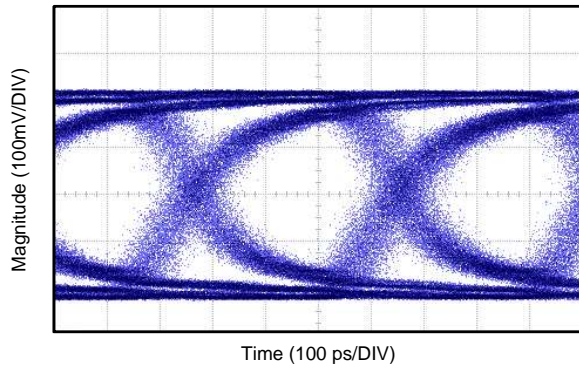


Figure 41. Loop-through CML Output at 2.6 Gbps Serial Line Rate

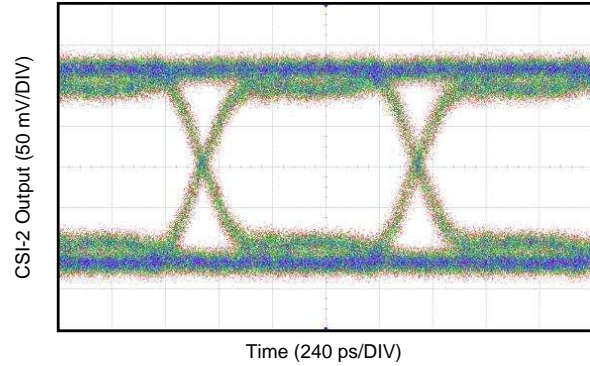


Figure 42. CSI-2 Data Output at 1040 Mbps

10 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description table provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

10.1 Power Up Requirements and PDB Pin

When power is applied, power from the highest voltage rail to the lowest voltage rail on any of the supply pins. For 3.3V IO operation, VDDIO and VDD33 can be powered by the same supply and ramped simultaneously. The power supply ramp (VDD12, VDD33, and VDDIO) should be faster than 1.5ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD33, a 10 k Ω pull-up and a >10 μ F capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both VDD33 and VDDIO has reached steady state. Pins VDD33_A and VDD33_B should both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μ F to 0.1 μ F. Tantalum capacitors may be in the 2.2 μ F to 10 μ F range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 μ F to 100 μ F range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

Layout Guidelines (continued)

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ω are typically recommended for CML interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: [AN-1187](#).

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in [Figure 43](#):

Table 15. No Pullback WQFN Stencil Aperture Summary

| Device | Pin Count | Mkt Dwg | PCB I/O Pad Size (mm) | PCB Pitch (mm) | PCB DAP Size (mm) | Stencil I/O Aperture (mm) | Stencil DAP Aperture (mm) | Number OF DAP Aperture Openings | Gap between DAP Aperture (Dim A mm) |
|--------------|-----------|---------|-----------------------|----------------|-------------------|---------------------------|---------------------------|---------------------------------|-------------------------------------|
| DS90UH940-Q1 | 64 | NKD | 0.25 x 0.6 | 0.5 | 7.2 x 7.2 | 0.25 x 0.6 | 1.16 x 1.16 | 25 | 0.2 |

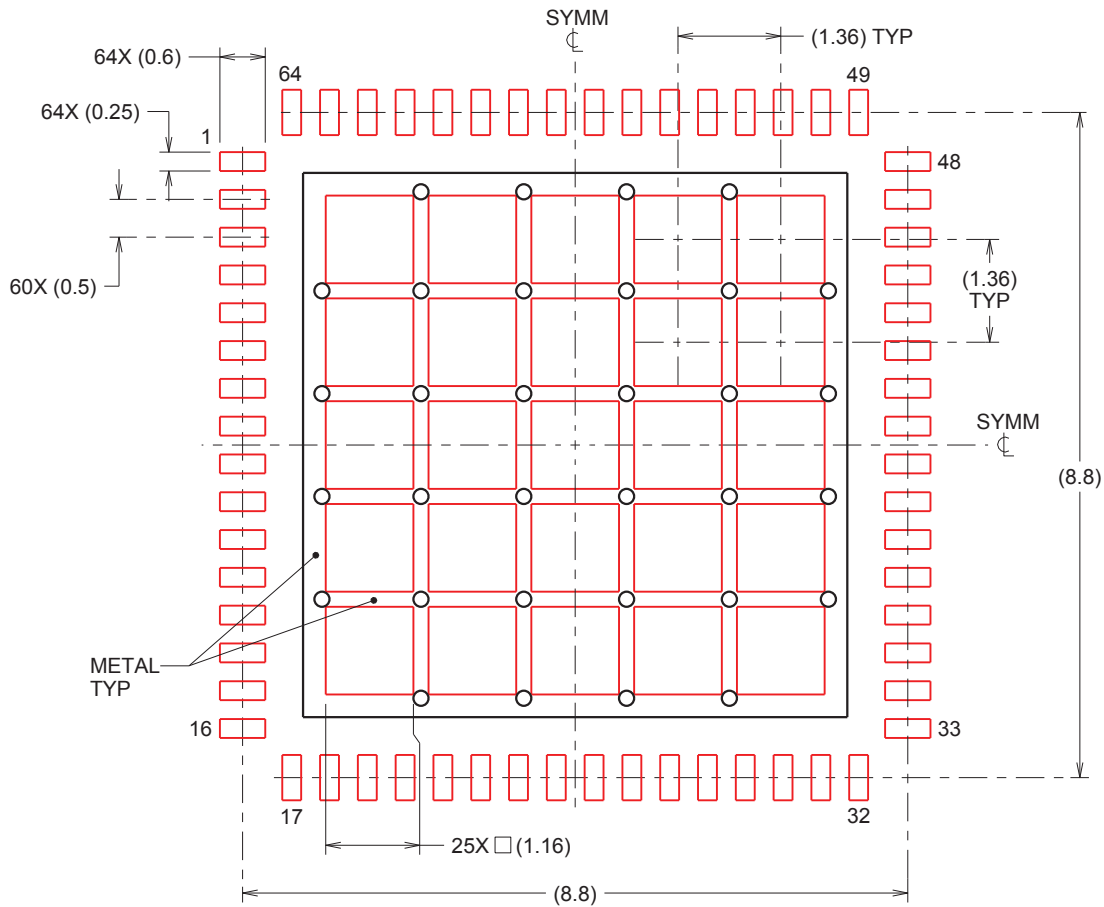


Figure 43. 64-Pin WQFN Stencil Example of Via and Opening Placement (dimensions in mm)

DS90UH940-Q1

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Figure 44 (PCB layout example) is derived from a layout design of the DS90UH940-Q1. This graphic and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

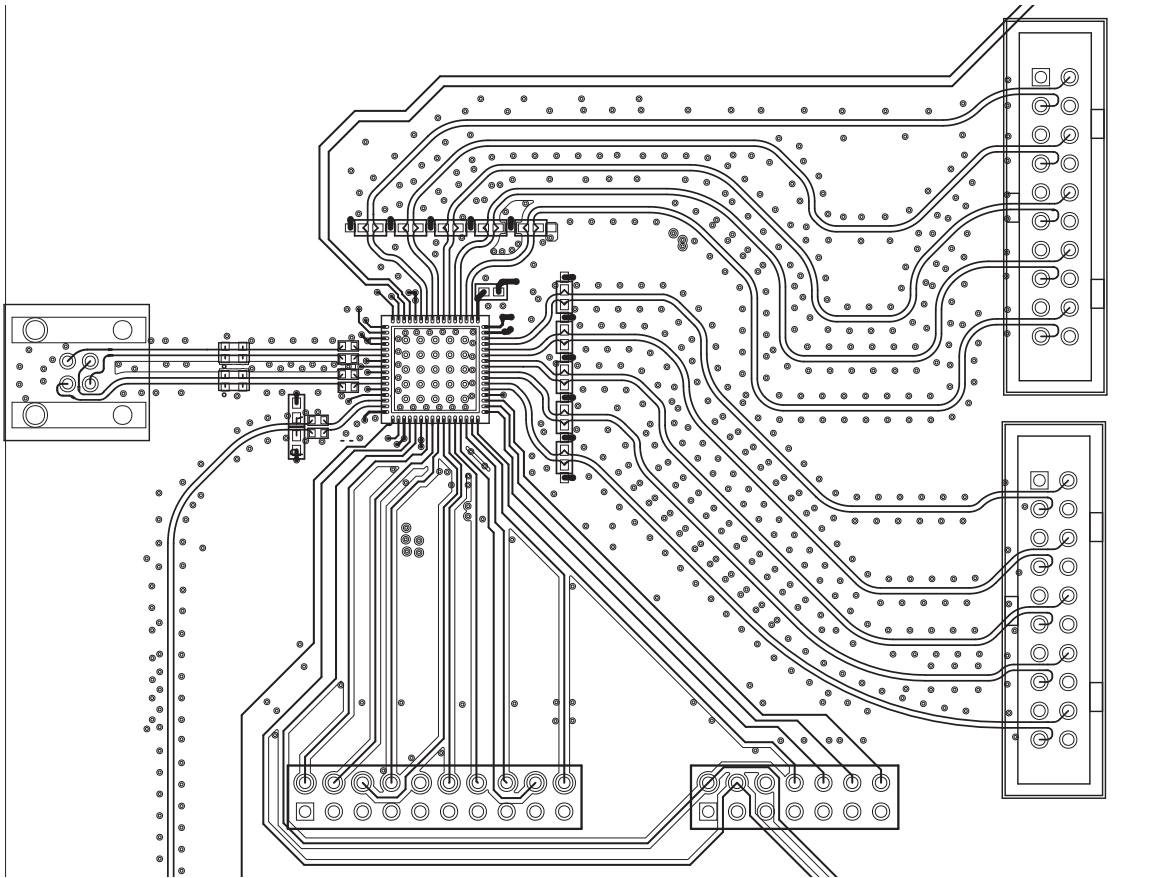


Figure 44. DS90UH940-Q1 Deserializer Example Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下:

- 《焊接规范应用报告》， [SNOA549](#)
- 《IC 封装热指标应用报告》， [SPRA953](#)
- 《通道链路 PCB 和互连设计指南》， [SNLA008](#)
- 《传输线路 RAPIDESIGNER 操作和应用指南》， [SNLA035](#)
- 《无引线框架封装 (LLP) 应用报告》， [SNOA401](#)
- 《LVDS 所有者手册》， [SNLA187](#)
- 《通过具有双向控制通道的 FPD-Link III 进行 I2C 通信》， [SNLA131](#)
- 《使用 DS90Ux92x FPD-Link III 器件的 I2S 音频接口》， [SNLA221](#)
- 《探索 720p FPD-Link III 器件的内部测试图案生成特性》， [SNLA132](#)

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DS90UH940TNKDRQ1 | Active | Production | WQFN (NKD) 64 | 2000 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 105 | 90UH940Q1 |
| DS90UH940TNKDRQ1.A | Active | Production | WQFN (NKD) 64 | 2000 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 105 | 90UH940Q1 |
| DS90UH940TNKDRQ1.B | Active | Production | WQFN (NKD) 64 | 2000 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 105 | 90UH940Q1 |
| DS90UH940TNKDTQ1 | Active | Production | WQFN (NKD) 64 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 105 | 90UH940Q1 |
| DS90UH940TNKDTQ1.A | Active | Production | WQFN (NKD) 64 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 105 | 90UH940Q1 |
| DS90UH940TNKDTQ1.B | Active | Production | WQFN (NKD) 64 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 105 | 90UH940Q1 |

(1) Status: For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90UH940TNKDRQ1 | WQFN | NKD | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.3 | 12.0 | 16.0 | Q1 |
| DS90UH940TNKDTQ1 | WQFN | NKD | 64 | 250 | 178.0 | 16.4 | 9.3 | 9.3 | 1.3 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

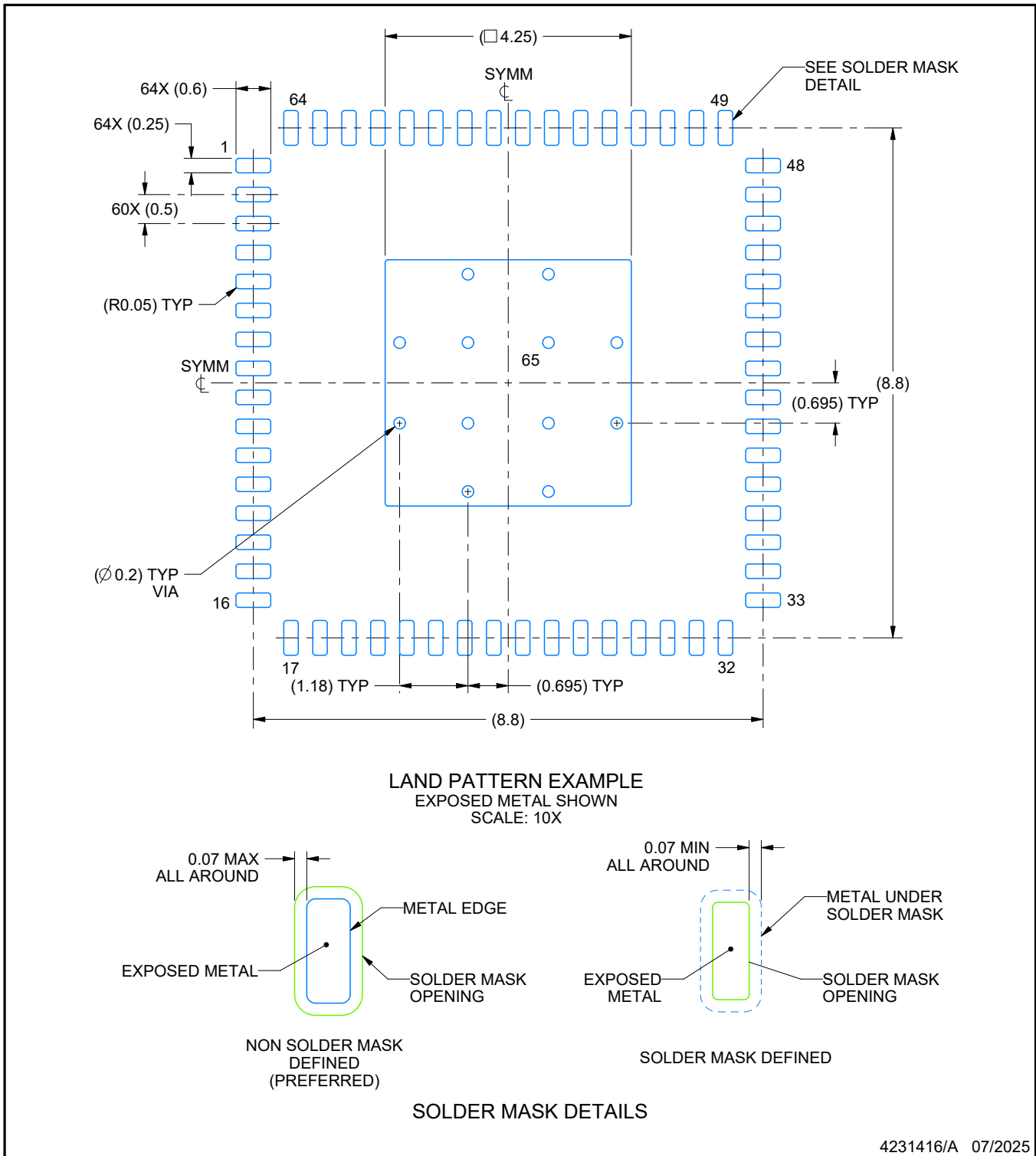
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90UH940TNKDRQ1 | WQFN | NKD | 64 | 2000 | 356.0 | 356.0 | 36.0 |
| DS90UH940TNKDTQ1 | WQFN | NKD | 64 | 250 | 208.0 | 191.0 | 35.0 |

EXAMPLE BOARD LAYOUT

NKD0064B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

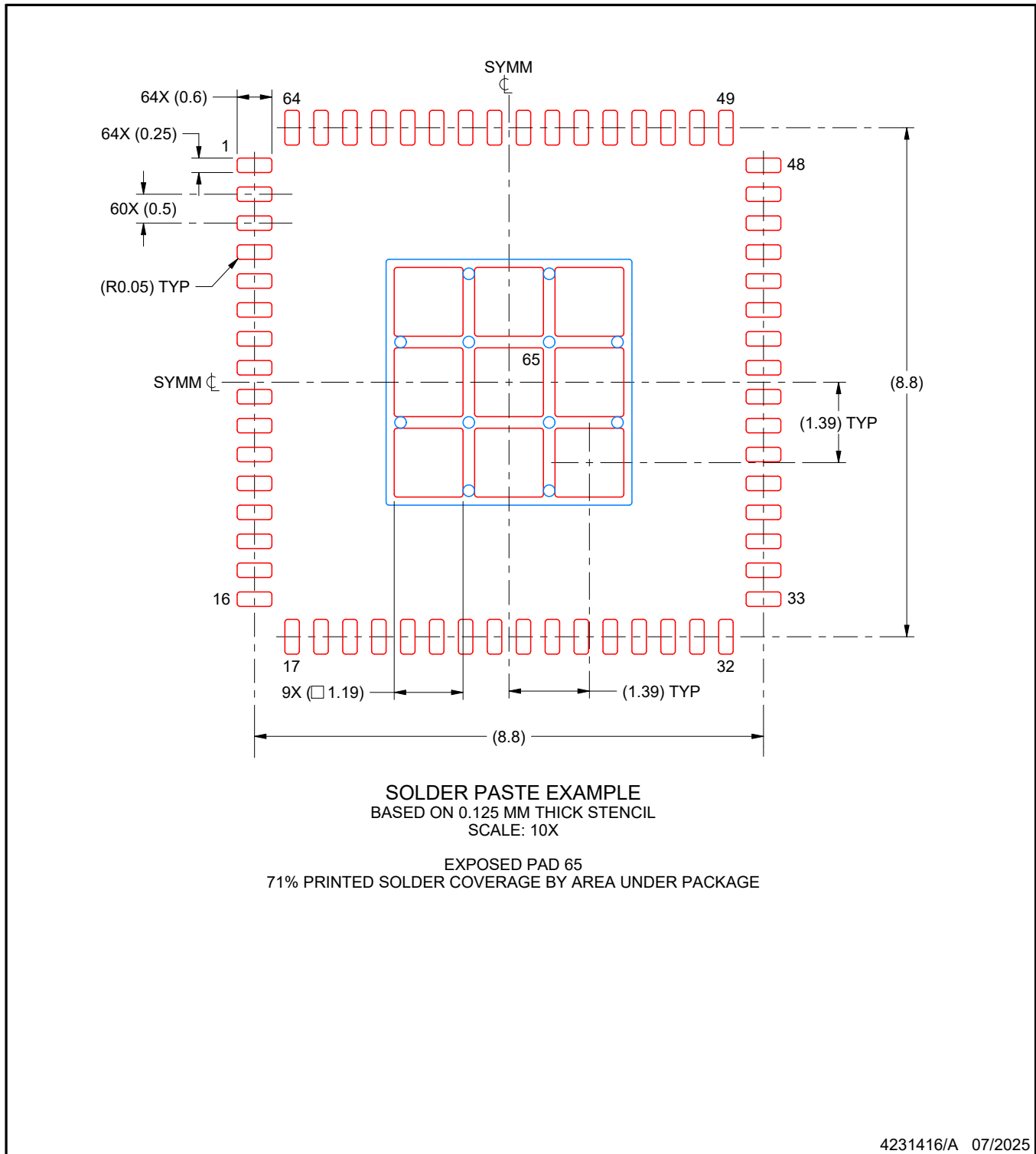
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

NKD0064B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

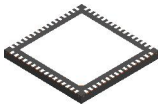


NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

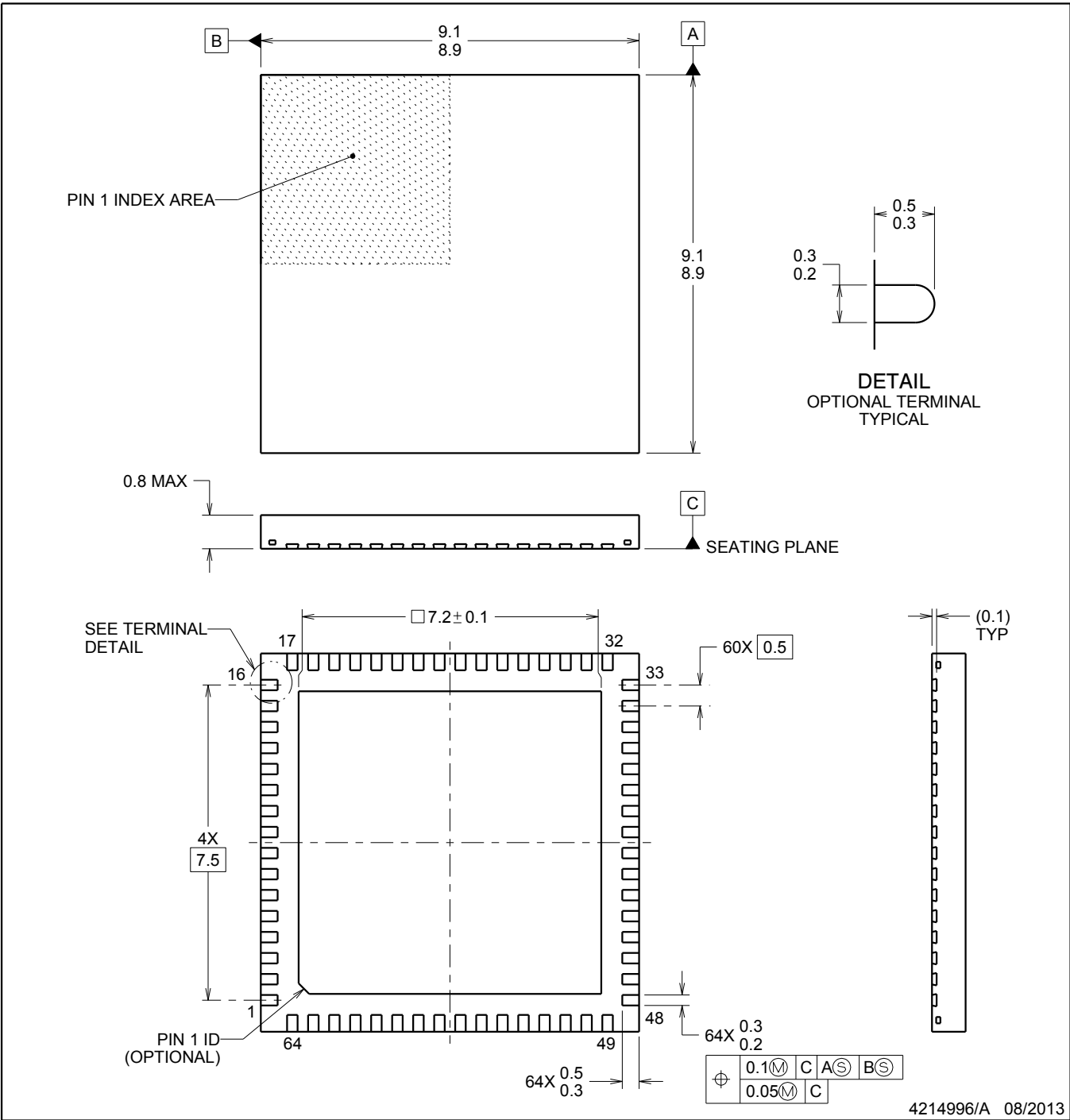
PACKAGE OUTLINE

NKD0064A



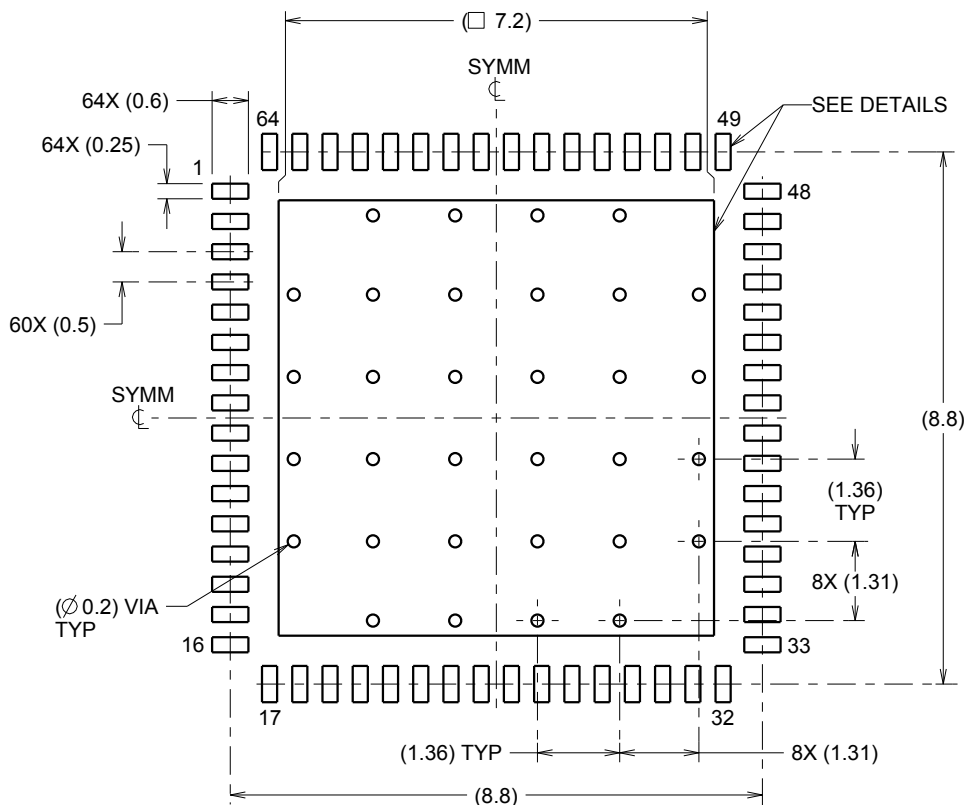
WQFN - 0.8 mm max height

WQFN

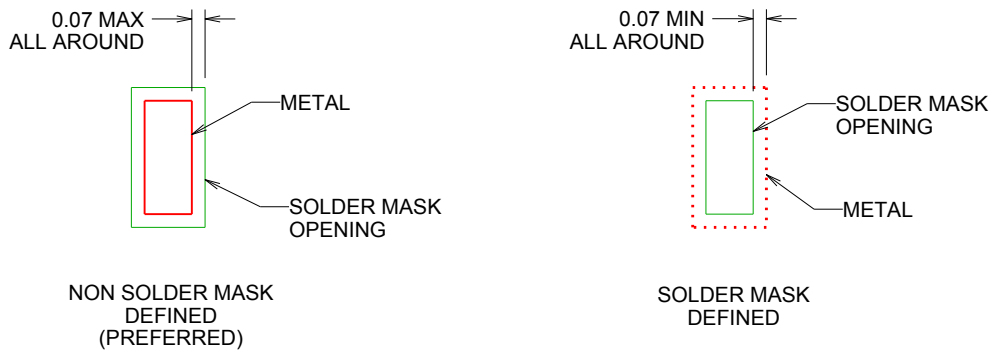


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

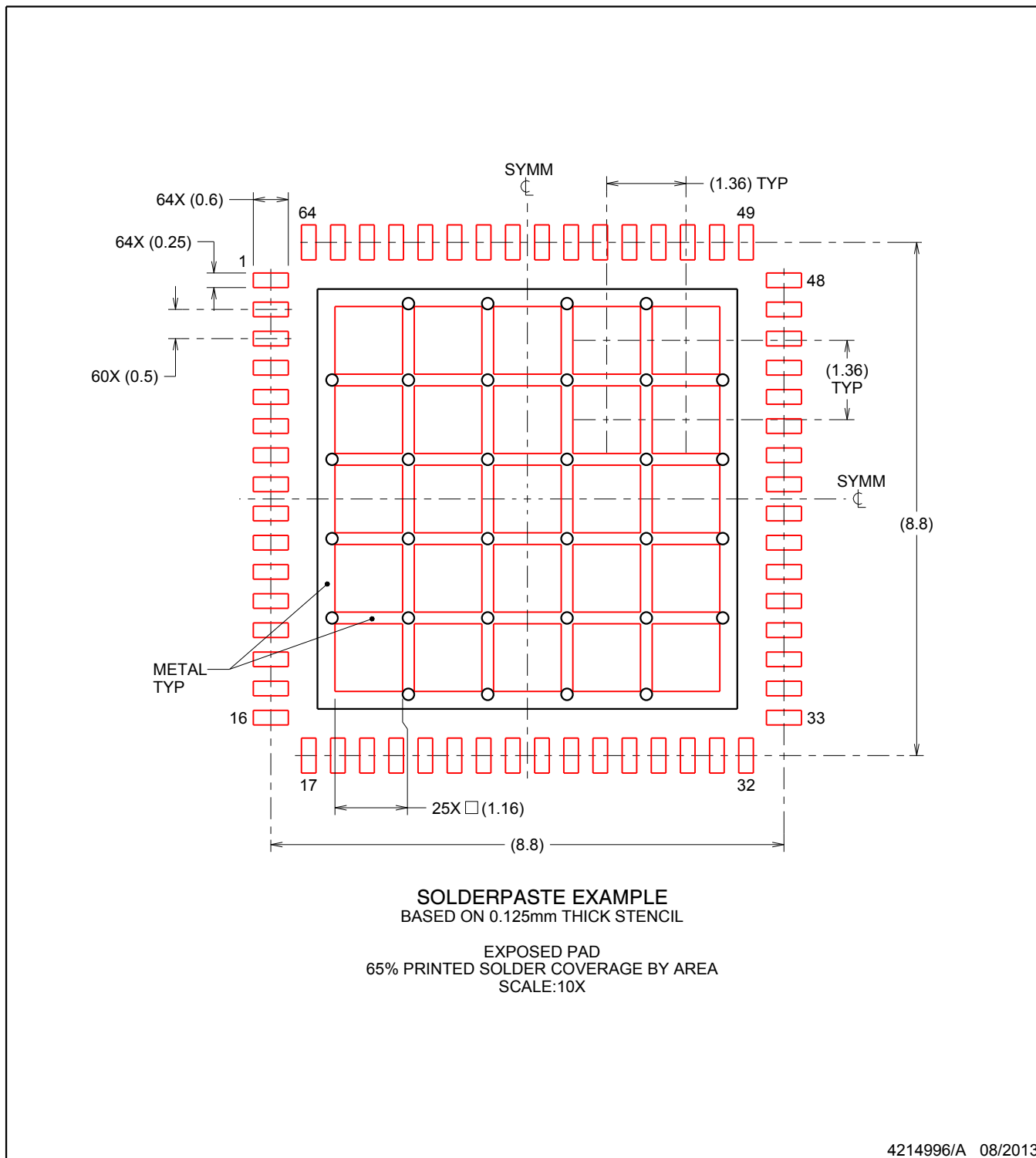


SOLDER MASK DETAILS

4214996/A 08/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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