ESD2CANFD24 用于车载网络的 24V、2 通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级 ESD 保护：
  - ±25kV 接触放电
  - ±25kV 气隙放电
- 经测试符合 IEC 61000-4-5
- 24V 工作电压
- 双向 ESD 保护
- 2 通道器件通过单个组件实现完整的 ESD 保护
- 低钳位电压可保护下游组件
- I/O 电容 = 2.5pF（典型值）
- SOT-23 (DBZ) 小型、标准、通用封装
- 引线式封装，用于自动光学检测 (AOI)

2 应用

- 工业控制网络：
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 和 EN 50325-4

3 说明

ESD2CANFD24 是一款用于控制器局域网 (CAN) 接口保护的双向 ESD 保护二极管。ESD2CANFD24 的额定消散接触 ESD 冲击能力超过了 IEC 61000-4-2 标准所规定的最高水平（±25kV 接触放电，±25kV 气隙放电）。低动态电阻和低钳位电压支持针对瞬态事件提供系统级保护。这种保护很关键，因为系统对安全应用的稳健性和可靠性要求很高。

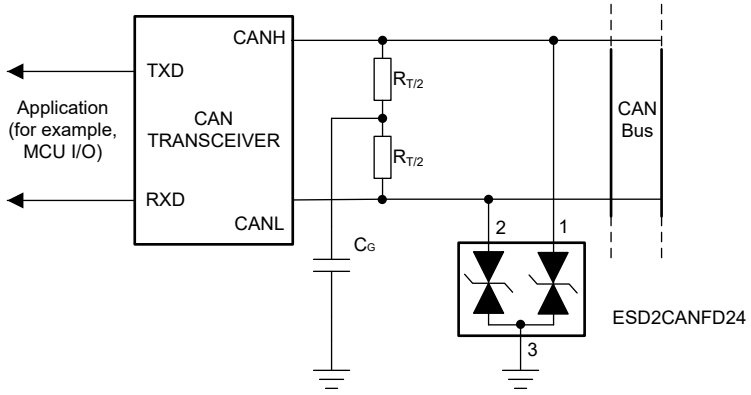
该器件具有每通道低 IO 电容和引脚排列，以便适合两条 CAN 总线（CANH 和 CANL），防止因静电放电 (ESD) 和其他瞬变造成损坏。此外，ESD2CANFD24 的 2.5pF（典型值）或更小线路电容适合 CAN、CANFD、CAN SiC 和支持高达 10Mbps 数据速率的 CAN-XL 应用。

ESD2CANFD24 采用引线式封装，以便轻松实现直通式路由。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
ESD2CANFD24	DBZ（SOT-23，3）	2.92mm × 1.30mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



ESD2CANFD24 典型应用

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4 Revision History

DATE	REVISION	NOTES
November 2022	*	Initial Release

5 Pin Configuration and Functions

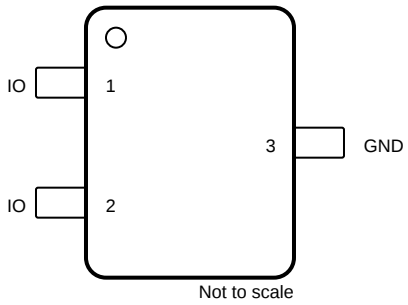


图 5-1. DBZ Package, 3-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

参数		器件	最小值	最大值	单位
P_{PP}	25°C 时的 IEC 61000-4-5 功率 (t_p – 8/20μs)	ESD2CANFD24		133	W
I_{PP}	25°C 时的 IEC 61000-4-5 电流 (t_p – 8/20μs)			3.5	A
T_A	自然通风工作温度		-55	150	°C
T_J	结温		-55	150	
T_{stg}	贮存温度		-65	155	

(1) 超出绝对最大额定值运行可能会对器件造成永久损坏。绝对最大额定值并不表示器件在这些条件下或在建议运行条件以外的任何其他条件下能够正常运行。如果超出建议运行条件但在绝对最大额定值范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。

6.2 ESD 等级 - JEDEC 规格

参数		测试条件	值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	± 2500	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JS-002(2)	± 1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

6.3 ESD 等级 - IEC 规格

在 TA = 25°C 条件下（除非另有说明）

参数		测试条件	器件	值	单位
$V_{(ESD)}$	静电放电	IEC 61000-4-2 接触放电，所有引脚	ESD2CANFD24	±25000	V
		IEC 61000-4-2 空气间隙放电，所有引脚		±25000	

6.4 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数		最小值	标称值	最大值	单位
V_{IN}	输入电压	-24		24	V
T_A	自然通风工作温度	-55		150	°C

6.5 热性能信息

热指标(1)		ESD2CANFD24 DBZ (SOT-23) 3 引脚	单位
$R_{\theta JA}$	结至环境热阻	316.3	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	170.7	°C/W
$R_{\theta JB}$	结至电路板热阻	156.2	°C/W
Ψ_{JT}	结至顶部特征参数	45.9	°C/W
Ψ_{JB}	结至电路板特征参数	155.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅半导体和 IC 封装热指标应用报告。

6.6 电气特性

在 T_A = 25°C 条件下（除非另有说明）(1)

参数		测试条件	器件	最小值	典型值	最大值	单位
V_{RWM}	反向关断电压		ESD2CANFD24	–24		24	V
V_{BRF}	击穿电压(2)	I_{IO} = 10mA、IO 至 GND	ESD2CANFD24	25.5		35.5	V
V_{BRR}	击穿电压(2)	I_{IO} = –10mA、IO 至 GND	ESD2CANFD24	-35.5		-25.5	V
V_{CLAMP}	钳位电压(3)	I_{PP} = 3.5A，t_p = 8/20μs，IO 到 GND	ESD2CANFD24		37		V
V_{CLAMP}	钳位电压(4)	I_{PP} = 16A、TLP、IO 至 GND 或 GND 至 IO	ESD2CANFD24		36		V
I_{LEAK}	漏电流	V_{IO} = ±24V、IO 至 GND	ESD2CANFD24	-50	5	50	nA
R_{DYN}	动态电阻(4)	IO 至 GND 或 GND 至 IO	ESD2CANFD24		0.45		Ω
C_L	线路电容(5)	V_{IO} = 0V、f = 1MHz、V_{pp} = 30mV	ESD2CANFD24		2.5	4.2	pF
V_{Hold}	快速复位后的保持电压	TLP	ESD2CANFD24		30		V

(1) 在每个 IO 通道上进行的测量
(2) V_{BRF} 和 V_{BRR} 被定义为在器件锁存到快速复位状态之前，分别在正向和负向方向上施加 ±10mA 的电压
(3) 根据 IEC 61000-4-5 器件承受 8/20 μ s 指数衰减波形的应力
(4) 非重复电流脉冲、传输线路脉冲 (TLP)；方波脉冲；ANSI / ESD STM5.5.1-2008
(5) 在每个通道上从 IO 测量到 GND

6.7 Typical Characteristics – ESD2CANFD24

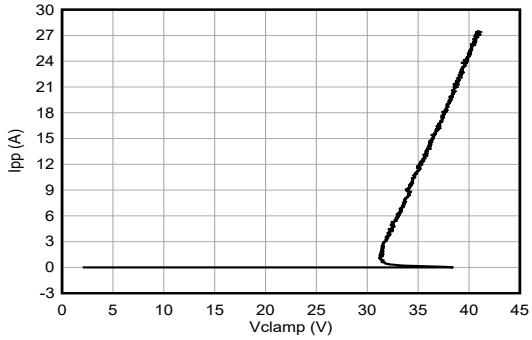


图 6-1. Positive TLP Curve

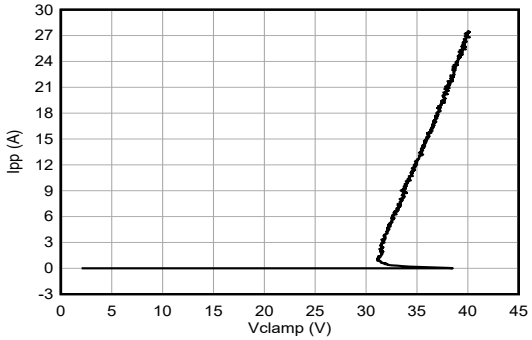


图 6-2. Negative TLP Curve

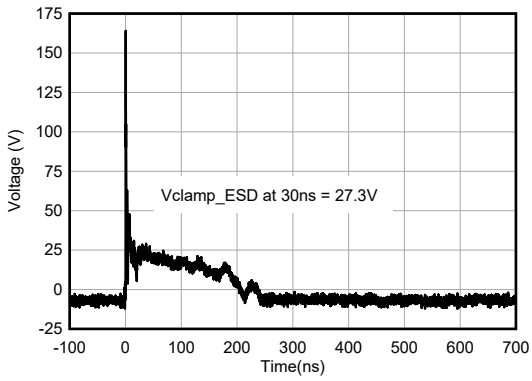


图 6-3. +8-kV Clamped IEC Waveform

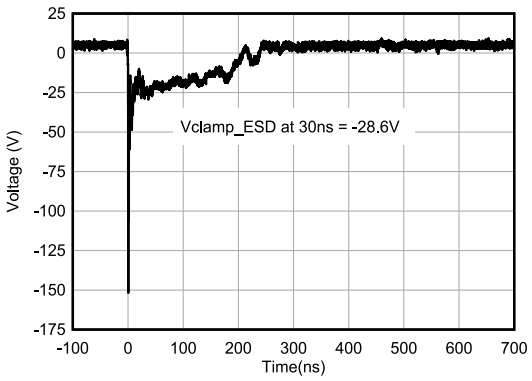


图 6-4. –8-kV Clamped IEC Waveform

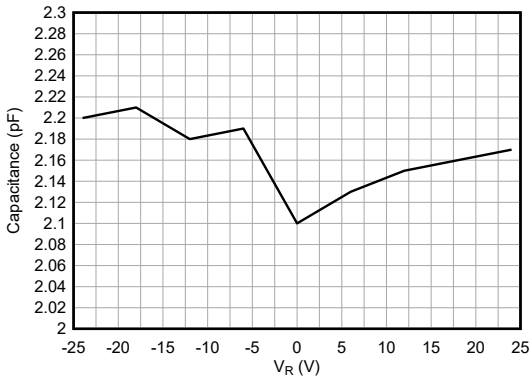


图 6-5. Capacitance vs. Bias Voltage

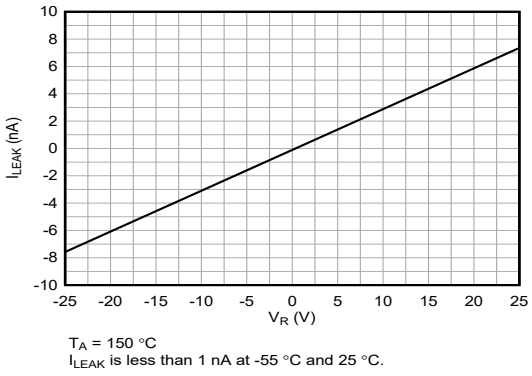


图 6-6. Leakage Current vs. Bias Voltage Across Temperature

6.7 Typical Characteristics – ESD2CANFD24 (continued)

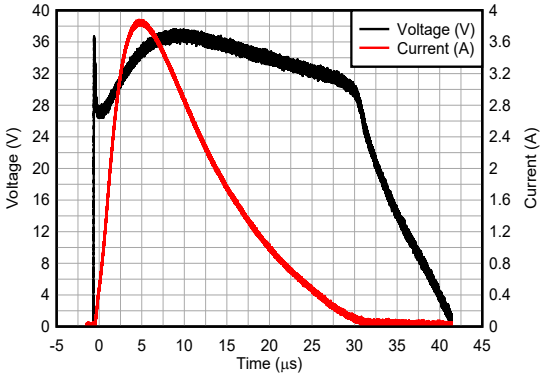


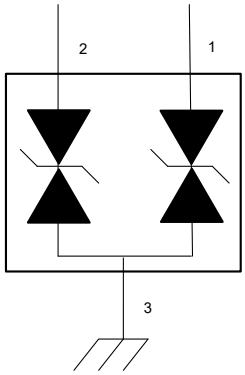
图 6-7. 8/20 µs Surge Response at 3.5 A

7 Detailed Description

7.1 Overview

The ESD2CANFD24 is a dual-channel ESD TVS diode in SOT-23 leaded package which is convenient for automatic optical inspection. This product offers IEC 61000-4-2 ±25-kV air-gap, ±25-kV contact ESD protection, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support. The 2.5 pF (typical) or less line capacitance of this ESD protection diode is suitable for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10 Mbps. A typical application for this product is ESD circuit protection for CAN transceivers.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD2CANFD24 is a bidirectional TVS with a high ESD protection level. This device protects the circuit from ESD strikes up to ±25-kV contact and ±25-kV air-gap specified in the IEC 61000-4-2 standard. The device can also handle up to 3.5 A surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 2.5-pF (typical) supports a data rate up to 10 Mbps. This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 37 V when the device is taking 3.5 A transient surge current. The breakdown is bidirectional so this protection device is a good fit for CAN which is a differential signal. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 package is good for applications requiring automatic optical inspection (AOI).

7.3.1 Temperature Range

This device is qualified to operate from –55°C to +150°C.

7.3.2 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events of at least ±25-kV contact and ±25-kV air-gap in the leaded SOT-23 package according to the IEC 61000-4-2 standard. An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3.5 A (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between the I/O pins is 2.5 pF (typical) or less. This capacitance supports data rates for CAN, CANFD, CAN SiC, and CAN-XL up to 10 Mbps.

7.3.5 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.45 Ω (Pin 1 or Pin 2 to Pin 3) and 0.45 Ω (Pin 3 to Pin 1 or Pin 2) or less which prevents system damage during ESD events.

7.3.6 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of ± 25.5 V. This protects sensitive equipment from surges above the reverse standoff voltage of ± 24 V.

7.3.7 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of ± 50 nA (maximum) with a bias of ± 24 V.

7.3.8 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V (I_{PP} = 3.5 A) and 36 V (I_{PP} = 16 A for TLP).

7.3.9 Industry Standard Leaded Packages

This device features an industry standard SOT-23 (DBZ) leaded package for automatic optical inspection (AOI).

7.4 Device Functional Modes

The ESD2CANFD24 is a dual channel passive clamp that has low leakage during normal operation when the voltage between pin 1 or pin 2 and pin 3 is below V_{RWM}, and activates when the voltage between pin 1 or pin 2 and pin 3 goes above V_{BR}. During IEC 61000-4-2 ESD events, transient voltages as high as ±25 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD2CANFD24 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on differential CAN signal lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

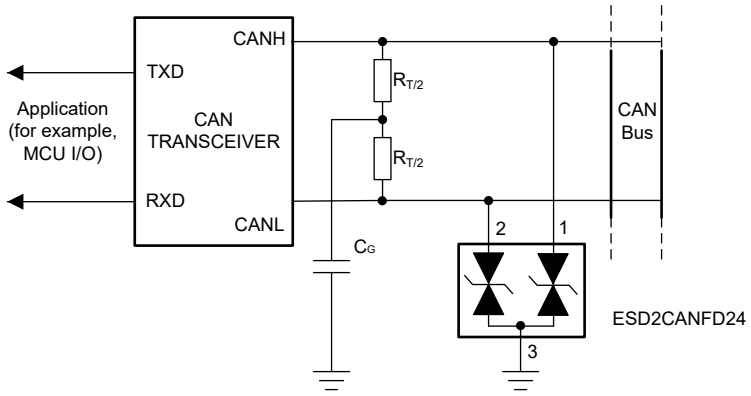


图 8-1. ESD2CANFD24 Typical Application

8.2.1 Design Requirements

For this design example, the ESD2CANFD24 is used to provide ESD protection for a CAN transceiver. 表 8-1 lists the known design parameters for this application.

表 8-1. Design Parameters for the ESD2CANFD24 Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} differential signal range	> ±1.5 V
V_{RWM}	±24 V
Data rate	Up to 10 Mbps
RT/2	60 Ω

8.2.2 Detailed Design Procedure

The ESD2CANFD24 has a V_{RWM} of ±24 V. The bidirectional characteristic enables the signal integrity of the differential CAN lines to not be impacted by the diode. The low capacitance of 2.5 pF (typical) or less enables data rates up to 10 Mbps, which allows the designer to meet the requirements for CAN, CANFD, CAN SiC, and CAN-XL. The 60 Ω split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

8.2.3 Application Curves

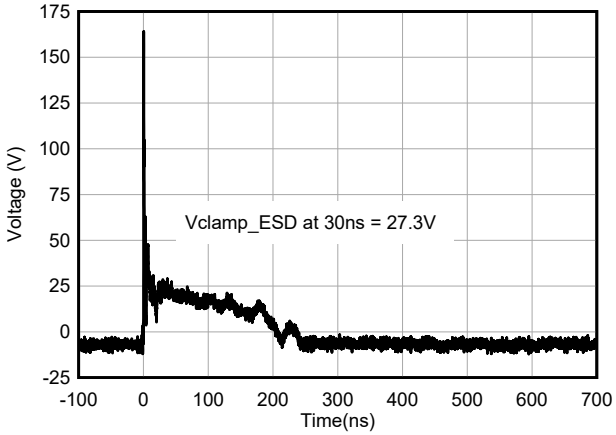


图 8-2. +8-kV Clamped IEC Waveform

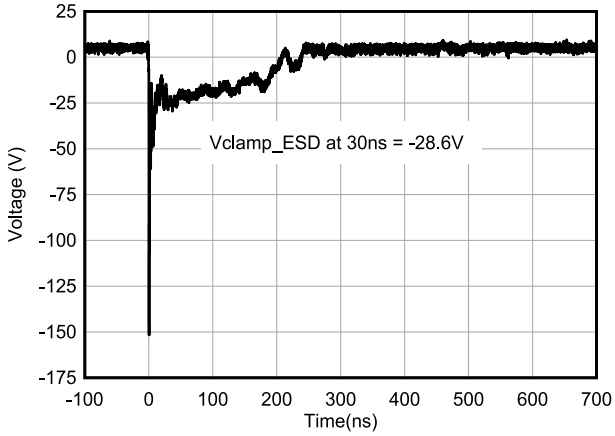


图 8-3. −8-kV Clamped IEC Waveform

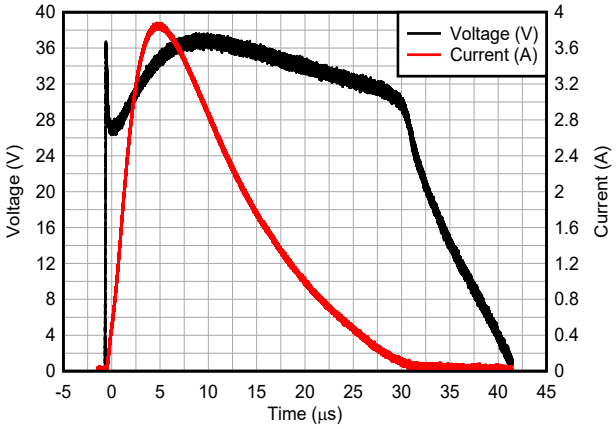


图 8-4. 8/20 µs Surge Response at 3.5 A

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

This example is typical of a dual channel differential data pair application, such as CAN.

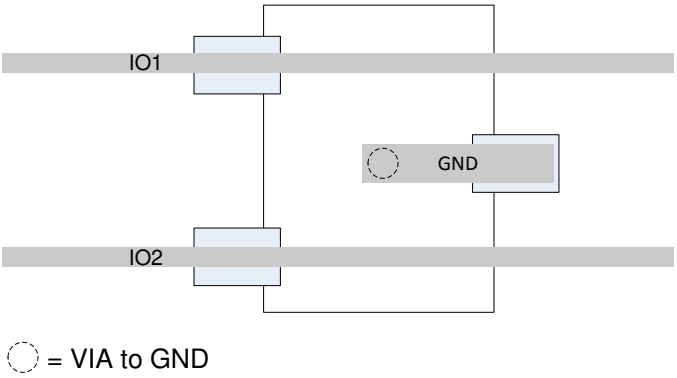


图 10-1. Routing with DBZ Package

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD2CANFD24DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-50 to 150	2QO8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ESD2CANFD24 :

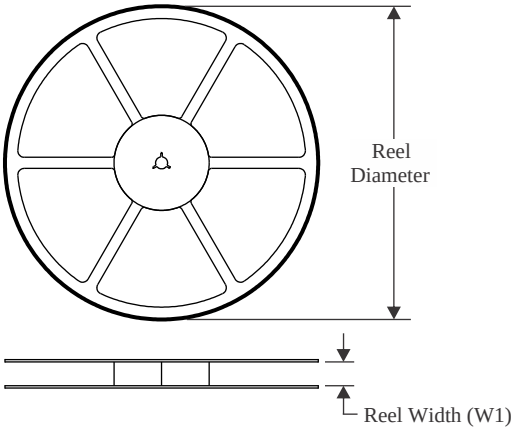
- Automotive : ESD2CANFD24-Q1

NOTE: Qualified Version Definitions:

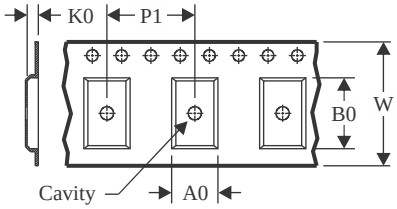
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

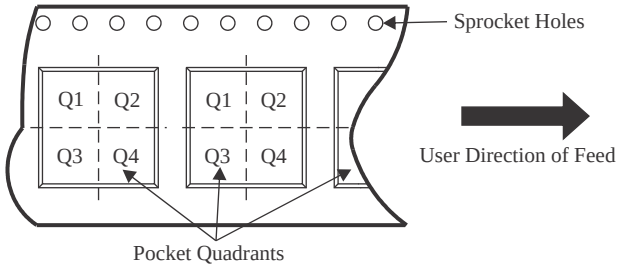


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

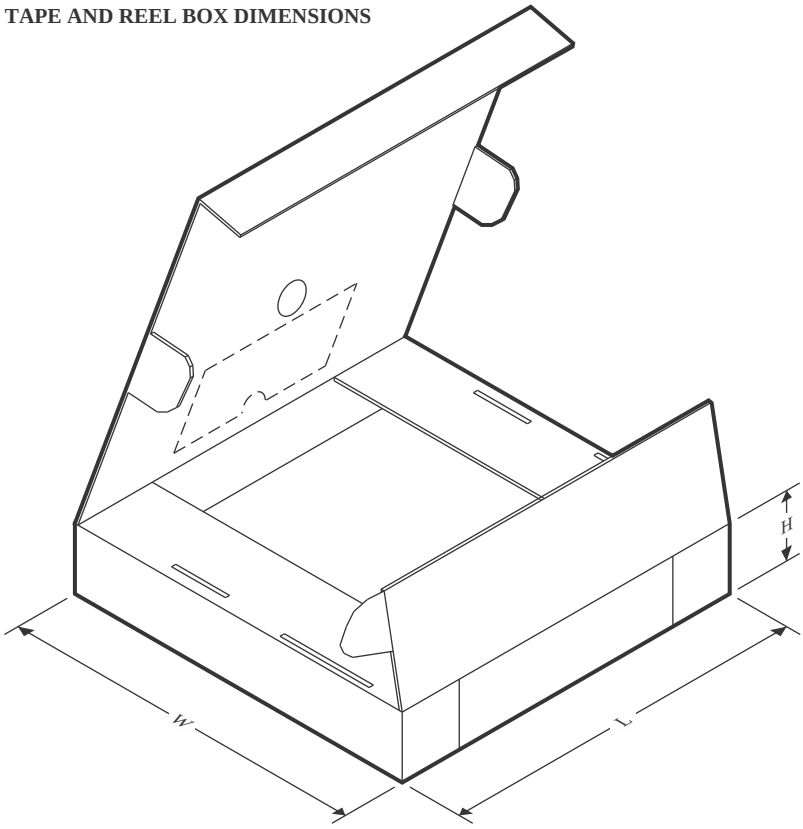
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CANFD24DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

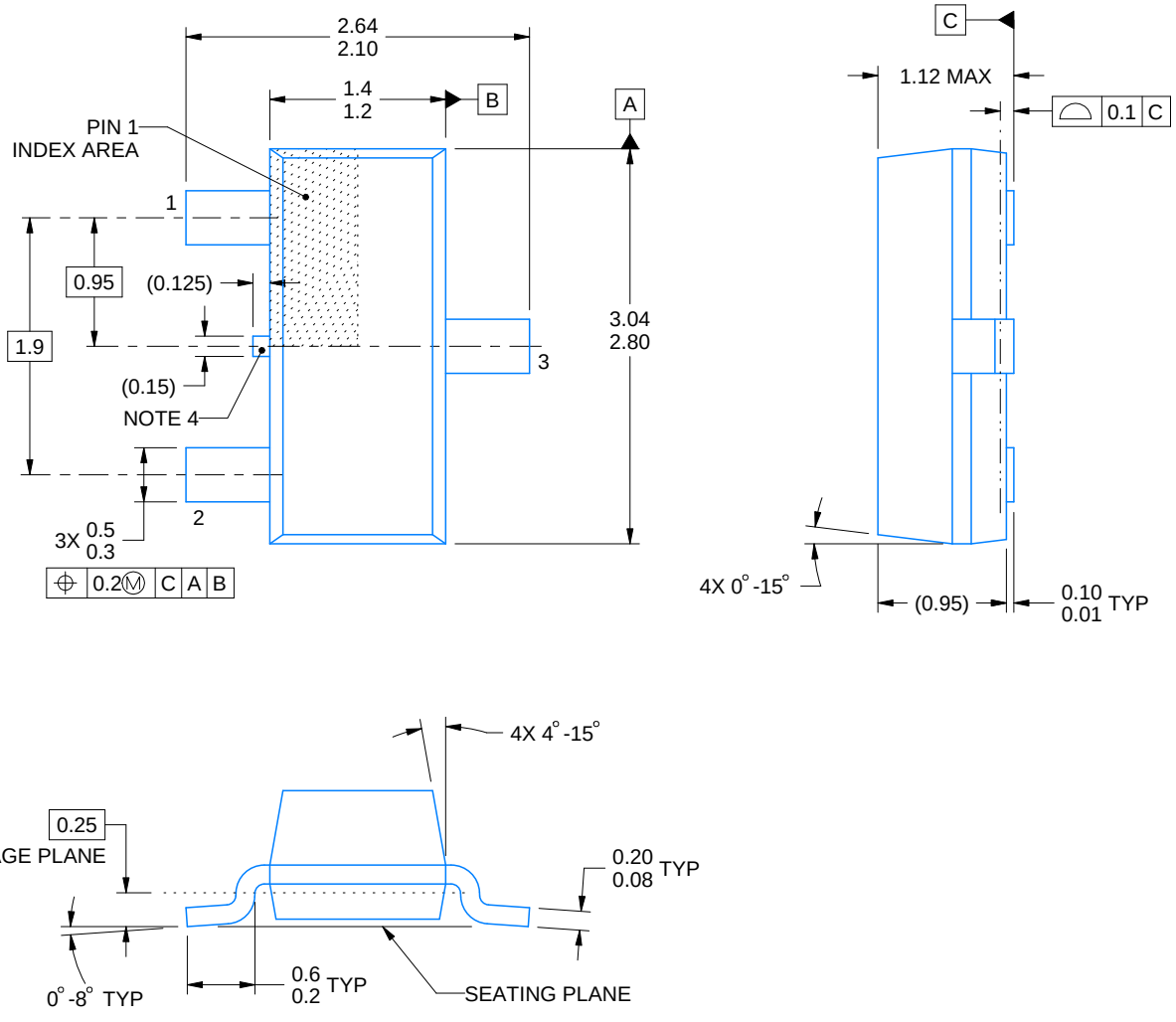
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CANFD24DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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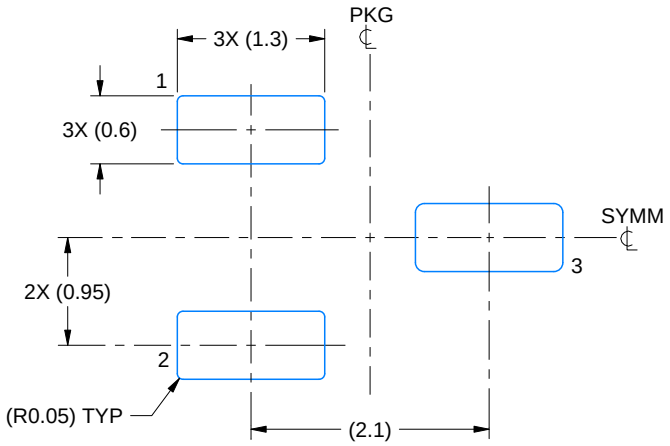
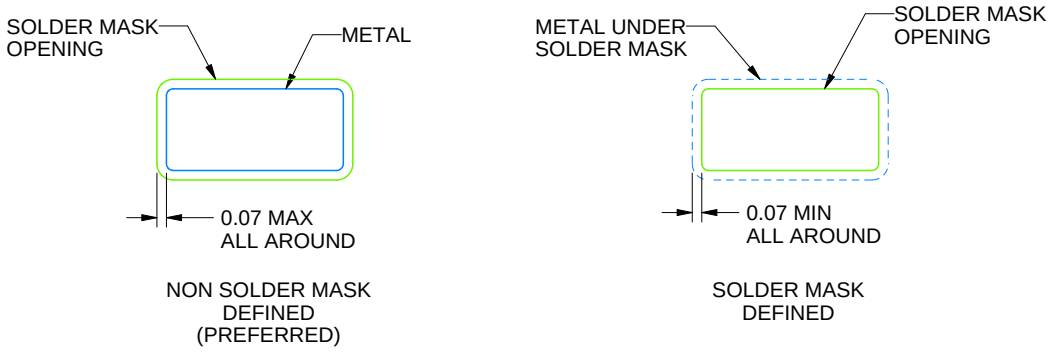
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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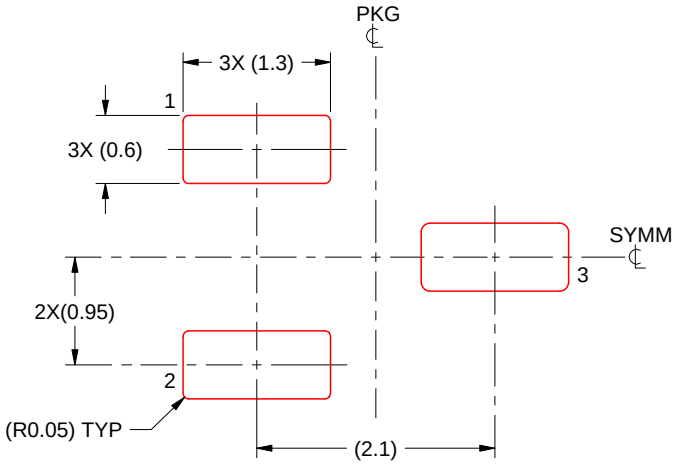
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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