TEXAS INSTRUMENTS ESD562
ZHCSUL9 – FEBRUARY 2024

ESD562 采用 SOT-23 封装的 12V 双向 ESD 保护

1 特性

- IEC 61000-4-5 浪涌保护：
  - 3.5A (8/20μs)
- IEC 61000-4-2 ESD 保护：
  - ±22kV 接触放电
  - ±30kV 空气间隙放电
- 12V 工作电压
- IO 电容：
  - 1.5pF（典型值）
- 双向极性，支持正负电压摆幅
- 双通道器件通过单个元件提供全面的 ESD 保护
- 小型引线式 SOT-23 可实现低成本的自动光学检测 (AOI)
- IO 电容：1.5

2 应用

- 终端设备：
  - 工厂自动化和控制
  - 楼宇自动化
  - 电网基础设施
  - HVAC 系统
  - 安全系统
- 接口：
  - RS-485
  - RS-422

3 说明

ESD562 是一款双向 ESD 保护二极管，用于 RS-485 和 RS-422 接口保护。ESD562 的额定 ESD 冲击消散值超出了 IEC 61000-4-2 国际标准所规定的最高水平（±22kV 接触放电，±30kV 空气间隙放电）。根据 IEC 61000-4-5 标准，该器件可以钳制峰值脉冲电流高达 3A 的 8/20μs 浪涌。

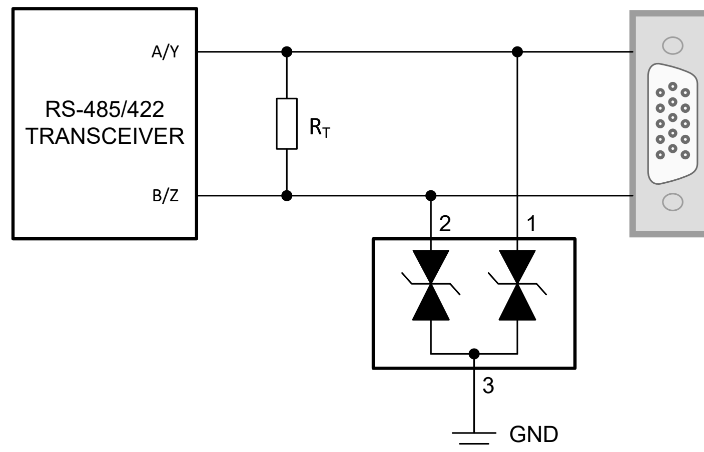
该器件具有 1.5pF（典型值）的 IO 电容，可实现高速接口保护。正向和负向的低钳位电压有助于保护系统免受瞬态事件的影响。这种保护对于对稳健性和可靠性要求很高的工业系统至关重要。

ESD562 采用小型引线式 SOT-23 (DBZ) 封装。

封装信息

器件型号	封装(1)	封装尺寸(2)
ESD562	DBZ（SOT-23，3）	2.92mm × 2.37mm

(1) 有关更多信息，请参阅 节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

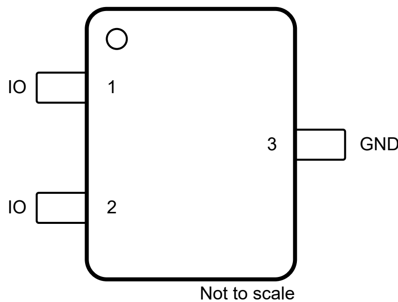

图 4-1. ESD562 DBZ Package, 3-Pin SOT-23 (Top View)

表 4-1. Pin Functions for ESD562

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	Surge and ESD protected IO
GND	3	GND	Ground. Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, GND = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Surge (t_p 8/20µs) Peak Pulse Power at 25 °C		84	W
I_{PP}	IEC 61000-4-5 Surge (t_p 8/20µs) Peak Pulse Current at 25°C		3.5	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±22000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage between any 2 pins	-12		12	V
T_A	Operating Free Air Temperature	-40		125	°C

5.5 Thermal Information

THERMAL METRIC[1]		ESD562	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	250.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	136.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.6 Electrical Characteristics

At T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50nA	-12		12	V
$I_{LEAKAGE}$	Leakage current at V_{RWM}	V_{IO} = ±12V, I/O to GND		10	50	nA
V_{BR}	Breakdown Voltage, IO to GND and GND to IO[(1)]	I_{IO} = ±1mA	13.2		18	V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20µs[(2)]	I_{PP} = ±3A, I/O to GND			21	V
	TLP clamping voltage, t_p = 100ns[(3)]	I_{PP} = 16A (100ns TLP), I/O to GND		22		V
	TLP clamping voltage, t_p = 100ns[(3)]	I_{PP} = 16A (100ns TLP), GND to I/O		22		V
V_{HOLD}	Holding Voltage, I/O to GND[(4)]	TLP, IO to GND or GND to IO		16.5		V
C_{Line}	Line capacitance, IO to GND	V_{IO} = 0V, f = 1MHz		1.5		pF

(1) V_{BR} is defined as the voltage obtained at 1mA when sweeping the voltage up, before the devices latches into the snapback state

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5.7 Typical Characteristics

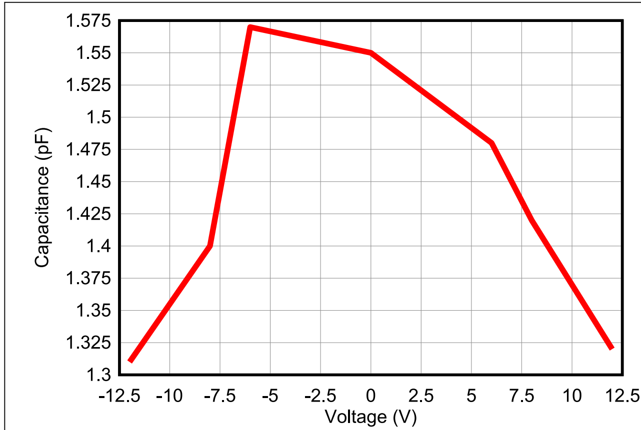

图 5-1. Capacitance vs. Bias Voltage

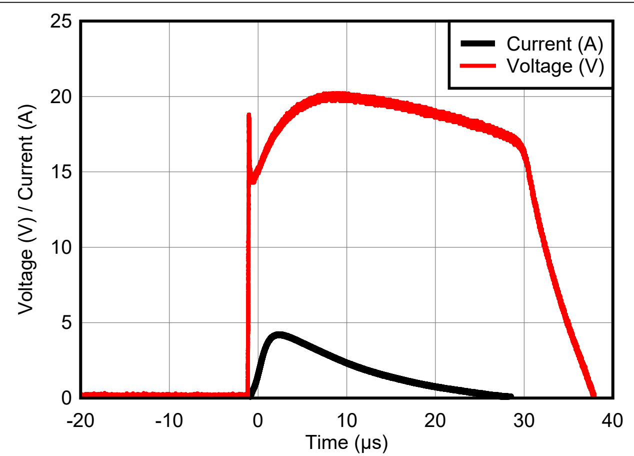

图 5-2. 8/20 µs Surge Response

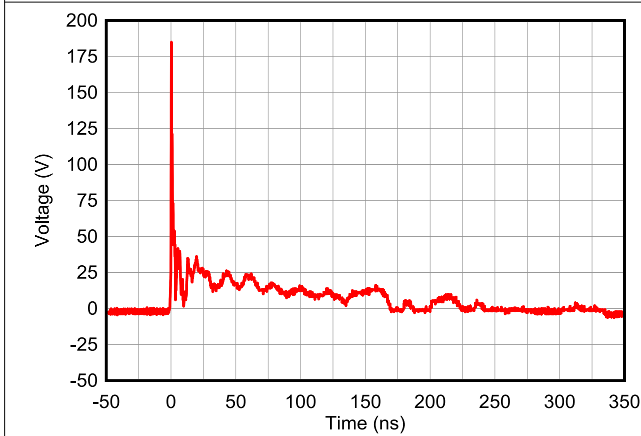

图 5-3. +8kV Clamped IEC Waveform

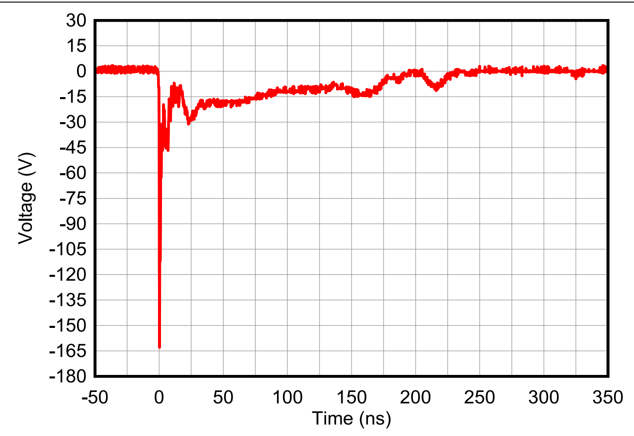

图 5-4. -8kV Clamped IEC Waveform

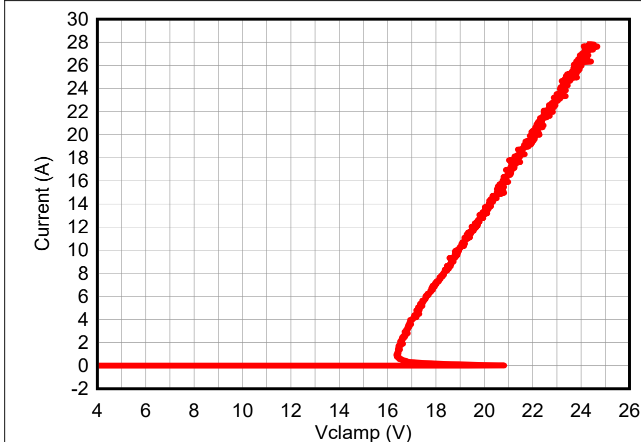

图 5-5. Positive TLP Curve

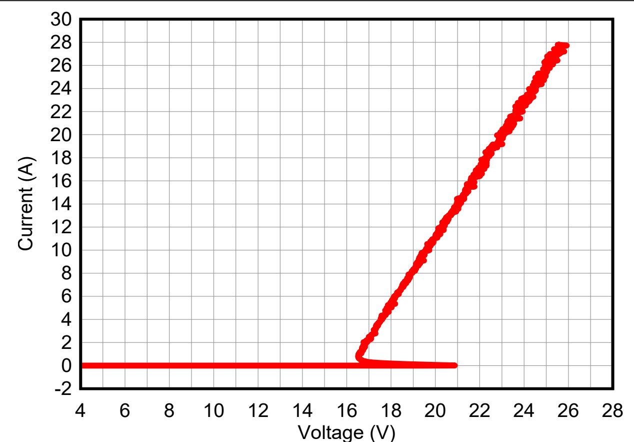

图 5-6. Negative TLP Curve

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5.7 Typical Characteristics (continued)

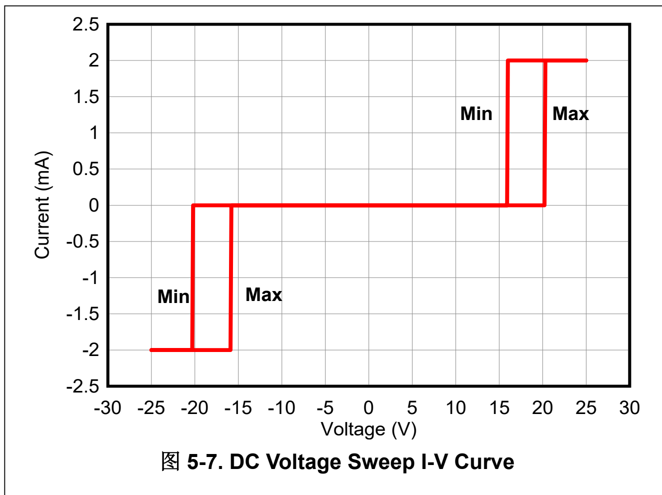

图 5-7. DC Voltage Sweep I-V Curve

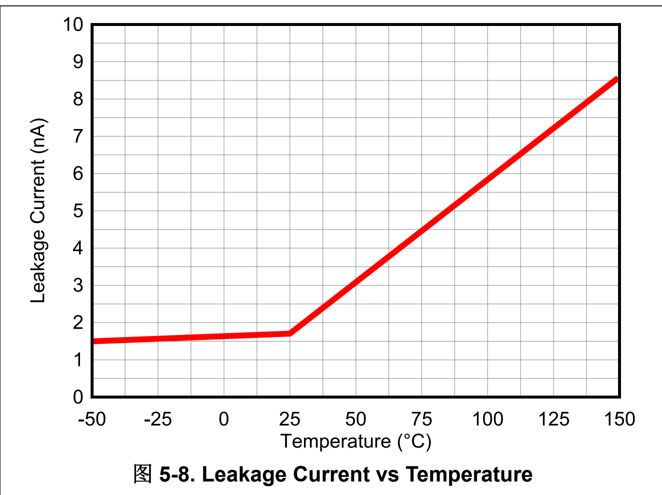

图 5-8. Leakage Current vs Temperature

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6 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD562 is a diode type TVS that provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide* for details.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Packaging and Layout Guide*
- Texas Instruments, *TI's IEC 61000-4-x Testing application note*
- Texas Instruments, *ESD Layout Guide user's guide*
- Texas Instruments, *ESD Protection Diodes EVM user's guide*
- Texas Instruments, *Generic ESD Evaluation Module user's guide*
- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet user's guide*

7.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.4 Trademarks

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7.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD562DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	36X8	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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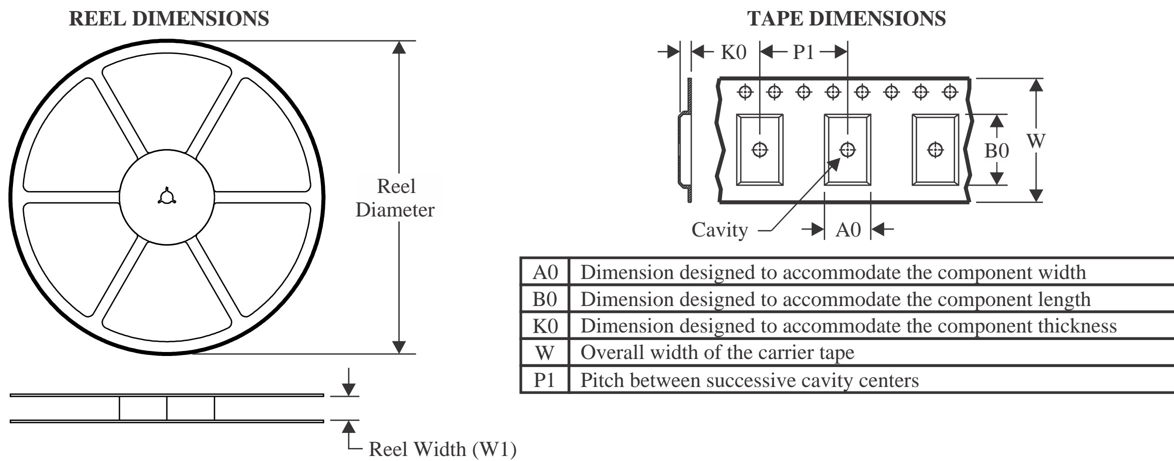
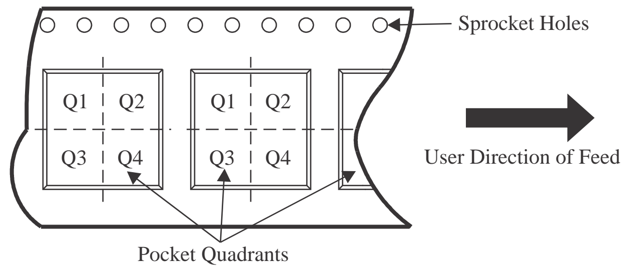
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

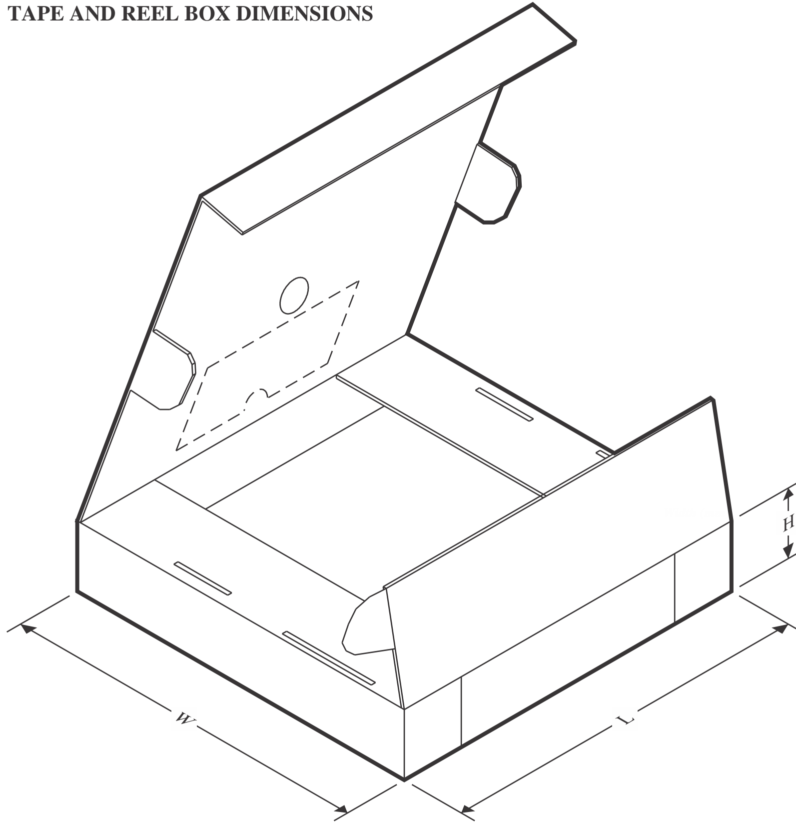
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD562DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



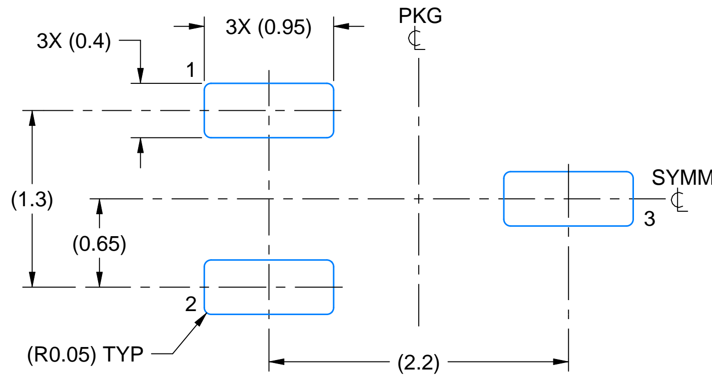
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD562DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

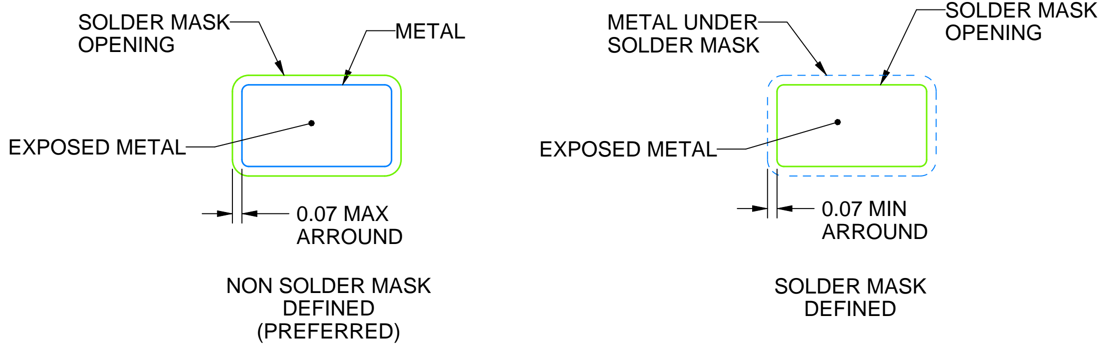
4220745/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

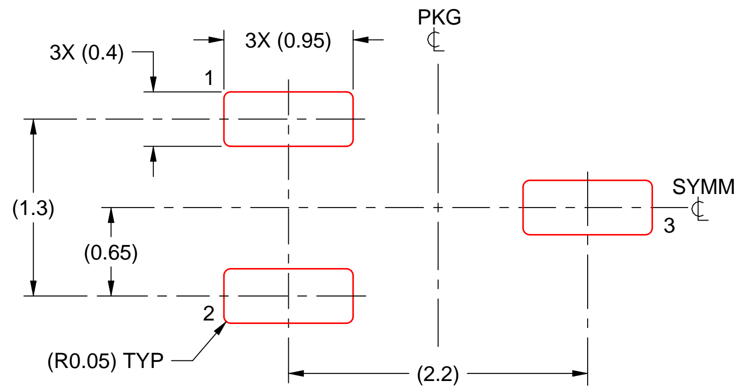


SOLDER MASK DETAILS

4220745/F 11/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

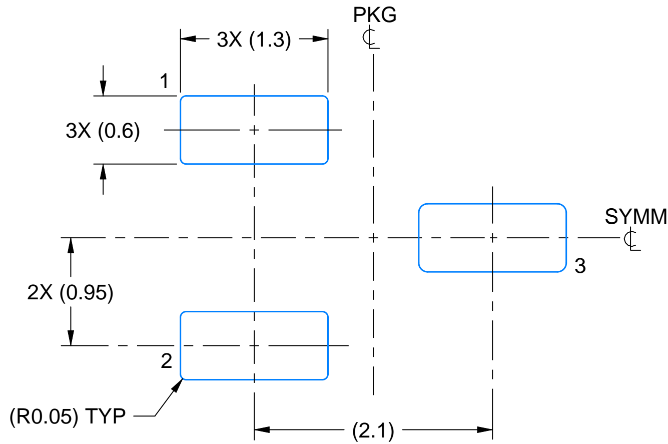
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

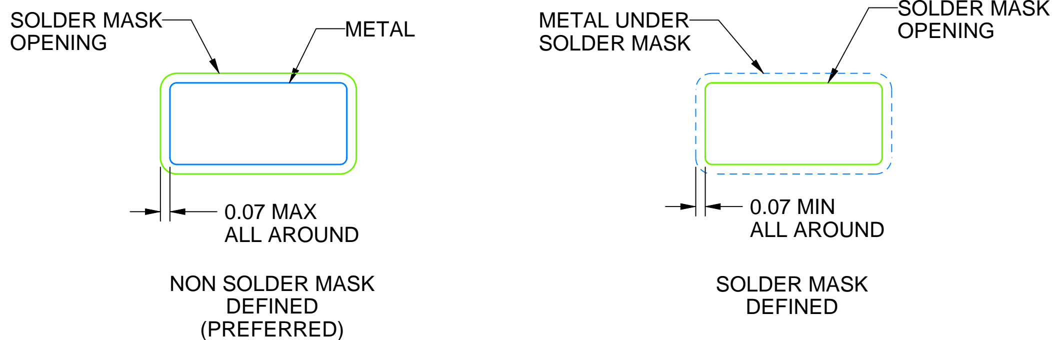
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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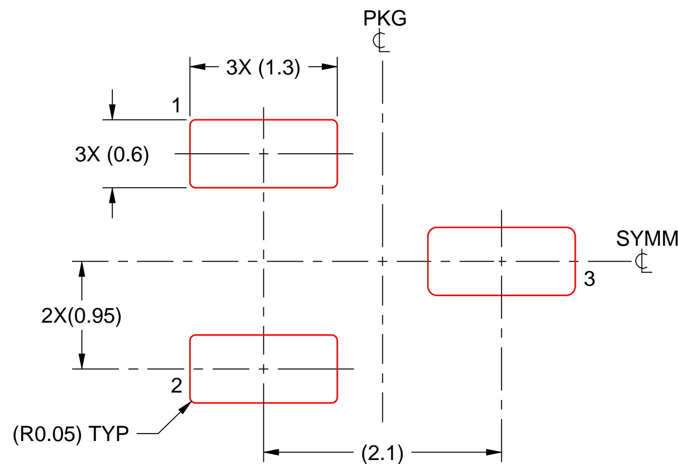
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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