GD65232、GD75232 多路 RS-232 驱动器和接收器

1 特性

- 单芯片，可轻松连接 UART 与 IBM PC/AT 串行端口连接器及兼容接口
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 设计支持高达 120kbits 的数据速率
- 引脚排列与 SN75C185 和 SN75185 兼容
- ESD 性能经测试符合 JESD 22：HBM：1500V、CDM：500V、MM：200V

2 应用

- 端子
- 调制解调器
- 计算机
- 有线网络
- 数据中心和企业级计算
- 手持设备

3 说明

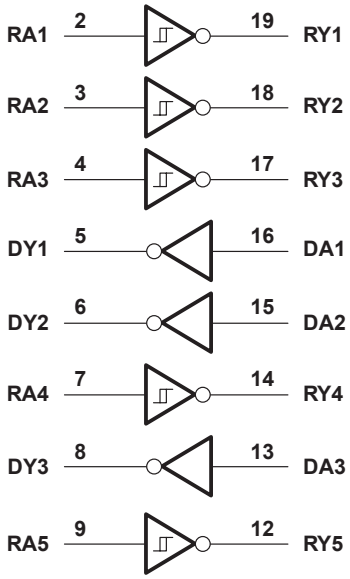
GD65232 和 GD75232 分别整合了来自德州仪器 (TI) 贸易标准 SN75188 和 SN75189 双极四路驱动器和接收器的三个驱动器和五个接收器。引脚排列与 SN75C185 的直通式设计相匹配，可减少器件数量，减少所需的布板空间，并轻松实现 UART 与 IBM™ PC/AT 串行端口连接器及兼容接口的互连。与 SN75C185 相比，GD65232 和 GD75232 的双极电路和处理过程以静态功率和外部无源器件为代价，为这一功能提供了一种坚固耐用的低成本解决方案。

GD65232 和 GD75232 符合 TIA/EIA-232-F 和 ITU（原 CCITT）V.28 标准的要求。这些标准适用于以高达 20kbits 的信号传输速率在主机与外设之间进行的数据交换。这些器件的开关速度非常快，足以在容性负载较低（电缆较短）时支持高达 120kbits 的速率。除非设计人员能够对电缆和两端接口电路进行设计上的控制，否则无法期望在更高信号传输速率下实现互操作性。要在高达 120kbits 的信号传输速率下实现互操作性，建议使用 TIA/EIA-423-B (ITU V.10) 和 TIA/EIA-422-B (ITU V.11) 标准。

封装信息

器件型号	封装(1)	封装尺寸(2)
GD65232 GD75232	SSOP（DB，20）	7.2mm x 7.8mm
	SOIC（DW，20）	12.8mm x 10.3mm
	PDIP（N，20）	24.33mm x 9.4mm
	TSSOP（PW，20）	6.5mm x 6.4mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

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4 Pin Configuration and Functions

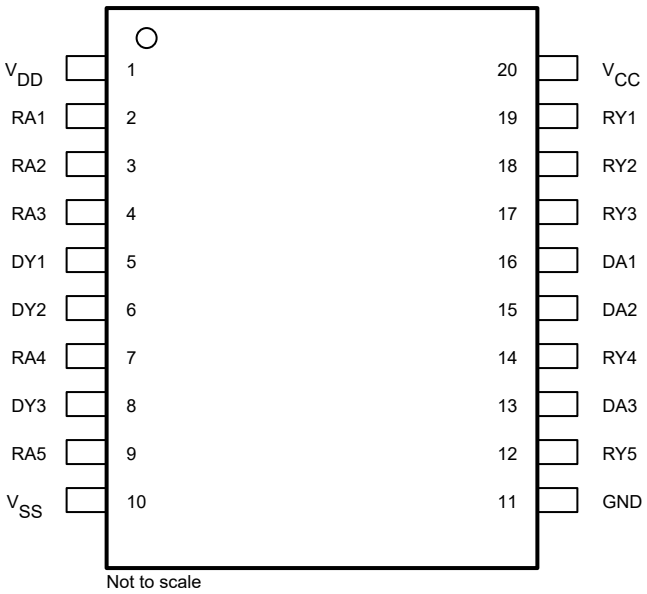


图 4-1. DB, DW, N, OR PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{DD}	1	–	Positive RS232 Power Supply
RA1	2	I	RS232 Input
RA2	3	I	RS232 Input
RA3	4	I	RS232 Input
DY1	5	O	RS232 Output
DY2	6	O	RS232 Output
RA4	7	I	RS232 Input
DY3	8	O	RS232 Output
RA5	9	I	RS232 Input
V_{SS}	10	–	Negative RS232 Power Supply
GND	11	–	Ground
RY5	12	O	TTL Output
DA3	13	I	TTL Input
RY4	14	O	TTL Output
DA2	15	I	TTL Input
DA1	16	I	TTL Input
RY3	17	O	TTL Output
RY2	18	O	TTL Output
RY1	19	O	TTL Output
V_{CC}	20	–	Device Power Supply for TTL

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage (see (2))		10	V
V_{DD}			15	V
V_{SS}			−15	V
V_I	Input voltage range, Driver	−15	7	V
	Input voltage range, Receiver	−30	30	V
V_O	Driver output voltage range	−15	15	V
I_{OL}	Receiver low-level output current		20	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the network ground terminal

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD	Supply voltage (see (1))		7.5	9	15	V
VSS	Supply voltage (see (1))		−7.5	−9	−15	V
V_{CC}	Supply voltage (see (1))		4.5	5	5.5	V
V_{IH}	High-level input voltage (driver only)		1.9			V
V_{IL}	Low-level input voltage (driver only)				0.8	V
I_{OH}	High-level output current	Driver			−6	mA
		Receiver			−0.5	
I_{OL}	Low-level output current	Driver			6	mA
		Receiver			16	
T_A	Operating free-air temperature	GD65232	−40		85	°C
		GD75232	0		70	

(1) When powering up the GD65232 and GD75232, the following sequence should be used:

- V_{SS}, V_{DD}, V_{CC}, I/Os

Applying V_{CC} before V_{DD} may allow large currents to flow, causing damage to the device. When powering down the GD65232 and GD75232, the reverse sequence should be used

5.3 Thermal Information

THERMAL METRIC[1]		DB (SSOP)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.0	73.0	59.8	97.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	40.2	39.1	41.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.0	45.7	36.1	59.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	12.8	18.3	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.3	45.0	35.7	58.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Supply Currents over Recommended Operating Free-air Temperature Range

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS				MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9V	No load	V_{DD} = 9V	V_{SS} = −9V		15	mA
				V_{DD} = 12V	V_{SS} = −12V		19	
				V_{DD} = 15V	V_{SS} = −15V		25	
		All inputs at 0.8V	No load	V_{DD} = 9V	V_{SS} = −9V		4.5	
				V_{DD} = 12V	V_{SS} = −12V		5.5	
				V_{DD} = 15V	V_{SS} = −15V		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9V	No load	V_{DD} = 9V	V_{SS} = −9V		−15	mA
				V_{DD} = 12V	V_{SS} = −12V		−19	
				V_{DD} = 15V	V_{SS} = −15V		−25	
		All inputs at 0.8V	No load	V_{DD} = 9V	V_{SS} = −9V		−3.2	
				V_{DD} = 12V	V_{SS} = −12V		−3.2	
				V_{DD} = 15V	V_{SS} = −15V		−3.2	
I_{CC}	Supply current from V_{CC}	All inputs at 5V	No load, V_{CC} = 5V		GD65232		38	mA
					GD75232		30	

5.5 Electrical Characteristics, Driver

over operating free-air temperature range V_{DD} = 9V, V_{SS} = −9V, V_{CC} = 5V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8V,	R_L = 3kΩ,	See 图 6-1	6	7.5		V
V_{OL}	Low-level output voltage (see (1))	V_{IH} = 1.9V,	R_L = 3kΩ,	See 图 6-1		−7.5	−6	V
I_{IH}	High-level input current	V_I = 5V,	See 图 6-2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See 图 6-2				−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see (2))	V_{IL} = 0.8V,	V_O = 0,	See Figure 1	−4.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2V,	V_O = 0,	See 图 6-1	4.5	12	19.5	mA
r_o	Output resistance (see (3))	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = −2V to 2V	300			Ω

(1) The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (that is, if −10V is maximum, the typical value is a more negative voltage).
(2) Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings,
(3) Test conditions are those specified by TIA/EIA-232-F and as listed above

5.6 Switching Characteristics, Driver

over operating free-air temperature range V_{CC} = 5V, V_{DD} = 12V, V_{SS} = −12V, T_A = 25°C (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3kΩ to 7kΩ,	C_L = 15pF,	See 图 6-3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3kΩ to 7kΩ,	C_L = 15pF,	See 图 6-3		75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3kΩ to 7kΩ	C_L = 15pF,	See 图 6-3		60	100	ns
			C = 2500 pF,	See 图 6-3 and (1)		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output	R_L = 3kΩ to 7kΩ	C_L = 15pF,	See 图 6-3		40	75	ns
			C_L = 2500pF,	See 图 6-3 and (1)		1.5	2.5	μs

(1) Measured between ±3V and ±3V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

5.7 Electrical Characteristics, Receiver

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	T_A = 25°C, See 图 6-5			1.75	1.9	2.3	V
		T_A = 0°C to 70°C, See 图 6-5			1.55		2.3	
V_{IT-}	Negative-going input threshold voltage				0.75	0.97	1.25	V
V_{hys}	Input hysteresis voltage (VIT+ − VIT−)				0.5			V
V_{OH}	High-level output voltage	I_{OH} = −0.5mA	V_{IH} = 0.75V		2.6	4	5	V
			Inputs open		2.6			
V_{OL}	Low-level output voltage	I_{OL} = 10mA, V_I = 3V				0.2	0.45	V
I_{IH}	High-level input current	V_I = 25V, See 图 6-5		GD65232	3.6		11	mA
				GD75232	3.6		8.3	
		V_I = 3V, See 图 6-5			0.43			
I_{IL}	Low-level input current	V_I = −25V, 图 6-5		GD65232	−3.6		−11	mA
				GD75232	−3.6		−8.3	
		V_I = −3V, See 图 6-5			−0.43			
I_{OS}	Short-circuit output current	See 图 6-4				−3.4	−12	mA

(1) All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = −9 V.

5.8 Switching Characteristics, Receiver

over operating free-air temperature range V_{CC} = 5V, V_{DD} = 12V, V_{SS} = −12V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50pF, RL = 5kΩ, See 图 6-6		107	250	ns
t_{PHL}	Propagation delay time, high- to low-level output			42	150	ns
t_{TLH}	Transition time, low- to high-level output			175	350	ns
t_{THL}	Transition time, high- to low-level output			16	60	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15pF, RL = 1.5kΩ, See 图 6-6		100	160	ns
t_{PHL}	Propagation delay time, high- to low-level output			60	100	ns
t_{TLH}	Transition time, low- to high-level output			90	175	ns
t_{THL}	Transition time, high- to low-level output			15	50	ns

5.9 Typical Characteristics Driver

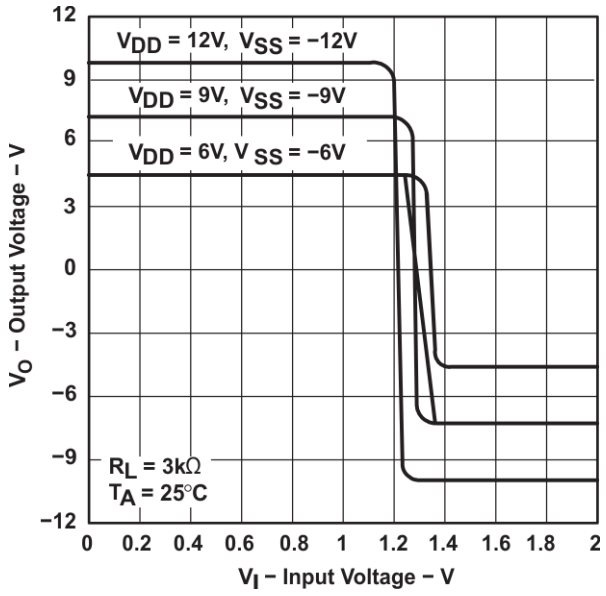


图 5-1. Voltage Transfer Characteristics

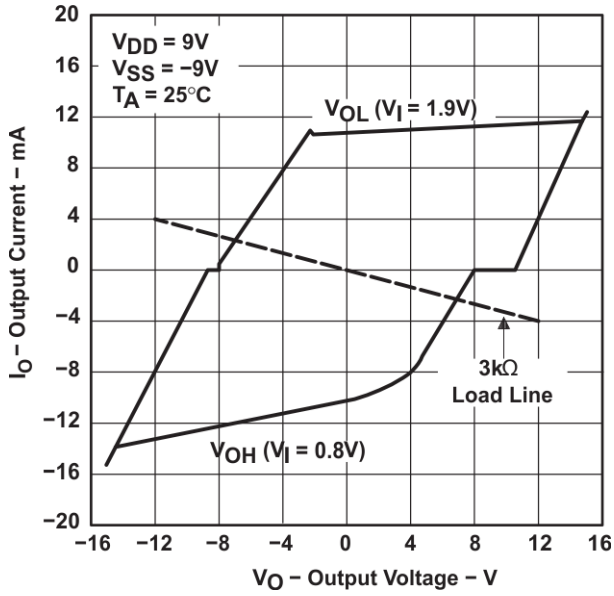


图 5-2. Output Current vs Output Voltage

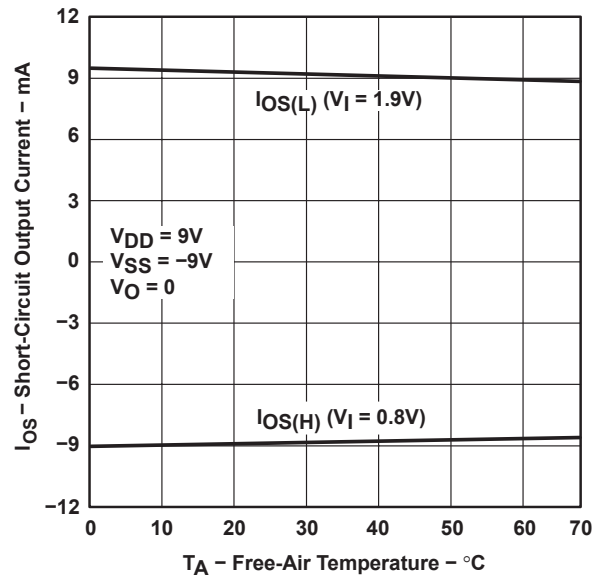


图 5-3. Short-Circuit Output Current vs Free-Air Temperature

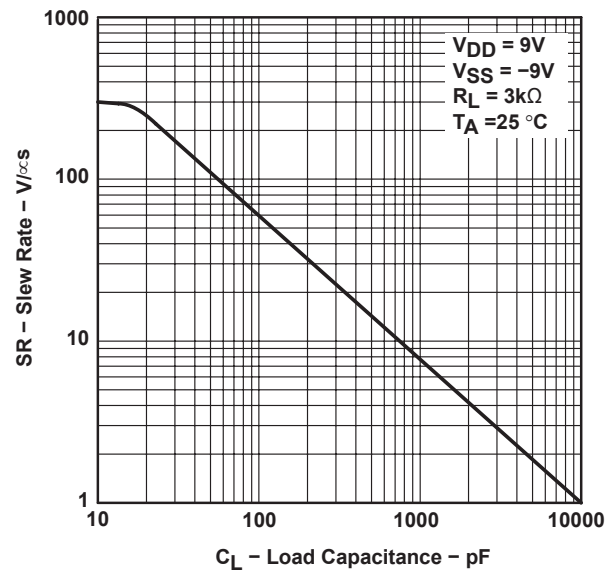


图 5-4. Slew Rate vs Load Capacitance

5.10 Typical Characteristics Receiver

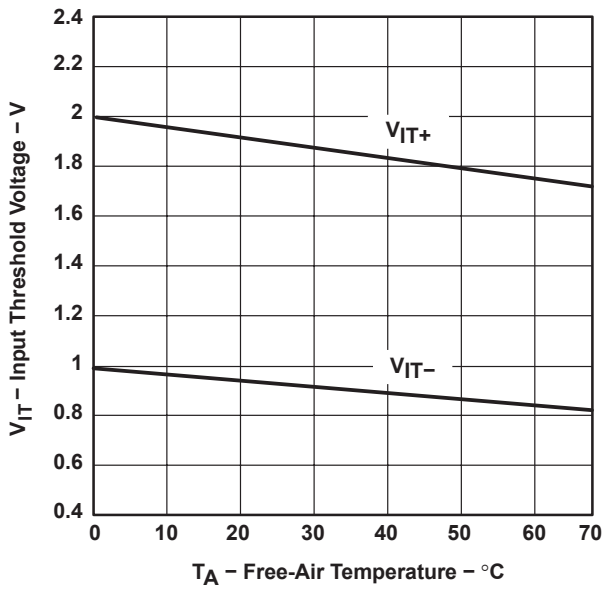


图 5-5. Input Threshold Voltage vs Free-Air Temperature

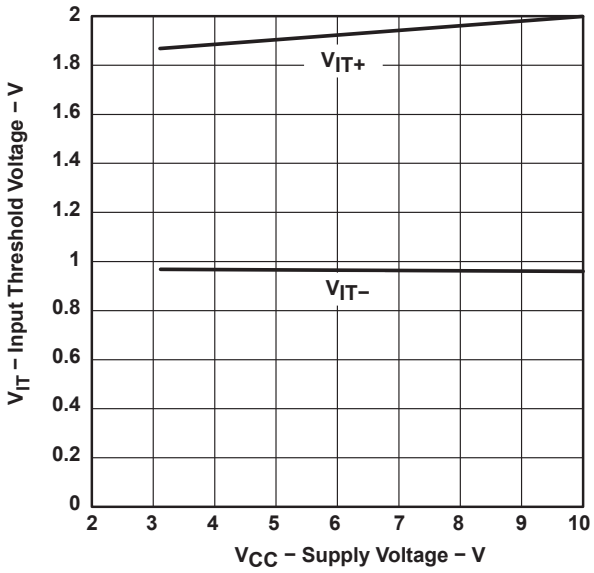
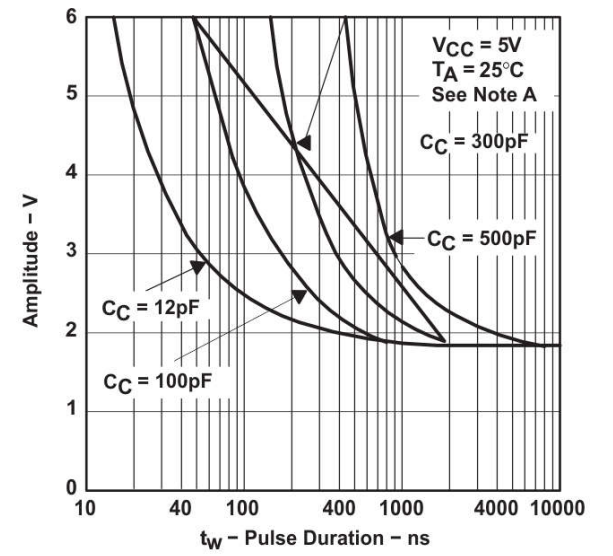


图 5-6. Input Threshold Voltage vs Supply Voltage



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0V, does not cause a change of the output level.

图 5-7. Noise Rejection

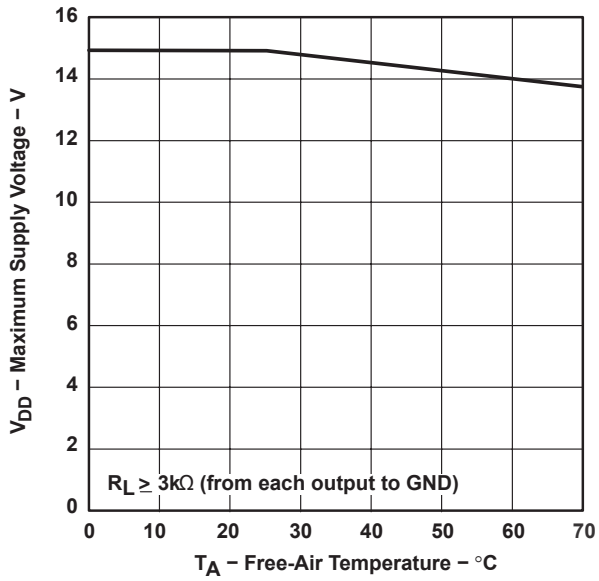


图 5-8. Maximum Supply Voltage vs Free-Air Temperature

6 Parameter Measurement Information

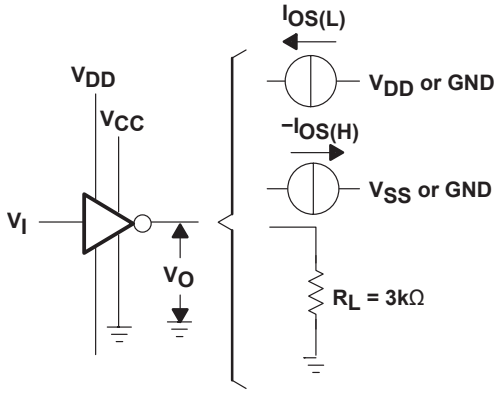


图 6-1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

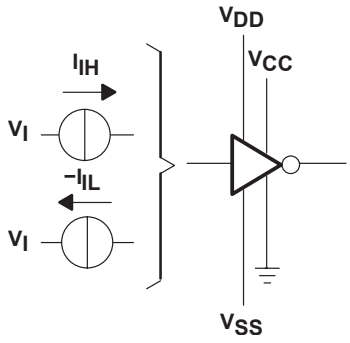
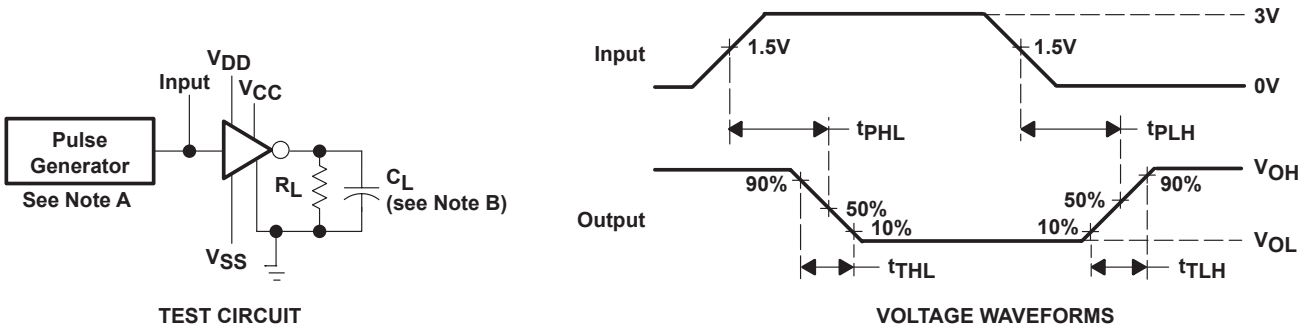


图 6-2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. The pulse generator has the following characteristics: t_w = 25μs, PRR = 20kHz, Z_O = 50Ω , t_r = t_f < 50ns.
B. C_L includes probe and jig capacitance.

图 6-3. Driver Test Circuit and Voltage Waveforms

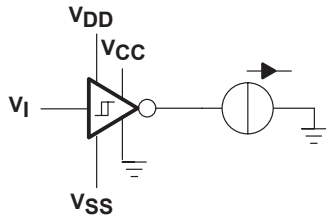


图 6-4. Receiver Test Circuit for I_{OS}

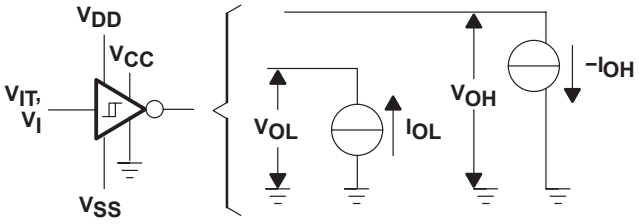
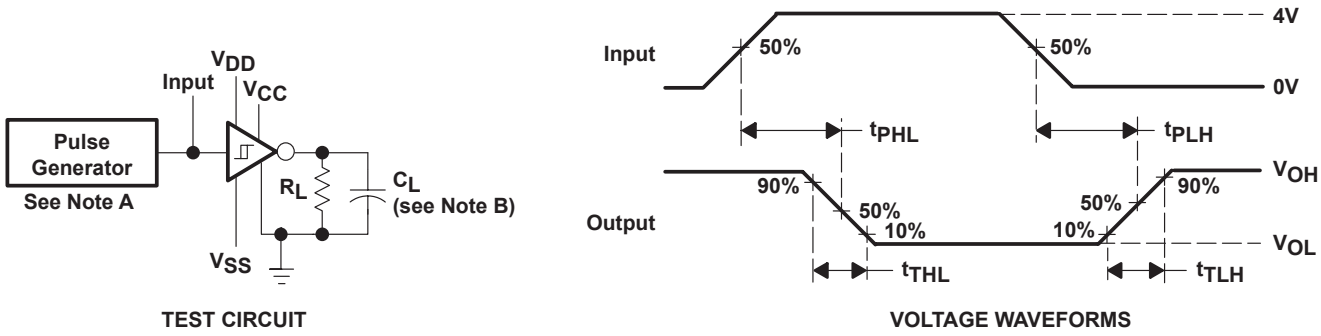


图 6-5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



NOTES: A. The pulse generator has the following characteristics: t_W = 25µs, PRR = 20kHz, Z_O = 50Ω, t_r = t_f < 50ns.
B. C_L includes probe and jig capacitance.

图 6-6. Receiver Propagation and Transition Times

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

Diodes placed in series with the VDD and VSS leads protect the GD65232 and GD75232 in the fault condition in which the device outputs are shorted to ±15V and the power supplies are at low and provide low-impedance paths to ground, see 图 7-1.

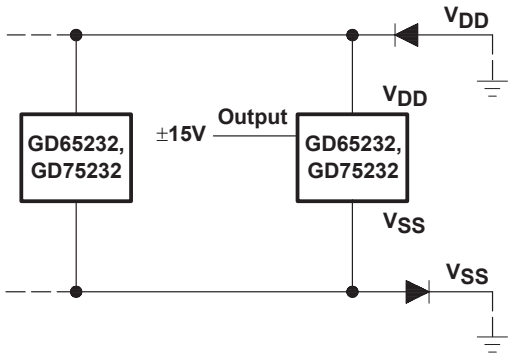


图 7-1. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

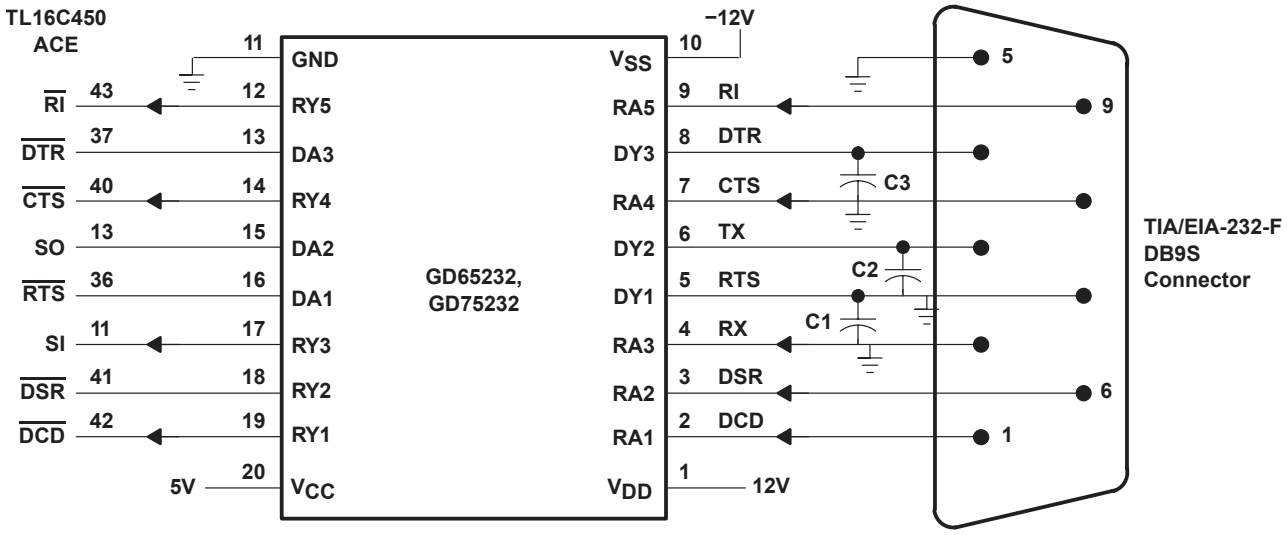
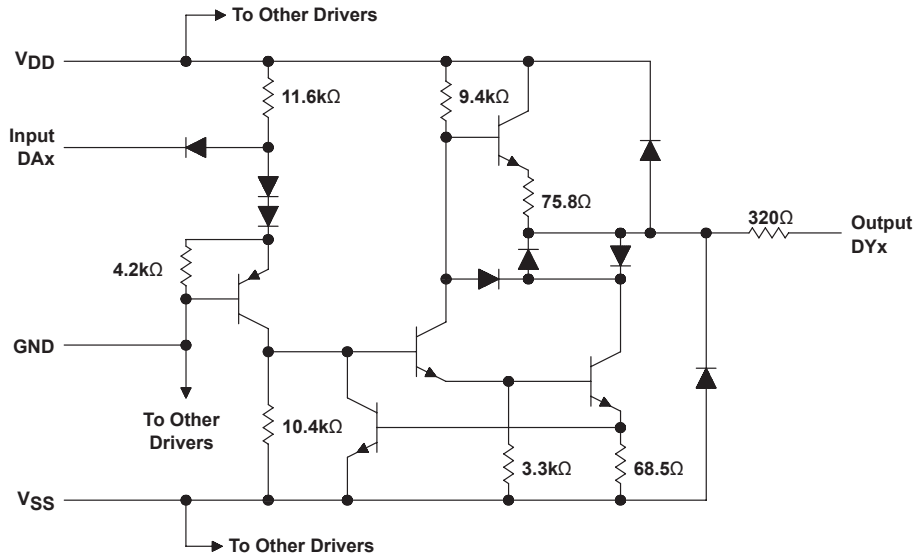


图 7-2. Typical Connection

7.2 Schematic



Resistor values shown are nominal.

图 7-3. Schematic (each driver)

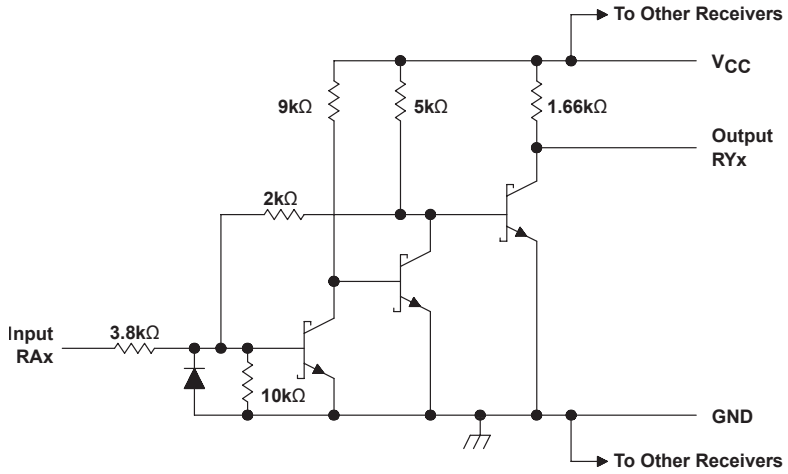


图 7-4. Schematic (each receiver)

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (August 2012) to Revision L (August 2024)	Page
• 通篇更改了表格、图和交叉参考的编号格式	1
• Added the *Thermal Information* table	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
GD65232DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	Samples
GD65232DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	Samples
GD65232PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GD65232	Samples
GD75232DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	GD75232N	Samples
GD75232PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	GD75232	Samples
GD75232PWRG4	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	0 to 70	GD75232	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

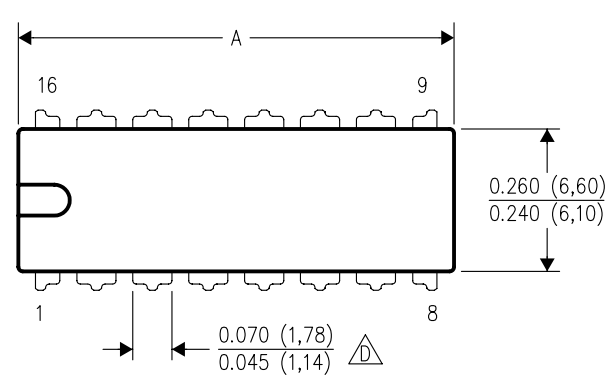
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

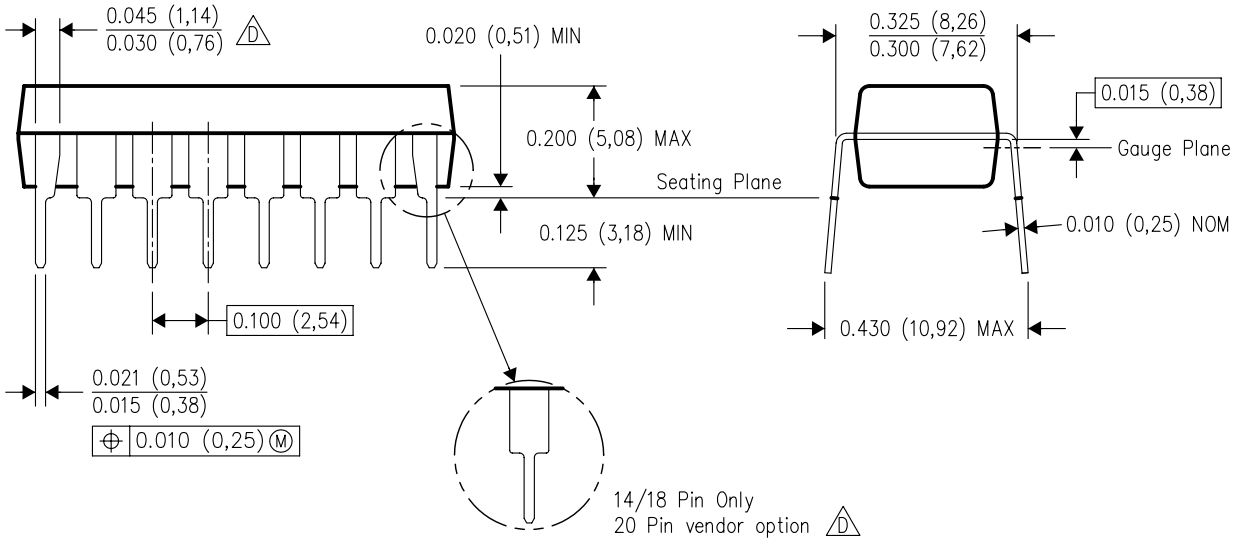
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

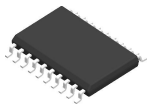


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

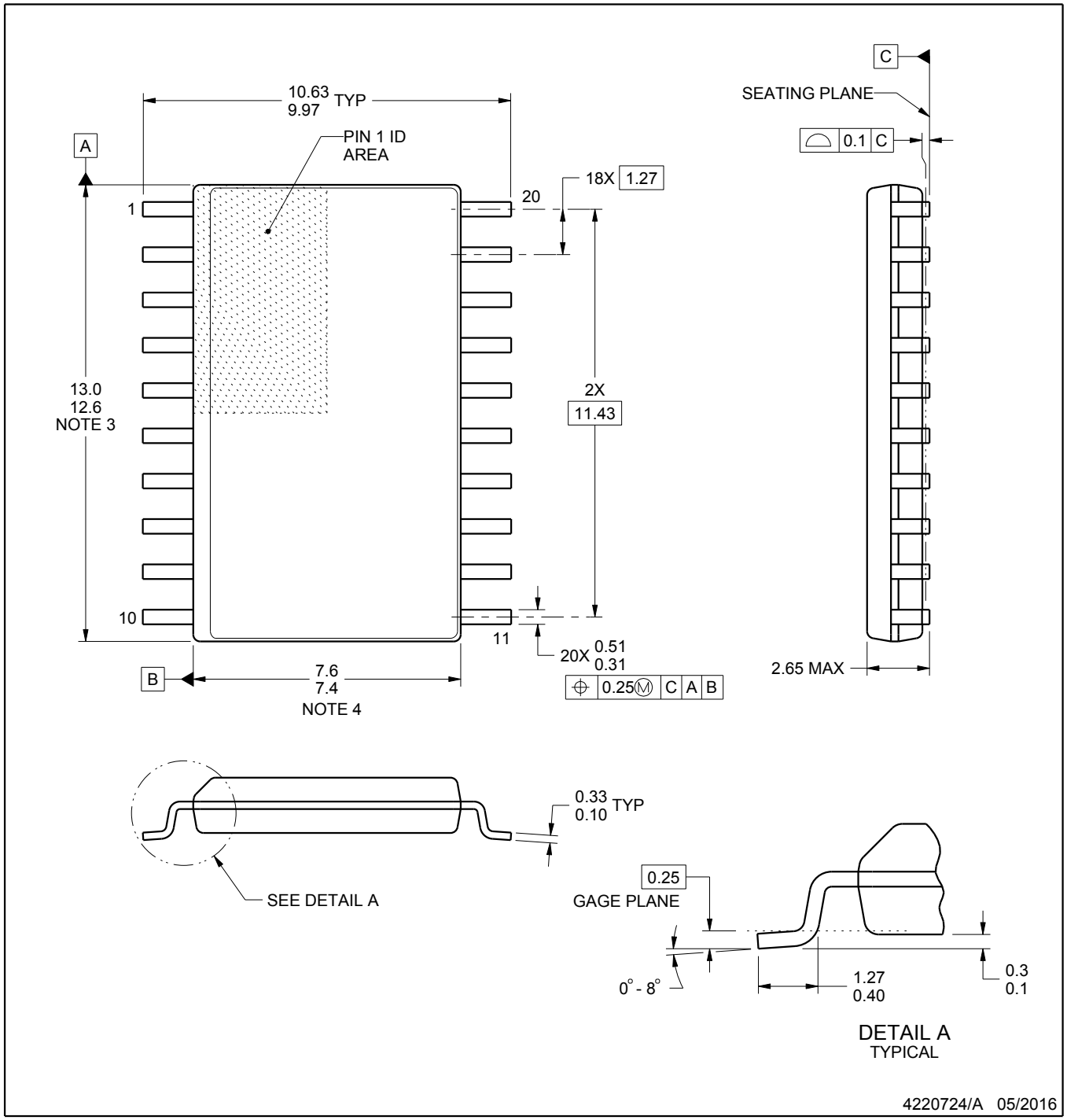


PACKAGE OUTLINE

DW0020A

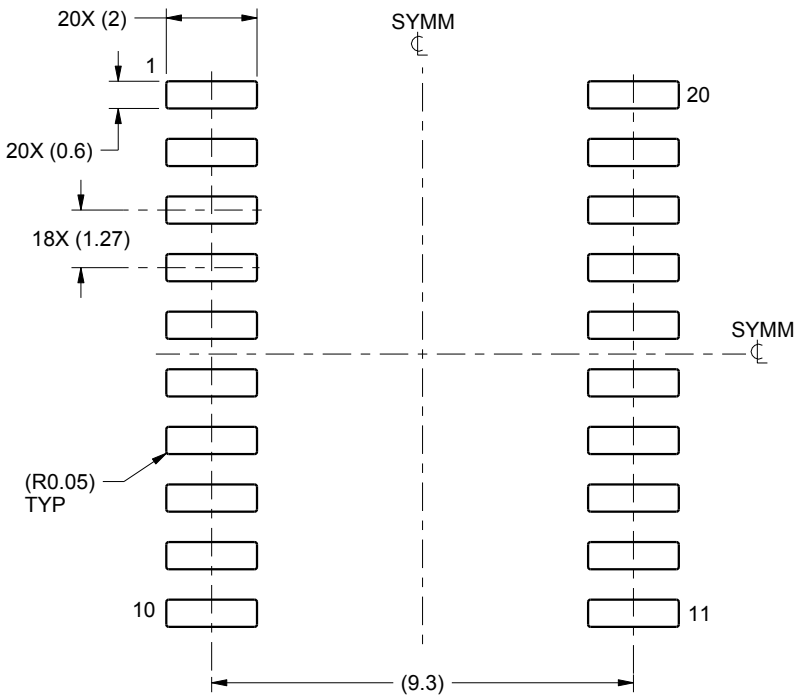
SOIC - 2.65 mm max height

SOIC

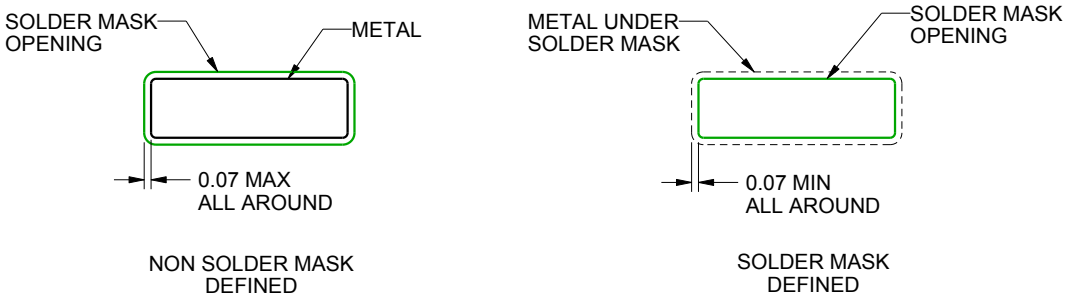


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

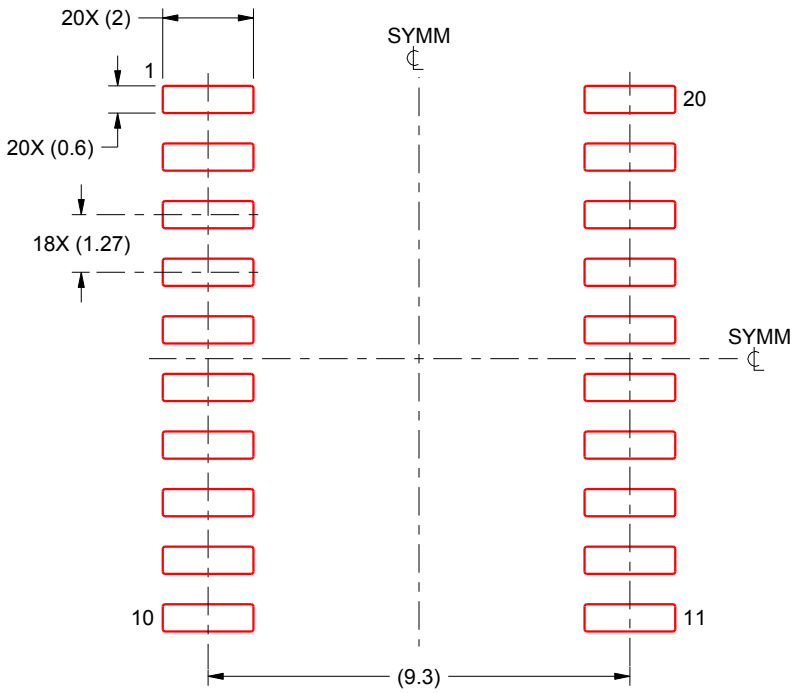


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

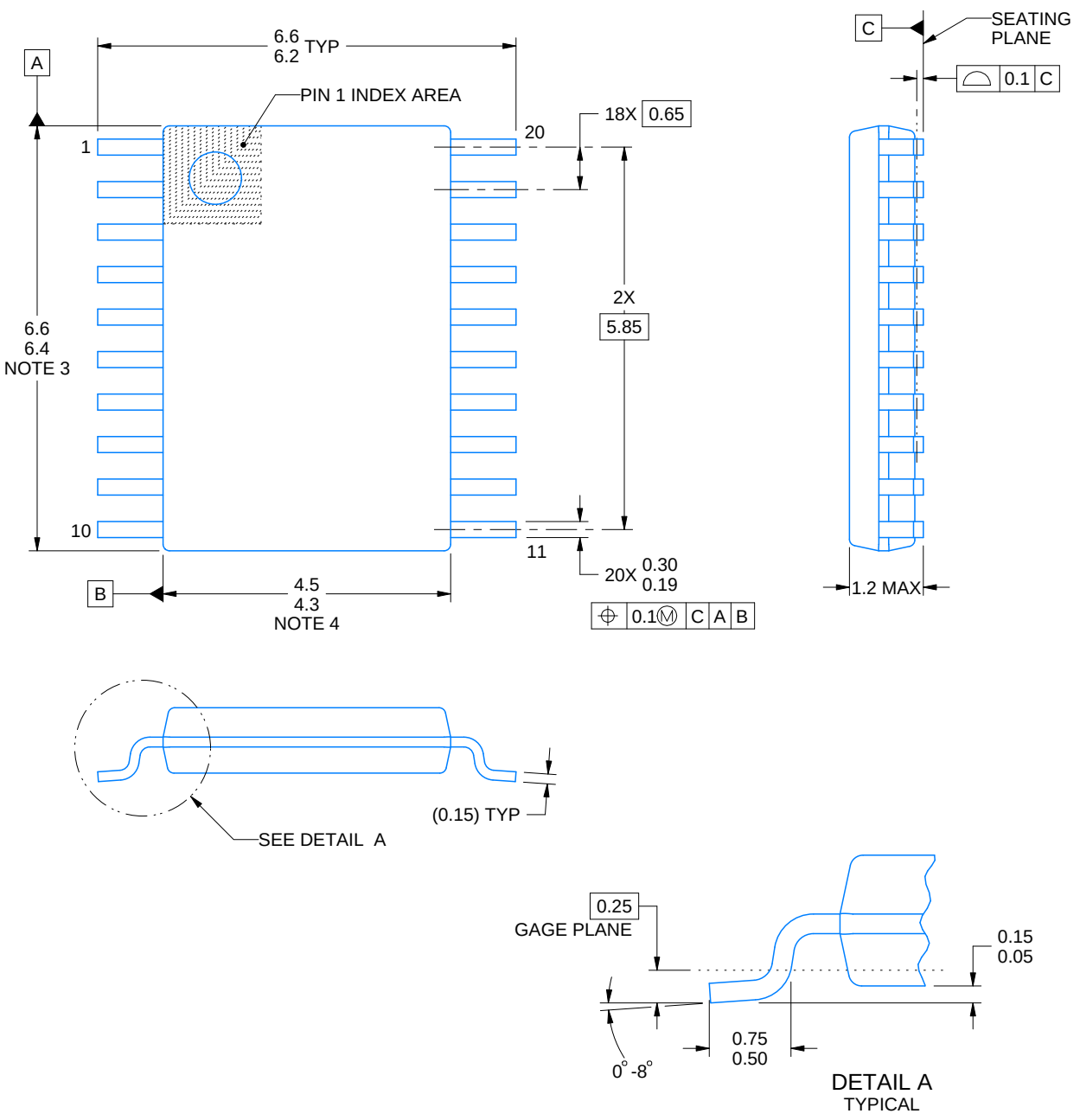
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

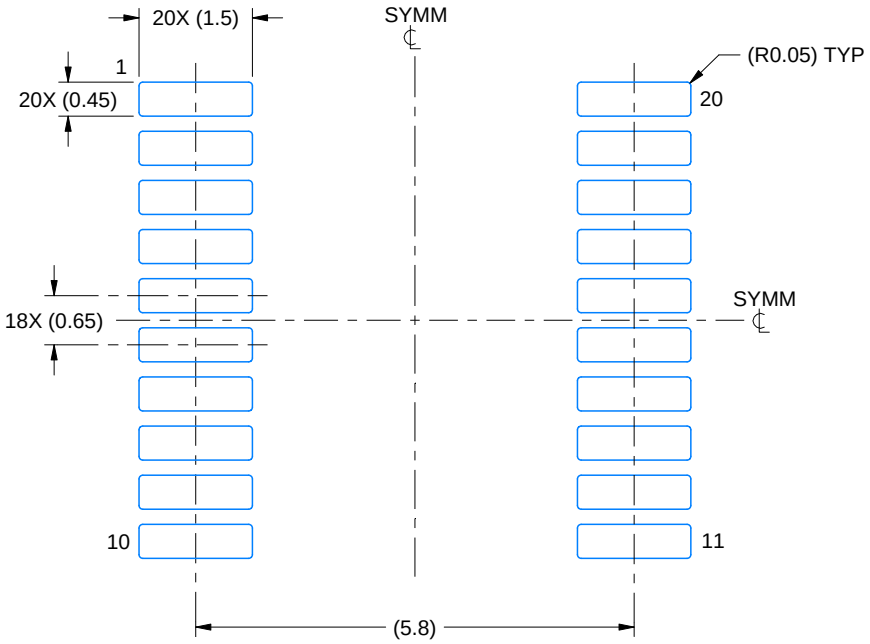
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



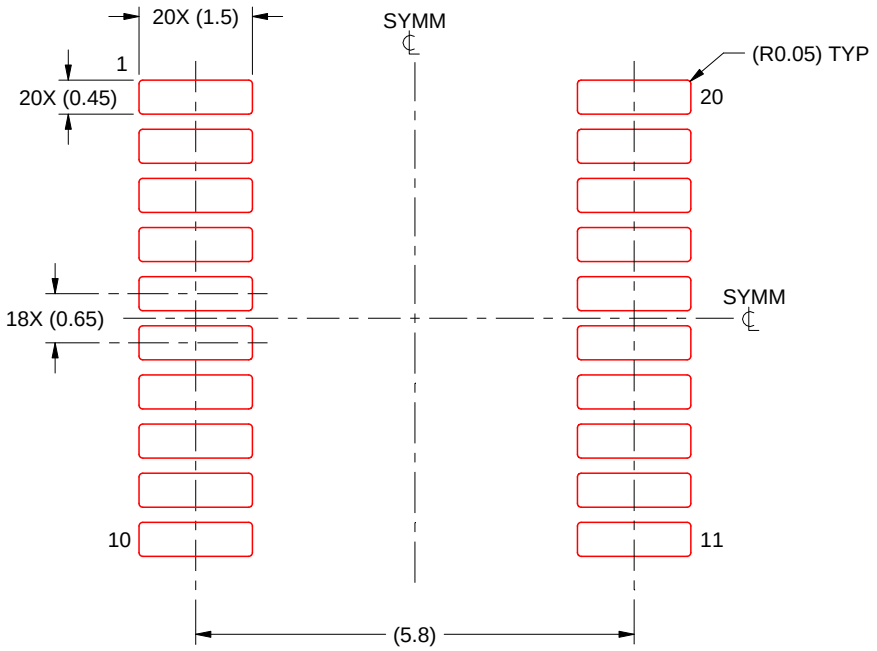
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

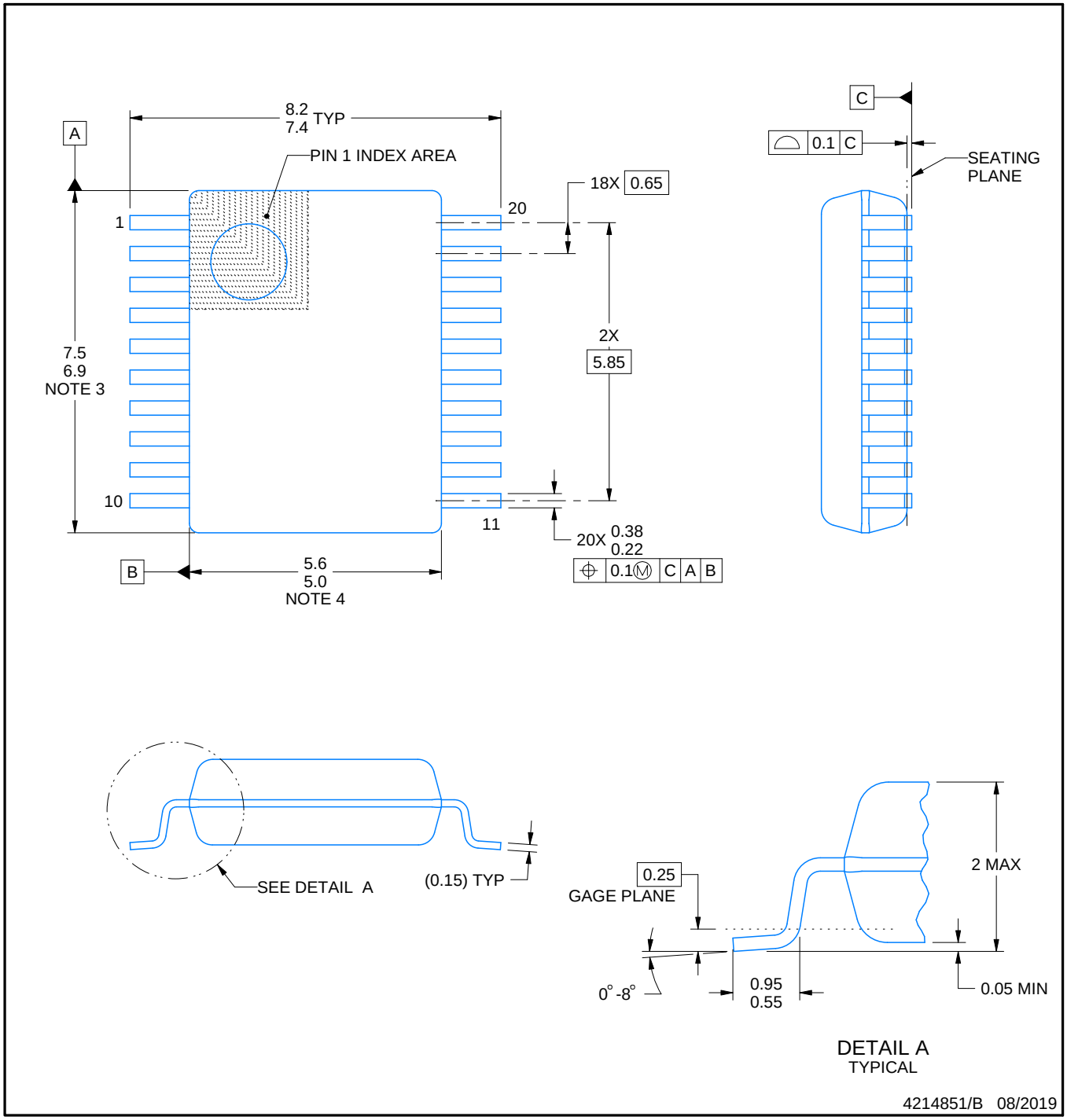
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

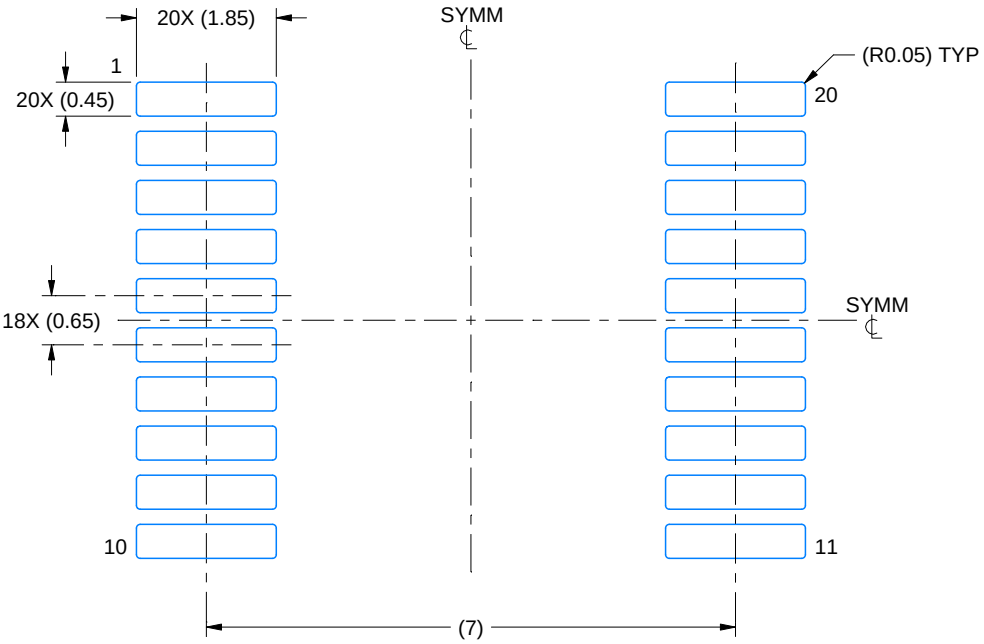
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

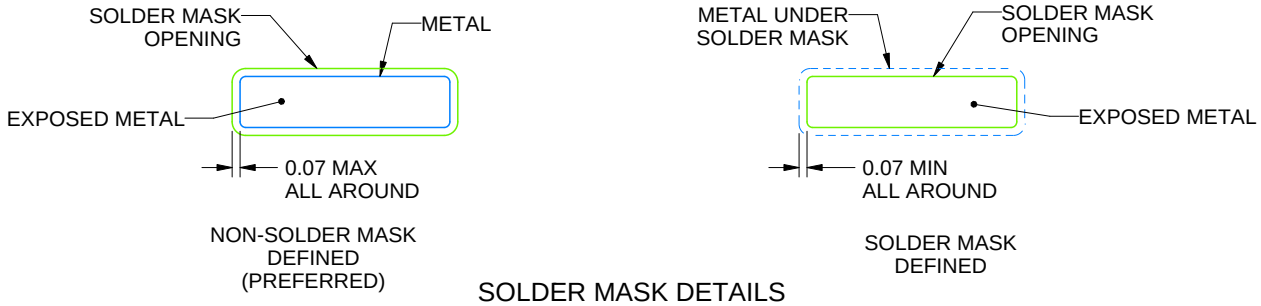


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

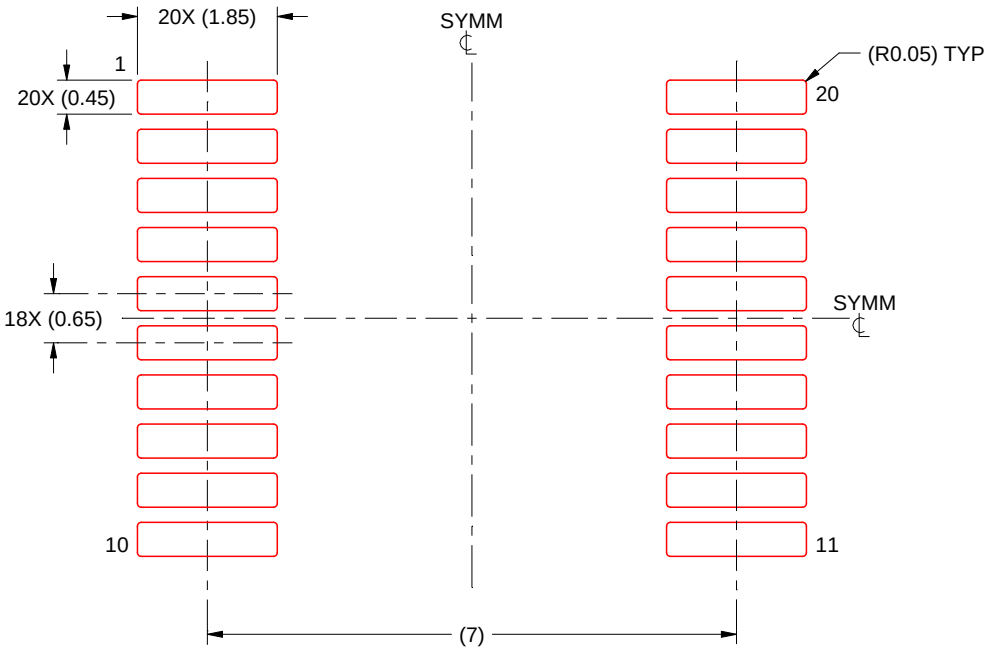
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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