HD3SS3202 双通道差动 2:1/1:2 USB 3.1 多路复用器/多路信号分离器

1 特性

- 提供面向支持 USB 3.1 第 1 代和第 2 代数据传输速率的 USB Type-C™ 生态系统的解决方案
- 兼容 MIPI DSI/CSI-2 DPHY、LVDS、第 III 代 PCIE、SATA Express、SATA
- 运行速率高达 10Gbps
- -3dB 差动带宽宽达 8GHz 以上
- 出色动态特性（5GHz 时）
  - 串扰 = -41dB
  - 断开隔离 = –20dB
  - 插入损耗 = –2.4dB
  - 回波损耗 = –8dB
- 双向“多路复用器/多路信号分离器”差动开关
- 支持 0 到 2V 共模电压
- 单电源电压 V_{CC}：3.3V±10%
- 0°C 至 70°C 的商用温度范围 (HD3SS3202)
- -40°C 至 85°C 的工业温度范围 (HD3SS3202I)

2 应用

- USB Type-C™ 生态系统
- 台式机和笔记本电脑
- 共享 I/O 端口
- 扩展坞
- 显示器、电视
- 机顶盒
- 网络监控摄像头

3 说明

HD3SS3202 是多路复用器或多路信号分离器配置中的高速双向无源开关， 适用于 支持 USB 3.1 第 1 代和第 2 代数据传输速率的 USB Type-C™ 应用。该器件可通过控制引脚 SEL 在两个差动通道（端口 B 到端口 A，或者端口 C 到端口 A）间切换。

HD3SS3202 是一款通用的模拟差动无源开关。该器件适用于任何要求共模电压范围为 0 至 2V 和要求差动信号的最大差动幅度为 1800mVpp 的应用。该器件具有自适应跟踪功能，可确保通道在完全共模电压范围内保持不变。

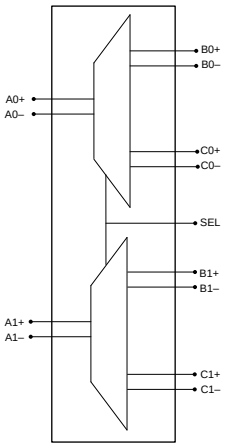
该器件可在确保信号眼图最低衰减程度的条件下实现高速开关，且不会明显增加抖动。它的运行功率低于 1.65mW（典型值）。它具有可供 OEn 引脚使用的关断模式，可实现低于 0.02µW（典型值）的功率。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
HD3SS3202 HD3SS3202I	UQFN (16)	2.60mm x 1.80mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



目录

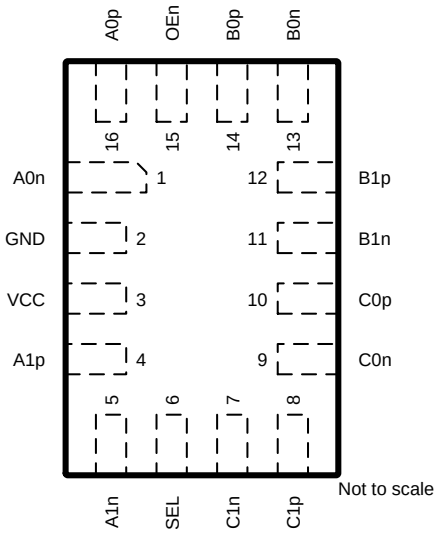
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2018) to Revision A	Page
• Changed I_{CC} max from 0.6mA to 0.8mA	5

5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0n	1	I/O	Port A, channel 0, high-speed negative signal
GND	2	G	Ground
V_{CC}	3	P	3.3-V power
A1p	4	I/O	Port A, channel 1, high-speed positive signal
A1n	5	I/O	Port A, channel 1, high-speed negative signal
SEL	6	I	Port select pin. To help with noise immunity, a 0.01 µF capacitor to GND on this pin is suggested. L: Port A to Port B H: Port A to Port C
C1n	7	I/O	Port C, channel 1, high-speed negative signal (connector side)
C1p	8	I/O	Port C, channel 1, high-speed positive signal (connector side)
C0n	9	I/O	Port C, channel 0, high-speed negative signal (connector side)
C0p	10	I/O	Port C, channel 0, high-speed positive signal (connector side)
B1n	11	I/O	Port B, channel 1, high-speed negative signal (connector side)
B1p	12	I/O	Port B, channel 1, high-speed positive signal (connector side)
B0n	13	I/O	Port B, channel 0, high-speed negative signal (connector side)
B0p	14	I/O	Port B, channel 0, high-speed positive signal (connector side)
OEn	15	I	Active-low chip enable. To help with noise immunity, a 0.01 µF capacitor to GND on this pin is suggested. L: Normal operation H: Shutdown
A0p	16	I/O	Port A, channel 0, high-speed positive signal

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4	V
	Voltage	Differential I/O	–0.5	2.5	V
		Control pins	–0.5	V_{CC}+ 0.5	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{ih}	Input high voltage (SEL, OEn pins)		2		V_{CC}	V
V_{il}	Input low voltage (SEL, OEn pins)		–0.1		0.8	V
V_{diff}	High-speed signal pins differential voltage		0		1.8	V_{pp}
V_{cm}	High speed signal pins common mode voltage		0		2	V
T_A	Operating free-air/ambient temperature	HD3SS3202RSV	0		70	°C
		HD3SS3202IRSV	–40		85	

6.4 Thermal Information

THERMAL METRIC(1)		HD3SS3202 RSV (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	V_{CC} = 3.3 V, OEn = 0		0.5	0.8	mA
I_{STDN}	Device shutdown current	V_{CC} = 3.3 V, OEn = V_{CC}		0.005	1	µA
C_{ON}	Output ON capacitance to GND			0.6		pF
C_{OFF}	Output OFF capacitance to GND			0.8		pF
R_{ON}	Output ON resistance	V_{CC} = 3.3 V; V_{CM} = 0 to 2 V; I_O = –8 mA		5	8	Ω
ΔR_{ON}	On-resistance match between pairs of the same channel	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 2.35 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX) – R_{ON}(MIN)	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 2.35 V			1	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, OEn)				1	µA
$I_{IL,CTRL}$	Input low current, control pins (SEL, OEn)				1	µA
$I_{IH,HS}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 2 V for selected port, A and B with SEL = 0, and A and C with SEL = V_{CC}			1	µA
$I_{IH,HS}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 2 V for non-selected port, C with SEL = 0, and B with SEL = V_{CC} (1)		100	140	µA
$I_{IL,HS}$	Input low current, high-speed pins [Ax/Bx/Cx][p/n]				1	µA

(1) There is a 20-kΩ pull-down in non-selected port.

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	f = 0.3 MHz		-0.4		dB
		f = 0.625 MHz		-0.4		
		f = 2.5 GHz		-1.3		
		f = 4 GHz		-2.0		
		f = 5 GHz		-2.4		
BW	–3-dB bandwidth			8		GHz
R_L	Differential return loss	f = 0.3 MHz		-27		dB
		f = 2.5 GHz		-11		
		f = 4 GHz		-9		
		f = 5 GHz		-8		
O_{IRR}	Differential OFF isolation	f = 0.3 MHz		-77		dB
		f = 2.5 GHz		-23		
		f = 4 GHz		-21		
		f = 5 GHz		-20		
X_{TALK}	Differential crosstalk	f = 0.3 MHz		-82		dB
		f = 2.5 GHz		-44		
		f = 4 GHz		-41		
		f = 5 GHz		-41		

6.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay (see 图 4)				80	ps
t_{SW_ON}	Switching time SEL-to-Switch ON (see 图 3)				0.5	µs
t_{SW_OFF}	Switching time SEL-to-Switch OFF (see 图 3)				0.5	µs
t_{SK_INTRA}	Intra-pair output skew (see 图 4)				6	ps
t_{SK_INTER}	Inter-pair output skew (see 图 4)				20	ps
t_{PD}	Average propagation delay, see 图 1	f = 100 MHz	16		54	ps
		f = 200 MHz	33		63	
		f = 300 MHz	33		59	
		f = 400 MHz	33		57	
		f = 500 MHz	33		56	
		f = 600 MHz	33		53	
		f = 700 MHz	33		50	
		f = 750 MHz	33		50	
		f = 800 MHz	33		50	
		f = 900 MHz	31		50	
		f = 1000 MHz	30		50	

6.8 Typical Characteristics

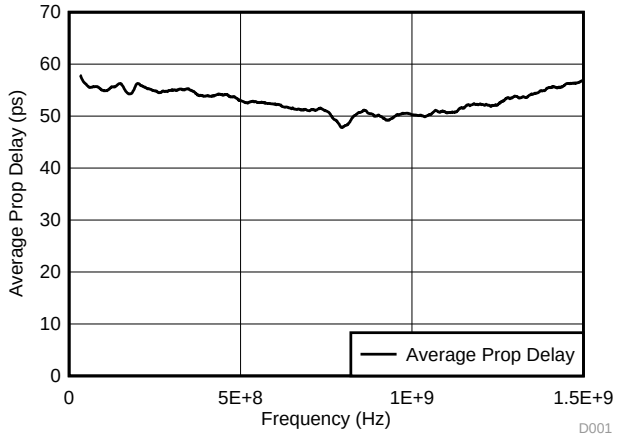


图 1. Average Propagation Delay vs Frequency

7 Parameter Measurement Information

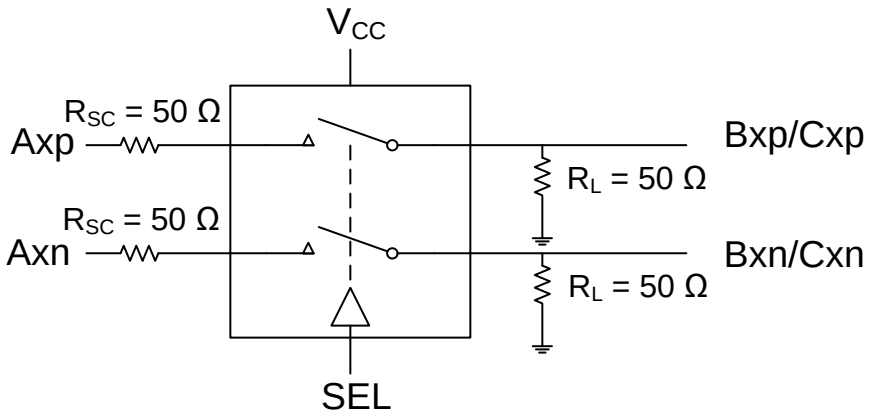


图 2. Test Setup

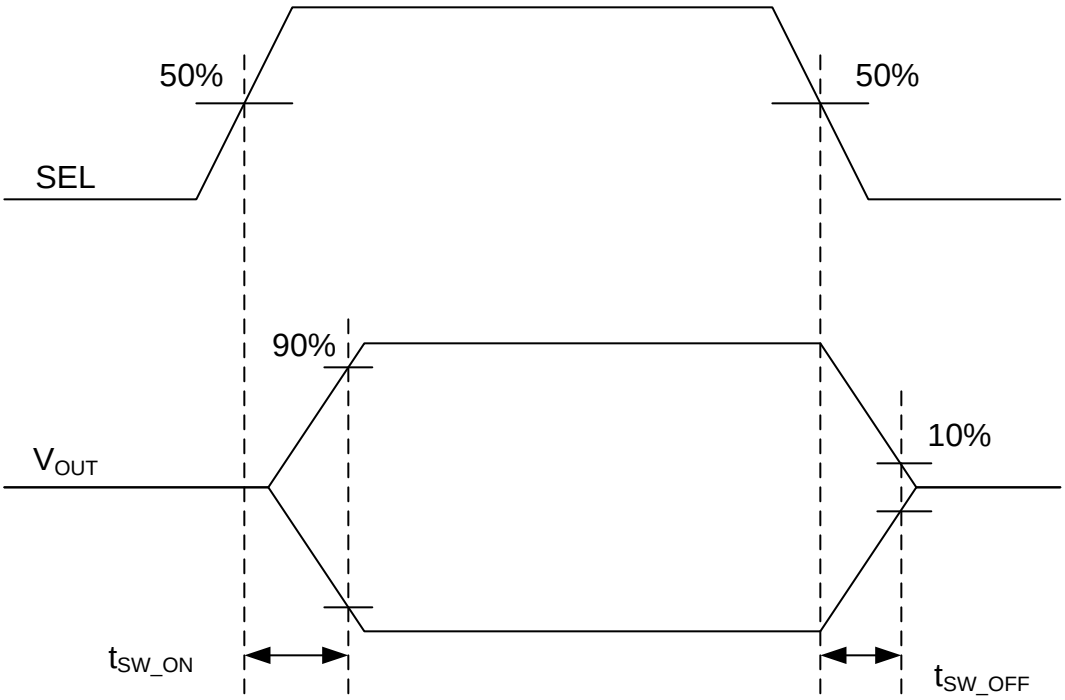


图 3. Switch On and Off Timing Diagram

Parameter Measurement Information (接下页)

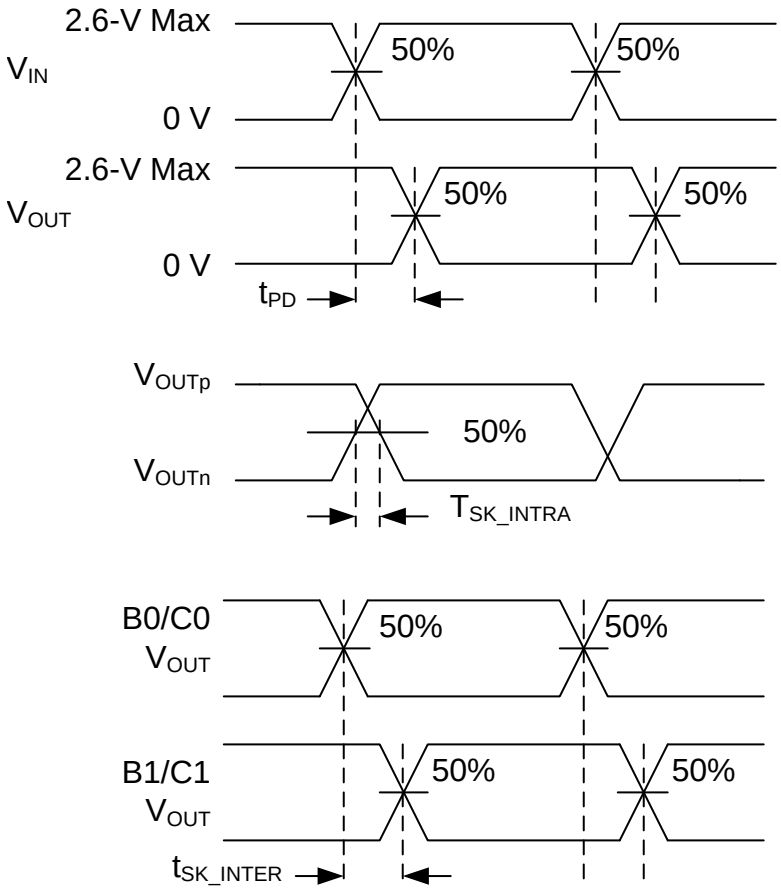


图 4. Timing Diagrams and Test Setup

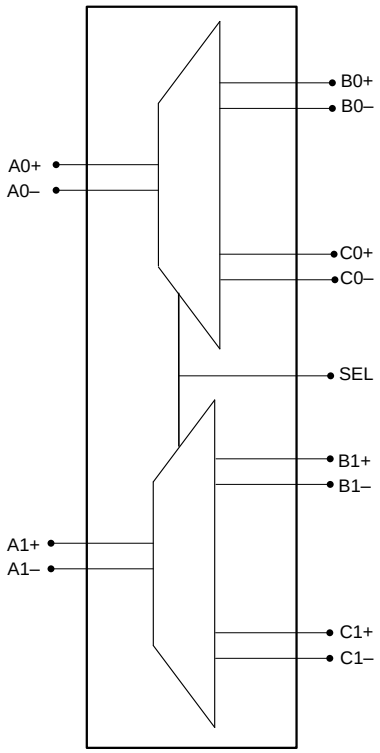
8 Detailed Description

8.1 Overview

The HD3SS3202 is a generic analog differential passive switch that can works for any high-speed interface applications requiring a common mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It uses adaptive tracking to ensures the channel remain unchanged for the entire common mode voltage range.

Excellent dynamic characteristics of the device allow high-speed switching with minimum attenuation to the signal eye diagram with little added jitter. It consumes < 1.65 mW (typ) of power when operational and has a shutdown mode exercisable by OEn pin resulting < .02 µW (typical).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Enable and Power Savings

The HD3SS3202 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes little current to save the maximum power. To enter standby mode, the OEn control pin is pulled high through a resistor and must remain high. For active/normal operation, the OEn control pin should be pulled low to GND.

HD3SS3202 consumes < 1.65 mW (typ) of power when operational and has a shutdown mode exercisable by the OEn pin resulting < .02 µW (typ).

8.4 Device Functional Modes

表 1. Port Select Control Logic(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

(1) The HD3SS3202 can tolerate polarity inversions for all differential signals on Ports A, B, and C. Take care to ensure the same polarity is maintained on Port A versus Ports B/C.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The HD3SS3202 is a generic 2-channel high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS3202 supports several high-speed data protocols with a differential amplitude of <1800 mVpp and a common mode voltage of < 2 V, as with USB 3.1 and DisplayPort 1.2. The device has one select input (SEL) pin that can be controlled by an available GPIO pin within a system or from a microcontroller.

The HD3SS3202 with its adaptive common mode tracking technology can support applications where the common mode is different between the RX and TX pair. The two USB3.1 Type C connector applications show both a host and device side. The cable between the two connectors swivels the pairs to properly route the signals to the correct pin. The other applications are more generic because different connectors can be used.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 capacitors are the preferred option to provide AC coupling; 0402 size capacitors also work. Avoid the capacitors greater than 0402 and C-packs. When placing AC coupling capacitors, symmetric placement is best. The designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board.

The AC coupling capacitors have several placement options. Because the HD3SS3202 requires a bias voltage, the designer must place the capacitors on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. 图 5 shows a few placement options. The coupling capacitors are placed between the HD3SS3202 and endpoint. In this situation, the HD3SS3202 is biased by the system/host controller.

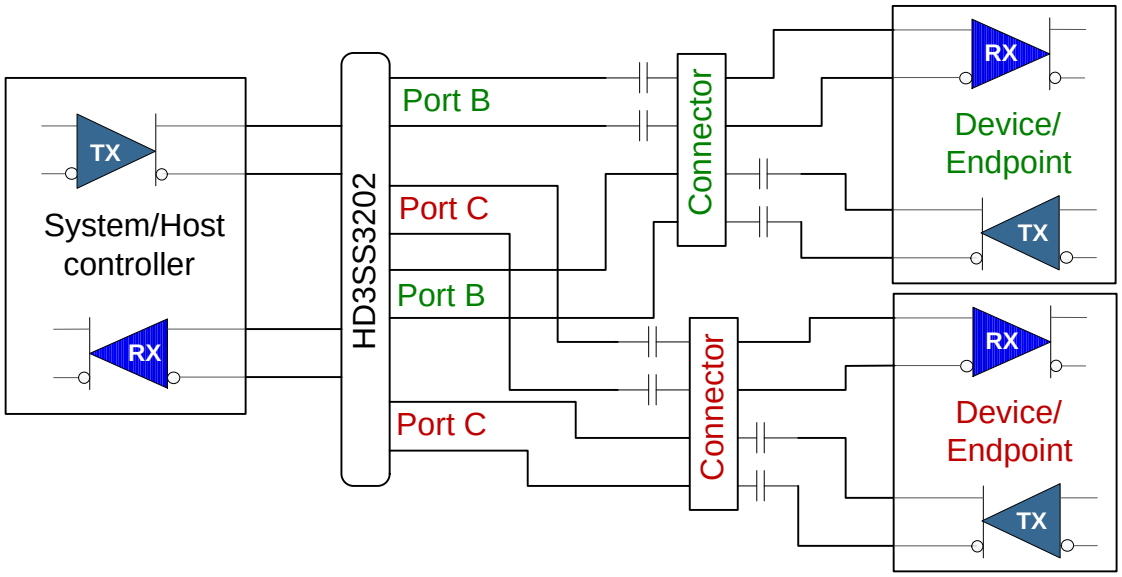


图 5. AC Coupling Capacitors between HD3SS3202 TX and Endpoint TX

Application Information (接下页)

In 图 6, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on top is biased by the endpoint and the lower switch is biased by the host controller.

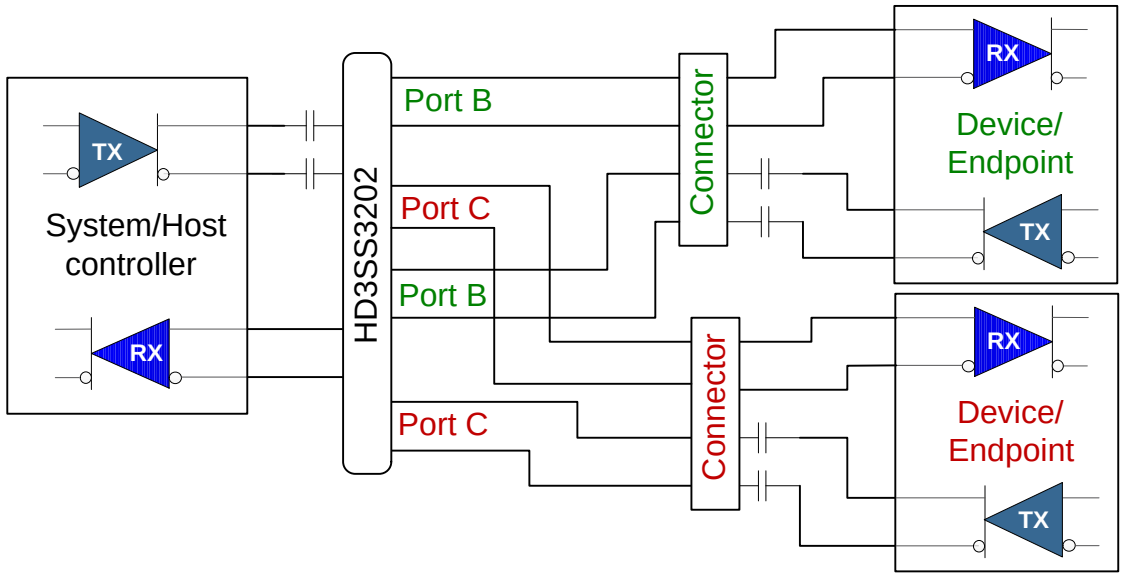
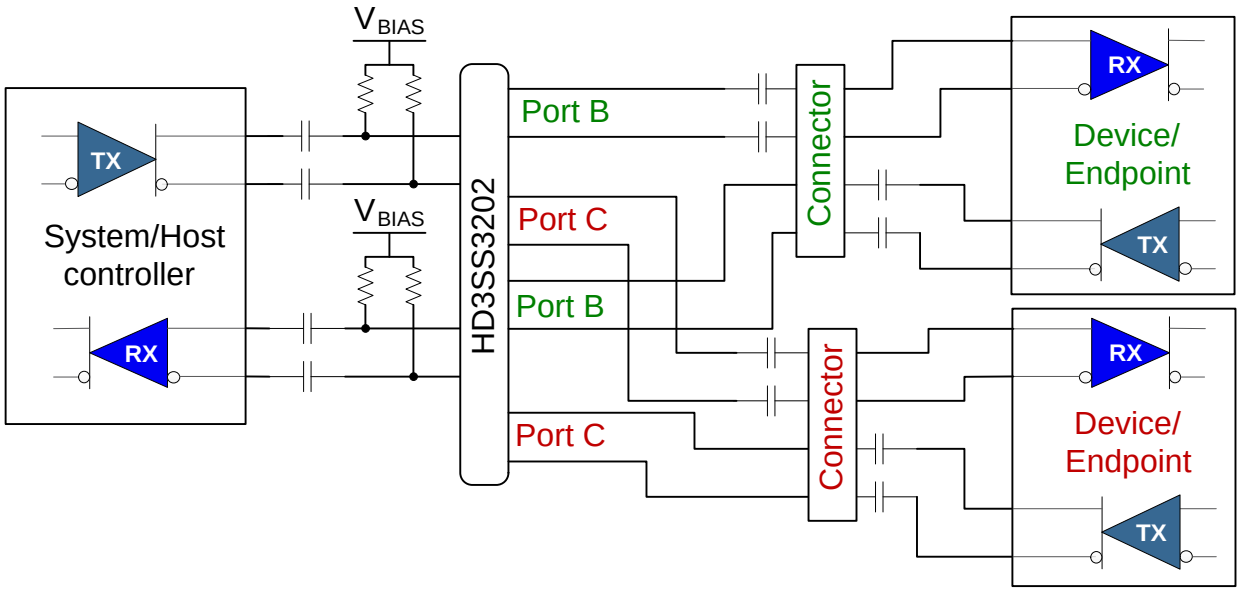


图 6. AC Coupling Capacitors on Host TX and Endpoint TX

If the common mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in 图 7). A biasing voltage of < 2 V is required in this case.



V_{BIAS} can be GND

Capacitor and resistor values depend upon application.

图 7. AC Coupling Capacitors on Both Sides of Switch

Application Information (接下页)

The HD3SS3202 can be used with the USB Type C connector to support the connector's flip ability. 图 8 provides the generic location for the AC coupling capacitors for this application.

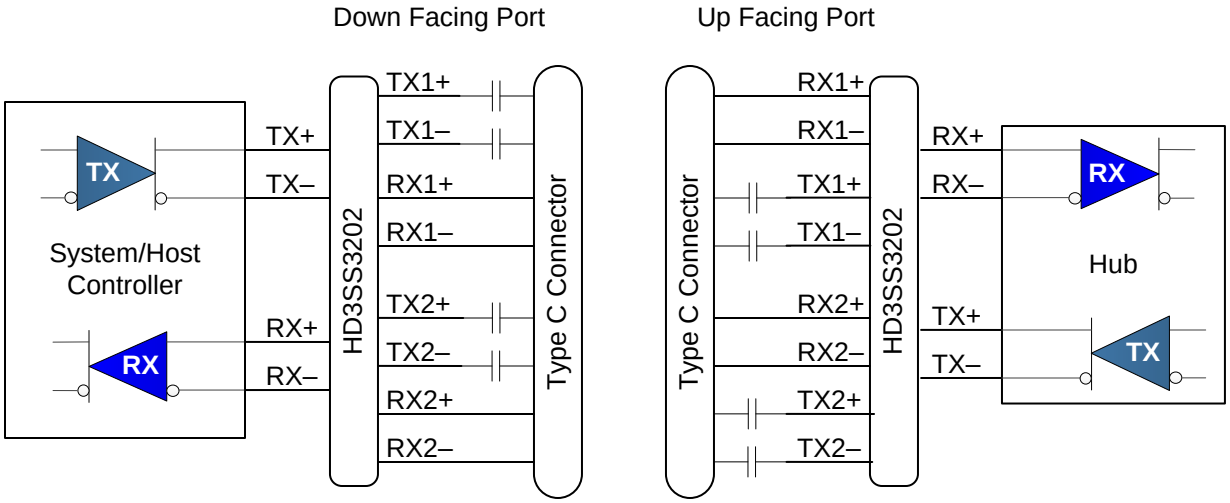


图 8. AC Coupling Capacitors for USB Type C

9.2 Typical Applications

9.2.1 Down Facing Port for USB3.1 Type C

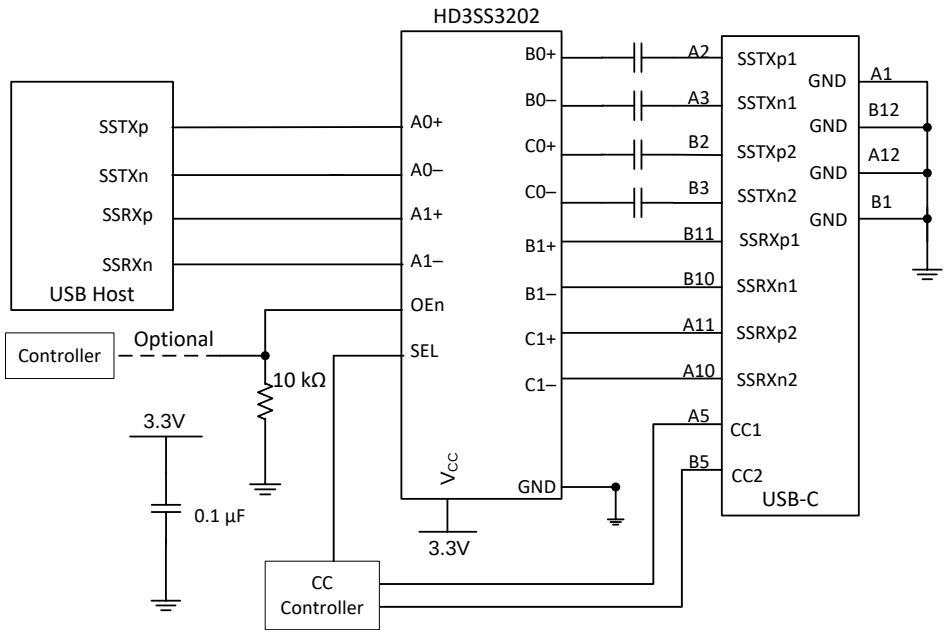


图 9. Down Facing Port for USB3.1 Type C Connector

9.2.1.1 Design Requirements

The HD3SS3202 can be designed into many different applications. All the applications have certain requirements for the system to work properly. The HD3SS3202 requires 3.3-V ±10% V_{CC} rail. The OEn pin must be low for device to work; otherwise, it disables the outputs. This pin can be driven by a processor. The expectation is that one side of the device has AC coupling capacitors. 表 2 provides information on expected values to perform properly.

表 2. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
AXp/n, BXp/n, CXp/n CM input voltage	0 to 2 V
Control/OEn pin max voltage for low	0.8 V
Control/OEn pin min voltage for high	2.0 V
AC coupling capacitor	75 nF to 265 nF.
R_{BIAS} (图 9) when needed	100 kΩ

9.2.1.2 Detailed Design Procedure

The HD3SS3202 is a high-speed passive switch device that can behave as a mux or demux. Because this is a passive switch, signal integrity is important because the device provides no signal conditioning capability. The device can support 1 to 2 inches of board trace and a connector on either end.

To design in the HD3SS3202, the designer needs to understand the following.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Depending upon the application, determine the best place to put the 100-nF coupling capacitor.
- Provide a control signal for the SEL and OEn pins. It may be necessary to include a 0.01µF to GND on each of these pins to help with noise immunity.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground

9.2.1.3 Application Curves

图 10 shows the eye at the input of the HD3SS3202 and 图 11 at the output of the HD3SS3202.

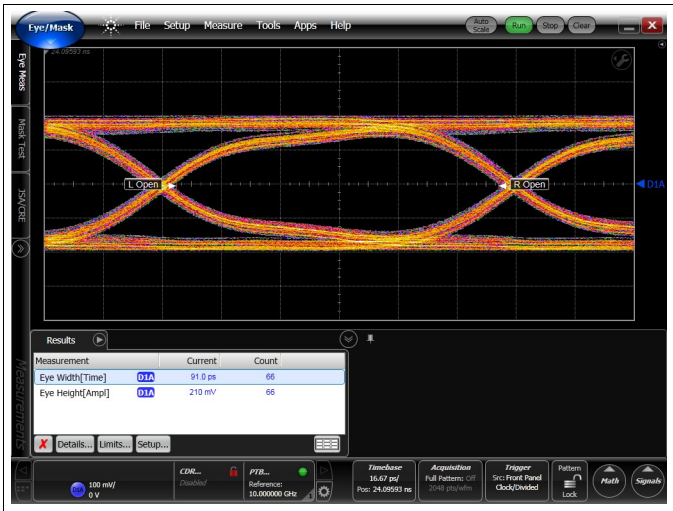


图 10. Source 10 Gbps Eye Diagram

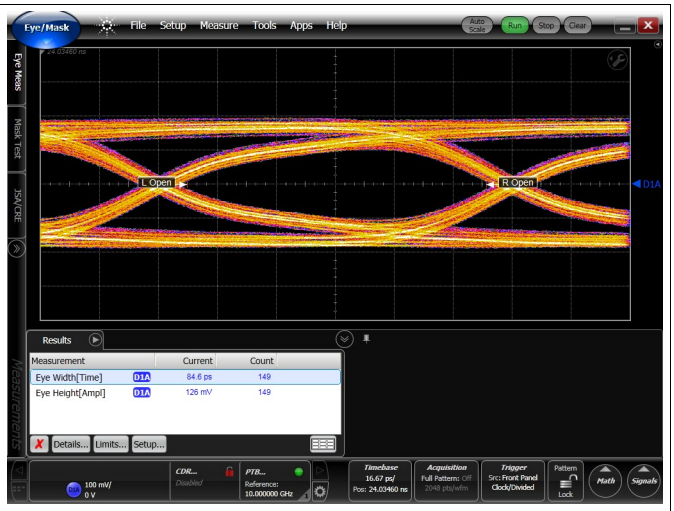


图 11. HD3SS3202 10 Gbps Output Eye Diagram

9.3 Systems Examples

9.3.1 Up Facing Port for USB3.1 Type C

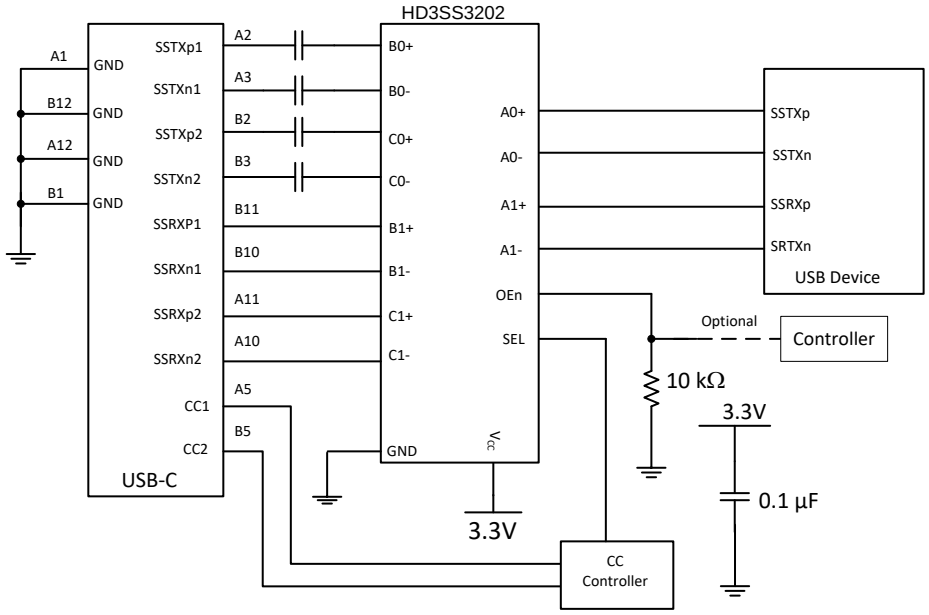


图 12. Up Facing Port for USB3.1 USB Type-C Connector

Systems Examples (接下页)

9.3.2 PCIE/USB

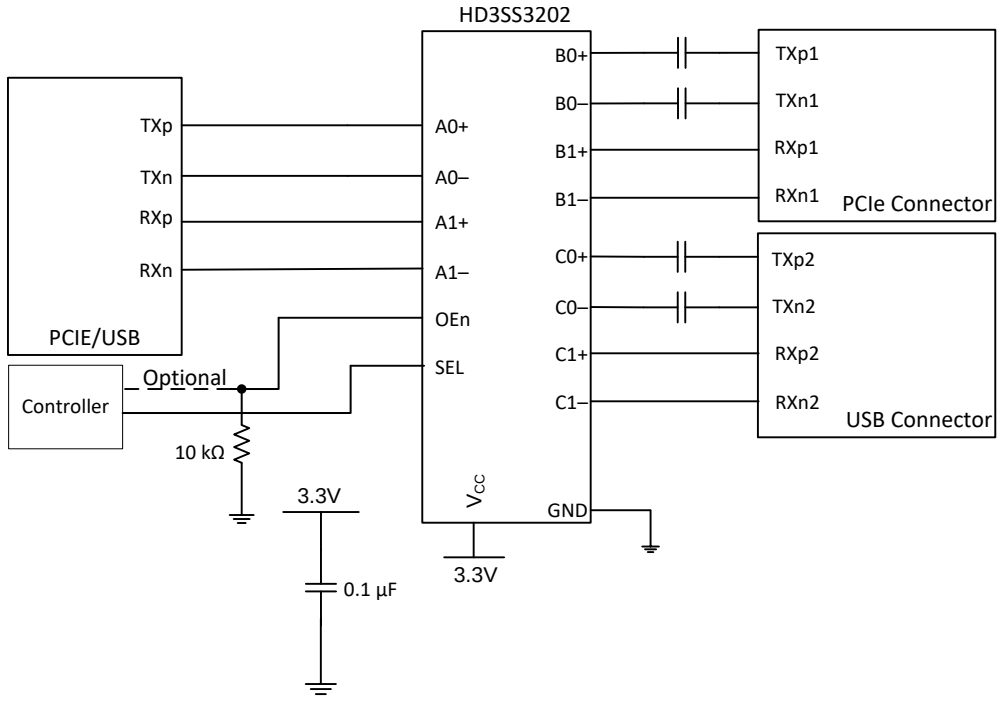


图 13. PCIE Motherboard

9.3.3 PCIE/eSATA

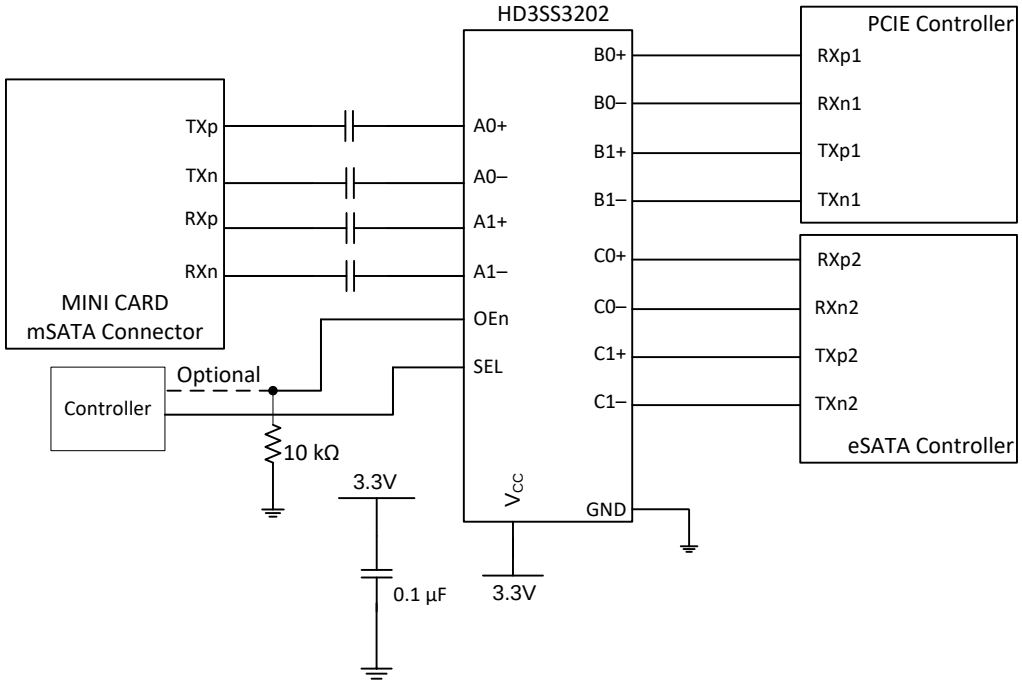


图 14. PCIE and eSATA Combo

Systems Examples (接下页)

9.3.4 USB/eSATA

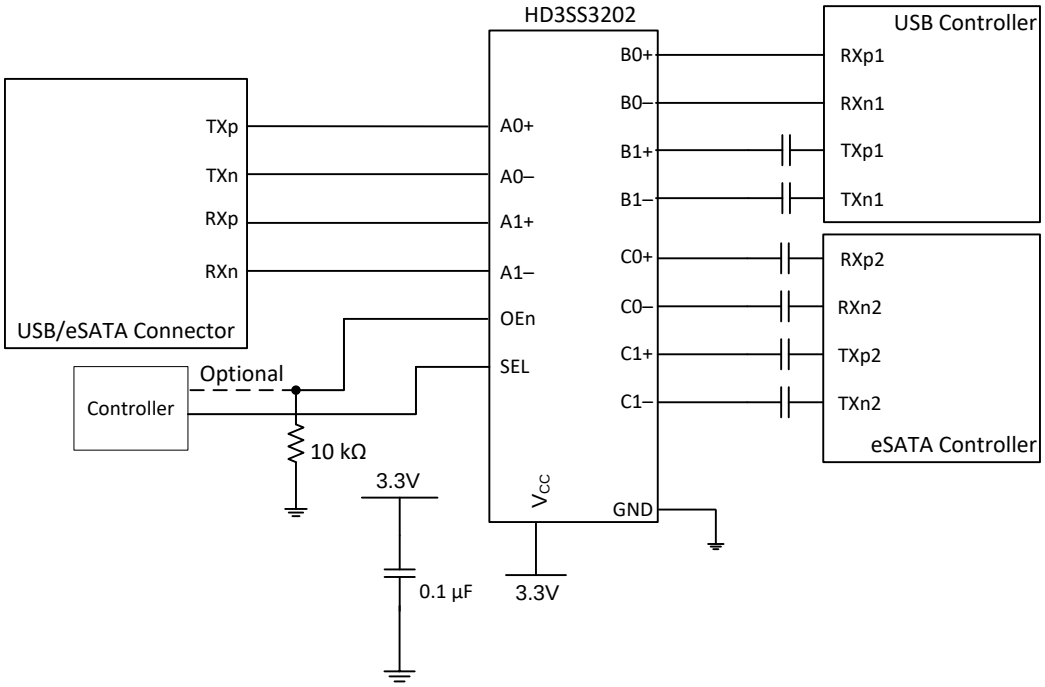


图 15. eSATA and USB 3.1 Combo Connector

9.3.5 MIPI Camera Serial Interface

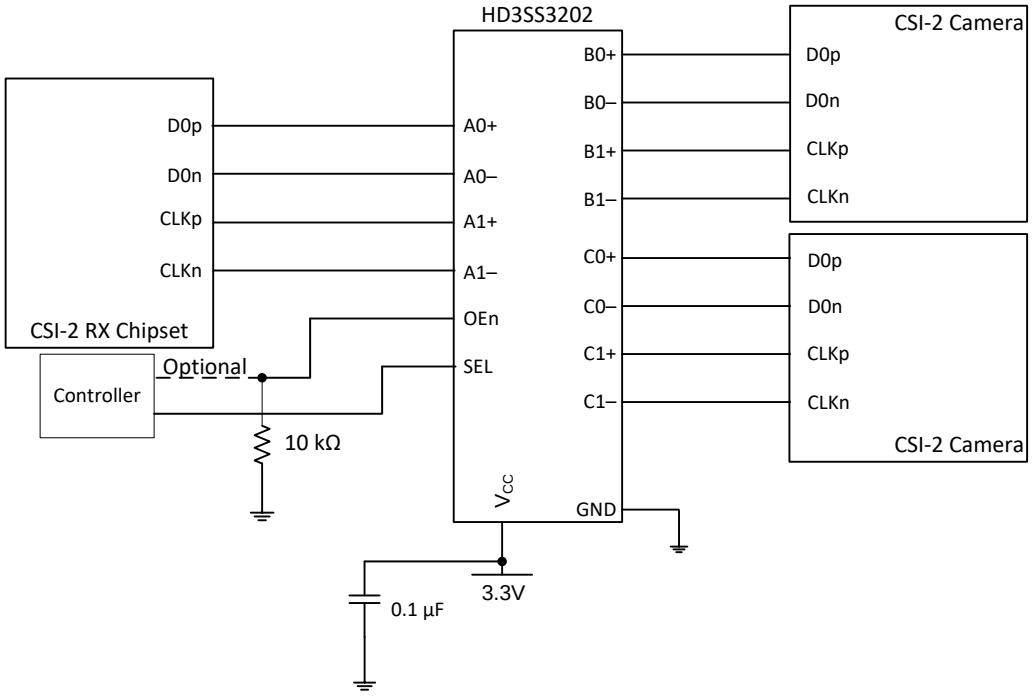


图 16. CSI Camera Array

10 Power Supply Recommendations

The HD3SS3202 does not require a power supply sequence. TI recommends placing a 100nF de-coupling capacitor at the device V_{CC} near the pin.

11 Layout

11.1 Layout Guidelines

11.2 Layout Example

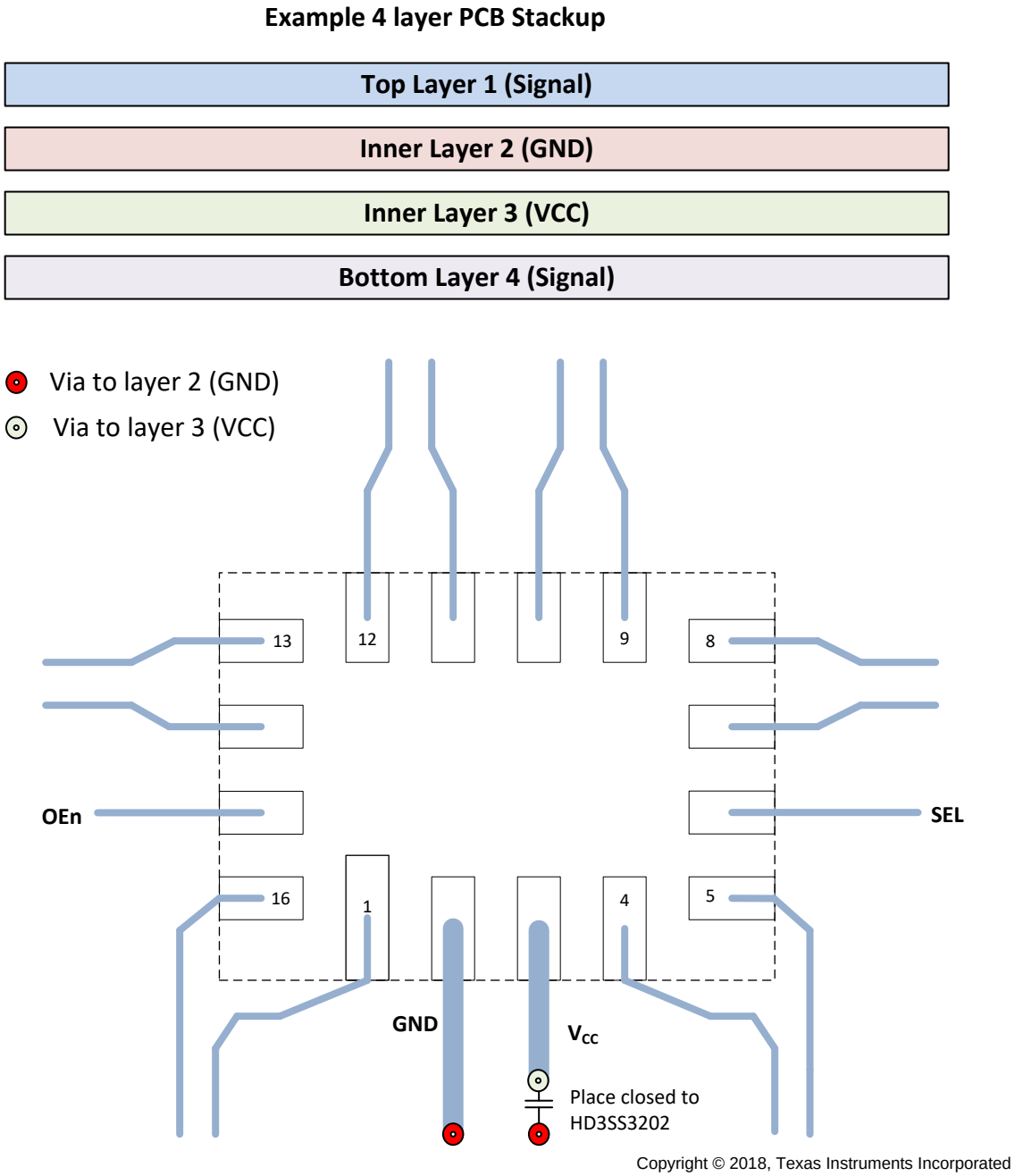


图 17. HD3SS3202 Basic Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.3 商标

E2E is a trademark of Texas Instruments.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS3202IRSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3202	Samples
HD3SS3202IRSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3202	Samples
HD3SS3202RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3202	Samples
HD3SS3202RSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

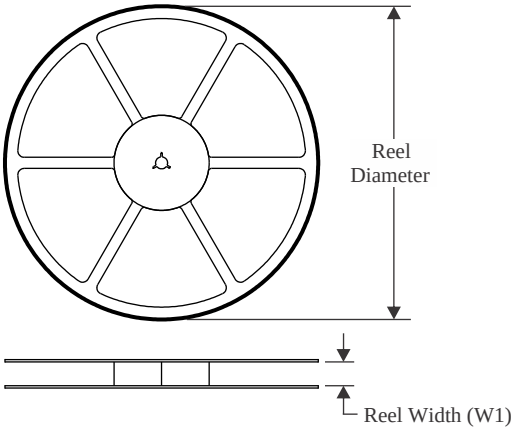
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

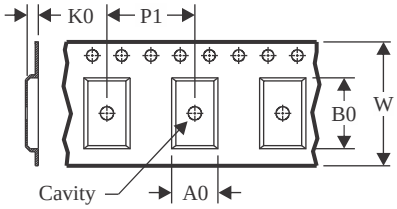
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

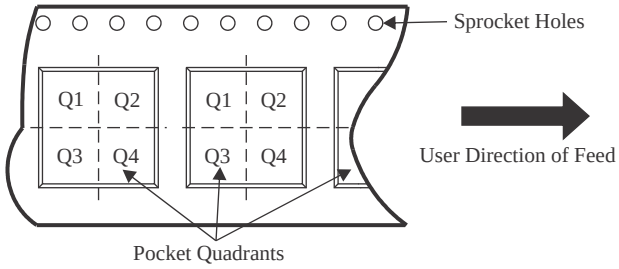


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

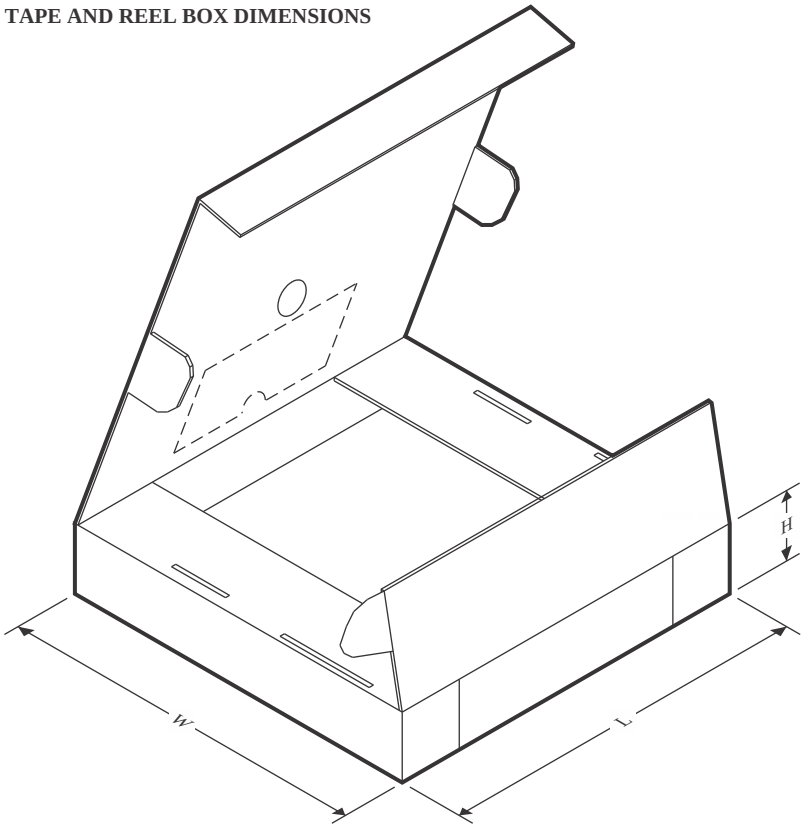
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3202IRSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
HD3SS3202IRSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
HD3SS3202RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
HD3SS3202RSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3202IRSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
HD3SS3202IRSVT	UQFN	RSV	16	250	189.0	185.0	36.0
HD3SS3202RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
HD3SS3202RSVT	UQFN	RSV	16	250	189.0	185.0	36.0

GENERIC PACKAGE VIEW

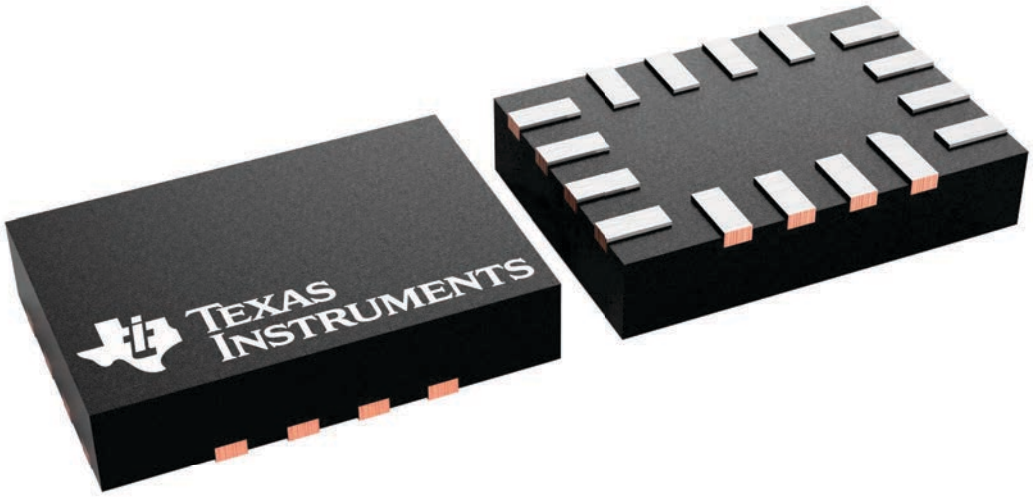
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



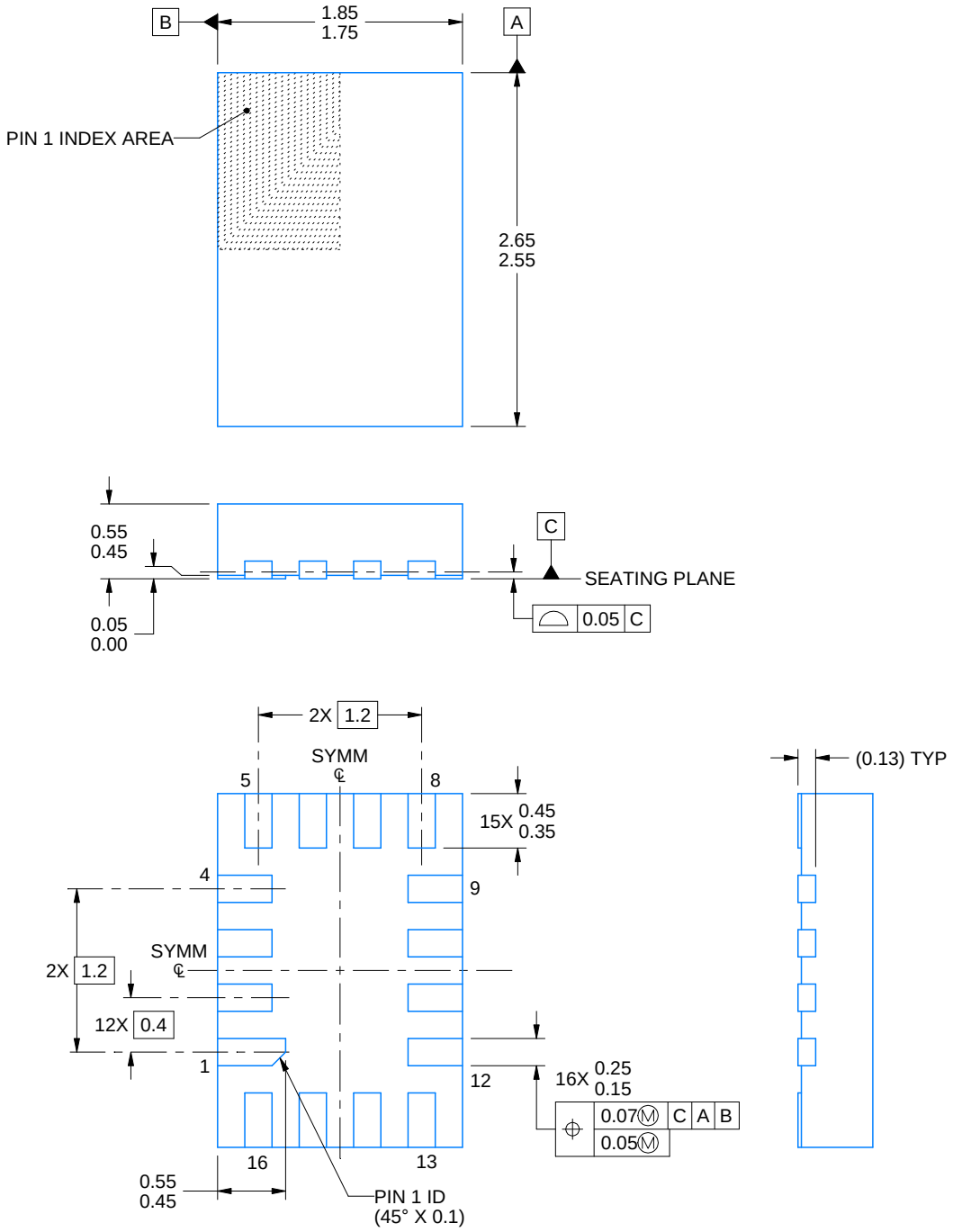
4231225/A

RSV0016A

PACKAGE OUTLINE

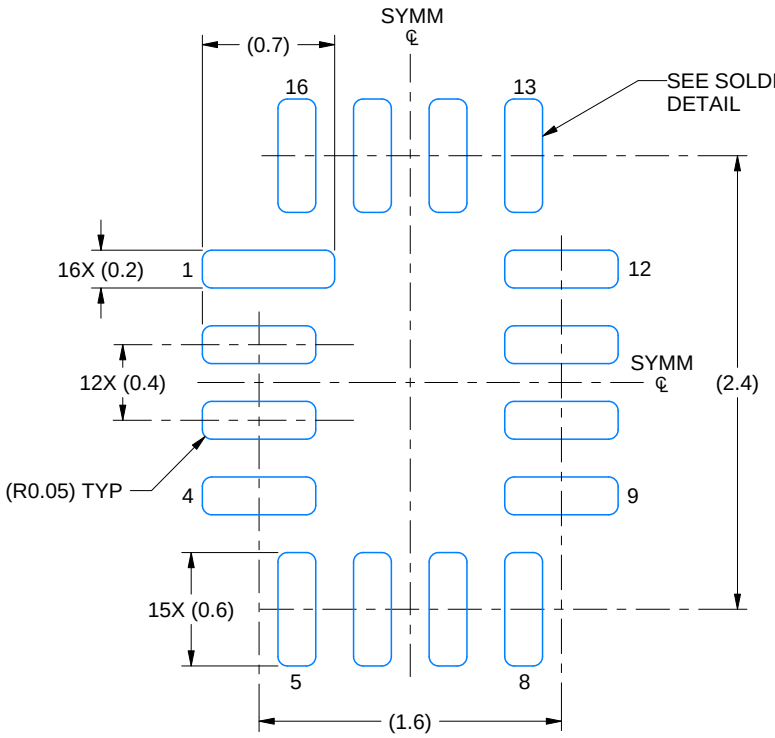
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

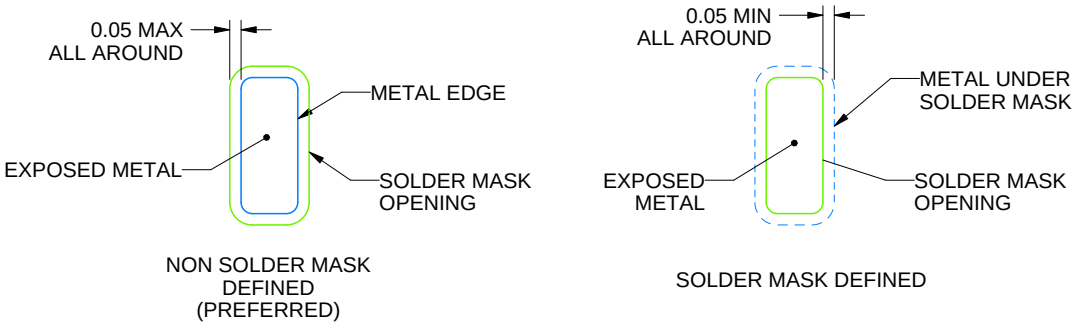


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

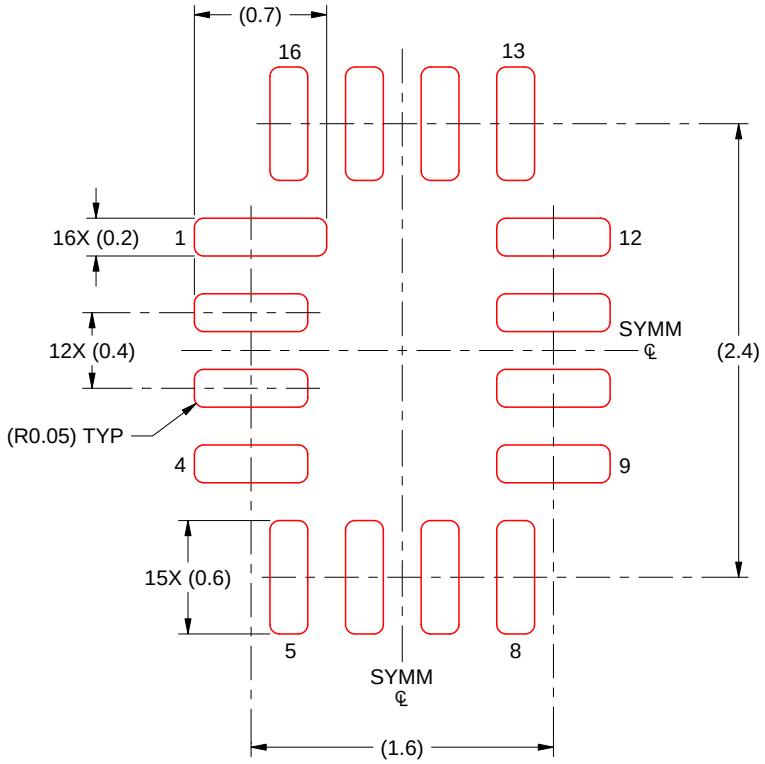


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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