

INA118 低功耗精密仪表放大器

1 特性

- 此器件的新版本现已上市：[INA818](#)
- 低失调电压：50μV，最大值
- 低漂移：0.5μV/°C，最大值
- 低输入偏置电流：5nA（最大值）
- 高 CMR：110dB（最小值）
- 输入保护电压可达 ±40V
- 宽电源电压范围：±2.25 至 ±18V
- 低静态电流：350μA
- 封装：8 引脚塑料 DIP，SO-8

2 应用

- [压力变送器](#)
- [温度变送器](#)
- [称重计](#)
- [心电图 \(ECG\)](#)
- [模拟输入模块](#)
- [数据采集 \(DAQ\)](#)

3 说明

INA118 是一款低功耗通用仪表放大器，可提供出色的准确性。此器件采用多功能三级运算放大器设计，尺寸小巧，适用于多种应用。即使在高增益（ $G = 100$ 时为 70kHz）情况下，电流反馈输入电路也可提供宽带宽。

可通过单个外部电阻器在 1 到 10000 范围内设置增益。内部输入保护可经受高达 ±40V 的电压且无损坏。

INA118 经过激光修整，具有低失调电压（50 μV）、低温漂（0.5 μV/°C）和高共模抑制（ $G = 1000$ 时为 110dB）。INA118 采用低至 ±2.25 V 的电源电压，静态电流仅 350μA，因此非常适合电池供电系统。

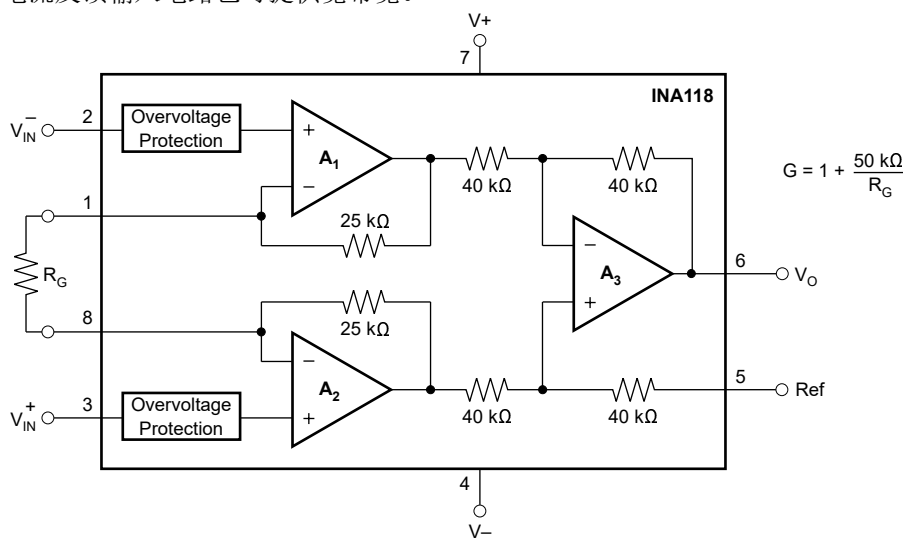
INA118 采用 8 引脚塑料 DIP 和 SO-8 表面贴装式封装，其额定温度范围为 -40°C 至 +85°C。

升级后的 [INA818](#) 在相同的静态电流下可提供更低的输入级失调电压（最大值 35μV）、更低的输入偏置电流（最大值 0.5nA）和更低的噪声（8nV/√Hz）。请参阅 [器件比较表](#)，了解如何选择德州仪器 (TI) 提供的精密仪表放大器。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
INA118	SOIC (8)	3.91mm × 4.90mm
	PDIP (8)	6.35mm × 9.81mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。



简化版原理图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2019) to Revision C (September 2022)	Page
• 通篇将最低电源电压从 $\pm 1.35\text{V}$ 更改为 $\pm 2.25\text{V}$ ，并从 2.7V 更改为 4.5V	1
• 更改了应用以链接到 ti.com 上全新的终端设备.....	1
• 将“简化版原理图”中的电阻器从 $60\text{k}\Omega$ 更改为 $40\text{k}\Omega$	1
• Changed minimum and maximum input common-mode voltage from $V^- + 1.1\text{V}$ and $V^+ - 1\text{V}$ to $V^- + 2\text{V}$ and $V^+ - 2\text{V}$ respectively in <i>Recommended Operating Conditions</i>	5
• Changed minimum and maximum ambient temperature from -55°C and $+150^\circ\text{C}$ to -40°C and $+125^\circ\text{C}$ respectively in <i>Recommended Operating Conditions</i>	5
• Added $V_{\text{CM}} = 0\text{V}$ to test conditions below title in <i>Electrical Characteristics</i>	6
• Changed input offset voltage vs temperature test condition from $T_A = T_{\text{MIN}}$ to T_{MAX} to $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ in <i>Electrical Characteristics</i>	6
• Changed input offset voltage vs power supply test condition from $V_S = \pm 1.35\text{V}$ to $\pm 18\text{V}$ to $V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$ in <i>Electrical Characteristics</i>	6
• Changed high-side linear input voltage range from $(V^+) - 1\text{V}$ minimum and $(V^+) - 0.65\text{V}$ typical to $(V^+) - 2\text{V}$ minimum and $(V^+) - 1.4\text{V}$ typical in <i>Electrical Characteristics</i>	6
• Changed low-side linear input voltage range from $(V^-) + 1.1\text{V}$ minimum and $(V^-) + 0.95\text{V}$ typical to $(V^-) + 2\text{V}$ minimum and $(V^-) + 1.2\text{V}$ typical in <i>Electrical Characteristics</i>	6
• Added test condition of $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ to bias current vs temperature and offset current vs temperature in <i>Electrical Characteristics</i>	6
• Added test condition of $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ to gain vs temperature and $50\text{-k}\Omega$ resistance vs temperature in <i>Electrical Characteristics</i>	6
• Changed single supply output voltage test condition from $V_S = 2.7\text{V}/0\text{V}$ to $V^+ = 4.5\text{V}$, $V^- = 0\text{V}$ in <i>Electrical Characteristics</i>	6
• Deleted power supply voltage range specification from <i>Electrical Characteristics</i>	6
• Deleted temperature range specifications from <i>Electrical Characteristics</i>	6
• Changed Figures 7-3, 7-4, 7-5, 7-6, 7-7, 7-8, 7-11, 7-12, 7-18, 7-19, and 7-20 in <i>Typical Characteristics</i>	8
• Changed FET transistor input current limit from approximately $1.5\text{-}5\text{mA}$ to 6mA in <i>Overview</i>	12
• Deleted internal node equations in <i>Overview</i> and <i>Functional Block Diagram</i>	12
• Changed schematic in <i>Functional Block Diagram</i>	12
• Changed linear input voltage range in <i>Input Common-Mode Range</i> and <i>Single-Supply Operation</i>	13

- Changed FET transistor input current limit from approximately 1.5-5 mA to 6 mA in *Input Protection* 13
- Changed resistors in Figure 9-1 from 60 k Ω to 40 k Ω in *Typical Application* 14
- Changed Figure 10-5 to use a 5-V supply voltage..... 19

Changes from Revision A (January 2016) to Revision B (April 2019)	Page
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- | | |
|--|---|
| • 添加了有关升级后的新版本 INA818 的信息..... | 1 |
| • Added <i>Device Comparison Table</i> | 4 |

Changes from Revision * (September 2000) to Revision A (January 2016)	Page
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- | | |
|---|---|
| • 添加了 <i>ESD</i> 等级表、特性说明部分、器件功能模式部分、应用和实现部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。..... | 1 |
|---|---|
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5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35- μ V Offset, 0.4- μ V/ $^{\circ}$ C V_{OS} Drift, 8-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA819	35- μ V Offset, 0.4- μ V/ $^{\circ}$ C V_{OS} Drift, 8-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	2, 3
INA821	35- μ V Offset, 0.4- μ V/ $^{\circ}$ C V_{OS} Drift, 7-nV/ $\sqrt{\text{Hz}}$ Noise, High-Bandwidth, Precision Instrumentation Amplifier	$G = 1 + 49.4 \text{ k}\Omega / R_G$	2, 3
INA828	50- μ V Offset, 0.5- μ V/ $^{\circ}$ C V_{OS} Drift, 7-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA333	25- μ V V_{OS} , 0.1- μ V/ $^{\circ}$ C V_{OS} Drift, 1.8-V to 5-V, RRO, 50- μ A I_Q , chopper-stabilized INA	$G = 1 + 100 \text{ k}\Omega / R_G$	1, 8
PGA280	20-mV to ± 10 -V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ± 18 V	Digital programmable	N/A
INA159	$G = 0.2$ V Differential Amplifier for ± 10 -V to 3-V and 5-V Conversion	$G = 0.2 \text{ V/V}$	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

6 Pin Configuration and Functions

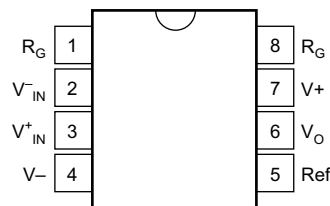


图 6-1. P (8-Pin PDIP) and D (8-Pin SOIC) Packages, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	R_G	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
2	V_{IN}^-	Input	Negative input
3	V_{IN}^+	Input	Positive input
4	V^-	Power	Negative supply
5	Ref	Input	Reference input. This pin must be driven by low impedance or connected to ground.
6	V_O	Output	Output
7	V^+	Power	Positive supply
8	R_G	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.

7 Specifications

7.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得 (除非另有说明) ⁽¹⁾

	最小值	最大值	单位
电源电压		±18	V
模拟输入电压		±40	V
输出短路 (至接地)	持续		
工作温度	-40	125	°C
结温		150	°C
引线温度 (焊接, 10s)		300	°C
T _{stg} 存储温度	-40	125	°C

(1) 应力超出绝对最大额定值下列出的值可能会对器件造成永久损坏。这些仅仅是应力额定值,并不意味着器件在这些条件或超出 [7.3](#) 下的任何其它条件下能够正常工作。长时间处于绝对最大额定条件下可能会影响器件的可靠性。

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Power supply	±2.25	±15	±18	V
	Input common-mode voltage (for V _O = 0 V)	V ⁻ + 2		V ⁺ - 2	V
T _A	Ambient temperature	- 40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA118		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	115	48	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	62	37	°C/W
R _{θJB}	Junction-to-board thermal resistance	59	25	°C/W
ψ _{JT}	Junction-to-top characterization parameter	14	14	°C/W
ψ _{JB}	Junction-to-board characterization parameter	58	25	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

7.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Offset voltage, RTI	Initial	$T_A = 25^\circ\text{C}$	INA118PB, UB	$\pm 10 \pm 50 / G$	$\pm 50 \pm 500 / G$		μV
			INA118P, U	$\pm 25 \pm 100 / G$	$\pm 125 \pm 1000 / G$		
	vs Temperature	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	INA118PB, UB	$\pm 0.2 \pm 2 / G$	$\pm 0.5 \pm 20 / G$		$\mu\text{V}/^\circ\text{C}$
			INA118P, U	$\pm 0.2 \pm 5 / G$	$\pm 1 \pm 20 / G$		
	vs Power supply	$V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$	INA118PB, UB	$\pm 1 \pm 10 / G$	$\pm 5 \pm 100 / G$		$\mu\text{V}/\text{V}$
INA118P, U	$\pm 1 \pm 10 / G$	$\pm 10 \pm 100 / G$					
Long-term stability			$\pm 0.4 \pm 5 / G$			$\mu\text{V}/\text{mo}$	
Impedance	Differential			$10^{10} \parallel 1$			$\Omega \parallel \text{pF}$
	Common-mode			$10^{10} \parallel 4$			
Linear input voltage				$(V^+) - 2$	$(V^+) - 1.4$		V
				$(V^-) + 2$	$(V^-) + 1.2$		
Safe input voltage						± 40	V
Common-mode rejection	$V_{CM} = \pm 10\text{ V}$, $\Delta R_S = 1\text{ k}\Omega$, $G = 1$	INA118PB, UB	80	90			dB
		INA118P, U	73	90			
	$V_{CM} = \pm 10\text{ V}$, $\Delta R_S = 1\text{ k}\Omega$, $G = 10$	INA118PB, UB	97	110			
		INA118P, U	89	110			
	$V_{CM} = \pm 10\text{ V}$, $\Delta R_S = 1\text{ k}\Omega$, $G = 100$	INA118PB, UB	107	120			
		INA118P, U	98	120			
	$V_{CM} = \pm 10\text{ V}$, $\Delta R_S = 1\text{ k}\Omega$, $G = 1000$	INA118PB, UB	110	125			
		INA118P, U	100	125			
Bias current		INA118PB, UB		± 1	± 5		nA
		INA118P, U		± 1	± 10		
Bias current drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			± 40			$\text{pA}/^\circ\text{C}$
Offset current		INA118PB, UB		± 1	± 5		nA
		INA118P, U		± 1	± 10		
Offset current drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			± 40			$\text{pA}/^\circ\text{C}$
Noise voltage, RTI	$G = 1000$, $R_S = 0\ \Omega$	$f = 10\text{ Hz}$		11			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		10			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		10			$\text{nV}/\sqrt{\text{Hz}}$
		$f_B = 0.1\text{ Hz}$ to 10 Hz		0.28			$\mu\text{Vp-p}$
Noise current		$f = 10\text{ Hz}$		2			$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.3			
		$f_B = 0.1\text{ Hz}$ to 10 Hz		80			
GAIN							
Gain equation				$1 + (50\text{ k}\Omega / R_G)$			V/V
Gain				1		10000	V/V
Gain error	$G = 1$			$\pm 0.01\%$		$\pm 0.024\%$	
	$G = 10$			$\pm 0.02\%$		$\pm 0.4\%$	
	$G = 100$			$\pm 0.05\%$		$\pm 0.5\%$	
	$G = 1000$			$\pm 0.5\%$		$\pm 1\%$	
Gain drift	$G = 1$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			± 1		± 10	$\text{ppm}/^\circ\text{C}$
50-k Ω resistance drift ⁽¹⁾	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			± 25		± 100	$\text{ppm}/^\circ\text{C}$
Nonlinearity	$G = 1$			± 0.0003		± 0.001	% of FSR
	$G = 10$			± 0.0005		± 0.002	
	$G = 100$			± 0.0005		± 0.002	
	$G = 1000$			± 0.002		± 0.01	

7.5 Electrical Characteristics (continued)

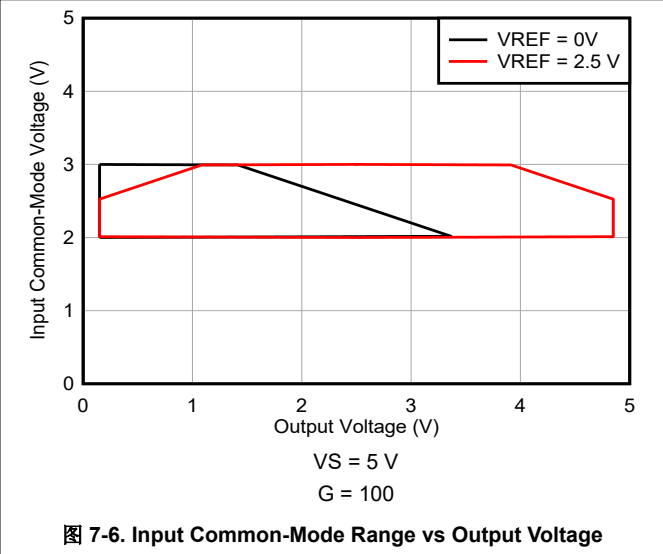
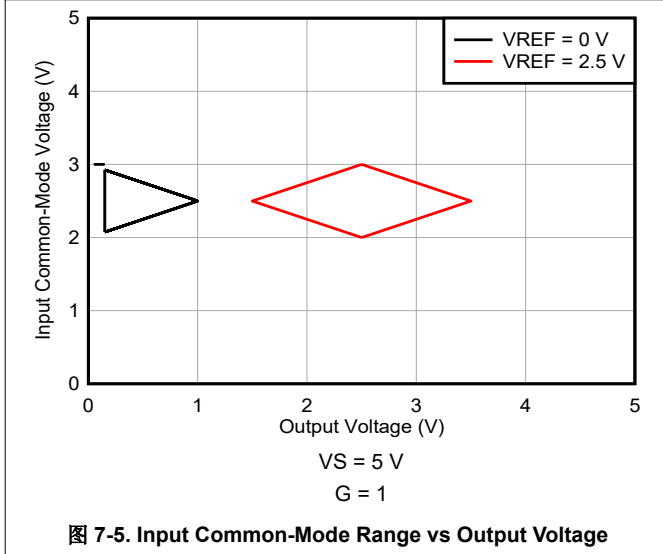
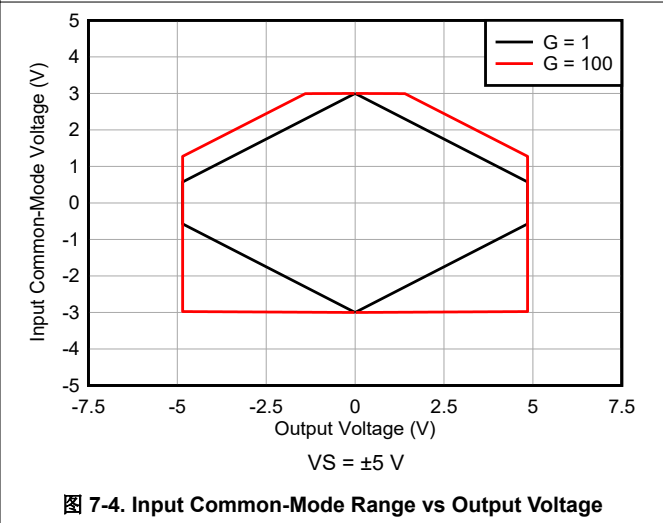
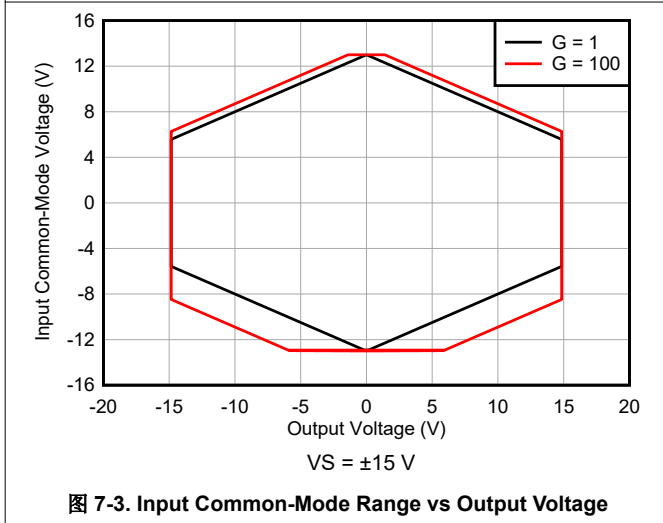
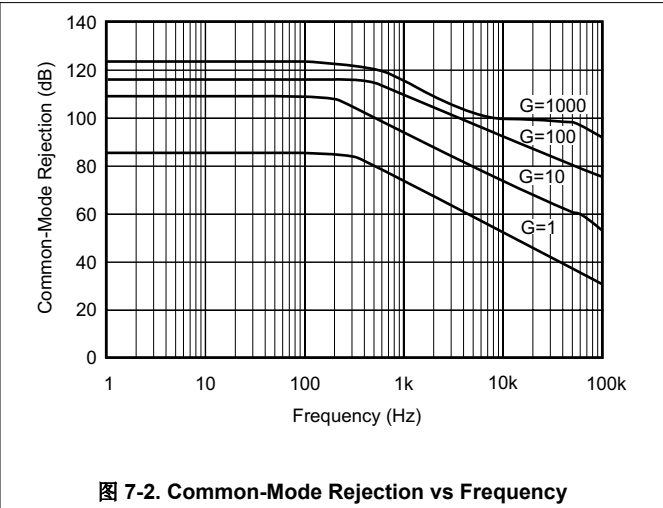
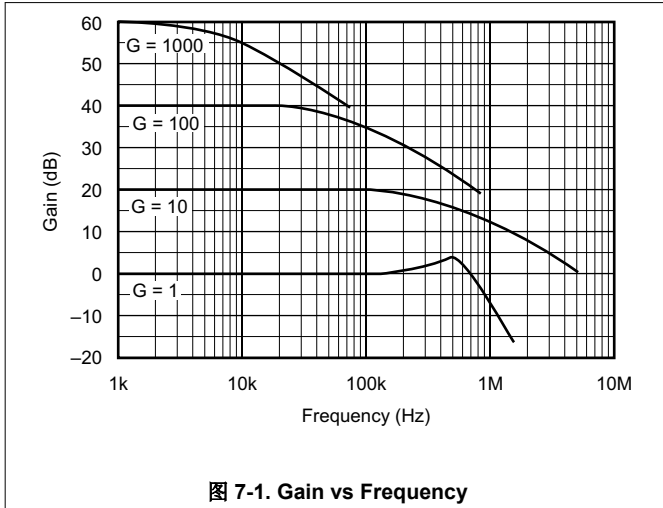
 at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage:	Positive	$R_L = 10\text{ k}\Omega$	$(V^+) - 1$	$(V^+) - 0.8$		V
	Negative	$R_L = 10\text{ k}\Omega$	$(V^-) + 0.35$	$(V^-) + 0.2$		
	Single supply high	$V^+ = 4.5\text{ V}$, $V^- = 0\text{ V}$ ⁽²⁾ , $R_L = 10\text{ k}\Omega$	1.8	2		
	Single supply low	$V^+ = 4.5\text{ V}$, $V^- = 0\text{ V}$ ⁽²⁾ , $R_L = 10\text{ k}\Omega$	60	35		mV
Load capacitance stability				1000		pF
Short circuit current				+5/ - 12		mA
FREQUENCY RESPONSE						
Bandwidth, - 3 dB	G = 1			800		kHz
	G = 10			500		
	G = 100			70		
	G = 1000			7		
Slew rate		$V_O = \pm 10\text{ V}$, G = 10		0.9		V/ μs
Settling time, 0.01%	G = 1			15		μs
	G = 10			15		
	G = 100			21		
	G = 1000			210		
Overload recovery		50% overdrive		20		μs
POWER SUPPLY						
Current		$V_{IN} = 0\text{ V}$		± 350	± 385	μA

- (1) Temperature coefficient of the 50-k Ω term in the gain equation.
 (2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

7.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ (unless otherwise noted)



7.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ (unless otherwise noted)

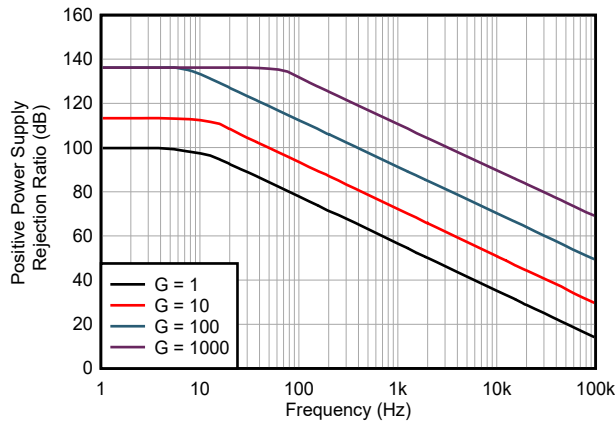


图 7-7. Positive Power Supply Rejection vs Frequency

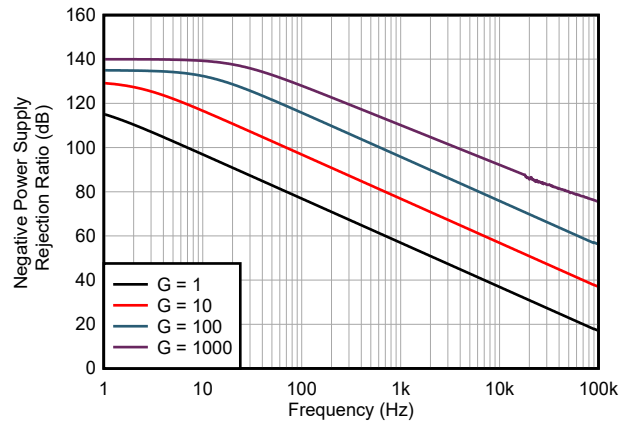


图 7-8. Negative Power Supply Rejection vs Frequency

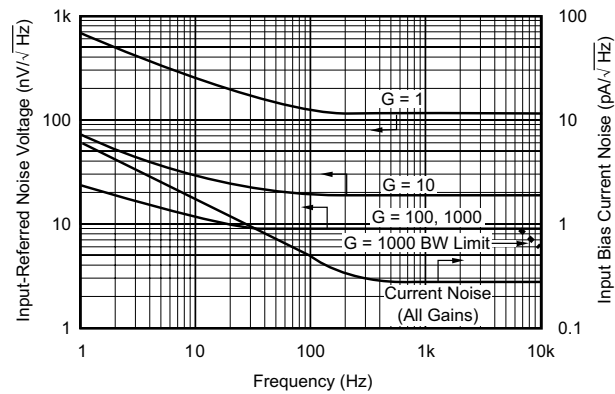


图 7-9. Input-Referred Noise Voltage vs Frequency

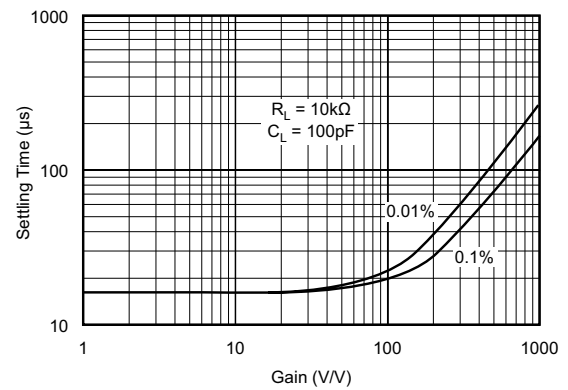


图 7-10. Settling Time vs Gain

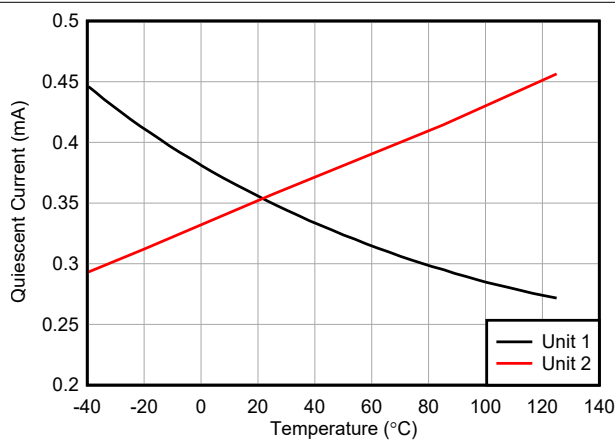


图 7-11. Quiescent Current and Slew Rate vs Temperature

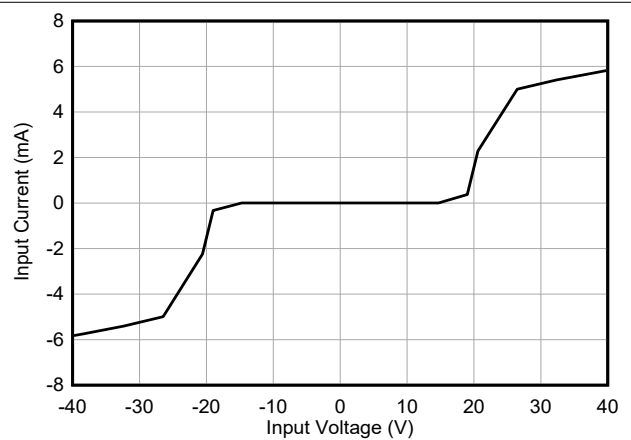


图 7-12. Input Bias Current vs Input Overload Voltage

7.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ (unless otherwise noted)

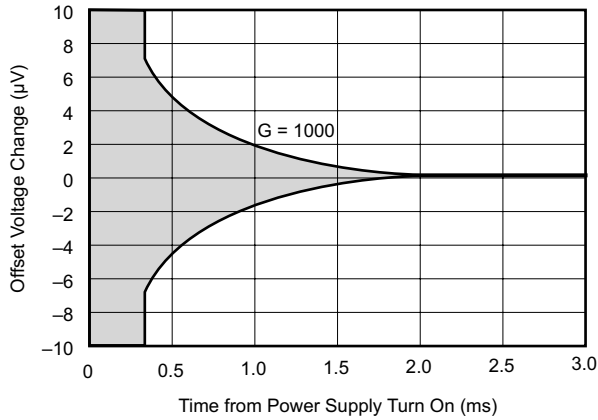


图 7-13. Offset Voltage vs Warm-Up Time

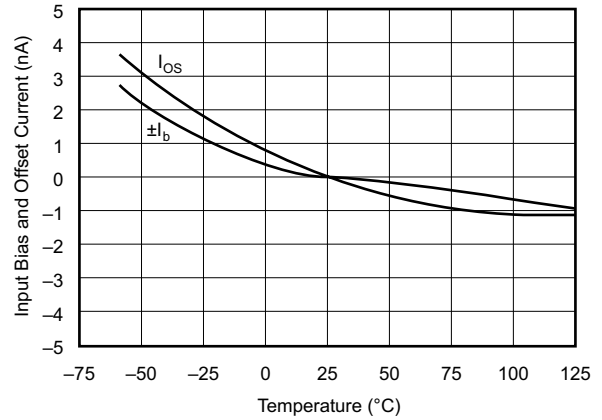


图 7-14. Input Bias and Offset Current vs Temperature

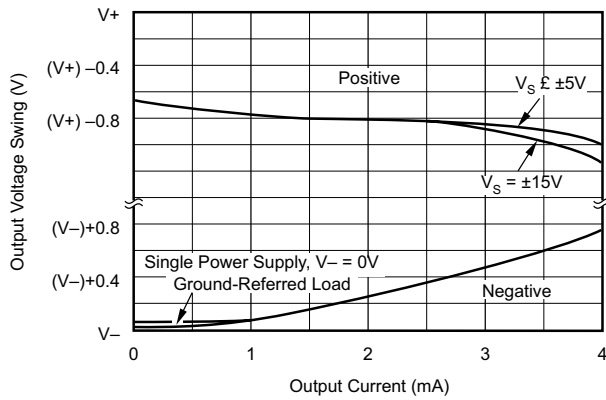


图 7-15. Output Voltage Swing vs Output Current

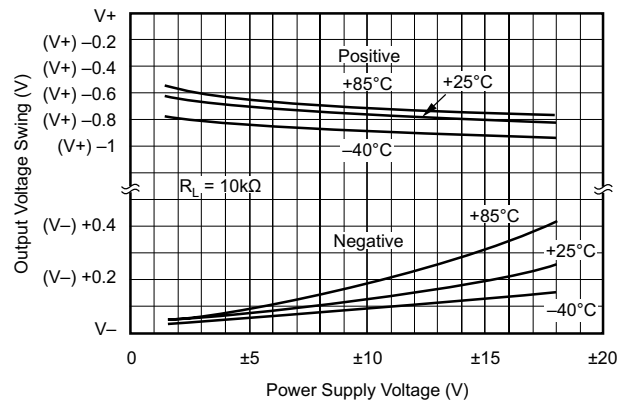


图 7-16. Output Voltage Swing vs Power Supply Voltage

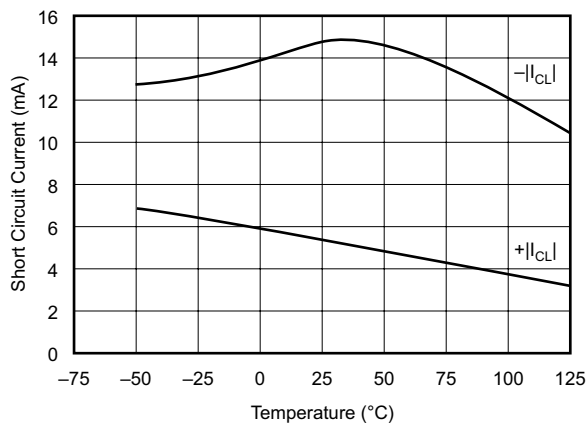


图 7-17. Output Current Limit vs Temperature

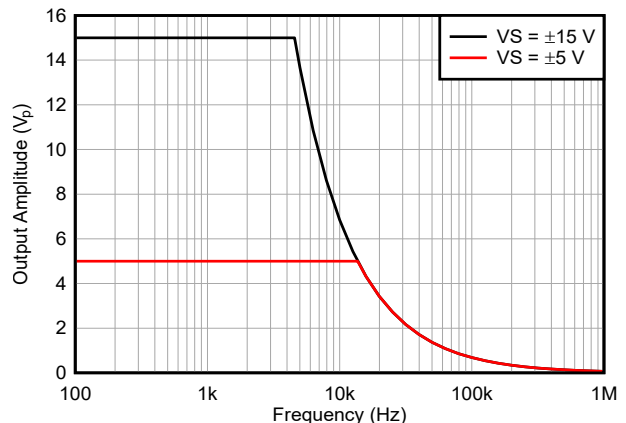
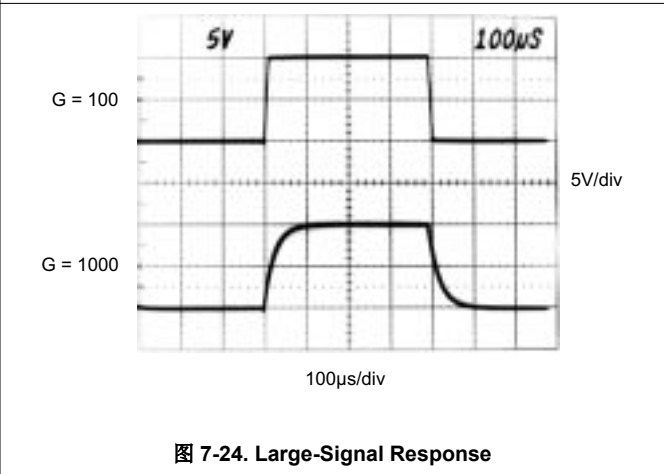
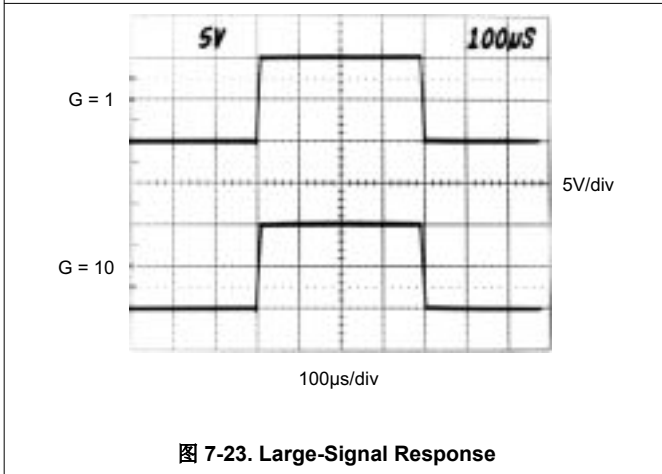
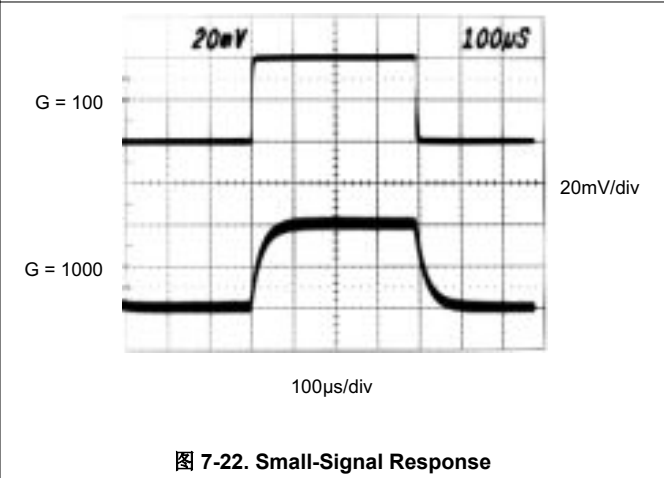
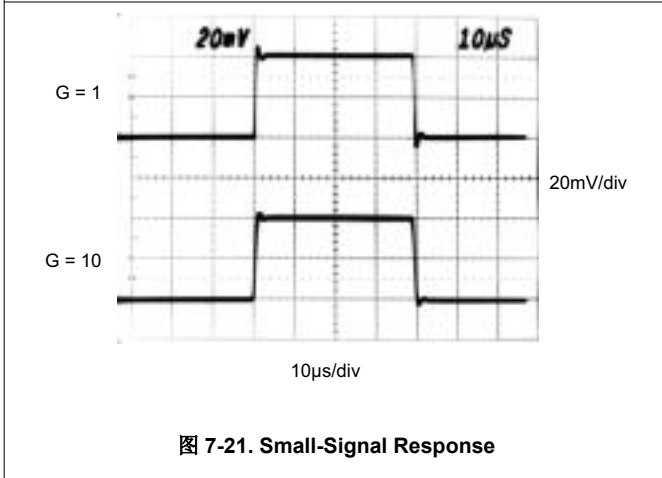
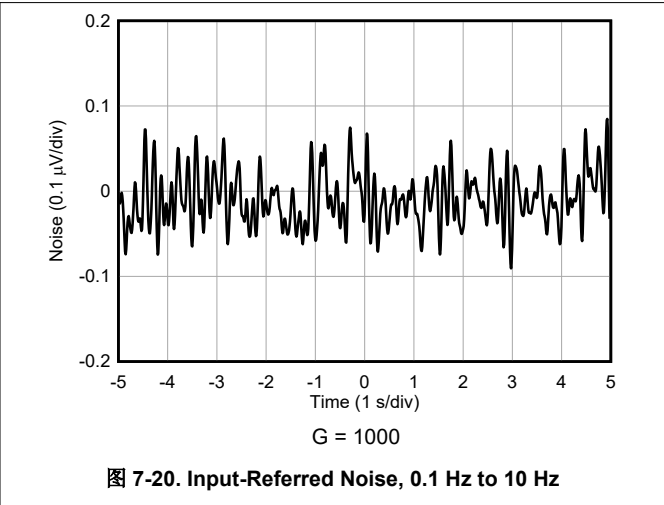
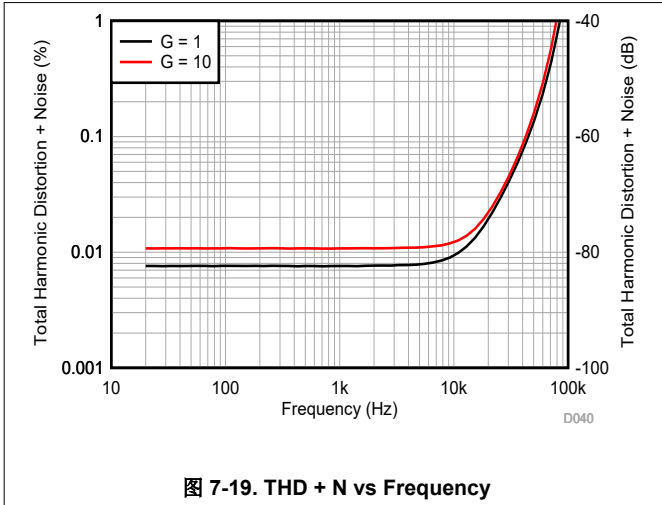


图 7-18. Maximum Output Swing vs Frequency

7.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ (unless otherwise noted)



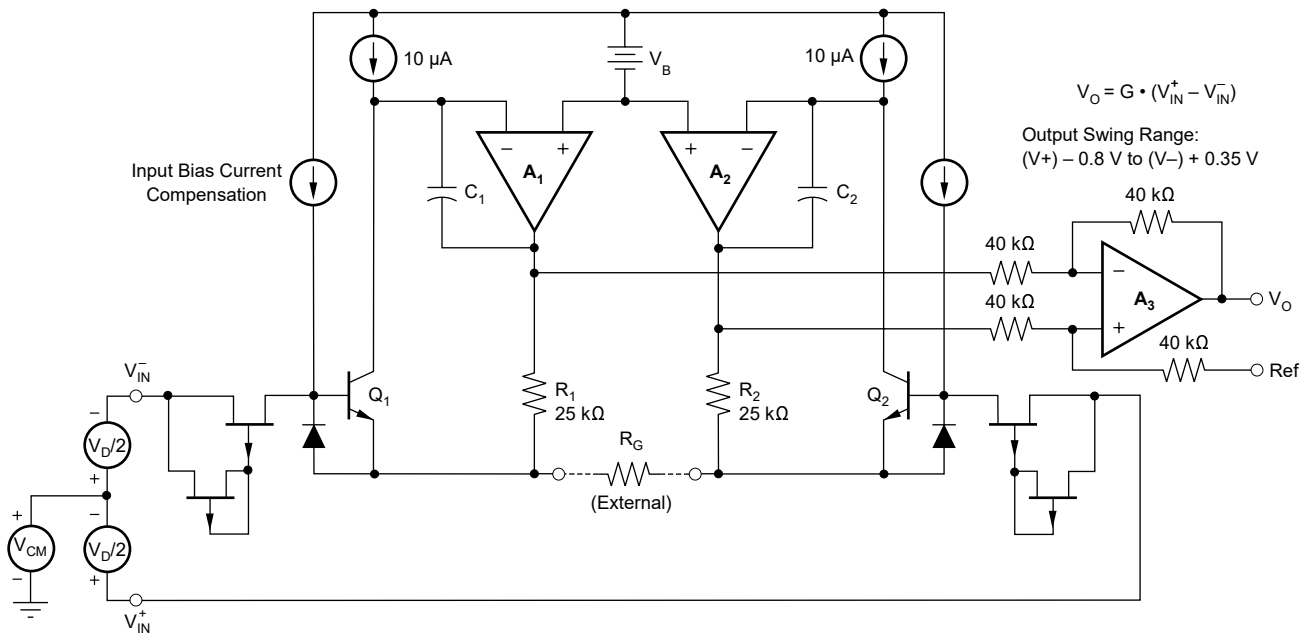
8 Detailed Description

8.1 Overview

节 8.2 shows a simplified representation of the INA118 and provides insight into device operation. Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, thus preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 6 mA.

The differential input voltage is buffered by Q_1 and Q_2 and impressed across R_G , causing a signal current to flow through R_G , R_1 , and R_2 . The output difference amp, A_3 , removes the common-mode component of the input signal and refers the output signal to the Ref pin.

8.2 Functional Block Diagram



8.3 Feature Description

The INA118 input sections use junction field effect transistors (JFET) connected to provide protection up to ± 40 V. The current-feedback architecture provides maximum bandwidth over the full range of gain settings.

8.4 Device Functional Modes

8.4.1 Noise Performance

The INA118 provides low noise in most applications. For differential source impedances less than $1\text{ k}\Omega$, the [INA103](#) may provide lower noise. For source impedances greater than $50\text{ k}\Omega$, the [INA111](#) FET-input instrumentation amplifier may provide lower noise.

The low-frequency noise of the INA118 is approximately $0.28\text{ }\mu\text{V}_{\text{PP}}$, measured from 0.1 Hz to 10 Hz ($G \geq 100$). The INA118 provides dramatically improved noise performance when compared to state-of-the-art, chopper-stabilized amplifiers.

8.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA118 is from approximately 1.4-V less than the positive supply voltage to 1.2-V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2 . Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see also [Figure 7-6](#).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. In this case, the output of the INA118 is near 0 V even though both inputs are overloaded.

8.4.3 Input Protection

The inputs of the INA118 are individually protected for voltages up to ± 40 V. For example, a condition of -40 V on one input and $+40$ V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 6 mA. [Figure 7-12](#) shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

9 应用和实现

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 应用信息

INA118 使用同相和反相输入之间产生的高共模电压测量小差分电压。高共模抑制使得 INA118 成为各种应用的理想选择。能够设置基准引脚来调节输出信号的功能，可提供额外的灵活性，这对于多种配置是实用的。

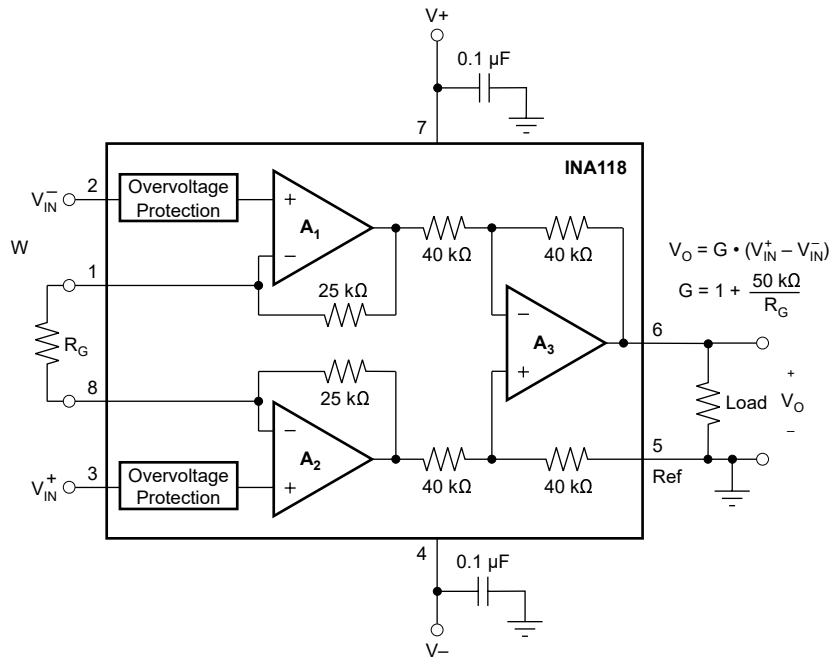
9.2 Typical Application

图 9-1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins, as shown. The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 12 Ω in series with the Ref pin causes a typical device to degrade to approximately 80-dB CMR ($G = 1$).

图 9-1 depicts an input signal with a 5-mV, 1-kHz signal with a 1-V_{PP} common-mode signal, a condition often observed in process-control systems. 图 9-2 depicts the output of the INA118 ($G = 250$) depicting the clean recovered 1-kHz waveform.

DESIRED GAIN	R _G (Ω)	NEAREST 1% R _G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



Also drawn in simplified form:

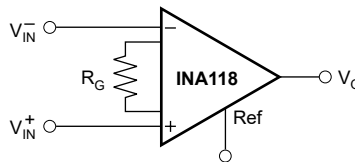


图 9-1. Basic Connections

9.2.1 Design Requirements

图 9-5 和 图 9-4 depict the performance of a typical application of the INA118 in a shop floor-vibration sensing application. Industrial process control systems often involve the interconnecting of multiple subsystems; therefore, ground loops are frequently encountered, and often are not easily solved. The inherent common-mode rejection of instrumentation amplifiers enables accurate measurements even in the presence of ground-loop potentials.

The typical application was tested in a system with these requirements:

- Transducer signal $\approx 5 \text{ mV}_{PP}$
- Transducer center frequency = 1 kHz
- Common-mode signal (required to be rejected): 1 V_{PP} at 60 Hz

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

As shown in 方程式 1, the gain of the INA118 is set by connecting a single external resistor, R_G, connected between pins 1 and 8.

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in 图 9-1.

The 50-k Ω term in 方程式 1 comes from the sum of the two internal feedback resistors of A₁ and A₂. These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from 方程式 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

图 7-1 shows that, despite a low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This achievement is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3-dB peaking at 500 kHz in unity gain. This peaking is a result of the current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable 6-dB/octave due to a zero in the amplifier response. A simple pole at 300 kHz or less produces a flat pass-band unity gain response.

9.2.2.3 Offset Trimming

The INA118 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. 图 9-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is summed at the output. The op amp buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

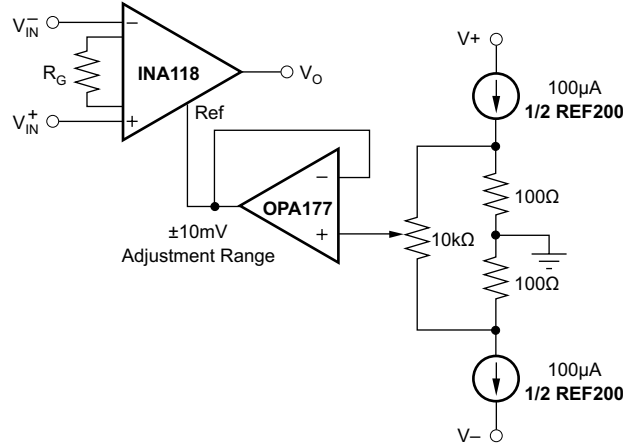


图 9-2. Optional Trimming of Output Offset Voltage

9.2.2.4 Input Bias Current Return Path

The input impedance of the INA118 is extremely high at approximately $10^{10} \Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 5 \text{ nA}$. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential which exceeds the common-mode range of the INA118, and the input amplifiers saturates.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in 图 9-3). With higher source impedance, using two equal resistors provides a balanced input, with the possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

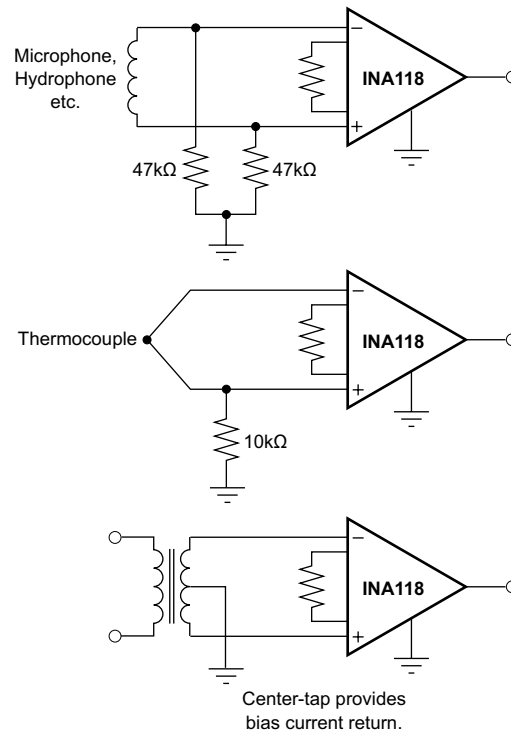
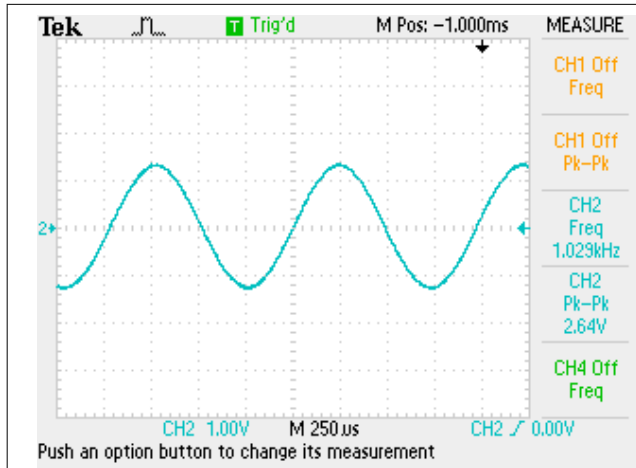


图 9-3. Providing an Input Common-Mode Current Path

9.2.3 应用曲线



1kHz 差分信号也存在，但在该波形中看不到。

图 9-4. 显示 60Hz 共模信号的典型应用的输入

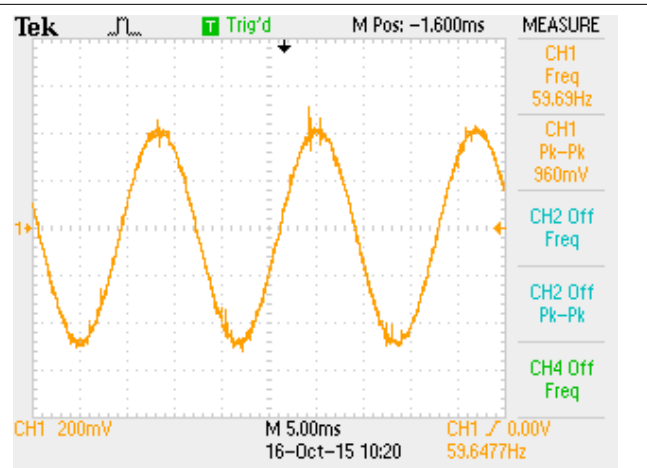


图 9-5. 典型应用的输出显示了所需的 1kHz 波形，共模干扰被抑制

9.3 Power Supply Recommendations

9.3.1 Low-Voltage Operation

The INA118 operates on power supplies as low as ± 2.25 V. Performance of the INA118 remains excellent with power supplies ranging from ± 2.25 V to ± 18 V. Most parameters vary only slightly throughout this supply voltage range; see also 节 7.6. Operation at low supply voltage requires careful attention to make sure that the input voltages remain within the respective linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. 图 7-3 shows the range of linear operation for a various supply voltages and gains.

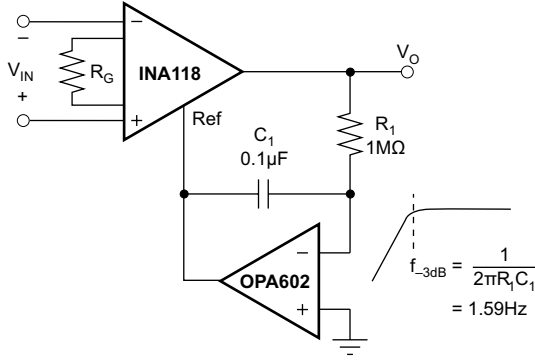
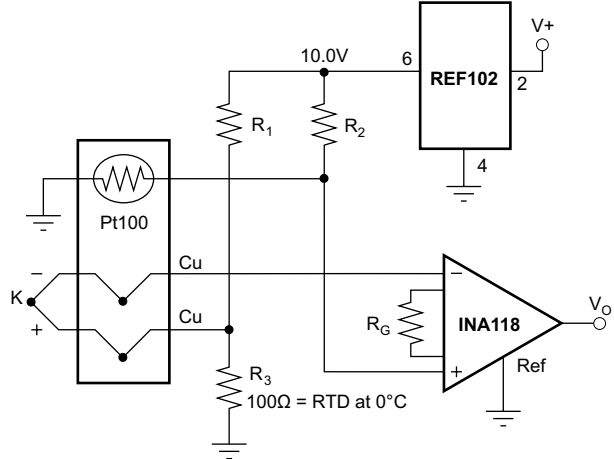


图 9-6. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	COEFFICIENT (μV/°C)	R ₁ , R ₂
E	+ Chromel	58.5	66.5kΩ
	- Constantan		
J	+ Iron	50.2	76.8kΩ
	- Constantan		
K	+ Chromel	39.4	97.6kΩ
	- Alumel		
T	+ Copper	38.0	102kΩ
	- Constantan		

图 9-7. Thermocouple Amplifier With Cold Junction Compensation

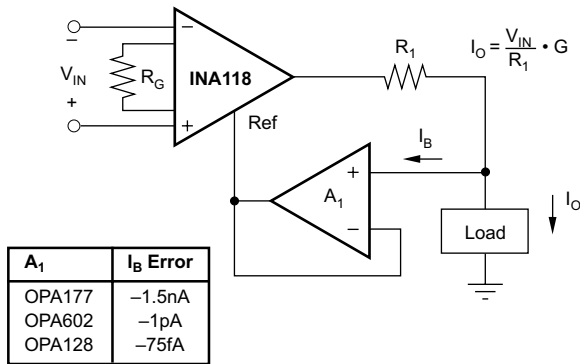


图 9-8. Differential Voltage to Current Converter

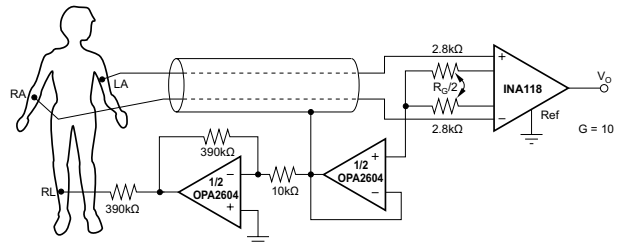


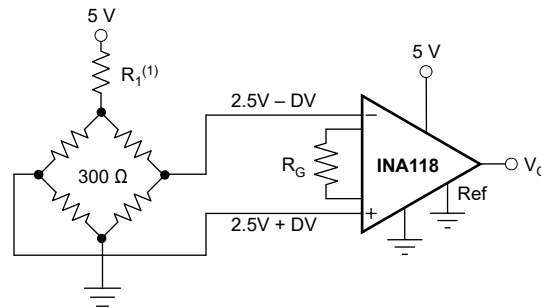
图 9-9. ECG Amplifier With Right-Leg Drive

9.3.2 Single-Supply Operation

The INA118 can be used on single power supplies of 4.5 V to 36 V. 图 9-10 shows a basic single-supply circuit. The output Ref pin is connected to ground. Zero differential input voltage demands an output voltage of 0 V (ground). The actual output voltage swing is limited to approximately 35-mV above ground, when the load is referred to ground as shown. 图 7-15 shows how the output voltage swing varies with output current.

With single supply operation, V^+_{IN} and V^-_{IN} must be 1.2-V greater than ground for linear operation. Connecting the inverting input to ground and measuring a voltage connected to the noninverting input is not possible.

To illustrate the issues affecting low-voltage operation, consider the circuit in 图 9-10, which shows the INA118 operating from a single 5-V supply. Depending on the desired gain, a resistor in series with the high side of the bridge can be required to make sure that the bridge output voltage is within the common-mode range of the amplifier inputs. See 图 7-5 for 5-V single supply operation.



NOTE: (1) R_1 may be required to create proper common-mode voltage, for low voltage operation with certain gains — see text.

图 9-10. Single-Supply Bridge Amplifier

9.4 Layout

9.4.1 Layout Guidelines

TI always recommends paying attention to good layout practices. For best operational performance of the device, use good printed-circuit-board (PCB) layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G , select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and of the individual device. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V^+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Keep the traces as short as possible.

9.4.2 Layout Example

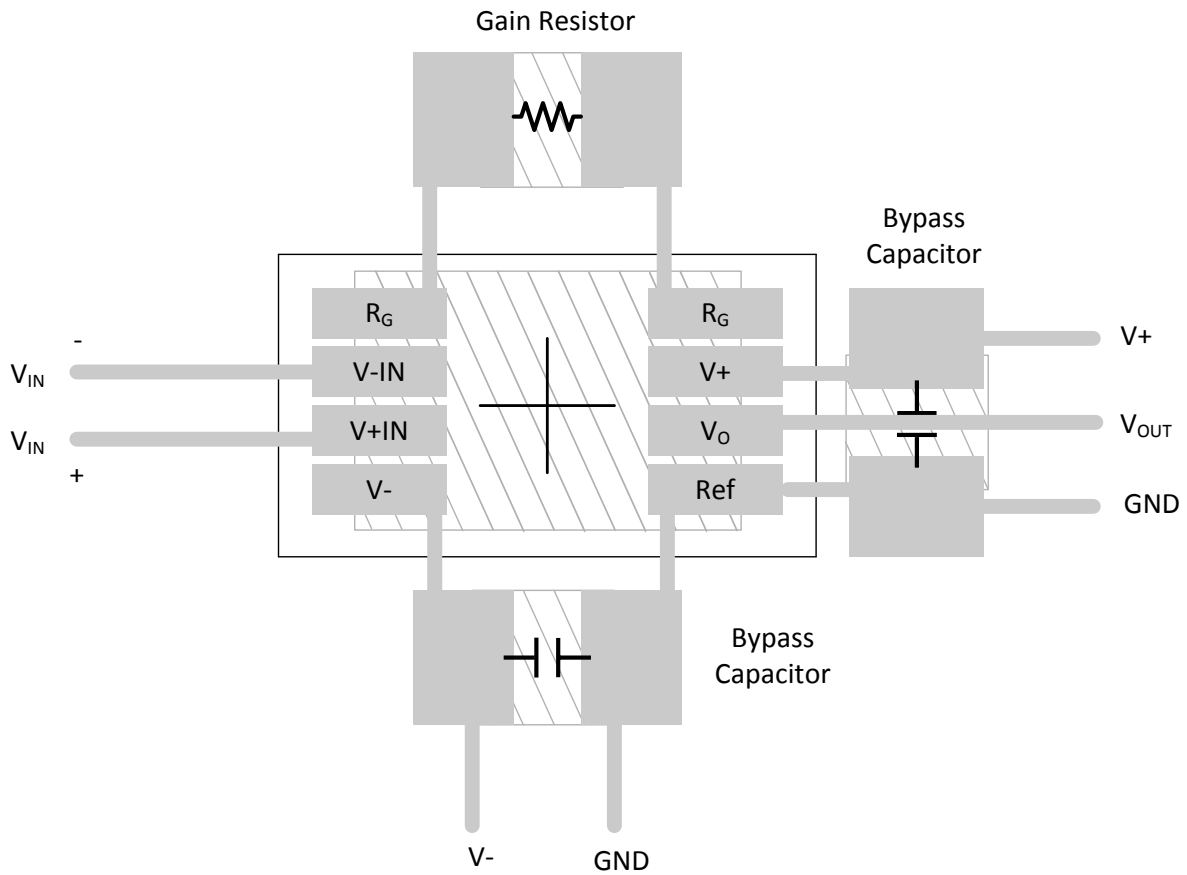


图 9-11. Layout Recommendation

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

表 10-1. Design Kits and Evaluation Modules

NAME	PART NUMBER	TYPE
DIP adapter evaluation module	DIP-ADAPTER-EVM	Evaluation modules and boards
Universal instrumentation amplifier evaluation module	INAEVM	Evaluation modules and boards

表 10-2. Development Tools

DESCRIPTION	PART NUMBER	TYPE
Analog engineer's calculator	ANALOG-ENGINEER-CALC	Calculation tool
TINA-TI™ software: SPICE-based analog simulation program	TINA-TI	Circuit design and simulation
PSpice® for TI design and simulation tool	PSPICE-FOR-TI	Circuit design and simulation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA118P	Last Time Buy	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 85	INA118P
INA118P.A	NRND	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 85	INA118P
INA118P.B	NRND	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 85	INA118P
INA118PB	Last Time Buy	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-	INA118P B
INA118PB.A	NRND	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 85	INA118P B
INA118PB.B	NRND	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 85	INA118P B
INA118U	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 118U
INA118U.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U
INA118U.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U
INA118U/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 118U
INA118U/2K5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U
INA118U/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U
INA118U/2K5G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	See INA118U/2K5	INA 118U
INA118UB	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 118U B
INA118UB.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U B
INA118UB.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U B

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA118UB/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 118U B
INA118UB/2K5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U B
INA118UB/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 118U B
INA118UBG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	See INA118UB	INA 118U B
INA118UG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	See INA118U	INA 118U

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA118U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA118U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA118UB/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA118P	P	PDIP	8	50	506	13.97	11230	4.32
INA118P	P	PDIP	8	50	506	13.97	11230	4.32
INA118P.A	P	PDIP	8	50	506	13.97	11230	4.32
INA118P.A	P	PDIP	8	50	506	13.97	11230	4.32
INA118P.B	P	PDIP	8	50	506	13.97	11230	4.32
INA118P.B	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB.A	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB.A	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB.B	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB.B	P	PDIP	8	50	506	13.97	11230	4.32
INA118U	D	SOIC	8	75	506.6	8	3940	4.32
INA118U.A	D	SOIC	8	75	506.6	8	3940	4.32
INA118U.B	D	SOIC	8	75	506.6	8	3940	4.32
INA118UB	D	SOIC	8	75	506.6	8	3940	4.32
INA118UB.A	D	SOIC	8	75	506.6	8	3940	4.32
INA118UB.B	D	SOIC	8	75	506.6	8	3940	4.32
INA118UBG4	D	SOIC	8	75	506.6	8	3940	4.32
INA118UG4	D	SOIC	8	75	506.6	8	3940	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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最后更新日期：2025 年 10 月