INA300 过流保护、电流检测比较器

1 特性

- 宽共模范围：0V 至 36V
- 可选响应时间：
  - 10μs、50μs、100μs
- 可编程阈值：
  - 使用单个电阻调节
  - 可编程范围为 0mV 到 250mV
- 精度：
  - 失调电压：±500 μ V（最大值）
  - 失调电压漂移：0.5 μ V/°C（最大值）
- 可选迟滞：
  - 2mV、4mV、8mV
- 有源静态电流：135 μ A（最大值）
- 可选禁用模式
  - 已禁用静态电流：3.5 μ A（最大值）
  - 已禁用输入偏置电流：500nA（最大值）
- 锁存模式可用时的开漏输出

2 应用

- 过流保护
- 计算机
- 服务器
- 电信设备
- 电源
- 电池充电器

3 说明

INA300 为过电流保护应用而设计，是一个电流检测比较器，通过测量分流电阻器上形成的电压，并将该电压与阈值电压输入水平进行比较，从而检测过电流。此器件可在 0V 至 36V 的共模电压范围内测量该差分电压信号，与电源电压无关。INA300 器件具有可调阈值范围，此范围由单个外部限值设定电阻器来设置。可选迟滞功能可调节比较器的运行情况，以适应 0mV 至 250mV 的宽输入信号范围。

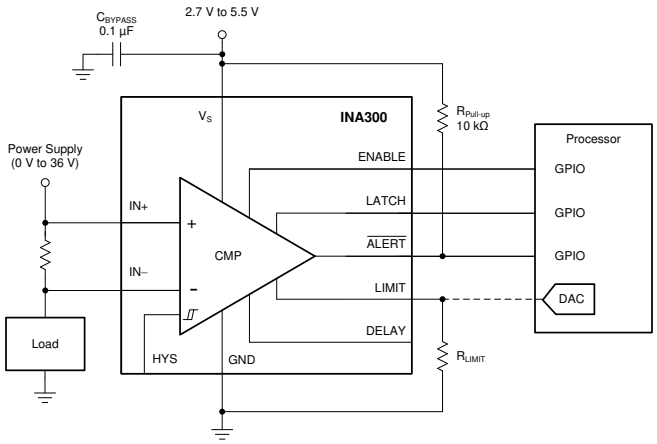
器件上的开漏警报输出可配置为透明模式（输出状态与输入状态保持一致）或锁存模式（清零锁存时清除报警输出）。器件响应时间设置是可选的，10μs 内即可迅速发出过流警报。

INA300 器件由 2.7V-5.5V 单电源供电运行，最大电源电流消耗为 135μA。INA300 器件的额定工作温度范围为 -40°C 至 +125°C，采用 WSON-10 和 VSSOP-10 封装。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
INA300	WSON (10)	2.00mm x 2.00mm
	VSSOP (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



典型应用原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2016) to Revision C (June 2021)	Page
• Changed 图 7-6 caption	16

Changes from Revision A (March 2014) to Revision B (April 2016)	Page
• 更改了数据表标题	1
• 向数据表添加了 VSSOP (DGS) 封装	1
• 更改了“说明”部分的文本，使之更加清晰	1
• Moved storage temperature from Handling Ratings table to Absolute Maximum Ratings table	4
• Changed Handling Ratings to ESD Ratings	4
• Added DGS data to *Thermal Information* table	4

Changes from Revision * (February 2014) to Revision A (March 2014)	Page
• 更改了产品预览数据表	1

5 Pin Configuration and Functions

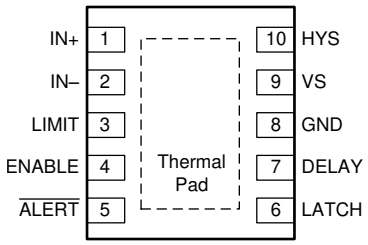


图 5-1. DSQ Package 10-Pin WSON Top View

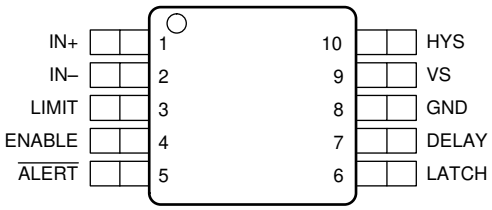


图 5-2. DGS Package 10-Pin VSSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN+	Analog input	Connect to supply side of shunt resistor.
2	IN –	Analog input	Connect to load side of shunt resistor.
3	LIMIT	Analog input	Alert threshold limit input. See *Setting The Current-Limit Threshold* for details on setting limit threshold.
4	ENABLE	Digital input	Enable or disable selection input
5	ALERT	Digital output	Overlimit alert, active-low, open-drain output.
6	LATCH	Digital input	Transparent or latch mode selection input.
7	DELAY	Digital input	Response time selection input.
8	GND	Analog	Ground
9	VS	Analog	Power supply, 2.7 V to 5.5 V.
10	HYS	Digital input	Hysteresis setting input. See *Selectable Hysteresis* for hysteresis settings.
	Thermal pad	—	This pad can be connected to ground or left floating.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs (IN+, IN–)	Differential (V_{IN+}) – (V_{IN-})(2)	–40	40	V
	Common-mode (3)	GND – 0.3	40	
Analog input	LIMIT	GND – 0.3	(V_S) + 0.3	V
Digital inputs	LATCH, DELAY, ENABLE, HYS	GND – 0.3	(V_S) + 0.3	V
Alert output		GND – 0.3	6	V
Operating temperature		–40	125	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– terminals, respectively.
(3) Input voltage may exceed the voltage shown if the current at that terminal is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage	2.7	3.3	5.5	V
	Delay setting		100		µs
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA300		UNIT
		DSQ (WSON)	DGS (VSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.5	169.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	59.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	89.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	88.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-} = 0 mV, V_S = 3.3 V, V_{IN+} = 12 V, V_{LIMIT} = 10 mV, and DELAY = 100 µs (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input voltage		0		36	V
V_{IN}	Differential input voltage	V_{IN} = V_{IN+} – V_{IN-}	0		250	mV
CMR	Common-mode rejection	V_{IN+} = 0 V to 36 V, T_A = –40°C to 125°C	100	120		dB
V_{OS}	Offset voltage, RTI(1)	V_S = 3.3 V, DELAY = 100 µs		–75	–500	µV
		V_S = +3.3 V, DELAY = 50 µs		–125	–500	
		V_S = +3.3 V, DELAY = 10 µs(2)		–350	–650	
dV_{OS}/dT	Offset voltage drift, RTI(1)	T_A = –40°C to 125°C		0.1	0.5	µV/°C
PSR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, T_A = –40°C to 125°C		75	150	µV/V
I_B	Input bias current			5	10	µA
		Disable mode		0.05	0.5	
I_{OS}	Input offset current			±0.1		µA
I_{LIMIT}	Limit threshold output current	T_A = 25°C	19.9	20	20.1	µA
		T_A = –40°C to 125°C	19.85		20.15	
DIGITAL INPUT/OUTPUT						
t_p	Alert propagation delay	Delay = open, overdrive = 1 mV		10		µs
		Delay = GND, overdrive = 1 mV		50		
		Delay = V_S, overdrive = 1 mV		100		
HYS	Hysteresis	HYS = open		2		mV
		HYS = GND		4		
		HYS = V_S		8		
V_{IH}	High-level input voltage	Latch, enable	1.4		6	V
		Delay, hysteresis	V_S – 0.5		6	
V_{IL}	Low-level input voltage	Latch, enable	0		0.4	V
		Delay, hysteresis	0		0.5	
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA		50	400	mV
	$\overline{\text{ALERT}}$ terminal leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	Digital leakage input current	0 ≤ V_{IN} ≤ V_S		1	2	µA
POWER SUPPLY						
I_Q	Quiescent current	V_{SENSE} = 0 mV, T_A = 25°C		115	135	µA
		T_A = –40°C to 125°C			150	
		V_{SENSE} = 0 mV, disable mode, HYS = 2 mV		2	3.5	

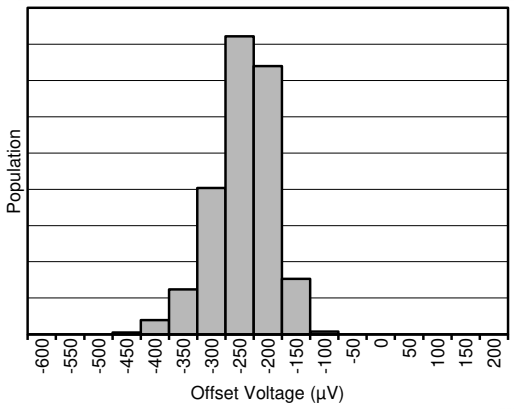
(1) RTI = referred-to-input.
(2) Absolute-maximum values are tested with the threshold limit set using the corresponding noise adjustment factor (NAF) value. See 节 7.3.7 for additional information on applying the NAF value.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
	Start-up time		1		ms
t_{en}	Enable time		300		µs
t_{dis}	Disable time		20		µs

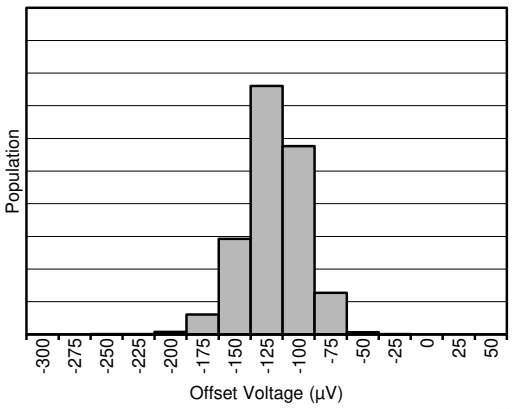
6.7 Typical Characteristics

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, alert pull-up resistor = 10 kΩ, and Delay = 100 µs (unless otherwise noted)



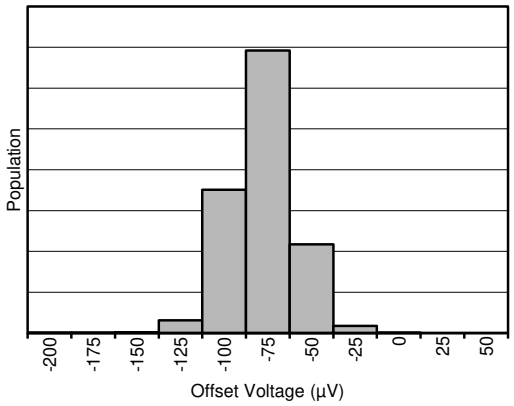
Delay = 10 µs

图 6-1. Input Offset Voltage



Delay = 50 µs

图 6-2. Input Offset Voltage



Delay = 100 µs

图 6-3. Input Offset Voltage

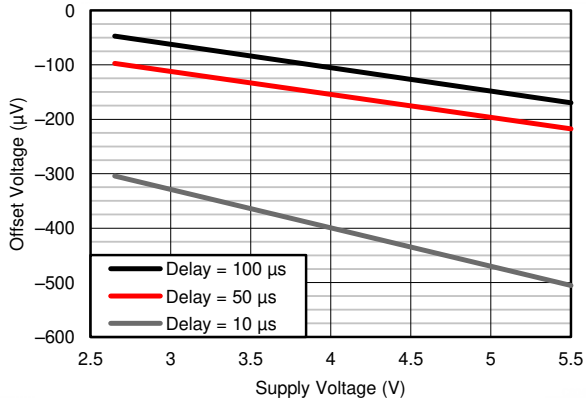


图 6-4. Input Offset Voltage vs Supply Voltage

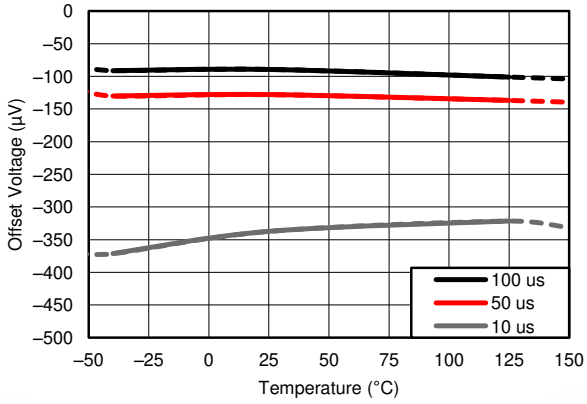


图 6-5. Input Offset Voltage vs Temperature

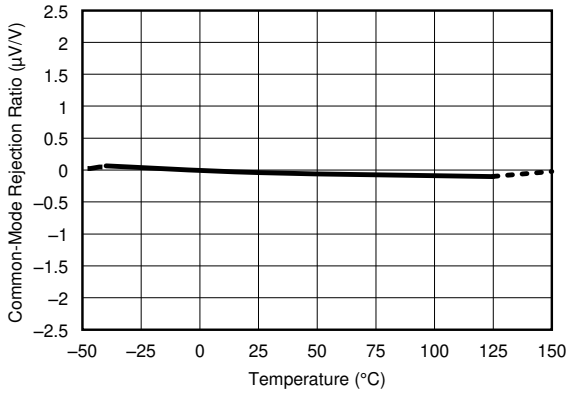


图 6-6. Common-Mode Rejection Ratio vs Temperature

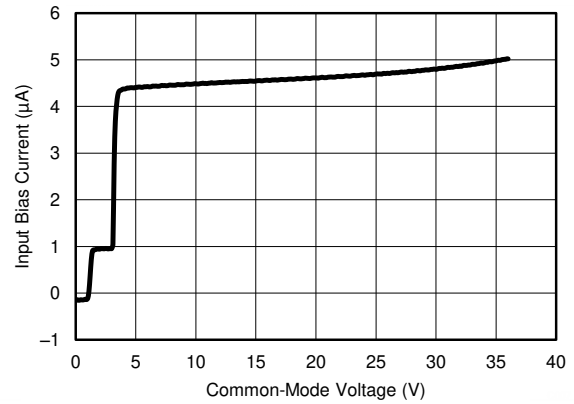


图 6-7. Input Bias Current vs Common-Mode Voltage (Enabled)

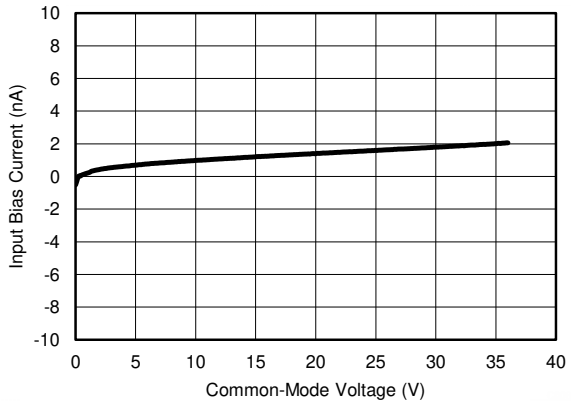


图 6-8. Input Bias Current vs Common-Mode Voltage (Disabled)

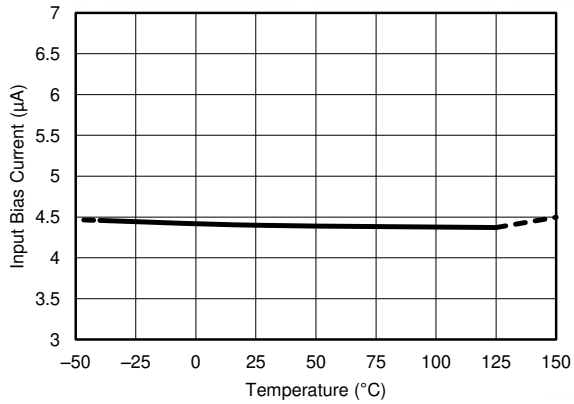


图 6-9. Input Bias Current vs Temperature (Enabled)

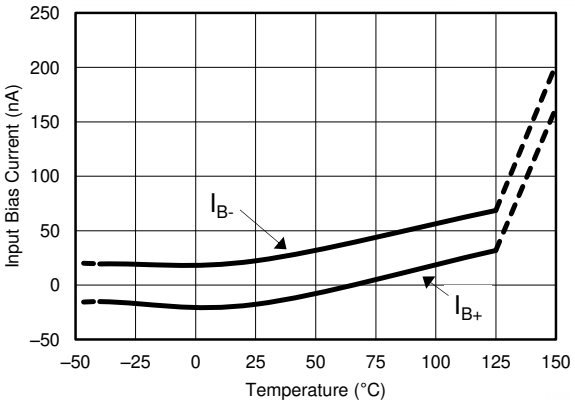


图 6-10. Input Bias Current vs Temperature (Disabled)

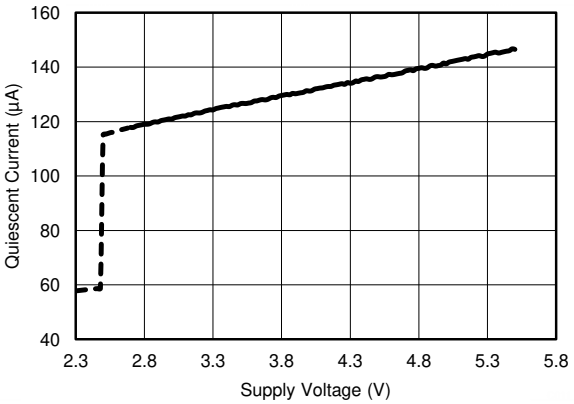


图 6-11. Quiescent Current vs Supply Voltage (Enabled)

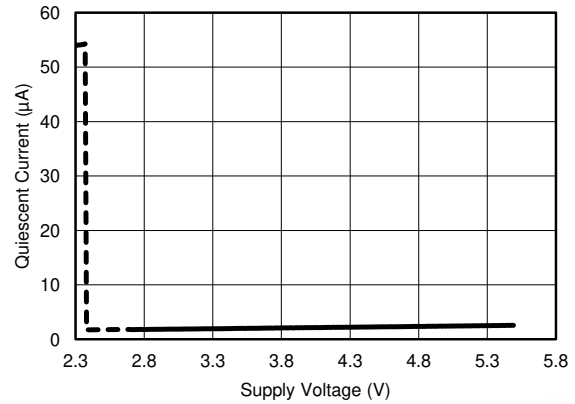


图 6-12. Quiescent Current vs Supply Voltage (Disabled)

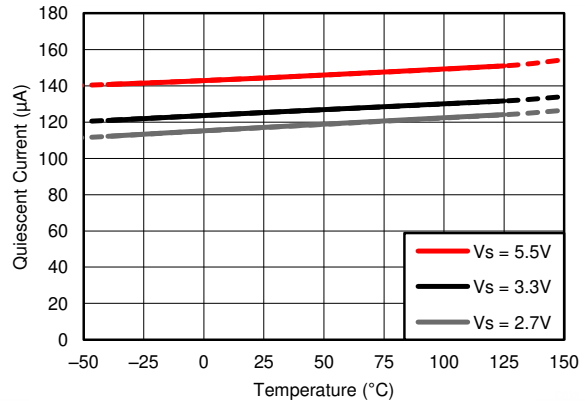


图 6-13. Quiescent Current vs Temperature (Enabled)

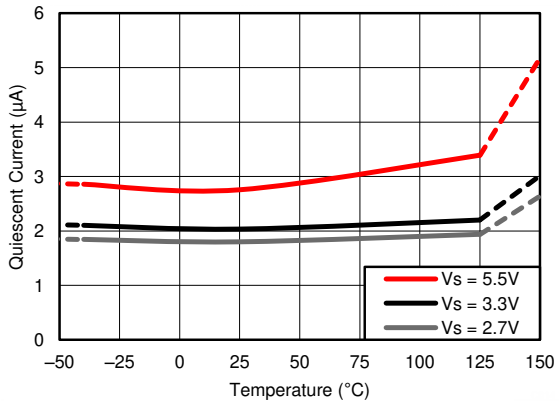


图 6-14. Quiescent Current vs Temperature (Disabled)

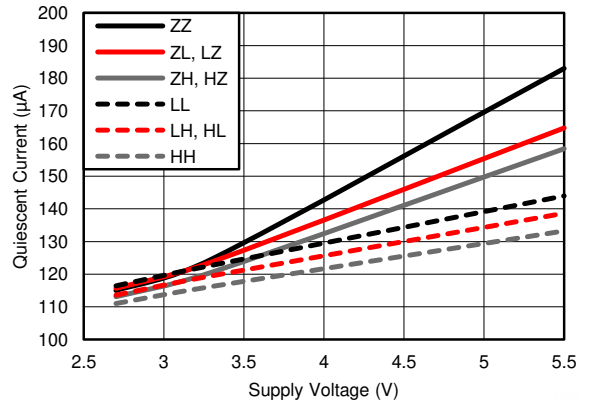


图 6-15. Quiescent Current vs HYS and DELAY Settings (Enabled)

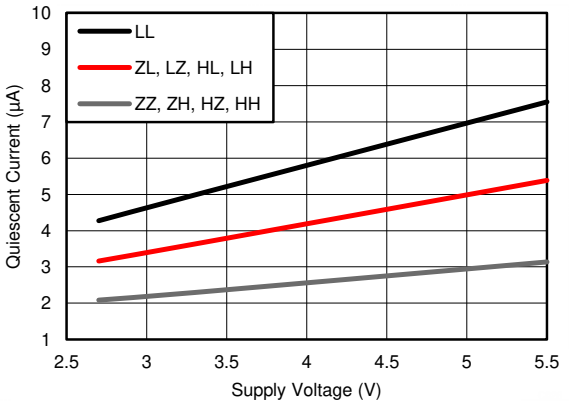


图 6-16. Quiescent Current vs HYS and DELAY Settings (Disabled)

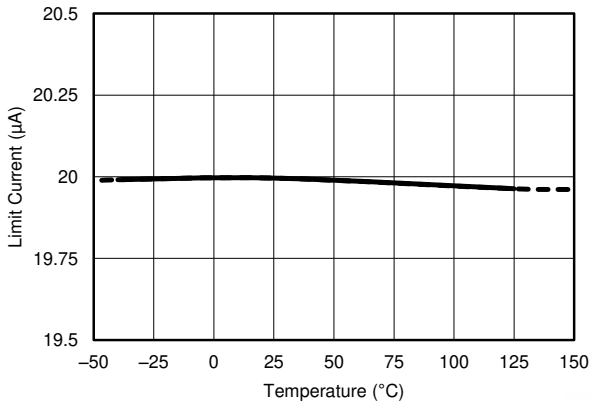


图 6-17. Limit Current Source vs Temperature

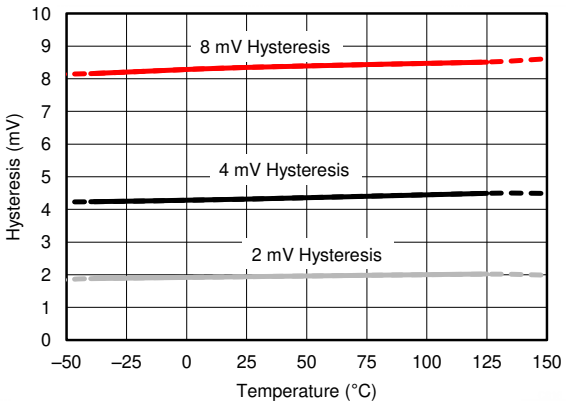


图 6-18. Hysteresis vs Temperature

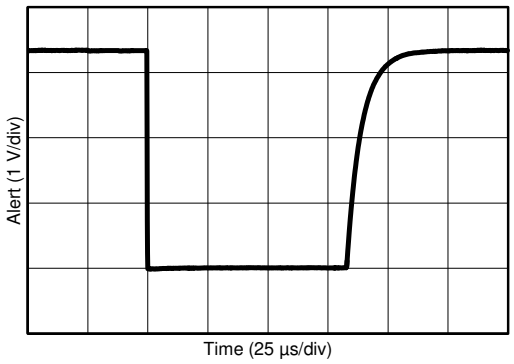


图 6-19. Alert Step Response

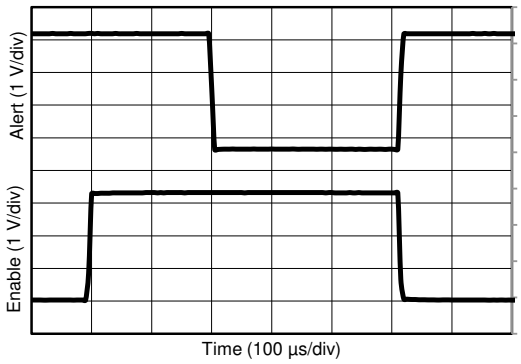


图 6-20. Alert Response (Disable to Enable)

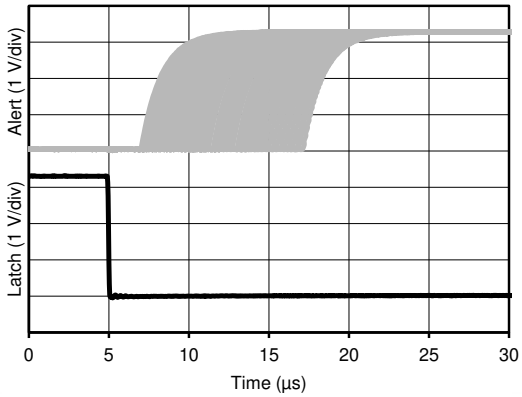


图 6-21. Alert Response (Latch Mode to Transparent Mode)

7 Detailed Description

7.1 Overview

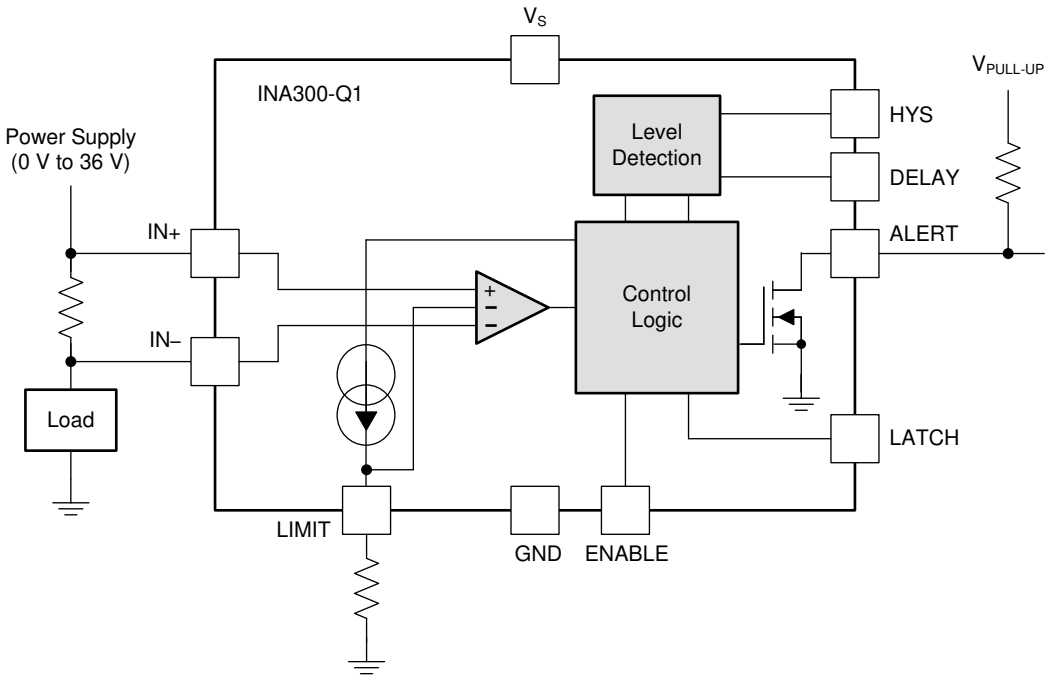
The INA300 INA300 is a 36-V, common-mode comparator designed for overcurrent protection applications. To reduce the system component count, this device combines the current-sense amplifier and threshold comparison into a single product for the overcurrent detection function. Programming this comparison threshold is configured through a single external resistor, which simplifies the current design while allowing for easy adjustments to the threshold when needed. The threshold setting resistor value is selected based on an internal 20-µA current source to achieve a corresponding signal to the voltage that develops across the current-sensing or current-shunt resistor in series with the monitored load current.

The device is designed to accommodate a range of application requirements, including common-mode voltage, noise thresholds, and signal ranges. A wide signal threshold range reaching up to 250 mV is available to accommodate both power-sensitive applications requiring small dissipations across a current sense resistor and larger current-sensing resistors used in lower current applications.

Additional features available with the INA300 INA300 device include a disable mode for reducing the current consumption of the device to below 10 µA, an output mode selector to enable a latched or transparent alert output, and a selectable hysteresis value and alert response delay.

The wide signal range of the device is further enhanced with an adjustable hysteresis value to adjust the characteristics of the comparator, which allows for better accommodation of the full input range. The selectable alert response delays present in the INA300 INA300 device assist in optimizing device operation to account for the system noise levels and operating characteristics required from this device. Longer delay settings allow for added rejection of system noise, thus reducing the potential for false alerts resulting from noise spikes that can occur in high-speed comparators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Selecting a Current-Sensing Resistor

The device measures the differential voltage developed across a resistor when current flows through it to determine if the monitored current exceeds a defined limit. This resistor is referred to as a *current-sensing*

resistor or a *current-shunt resistor*, with each term used interchangeably. The flexible design of the device allows for measuring a wide differential input signal range across this current-sensing resistor, which can extend up to 250 mV.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow more accurate measurements. This large signal accuracy improvement results from the fixed internal amplifier errors that are dominated by the inherent input offset voltage of the device. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of measured signal.

A system design trade-off for improving the measurement accuracy using larger input signals is the increase in power across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of low ohmic-value resistors are becoming available with values as low as 200 μΩ, with power dissipations of up to 5 W that enable large currents to be monitored with sensing resistors.

7.3.1.1 Selecting a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires a 5% measurement accuracy for detecting a 10-A overcurrent event at a 50-μs delay setting where only 250 mW is allowable for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Some initial assumptions are made that are used in this example: the limit setting resistor, R_{LIMIT}, is a 1% component and the maximum tolerance specification for the internal threshold setting current source, 0.5%, is used. Given the total error budget of 5%, up to 3.5% of error is available to be attributed to the internal offset of the device.

As shown in 表 7-1, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 5% maximum total error to reduce the value of the current-sensing resistor and reduce the power dissipation further. Selecting a 1.5-mΩ, current-sensing resistor value offers a tradeoff for reducing the power dissipation in this scenario by approximately 40%, while still remaining within the defined accuracy region.

表 7-1. Calculating the Current-Sensing Resistor, R_{SENSE}

PARAMETER		EQUATION	VALUE	UNIT
	Maximum measurement error		5%	
I_{MAX}	Maximum current		10	A
P_{RSENSE}	Maximum allowable R_{SENSE} power dissipation	$R_{SENSE} \times I_{MAX}^2$	250	mW
	Initial error	R_{LIMIT} + I_{LIMIT} tolerances	1.5%	
R_{SENSE_MAX}	Maximum sensing resistor value	P_{RSENSE} / I_{MAX}^2	2.5	mΩ
V_{SENSE_MAX}	Input sense voltage	$R_{SENSE\_MAX} \times I_{MAX}$	25	mV
V_{OS} Error	Offset voltage error	(V_{OS} / V_{SENSE_MAX}) × 100	2%	
Error_Available	Maximum allowable offset error	Maximum Error – Initial Error	3.5%	
V_{SENSE_MIN}	Minimum input sense voltage	V_{OS} / (Error_Available / 100)	14.3	mV
R_{SENSE_MIN}	Minimum sensing resistor value	V_{SENSE_MIN} / I_{MAX}	1.43	mΩ
P_{RSENSE_MIN}	Minimum power dissipation	$R_{SENSE\_MIN} \times I_{MAX}^2$	143	mW

7.3.2 Setting The Current-Limit Threshold

The device determines if an overcurrent event is present by comparing the measured differential voltage developed across the current-sensing resistor to the corresponding signal programmed at the LIMIT terminal. The threshold voltage for the LIMIT terminal can be set using a resistor or an external voltage source.

7.3.2.1 Resistor-Controlled Current Limit

The typical approach for setting the limit threshold voltage is to connect a resistor from the LIMIT terminal to ground. The value of this resistor, R_{LIMIT}, is chosen to create a corresponding voltage at the LIMIT terminal equivalent to the voltage, V_{TRIP}, developed by the load current flowing through the current-sensing resistor. An internal 20-µA current source is present at the LIMIT terminal that creates the corresponding voltage depending on the value of R_{LIMIT}. In the equations from 表 7-2, V_{TRIP} represents the overcurrent threshold the device is programmed to monitor for and V_{LIMIT} is the programmed signal set to detect the V_{TRIP} level. The term *noise adjustment factor* (NAF) is included in the V_{LIMIT} equation for the 10-µs delay setting. This value is equal to 500 µV and adjusts the operating point for the internal noise in this delay setting. The 50-µs and 100-µs delay settings do not use the NAF term in calculating the V_{LIMIT} threshold. See *Noise Adjustment Factor (NAF)* for more details on the noise adjustment factor.

In 表 7-2, the process for calculating the required value for R_{LIMIT} to set the appropriate threshold voltage, V_{LIMIT}, is shown. This calculation is based on the 10-µs delay setting so the NAF term is included in the calculation. For a delay setting of 50 µs or 100 µs, the NAF term is omitted.

表 7-2. Calculating the Limit Threshold Setting Resistor, R_{LIMIT}

PARAMETER		EQUATION
V_{TRIP}	Desired current trip value	$I_{LOAD} \times R_{SENSE}$
V_{LIMIT}	Programmed threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
V_{LIMIT} (1)	Threshold voltage	($I_{LIMIT} \times R_{LIMIT}$) – NAF
R_{LIMIT} (1)	Threshold limit setting resistor	(V_{LIMIT} + NAF) / I_{LIMIT}
R_{LIMIT} (1)	Limit setting resistor	(V_{LIMIT} + 500 µV) / 20 µA

(1) NAF is used with the 10-µs delay setting. NAF can be omitted in the R_{LIMIT} calculation for the 50-µs and 100-µs delay settings.

TI recommends using NAF in calculating the value for V_{LIMIT} and R_{LIMIT} at the 10-µs delay setting. Removing NAF from the V_{LIMIT} and R_{LIMIT} calculation at the 10-µs delay setting lowers the trigger point of the alert output. Lowering the trigger point results in the device issuing an overcurrent alert prior to reaching the corresponding V_{TRIP} threshold. The averaging effect included with the 50-µs and 100-µs delay settings inherently eliminates the effect internal noise has on the threshold voltage.

7.3.2.2 Voltage Source-Controlled Current Limit

The second method for setting the limit voltage is to connect the LIMIT terminal to a programmable DAC (digital-to-analog converter) or other external voltage source. The benefit of this method is the ability to adjust the current limit to account for different threshold voltages that are used for different system operating conditions. For example, this method can be used in a system that has one current-limit threshold level that must be monitored during the power-up sequence but different thresholds must be monitored during other system operating modes.

In 表 7-3, V_{TRIP} represents the overcurrent threshold the device is programmed to monitor for and V_{SOURCE} is the programmed signal set to detect the V_{TRIP} level. NAF is included in the V_{SOURCE} equation for the 10-µs delay setting. This value equals 500 µV and is adjusts the operating point for the noise in the delay setting. The 50-µs and 100-µs delay settings do not use the NAF term in calculating the V_{SOURCE} threshold. For these delay settings, the NAF term is omitted. See the *Noise Adjustment Factor (NAF)* section for more details on the noise adjustment factor.

表 7-3. Calculating the Limit Threshold Voltage Source, V_{SOURCE}

PARAMETER		EQUATION
V_{TRIP}	Desired current trip value	$I_{LOAD} \times R_{SENSE}$
V_{SOURCE} (1)	Programmed threshold limit voltage	V_{TRIP} + NAF
V_{SOURCE} (1)	Programmed signal set to detect the V_{TRIP} level	V_{TRIP} + 500 µV

(1) NAF is used with the 10-µs delay setting. NAF can be omitted in the V_{SOURCE} calculation for the 50-µs and 100-µs delay settings.

TI recommends using NAF in calculating the value for V_{SOURCE} at the 10-µs delay setting. Removing NAF from the V_{SOURCE} calculation at the 10-µs delay setting lowers the trigger point of the alert output. Lowering the trigger point results in the device issuing an overcurrent alert prior to reaching the corresponding V_{TRIP} threshold. The averaging effect included with the 50-µs and 100-µs delay settings inherently eliminates the effect internal noise has on the threshold voltage.

7.3.3 Delay Setting

The device response time for overcurrent events is adjustable based on the DELAY terminal setting. Three response time settings are available, ranging from 10 µs to 100 µs. The primary purpose for the three different delay settings is to offer a trade-off between a faster alert response and a more precise overcurrent threshold level detection.

The device has a 10-µs internal comparison window. This single comparison window is the fundamental time unit used for all three delay settings. For the 10-µs delay setting, the device compares the average of the input signal during the 10-µs comparison window to the threshold limit programmed at the LIMIT terminal. If the averaged input signal exceeds the threshold at the end of the 10-µs comparison window, the output alert triggers and pulls the $\overline{\text{ALERT}}$ terminal low. However, if the averaged input does not exceed the threshold at the end of the 10-µs comparison window, there is no change in the output alert status, which remains high to indicate that no overcurrent event is detected.

For the 50-µs delay setting, there must be five consecutive 10-µs comparison windows that result in an average input signal exceeding the threshold limit in order for the output alert to trigger and pull the $\overline{\text{ALERT}}$ terminal low. If any single 10-µs comparison window fails to detect an overcurrent condition before reaching five consecutive overcurrent comparisons, the internal counter is reset and no output alert is issued. With the internal counter reset, a new group of five consecutive 10-µs comparison windows of overcurrent conditions are required in order to trigger the alert and pull the $\overline{\text{ALERT}}$ terminal low.

The 100-µs delay setting operates in the same manner as the 50-µs method, but instead requires ten consecutive 10-µs comparison windows with an input signal exceeding the threshold limit to issue an output alert and pull the $\overline{\text{ALERT}}$ terminal low.

Requiring multiple consecutive overcurrent detections aides significantly in reducing the likelihood of system noise causing false alerts, which can be detrimental to critical system operations. However, by enabling an alert window equal to the comparison window of 10 µs, the device still has the flexibility to be used in fast overcurrent detection applications that require quick responses to rapidly changing system operating characteristics.

In 图 7-1, the device alert output response is shown for a 10-µs delay setting and a 50-µs delay setting based on the same input signal condition. The initial increase of the input signal, V_{IN}, above the V_{LIMIT} level remains above the limit for approximately 30 µs. With the device set to the 10-µs delay setting, the overcurrent condition is detected and the alert output terminal is pulled low approximately 10 µs later. With the device set to the 50-µs delay setting, an alert is not issued because five consecutive 10-µs overcurrent measurements are not detected. With the input signal only being over the limit for 30 µs rather than the corresponding 50 µs needed for this delay setting, the device does not issue an alert under this condition. For the second instance where V_{IN} rises above the V_{LIMIT} threshold, the input remains above the limit for more than five consecutive 10-µs measurements, indicating an overcurrent condition and the alert output terminal is pulled low.

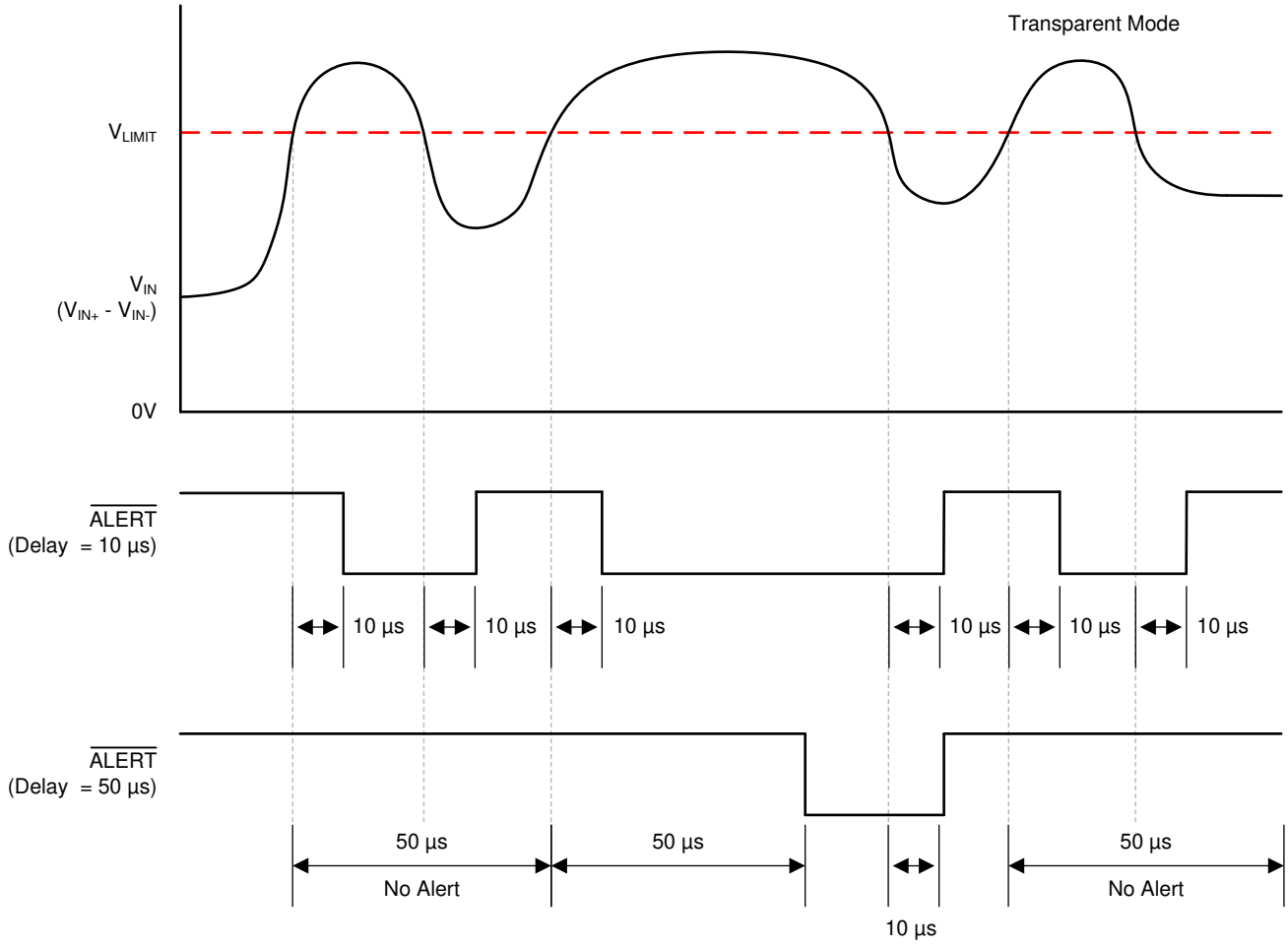


图 7-1. DELAY Terminal Settings

As discussed previously, there are three different available delay settings that are configured based on the signal connected to the DELAY terminal, as shown in 图 7-2 and 表 7-4. The DELAY terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors must not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connection to the DELAY terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level-detection circuitry.

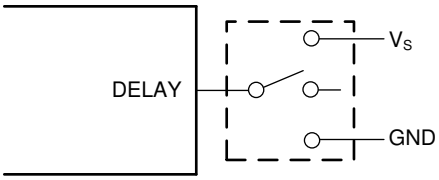


图 7-2. Delay Response

表 7-4. Delay Settings

DELAY	ALERT DELAY (µs)
Open or floating	10
GND	50
V_S	100

7.3.4 Alert Timing Response

The device has a 10-µs internal comparison window where the input signal is measured to compare to the limit threshold voltage. This window continuously runs internal to the device without any external indicator or control. A comparison is made at the completion of each 10-µs comparison window to determine if the averaged input over the comparison window exceeds the limit threshold, thus indicating if an overcurrent event has occurred.

This comparison window is not synchronized with the input signal so there is an unknown timing component present. With this free-running internal timing window, an overcurrent event can occur anywhere within the 10-µs comparison window. This condition causes a variation in the amount of time before the alert appears at the output because the comparison is always made at the end of the 10-µs comparison window. 图 7-3 shows the variation in time between when the input signal rises above the threshold voltage and when a change at the alert output terminal occurs.

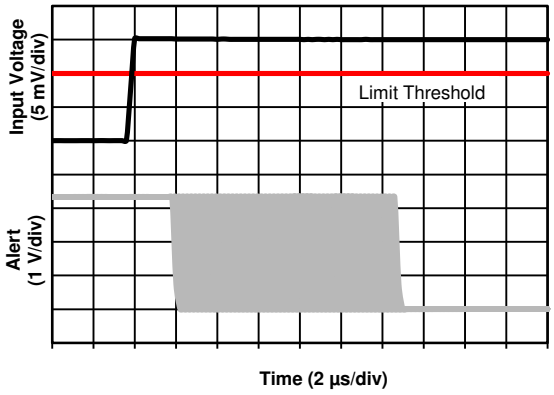


图 7-3. 10-µs Alert Response Window

The delay shown in 图 7-3 represents the response time of the device with a 10-µs delay setting. With a 50-µs delay setting, an additional 40 µs is added to the timing response, as shown in 图 7-4. A 100-µs delay setting adds 90 µs to the response time, as shown in 图 7-5.

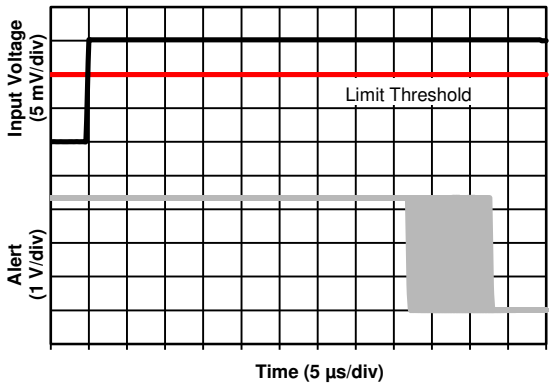


图 7-4. 50-µs Alert Response Window

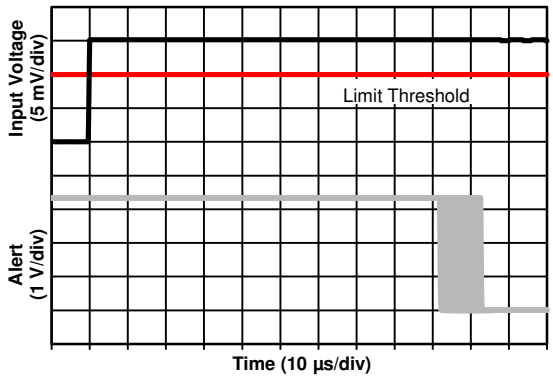


图 7-5. 100-µs Alert Response Window

7.3.5 Selectable Hysteresis

Device hysteresis is adjustable based on the setting at the hysteresis (HYS) terminal. The smallest setting for hysteresis on the device, 2 mV, is enabled by leaving the HYS terminal open and floating. A 4-mV hysteresis is set by connecting the HYS terminal to ground; connecting this terminal to the supply voltage sets the hysteresis to 8 mV, as shown in 图 7-6. The HYS terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors must not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connections to the HYS terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level-detection circuitry.

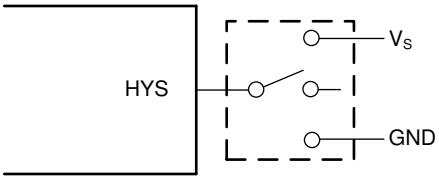


图 7-6. Hysteresis

The wide dynamic input range of the INA300 INA300 necessitates an adjustable hysteresis to ensure that the device can be appropriately configured based on the specific operating conditions and application requirements. 图 7-7 illustrates the transition locations for the $\overline{ALERT}$ terminal based on where the input signal, V_{IN}, is measured relative the limit threshold, V_{LIMIT}. The corresponding hysteresis levels and physical terminal settings for the device are shown in 表 7-5.

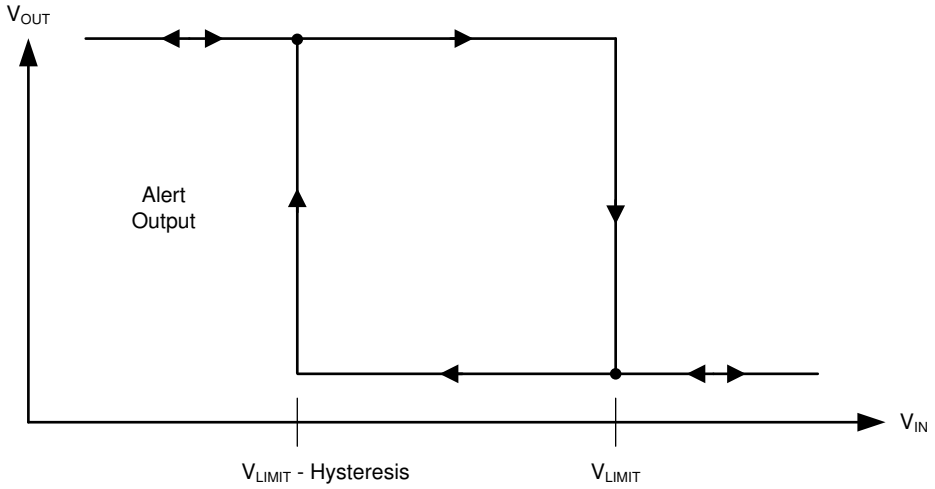


图 7-7. Typical Comparator Hysteresis

表 7-5. Hysteresis Settings

HYSTERESIS	HYSTERESIS SETTING
Float	2 mV
GND	4 mV
V_S	8 mV

7.3.6 Alert Output

The device $\overline{ALERT}$ terminal is an active-low, open-drain output. This output is designed to be pulled low when the input conditions are detected as out-of-range. This open-drain output pin is recommended to include a 10-kΩ, pull-up resistor to the supply voltage. This open-drain terminal can be pulled up to a voltage beyond the supply voltage, V_S, but must not exceed 5.5 V.

7.3.7 Noise Adjustment Factor (NAF)

The device is a high-speed, low-noise comparator that is designed to alert when the measured input signal exceeds the programmed limit level. Internal noise in the device couples into the measurement and can result in alerts being issued prior to the input signal exceeding the voltage level present at the LIMIT terminal. This known internal noise component effects the input signal measurement by causing a consistent shift in the device internal offset, resulting in a shifted trip threshold. NAF adjusts the V_{LIMIT} setting to account for this internal shift, thus allowing for a more precise level detection of the measured current.

The NAF value is based on the noise contribution on the measurement at the 10-µs delay setting. This value is equal to 500 µV and is applied in the calculation to adjust the V_{LIMIT} threshold level to allow for a more accurate alert trip point. The NAF term is only applied in the V_{LIMIT} calculation at the 10-µs delay setting. The averaging effect included with the 50-µs and 100-µs delay settings inherently eliminates the effect internal noise has on the threshold voltage. The NAF term can be omitted from the R_{LIMIT} calculation at the 10-µs delay setting with the effect of a lower trigger point of the alert output. Lowering the trigger point results in an overcurrent alert prior to reaching the corresponding V_{TRIP} threshold.

7.4 Device Functional Modes

7.4.1 Alert Mode

The device has two output operating modes that are selected based on the LATCH terminal setting: transparent mode and latch mode. These modes change how the $\overline{\text{ALERT}}$ terminal responds to the changing input signal conditions.

7.4.1.1 Transparent Output Mode

The device is set to transparent mode when the LATCH terminal is pulled low, thus allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the alert output terminal is pulled low. When the differential input signal drops below the alert threshold for 10 µs, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the $\overline{\text{ALERT}}$ terminal to a hardware interrupt input on a controller. As soon as an overcurrent condition is detected in the device and the $\overline{\text{ALERT}}$ terminal is pulled low, the controller interrupt terminal detects the output state change and can begin making changes to the system operation needed to address the overcurrent condition.

7.4.1.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the output $\overline{\text{ALERT}}$ terminal to detect an overcurrent condition. A typical example of this application is a system that is only able to poll the $\overline{\text{ALERT}}$ terminal state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, missing the change in state of the $\overline{\text{ALERT}}$ terminal is possible when $\overline{\text{ALERT}}$ is pulled low to indicate an out-of-range event if the out-of-range condition does not appear during one of these periodic polling events.

Latch mode is specifically intended to accommodate these applications. As shown in 表 7-6, the device is placed in latch mode by setting the voltage on the LATCH terminal to a logic high level. The difference between latch mode and transparent mode is how the alert output responds when an overcurrent event ends. In transparent mode, when the differential input signal drops below the limit threshold level for 10 µs, the output state returns to the default high setting to indicate that the overcurrent event had ended.

In latch mode, when an overlimit condition is detected and the $\overline{\text{ALERT}}$ terminal is pulled low, the $\overline{\text{ALERT}}$ terminal does not return to the default high level when the differential input signal drops below the alert threshold level for 10 µs. To clear the alert the LATCH terminal must be pulled low for at least 20 µs. Pulling the LATCH terminal low allows the $\overline{\text{ALERT}}$ terminal to return to the default high level, provided that the differential input signal has dropped below the alert threshold. If the input signal is still above the threshold limit when the LATCH terminal is pulled low, the $\overline{\text{ALERT}}$ terminal remains low. When the alert condition is detected by the system controller (the LATCH terminal) can be set back to high in order to place the device back in latch mode.

表 7-6. Output Mode Settings

OUTPUT MODE	LATCH TERMINAL SETTING
Transparent mode	LATCH = low
Latch mode	LATCH = high

The latch and transparent modes are represented in 图 7-8. In 图 7-8 when V_{IN} drops back below the V_{LIMIT} threshold for the first time, the LATCH terminal is pulled high. With the LATCH terminal pulled high, the device is set to latch mode so that the alert output state does not return high when the input signal drops below the V_{LIMIT} threshold. Only when the LATCH terminal is pulled low does the $\overline{ALERT}$ terminal return to the default high level, indicating that the input signal is below the limit threshold. When the input signal drops below the limit threshold for the second time, the LATCH terminal is already pulled low. The device is set to transparent mode at this point and the $\overline{ALERT}$ terminal is pulled back high when the input signal drops below the alert threshold.

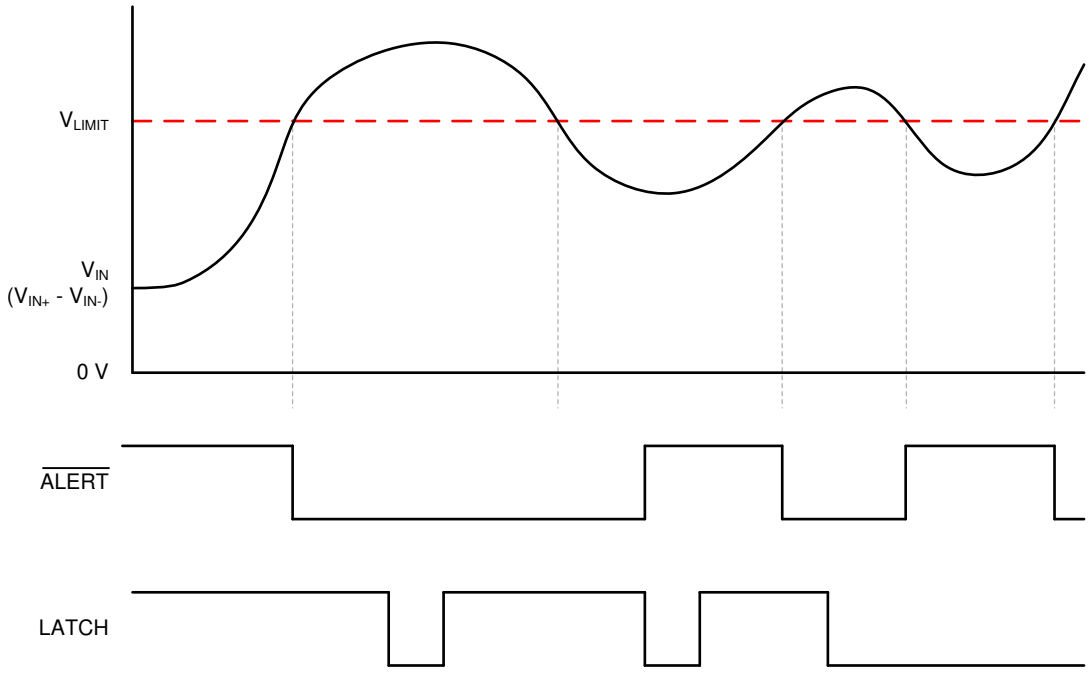


图 7-8. Transparent vs Latch Mode

7.4.2 Disable Mode

The INA300 INA300 device has an ENABLE terminal that allows the device to be placed into an active enabled state or a low-power disabled state where less than 10 µA is consumed from all terminals. This disable state allows the device to be used in applications where low current consumption is required to extend battery life where constant monitoring is not required. The INA300 device requires approximately 20 µs to enter the low-power state when the ENABLE terminal transitions from high to low, as shown in 表 7-7. To return to the enabled active state, the INA300 device requires approximately 300 µs to return to normal operation when the ENABLE terminal transitions from low to high, taking the device out of the low-power state.

表 7-7. Enable and Disable Mode Settings

ENABLE MODE	ENABLE TERMINAL SETTING
Disable mode	ENABLE = low
Enable mode	ENABLE = high

The internal counter that determines if the necessary consecutive 10-µs window comparison alert conditions are reached for the 50-µs and 100-µs delay setting is reset when the device is put into a disabled state. When the device is re-enabled, the counter restarts.

7.4.3 Input Filtering

External system noise can have a significant effect in the ability of a comparator to accurately measure and detect whether input signals exceed the reference threshold levels, indicating an overrange condition. The device is susceptible to external noise, although the 50-µs and 100-µs delay settings are can mitigate the impact of noise based on the effective averaging achieved in these modes. The obvious effect that external noise can have on the operation of a comparator is to cause a false alert condition. If a comparator detects a large noise transient coupled into the signal, the device can interpret this transient as an overrange condition.

External filtering can help reduce the amount of noise that reaches the comparator inputs, and can reduce the likelihood of a false alert from occurring. The tradeoff to adding this noise filter is increased comparator response time, because of the input signal being filtered as well as the noise. 图 7-9 shows the implementation of an input filter for the device.

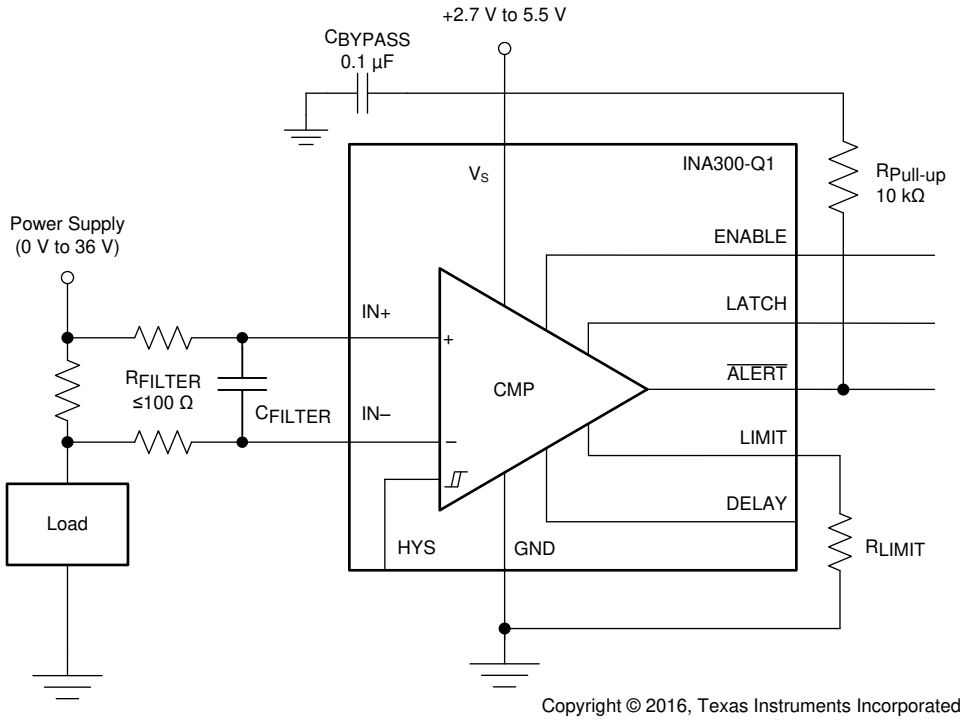


图 7-9. Input Filter

Limiting the amount of input resistance used in this filter is important because this resistance can have a significant effect on the input signal that reaches the device input pins resulting from the device input bias currents. A typical system implementation involves placing the current-sensing resistor near the device so the traces are short and the trace impedance is small. This layout helps reduce the ability of coupling additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal effect on device performance.

As shown in 图 7-10, the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from the design of the device, which allows common-mode input voltages to far exceed the device supply voltage range. With input filter resistors now placed in series with these unequal input bias currents, there are unequal voltage drops developed across the input resistors. The difference between the two drops appears as an added signal that (in this case) subtracts from the voltage developed across the current-sensing resistor, reducing the signal that reaches the device input terminals. Smaller value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.

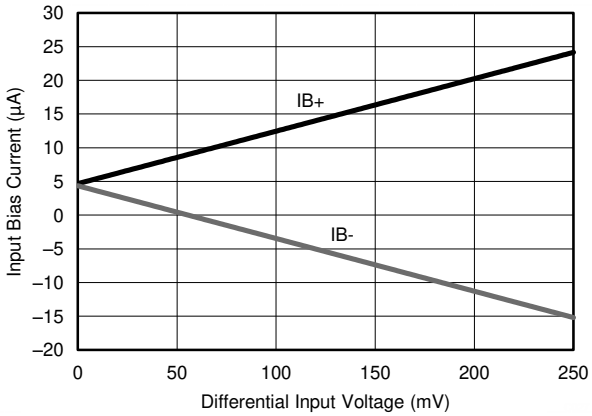


图 7-10. Input Bias Current vs Differential Input Voltage

For example, with a differential voltage of 10 mV developed across a current-sensing resistor and using 100-Ω resistors, the differential signal that reaches the device is 9.8 mV. A measurement error of 2% is created as a result of the external input filter resistors. Using 10-Ω input filter resistors instead of the 100-Ω resistors reduces this added error from 2% to 0.2%.

7.4.4 Using the INA300 INA300 With Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device can be used in circuits subject to transients higher than 36 V. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *Transzorbs*). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in 图 7-11, as a working impedance for the zener diode. Keeping these resistors as small as possible is best, preferably 100 Ω or less. Larger values can be used with an additional error induced resulting from a reduced signal that reaches the device input terminals. Because this circuit limits only short-term transients, many applications are satisfied with a 100-Ω resistor along with conventional zener diodes of the lowest power rating available. This combination uses the least amount of board space. These diodes can be found in SOT-523 or SOD-523 packages.

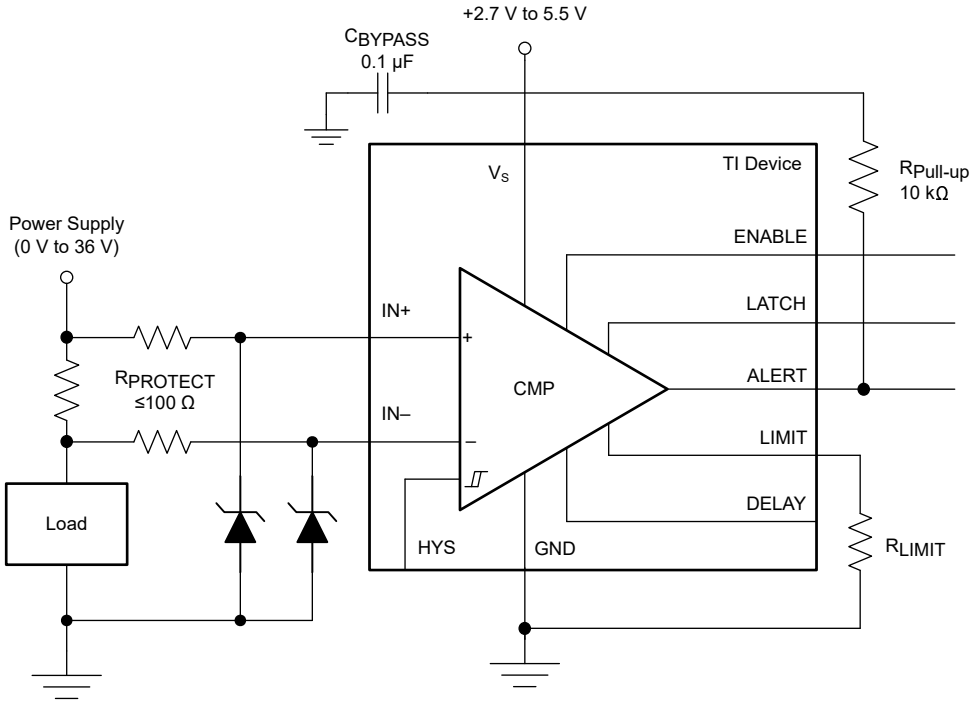


图 7-11. Transient Protection

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The INA300 INA300 is designed to enable configuration for detecting overcurrent conditions in an application. This device is individually targeted towards overcurrent detection of a single threshold. However, this device can be paired with additional devices and circuitry to create more complex monitoring functional blocks.

8.2 Typical Applications

8.2.1 Unidirectional Operation

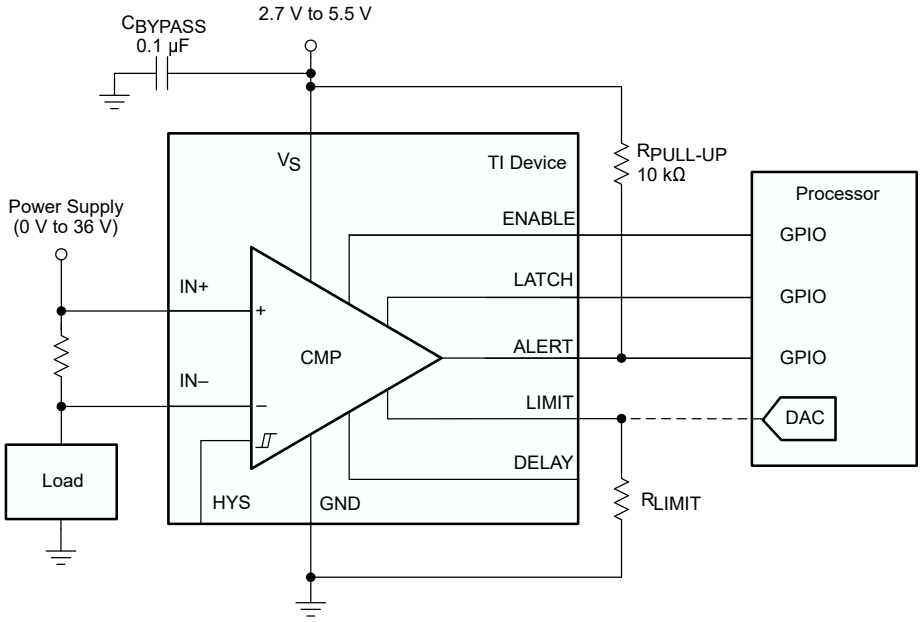


图 8-1. Unidirectional Application Schematic

8.2.1.1 Design Requirements

The INA300 device measures current through a resistive shunt with current flowing in one direction, enabling detection of an overcurrent event only when the differential input voltage exceeds the threshold limit.

8.2.1.2 Detailed Design Procedure

图 8-1 shows the basic connections of the INA300 device. The input terminals, IN+ and IN – , must be connected as closely as possible to the current-sensing resistor to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input terminals can result in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor can differ from the voltage reaching the input terminals.

8.2.1.3 Application Curve

图 8-2 shows the alert response transitioning from a high to a low state following the input signal exceeding the limit threshold voltage. The time required for the output to respond varies as a result of when the input signal crosses the threshold limit voltage relative to where in the continuous running internal 10-µs comparison window the overrange condition occurs. In 图 8-2, the output response varies from roughly 2 µs to approximately 12 µs when the input exceeds the threshold level. This variance is a result of where in the 10-µs comparison window the overrange event occurs. If the overrange event occurs late in the 10-µs comparison window and is large enough to average the entire window measurement up above the threshold level, the alert appears to respond very quickly. If the alert occurs late in the 10-µs comparison window and is not large enough to average the entire window measurement up above the threshold level, the alert does not appear until the next 10-µs comparison window completes, assuming the input signal remains above the threshold for the entire duration.

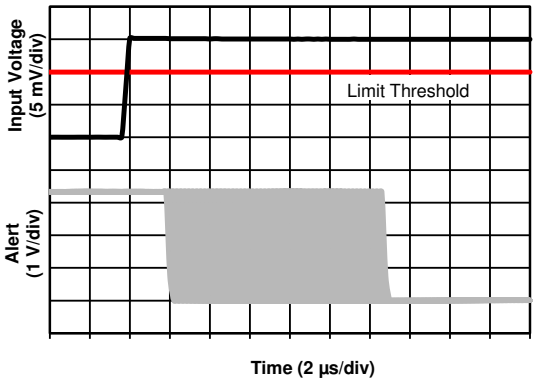


图 8-2. Alert Response

8.2.2 Bidirectional Operation

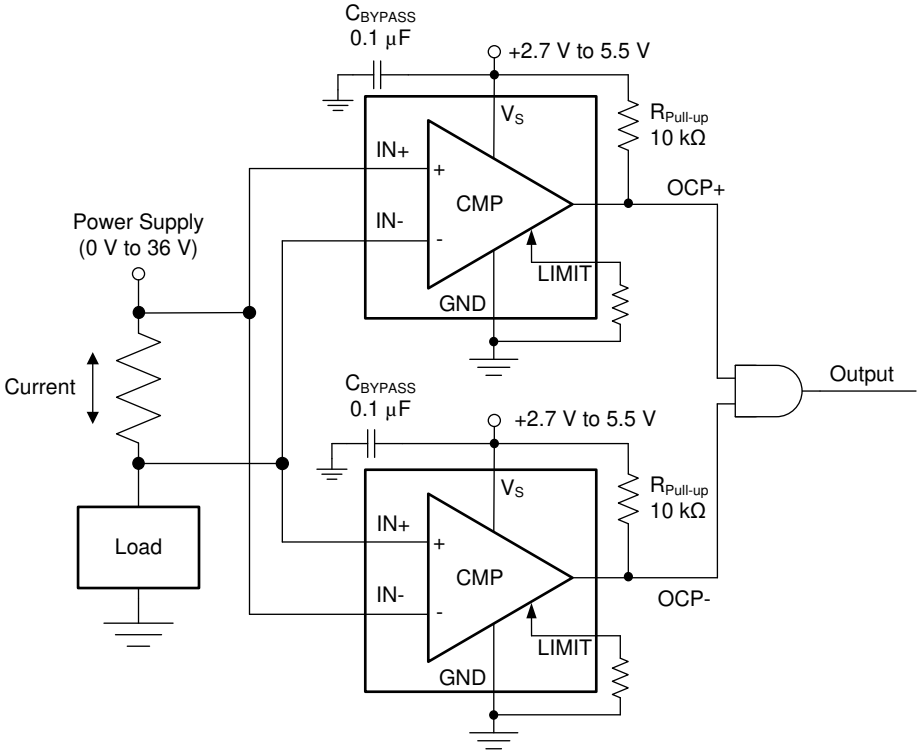


图 8-3. Bidirectional Application

8.2.2.1 Design Requirements

Although the INA300 device is only able to measure current through a current-sensing resistor flowing in one direction, a second INA300 INA300 device can be used to create a bidirectional monitor.

8.2.2.2 Detailed Design Procedure

With the input terminals of a second INA300 device reversed across the same current-sensing resistor, the second INA300 device is now able to detect current flowing in the other direction relative to the first device, as shown in 图 8-3. The outputs of each INA300 device connect to an AND gate to detect if either of the limit threshold levels are exceeded. The output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that either the positive overcurrent limit or the negative overcurrent limit are surpassed.

表 8-1. Bidirectional Overcurrent Output Status

OCP STATUS	OUTPUT
OCP+	0
OCP –	0
No OCP	1

8.2.2.3 Application Curve

图 8-4 illustrates two INA300 INA300 devices being used in a bidirectional configuration and an output control circuit to detect if one of the two alerts is exceeded.

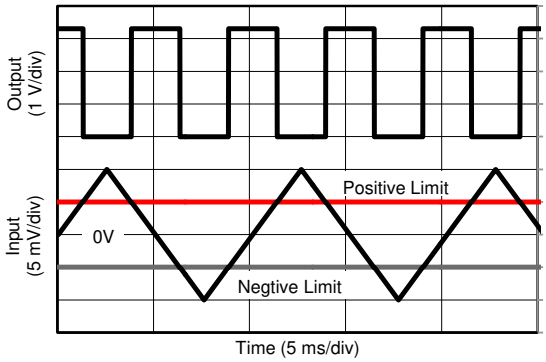


图 8-4. Bidirectional Application Curve

8.2.3 Window Comparator

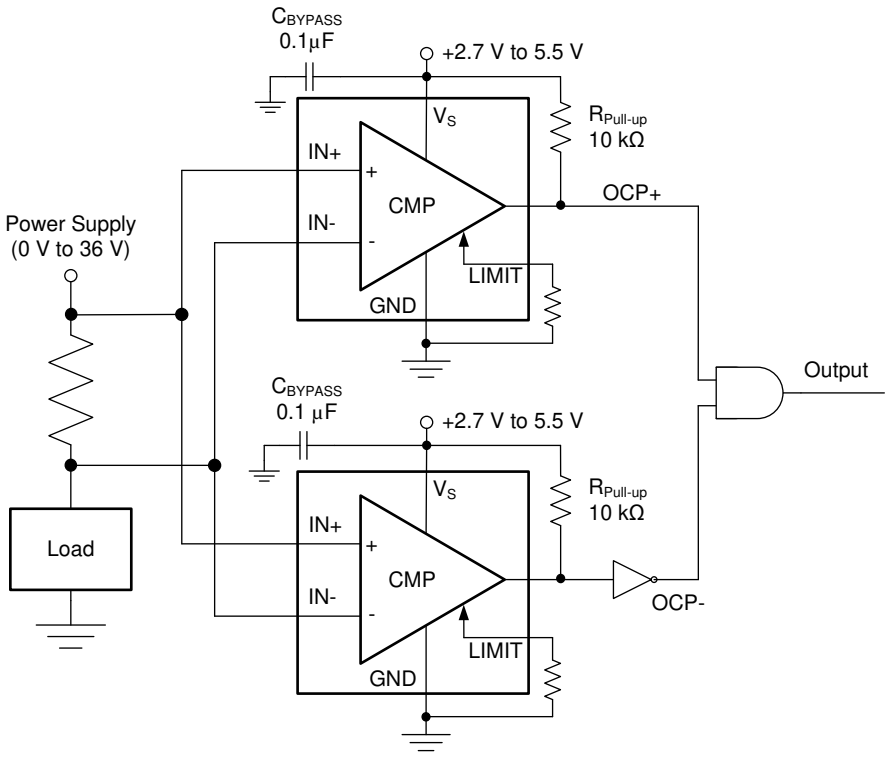


图 8-5. Window Comparator Application

8.2.3.1 Design Requirements

The INA300 device can be used to create a window comparator function, detecting whether the current being monitored is within a programmed range or has fallen outside of the expected operating region.

8.2.3.2 Detailed Design Procedure

图 8-5 shows how the window comparator function is setup using two INA300 devices. The input terminals of each INA300 device are connected to the same current-sensing resistor. The limit threshold for the top device is set to the upper limit of the window range. The bottom device limit threshold is set to the desired lower limit of the range. With a logic inverter placed at the output of the device monitoring the lower limit, the OCP – signal is high when the input signal is above the lower limit threshold. The OCP+ signal is high when the input signal is below the upper limit threshold. A high value at the output (output of the AND gate) indicates that the monitored current is operating within the desired window range.

表 8-2. Window Comparator Output Status

INPUT CONDITION	OUTPUT STATUS
Above range	0
Below range	0
In range	1

8.2.3.3 Application Curve

图 8-6 shows the output waveform from the device window comparator application. In 图 8-6, the output signal is high when OCP – is low (the input signal is above the lower limit) and when OCP+ is high (the input signal is below the upper limit). If the signal rises above the upper limit or drops below the lower limit, the corresponding OCP output changes state, causing the state of the output (following the AND gate) to change to zero to indicate an out-of-range condition.

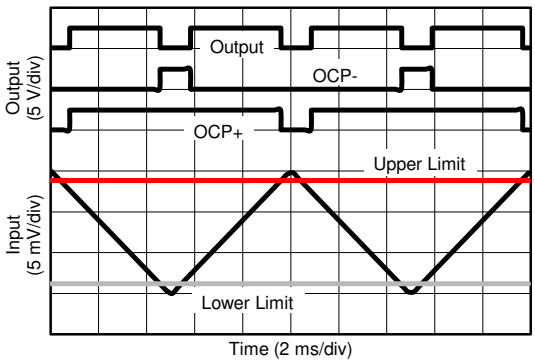


图 8-6. Output Waveform

9 Power Supply Recommendations

The INA300 device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power-supply terminal can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 36 V. Note that the INA300 device can withstand the full –0.3 V to +36 V range at the input terminals, regardless of whether the device has power applied or not.

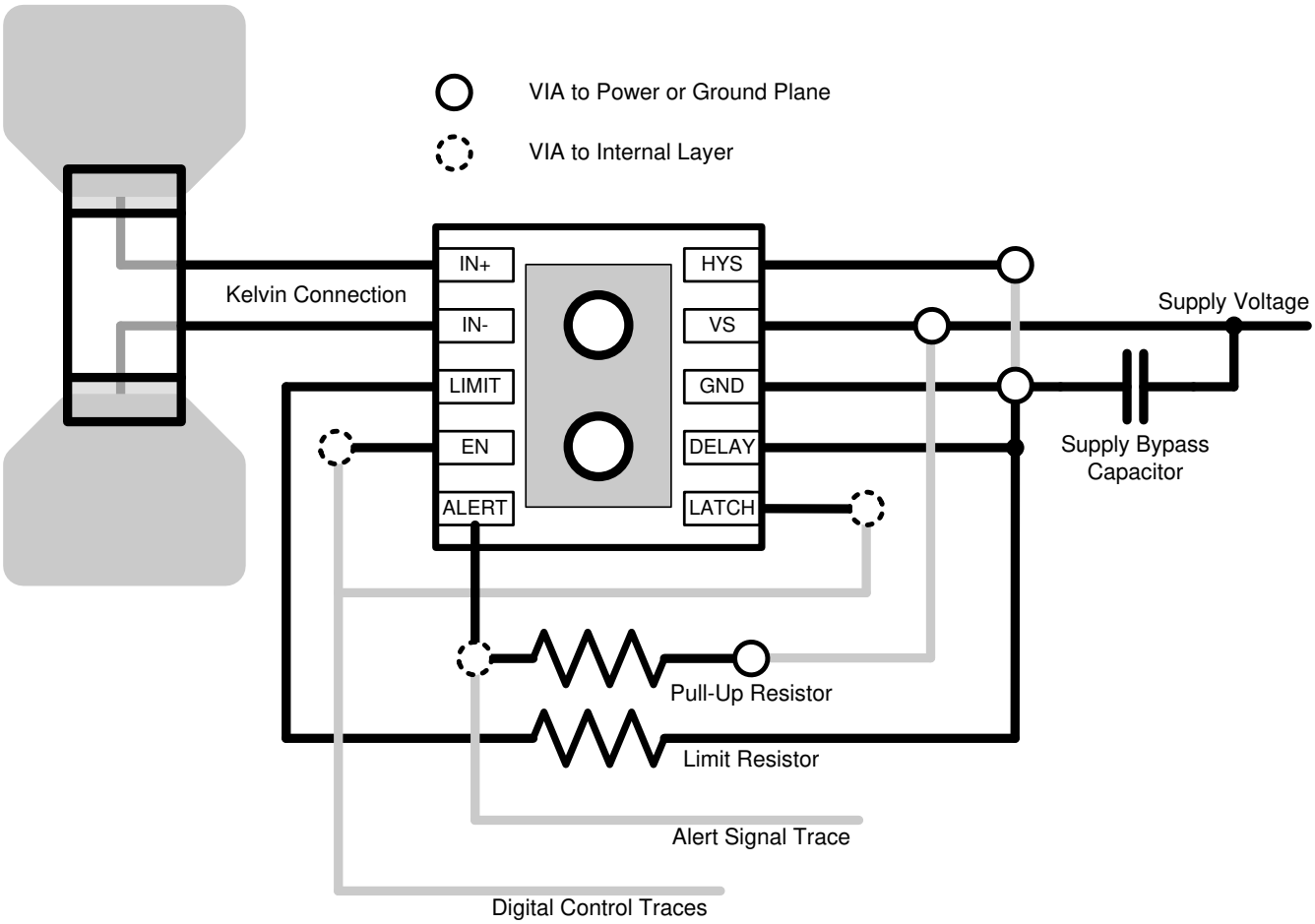
Power-supply bypass capacitors are required for stability and must be placed as closely as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

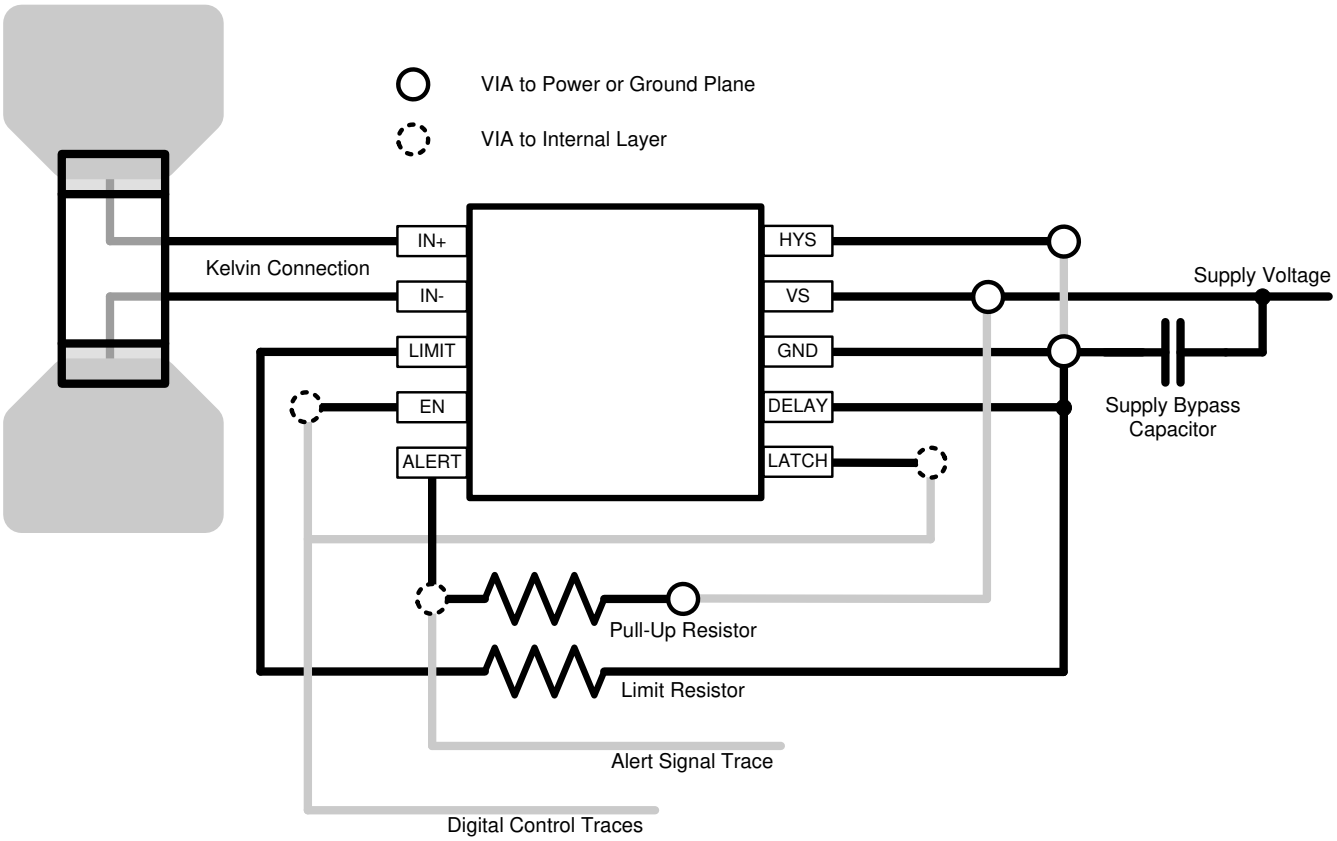
- The power-supply bypass capacitor must be placed as closely as possible to the supply and ground terminals. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- The connection of R_{LIMIT} to the ground terminal must be made as direct as possible to limit additional capacitance on this node. Routing this connection must be limited to the same plane if possible avoiding vias to internal planes. If the routing cannot be made on the same plane and must pass through vias, ensure that a path is routed from the R_{LIMIT} back to the ground terminal and that the R_{LIMIT} is not connected directly to a ground plane.
- The DELAY terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors must not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connection to the DELAY terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level detection circuitry.
- The HYS terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors must not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connections to the HYS terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level detection circuitry.
- The open-drain output pin is recommended to be pulled up to the supply voltage rail through a 10-kΩ pull-up resistor.

10.2 Layout Example



NOTE: Connect the limit resistor directly to the GND terminal.

图 10-1. Recommended Layout for WSON Package



NOTE: Connect the limit resistor directly to the GND terminal.

图 10-2. Recommended Layout for VSSOP Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *INA300EVM User's Guide* (SBAU220).

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA300AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	12T6
INA300AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12T6
INA300AIDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12T6
INA300AIDSQR	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD
INA300AIDSQR.A	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD
INA300AIDSQR.B	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD
INA300AIDSQRG4	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD
INA300AIDSQRG4.A	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD
INA300AIDSQRG4.B	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA300 :

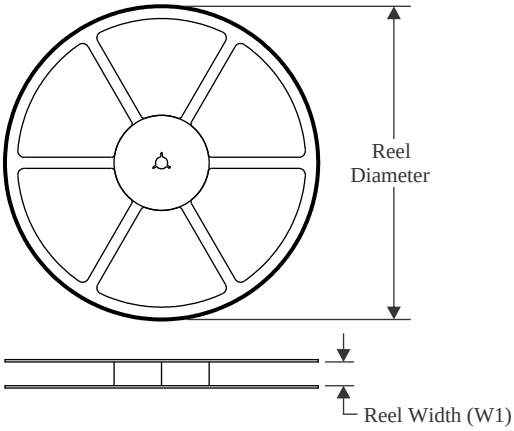
- Automotive : INA300-Q1

NOTE: Qualified Version Definitions:

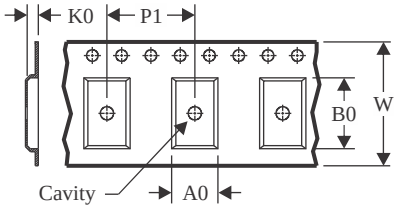
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

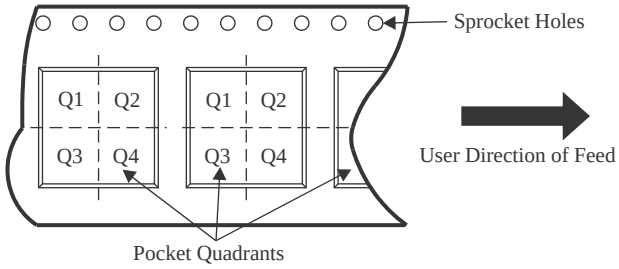


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

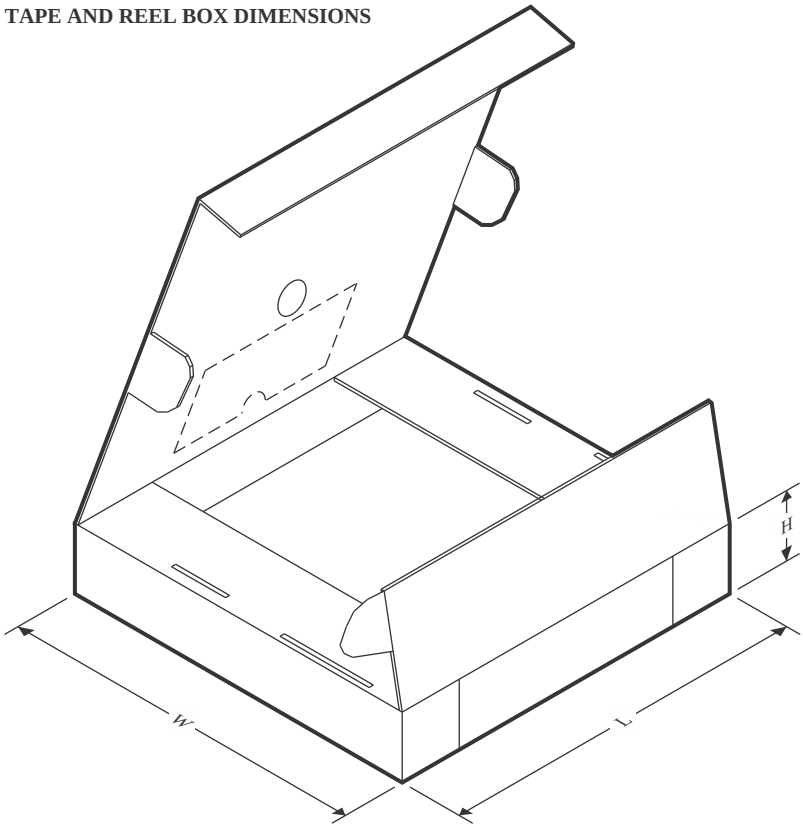
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA300AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA300AIDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA300AIDSQRG4	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

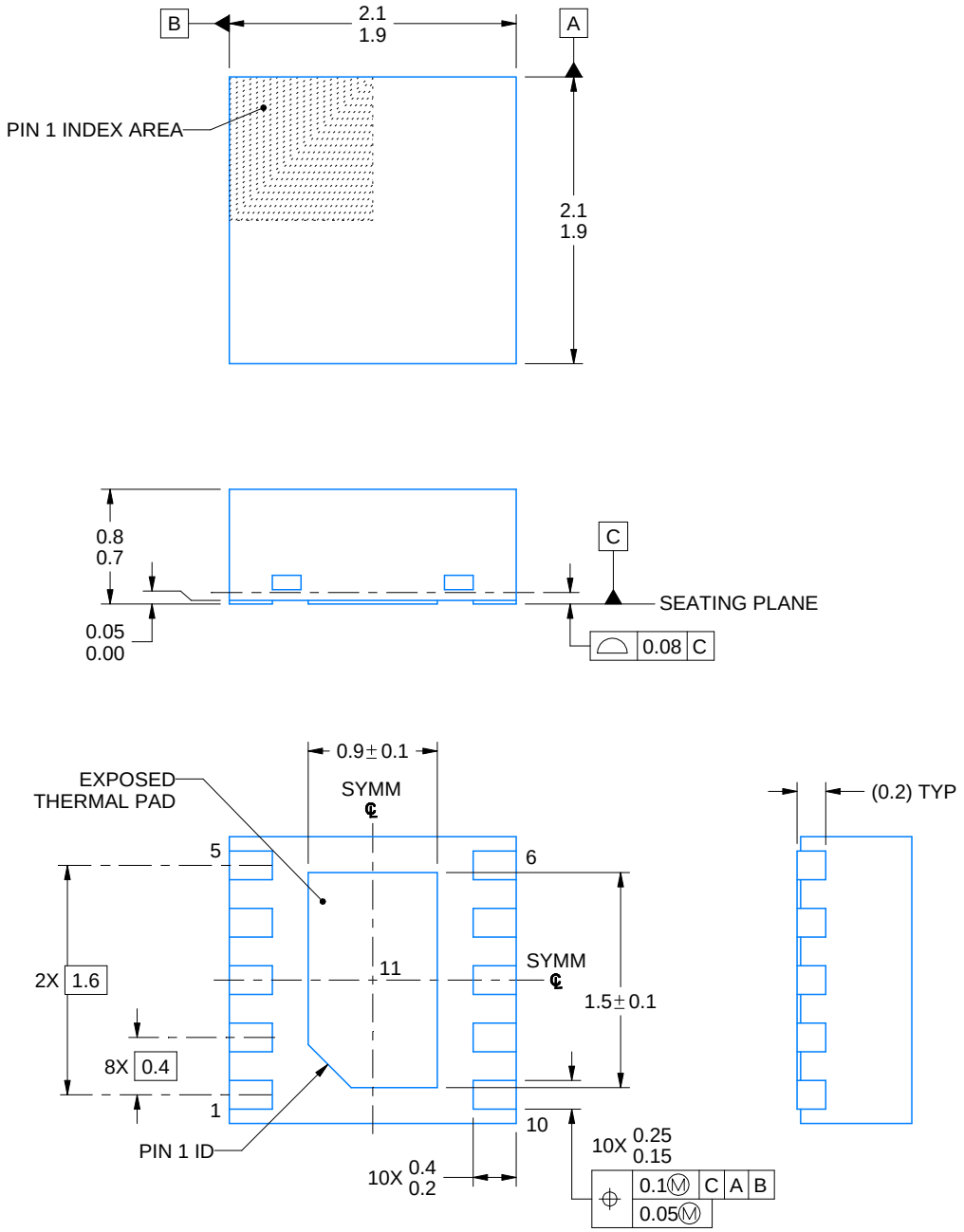
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA300AIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA300AIDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA300AIDSQRG4	WSON	DSQ	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218906/A 04/2019

NOTES:

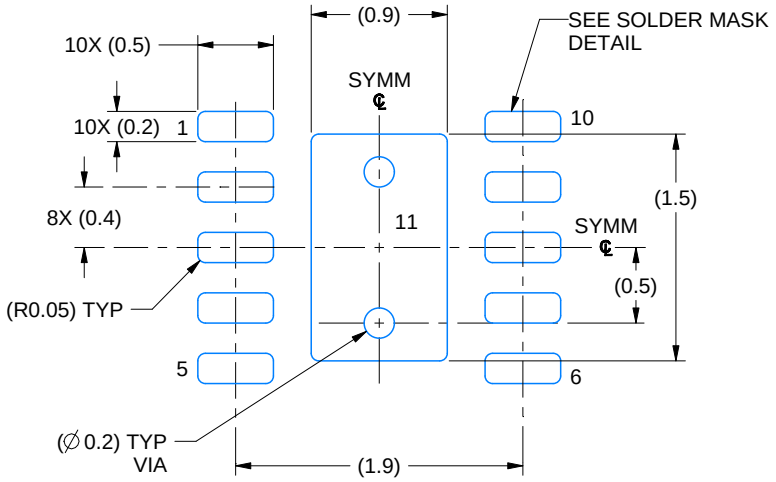
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

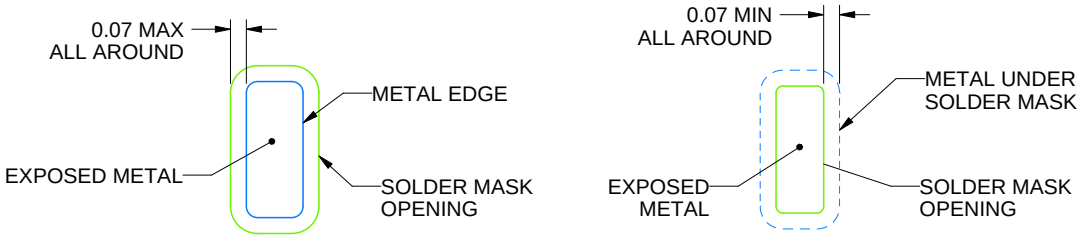
DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

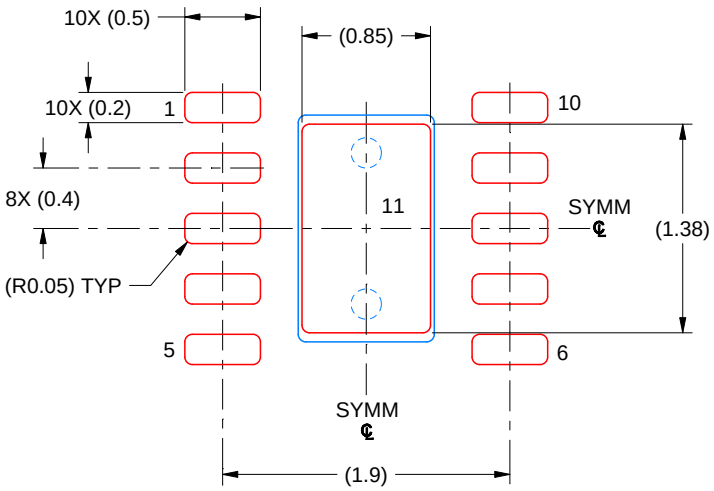
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218906/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218906/A 04/2019

NOTES: (continued)

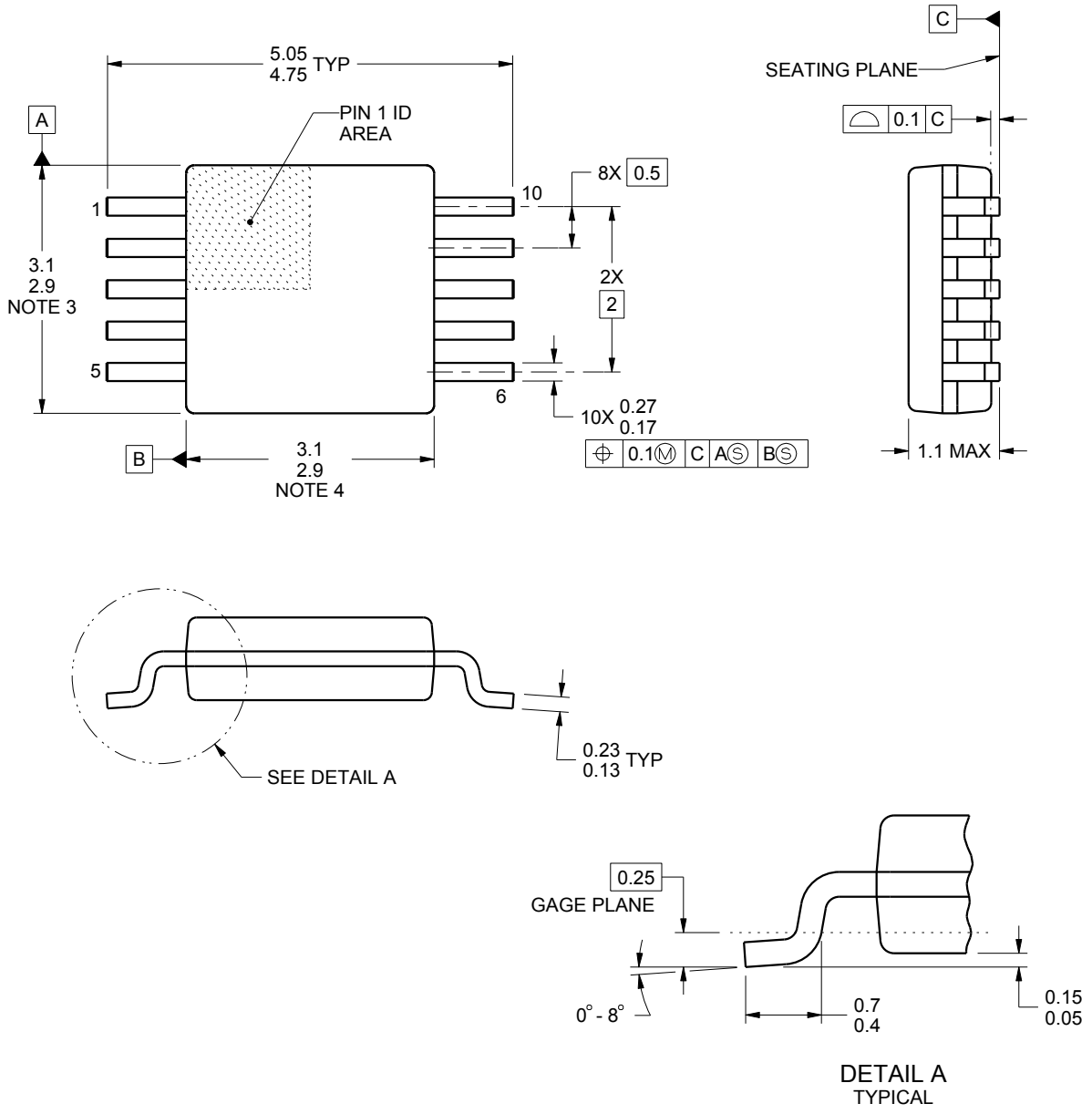
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

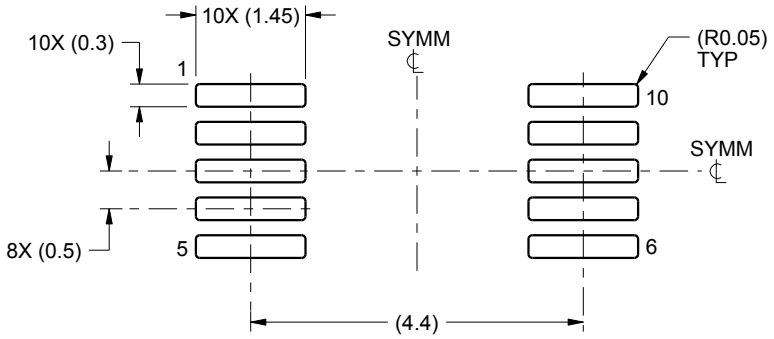
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

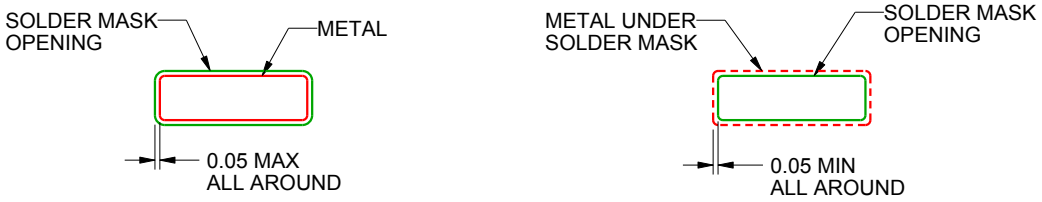


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

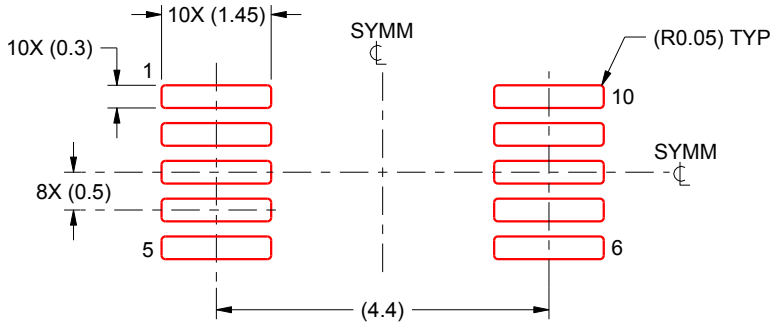


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月