

ISO724xC-Q1 高速四通道数字隔离器

1 特性

- 25Mbps 信号传输速率选项
 - 低通道间输出偏斜；
最大值为 1ns
 - 低脉宽失真 (PWD)；
最大值为 2ns
 - 低抖动内容；速率为 25Mbps 时的典型值为 1ns
- 可选默认输出 (ISO7240CF)
- 额定工作电压下的使用寿命 > 25 年 (请参阅 [绝缘特性曲线](#))
- 4kV 静电放电 (ESD) 保护
- 由 3.3V 或 5V 电源供电
- -40°C 至 +125°C 工作温度范围
- [安全相关认证](#)：
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL 1577 组件认证计划
 - IEC 61010-1、IEC 62368-1 认证

2 应用

- [工厂自动化](#)
 - [Modbus](#)
 - [Profibus™](#)
 - [DeviceNet™ 数据总线](#)
- [计算机外设接口](#)
- [伺服器控制接口](#)
- [数据采集](#)

3 说明

ISO7240CF-Q1、ISO7241C-Q1 和 ISO7242C-Q1 器件是四通道数字隔离器，具有多个通道配置和输出使能功能。这些器件具有通过德州仪器 (TI) 的二氧化硅 (SiO₂) 隔离栅隔离的逻辑输入和逻辑输出缓冲器。与隔离电源配合使用时，这些器件有助于阻止高电压、隔离接地，并防止噪声电流进入本地接地和干扰或损坏敏感电路。

ISO7240C-Q1 系列器件的所有四个通道均为相同方向。ISO7241C-Q1 系列器件的三个通道为相同方向，一个通道为相反方向。ISO7242C-Q1 系列器件在每个方向有两个通道。

带有后缀 C (C 选项) 的器件具有 TTL 输入阈值，并且在输入端具有噪声滤波器，可防止将瞬态脉冲传递到器件的输出。带有 M 后缀 (M 选项) 的器件具有 CMOS $V_{CC}/2$ 输入阈值，没有输入噪声滤波器或额外的传播延迟。

ISO7240CF 器件在引脚 7 上具有输入禁用功能，并可通过 CTRL 引脚 (引脚 10) 选择高电平或低电平失效防护输出功能。当在 CTRL 引脚上施加逻辑高电平信号或该引脚未连接时，失效防护输出为逻辑高电平。如果向 CTRL 引脚施加逻辑低电平信号，则失效防护输出变为逻辑低电平输出状态。ISO7240CF 器件的输入禁用功能可防止数据跨越隔离栅传递到输出端。当输入被禁用或 V_{CC1} 断电时，输出由 CTRL 引脚设置。

这些器件可由任一侧的 3.3V 或 5V 电源 (任意组合) 供电。无论使用的电源电压电平如何，信号输入引脚均可耐受 5V 电压。

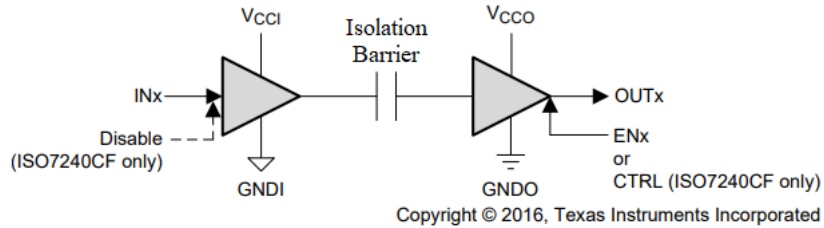
这些器件可在 -40°C 至 +125°C 的环境温度下运行。



封装信息

器件型号	封装 ⁽¹⁾	本体尺寸 (标称值)	封装尺寸 ⁽²⁾
ISO7240CF-Q1	DW (SOIC , 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7241C-Q1			
ISO7242C-Q1			

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



V_{CCI} 和 $GNDI$ 分别是输入通道的电源和接地连接引脚。
 V_{CCO} 和 $GNDO$ 分别是输出通道的电源和接地连接引脚。

简化版原理图

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4 Pin Configurations and Functions

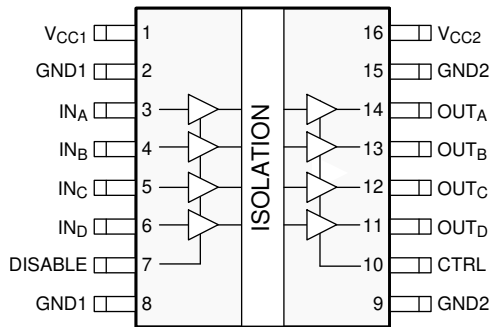


图 4-1. ISO7240CF-Q1 DW Package 16-Pin SOIC Top View

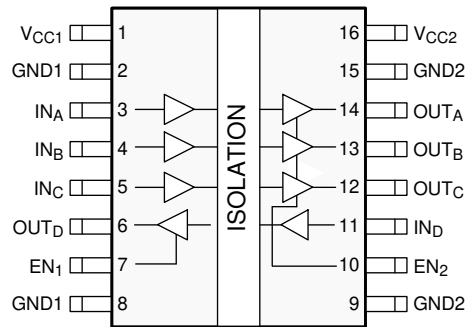


图 4-2. ISO7241C-Q1 DW Package 16-Pin SOIC Top View

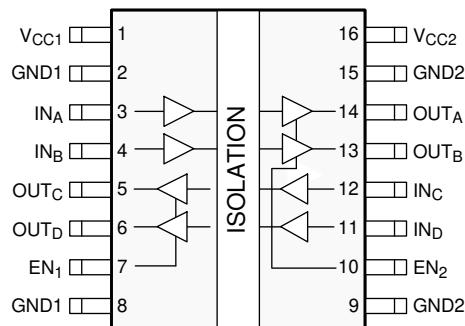


图 4-3. ISO7242C-Q1 DW Package 16-Pin SOIC Top View

表 4-1. Pin Functions

NAME	PIN			Type ⁽¹⁾	DESCRIPTION
	ISO7240CF-Q1	ISO7241C-Q1	ISO7242C-Q1		
CTRL	10	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V _{CC1} is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN ₁	—	7	7	I	Output enable 1. Output pins on side-1 are enabled when EN ₁ is high or open and disabled when EN ₁ is low.
EN ₂	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN ₂ is high or open and disabled when EN ₂ is low.
GND1	2, 8	2, 8	2, 8	—	Ground connection for V _{CC1}
GND2	9, 15	9, 15	9, 15	—	Ground connection for V _{CC2}
IN _A	3	3	3	I	Input, channel A
IN _B	4	4	4	I	Input, channel B
IN _C	5	5	12	I	Input, channel C
IN _D	6	11	11	I	Input, channel D
NC	—	—	—	—	No Connect pins are floating with no internal connection
OUT _A	14	14	14	O	Output, channel A
OUT _B	13	13	13	O	Output, channel B
OUT _C	12	12	5	O	Output, channel C
OUT _D	11	6	6	O	Output, channel D
V _{CC1}	1	1	1	—	Power supply, V _{CC1}
V _{CC2}	16	16	16	—	Power supply, V _{CC2}

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

See⁽¹⁾

			VALUE	UNIT
V _{CC}	Supply voltage ⁽²⁾ , V _{CC1} , V _{CC2}		- 0.5 to 6	V
V _I	Voltage at IN, OUT, EN, DISABLE, CTRL		- 0.5 to 6	V
ESD	Electrostatic discharge	Human-Body Model	±4	kV
		Field-Induced-Charged Device Model	±1	
T _J	Maximum junction temperature		150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾ , V _{CC1} , V _{CC2}	3.15		5.5	V
I _{OH}	High-level output current			4	mA
I _{OL}	Low-level output current	- 4			mA
t _{ui}	Input pulse width	40			ns
1/t _{ui}	Signaling rate	0	30 ⁽¹⁾	25	Mbps
V _{IH}	High-level input voltage (IN, DISABLE, CTRL, EN)	2		V _{CC}	V
V _{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN)	0		0.8	V
T _A	Operating free-air temperature	-40		125	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

- (1) Typical value at room temperature and well-regulated power supply.
- (2) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.4 Thermal Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ _{JA}	Junction-to-air	Low-K Thermal Resistance ⁽¹⁾		168		°C/W
		High-K Thermal Resistance		68.6		
θ _{JB}	Junction-to-Board Thermal Resistance			33.5		°C/W
θ _{JC}	Junction-to-Case Thermal Resistance			33.9		°C/W

- (1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

5.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150C, C_L = 15 pF, Input a 25-Mbps 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D	Device power dissipation, ISO724xC				220	mW

5.6 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

5.7 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = 212°C/W, V _I = 5.5 V, T _J = 170°C, T _A = 25°C, see Thermal Characteristics			124	mA
		R _{θJA} = 212°C/W, V _I = 3.6 V, T _J = 170°C, T _A = 25°C, see Thermal Characteristics			190	
T _S	Safety temperature				150	°C

- (1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air [thermal resistance](#) in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.8 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤ 150 V _{RMS}	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-III	
		Rated mains voltage ≤ 400 V _{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):BASIC				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V _{PK}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} t = 60 s (qualification), t = 1 s (100% production)	4000	V _{PK}
q _{pd}	Apparent charge ⁽³⁾	Method a: After I/O safety test subgroup 2/3. V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IOR}	≤ 5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.3 × V _{IORM} , t _m = 10 s,	≤ 5	
		Method b1: At routine test (100% production) V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s,	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁴⁾	V _I = 0.4 sin(2πft), f = 1 MHz	1	pF
R _{IO}	Isolation resistance, input to output ⁽⁴⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 2500 V _{RMS} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} = 3000 V _{RMS} , t = 1 s (100% production)	2500	V _{RMS}

- Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier tied together creating a two-terminal device

5.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

, over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{CC1}	ISO7240CF	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V	1	3	mA
		25 Mbps		7	10.5	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	6.5	11	mA
		25 Mbps		12	18	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	10	16	mA
		25 Mbps		15	24	
I _{CC2}	ISO7240CF	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₂ at 3 V	15	22	mA
		25 Mbps		17	25	
	ISO7241C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	13	20	mA
		25 Mbps		18	28	
	ISO7242C	Quiescent	V _I = V _{CC} or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	10	16	mA
		25 Mbps		15	24	
ELECTRICAL CHARACTERISTICS						
I _{OFF}	Sleep mode output current	EN at 0 V, Single channel	0		μA	
V _{OH}	High-level output voltage	I _{OH} = -4 mA	V _{CC} - 0.8		V	
		I _{OH} = -20 μA	V _{CC} - 0.1			
V _{OL}	Low-level output voltage	I _{OL} = 4 mA	0.4		V	
		I _{OL} = 20 μA	0.1			
V _{I(HYS)}	Input voltage hysteresis		150		mV	
I _{IH}	High-level input current	IN from 0 V to V _{CC}	10		μA	
I _{IL}	Low-level input current		-10			
C _I	Input capacitance to ground	IN at V _{CC} , V _I = 0.4 sin(2πft), f=2MHz	2		pF	
CMTI	Common-mode transient immunity	V _I = V _{CC} or 0 V; 图 6-5	25	50	kV/μs	

- For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.10 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V	0.5	1.2		mA
		25 Mbps		3	5		
	ISO7241C	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	4	7		mA
		25 Mbps		6.5	11		
	ISO7242C	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	6	10		mA
		25 Mbps		9	14		
I_{CC2}	ISO7240CF	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V	9.5	15		mA
		25 Mbps		10.5	17		
	ISO7241C	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	8	13		mA
		25 Mbps		11.5	18		
	ISO7242C	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	6	10		mA
		25 Mbps		9	14		
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current	EN at 0 V, single channel		0			μ A
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA		$V_{CC} - 0.4$			V
		$I_{OH} = -20$ μ A		$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA		0.4			V
		$I_{OL} = 20$ μ A		0.1			
$V_{I(HYS)}$	Input voltage hysteresis			150			mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}		10			μ A
I_{IL}	Low-level input current					- 10	
C_1	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(2\pi ft)$, $f=2$ MHz		2			pF
CMTI	Common-mode transient immunity	$V_1 = V_{CC}$ or 0 V; 图 6-5		25	50		kV/ μ s

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.11 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₂ at 3 V	0.5	1.2		mA
		25 Mbps		3	5		
	ISO7241C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	4	7		mA
		25 Mbps		6.5	11		
	ISO7242C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	6	10		mA
		25 Mbps		9	14		
I_{CC2}	ISO7240CF	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₂ at 3 V	15	22		mA
		25 Mbps		17	25		
	ISO7241C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	13	20		mA
		25 Mbps		18	28		
	ISO7242C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V	10	16		mA
		25 Mbps		15	24		
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel		0			μ A
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA	ISO7240	$V_{CC} - 0.4$			V
			ISO724x (5-V side)	$V_{CC} - 0.8$			
		$I_{OH} = -20$ μ A	$V_{CC} - 0.1$				
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA		0.4			V
		$I_{OL} = 20$ μ A		0.1			
$V_{I(HYS)}$	Input voltage hysteresis			150			mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}		10			μ A
I_{IL}	Low-level input current						
C_1	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(2\pi ft)$, $f=2$ MHz		2			pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; 图 6-5		25	50		kV/ μ s

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.12 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation over recommended operating conditions (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V	1	3		mA
		25 Mbps		7	10.5		
	ISO7241C	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V	6.5	11		mA
		25 Mbps		12	18		
	ISO7242C	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V	10	16		mA
		25 Mbps		15	24		
I_{CC2}	ISO7240CF	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V	9.5	15		mA
		25 Mbps		10.5	17		
	ISO7241C	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V	8	13		mA
		25 Mbps		11.5	18		
	ISO7242C	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V	6	10		mA
		25 Mbps		9	14		
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel		0			μ A
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA	ISO7240	$V_{CC} - 0.4$			V
			ISO724x (5-V side)	$V_{CC} - 0.8$			
		$I_{OH} = -20$ μ A	$V_{CC} - 0.1$				
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA		0.4			V
		$I_{OL} = 20$ μ A		0.1			
$V_{I(HYS)}$	Input voltage hysteresis			150			mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}		10			μ A
I_{IL}	Low-level input current			-10			
C_I	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(2\pi ft)$, $f=2$ MHz		2			pF
CMTI	Common-mode transient immunity	$V_1 = V_{CC}$ or 0 V; 图 6-5		25	50		kV/ μ s

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
 For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See 图 6-1	25		56	ns
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} ^{(1)}$				4	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				10	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C			3.5	ns
		ISO7242C			4	
t_r	Output signal rise time	See 图 6-1		2		ns
t_f	Output signal fall time			2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 图 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See 图 6-3		18		μ s
t_{wake}	Wake time from input disable	See 图 6-4		15		μ s

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.14 Switching Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See 图 6-1	18		45	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				5	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				8	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C			3	ns
		ISO7242C			4	
t_r	Output signal rise time	See 图 6-1		2.4		ns
t_f	Output signal fall time			2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 图 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See 图 6-3		12		μ s
t_{wake}	Wake time from input disable	See 图 6-4		15		μ s

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.15 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} , t_{PHL}	Propagation delay	See 图 6-1	20		51	ns	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $	See 图 6-1			3		ns
					4		
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				10	ns	
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7240C, ISO7241C			3	ns	
		ISO7242C			4		
t_r	Output signal rise time	See 图 6-1		2.4		ns	
t_f	Output signal fall time			2.3			
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 图 6-2		15	25	ns	
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25		
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25		
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25		
t_{fs}	Failsafe output delay time from input power loss	See 图 6-3		12		μ s	
t_{wake}	Wake time from input disable	See 图 6-4		15		μ s	

(1) Also known as pulse skew

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.16 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} , t_{PHL}	Propagation delay	See 图 6-1	20		50	ns	
PWD ⁽¹⁾	See 图 6-1	ISO7240C, ISO7241C			3		ns
		ISO7242C			4		
PWD	See 图 6-1				3	ns	
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾				10	ns	
t_r	Output signal rise time	See 图 6-1		2.4		ns	
t_f	Output signal fall time			2.3			
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 图 6-2		15	25	ns	
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25		
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25		
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25		
t_{fs}	Failsafe output delay time from input power loss	See 图 6-3		18		μ s	
t_{wake}	Wake time from input disable	See 图 6-4		15		μ s	

(1) Also known as pulse skew

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.17 Insulation Characteristics Curves

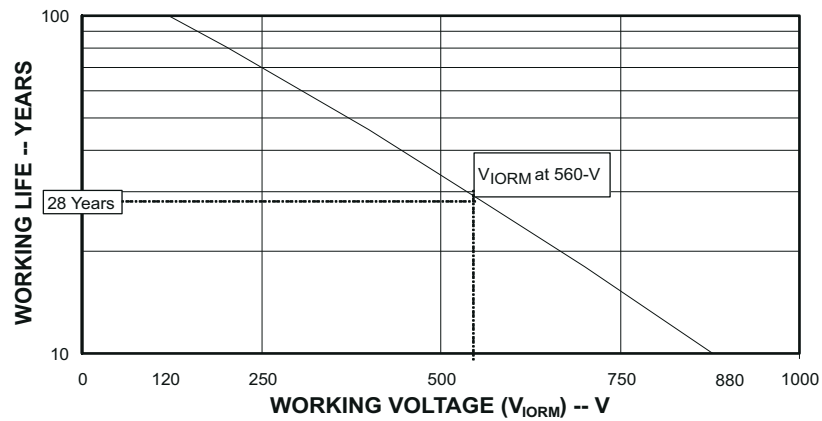


图 5-1. Time Dependent Dielectric Breakdown Testing Results

5.18 Typical Characteristic

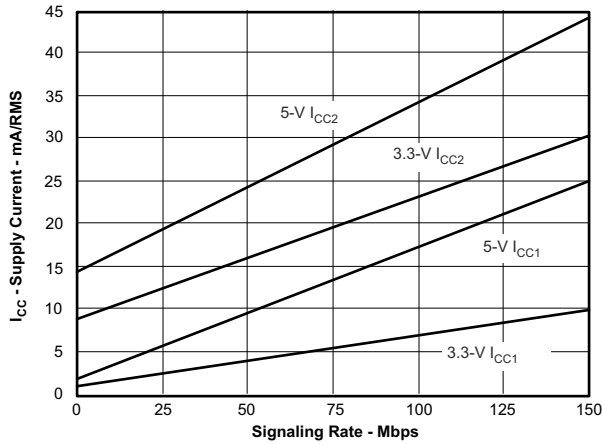


图 5-2. ISO7240C RMS Supply Current vs Signaling Rate

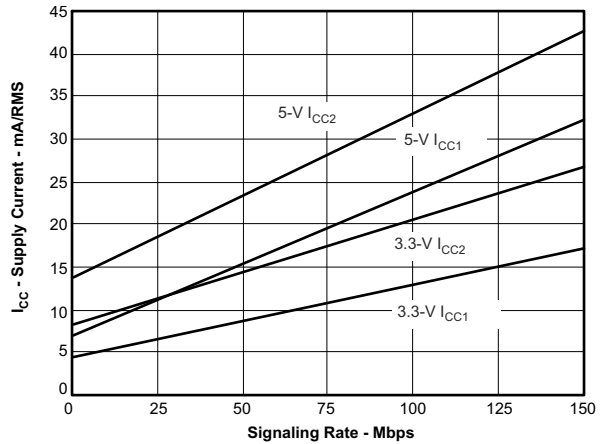


图 5-3. ISO7241C RMS Supply Current vs Signaling Rate

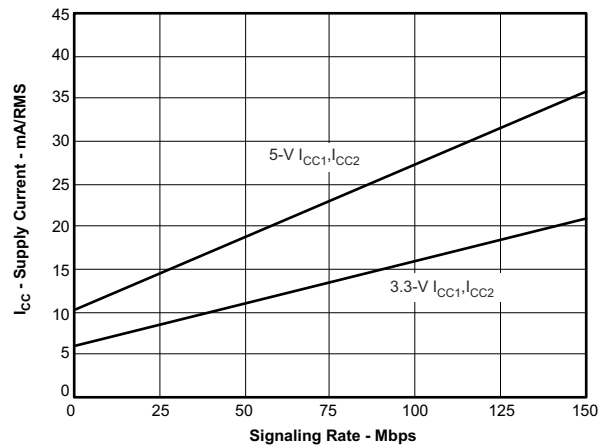


图 5-4. ISO7242C RMS Supply Current vs Signaling Rate

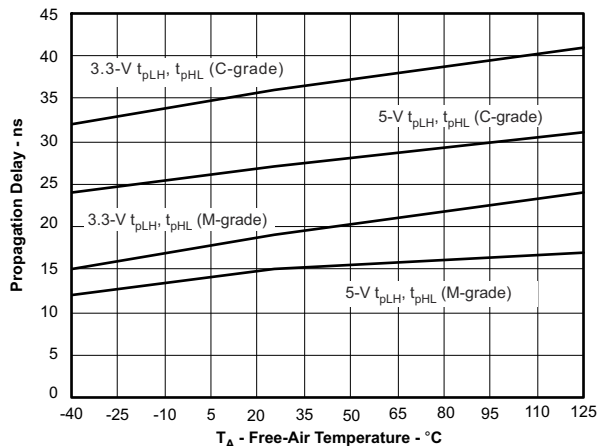


图 5-5. Propagation Delay vs Free-Air Temperature

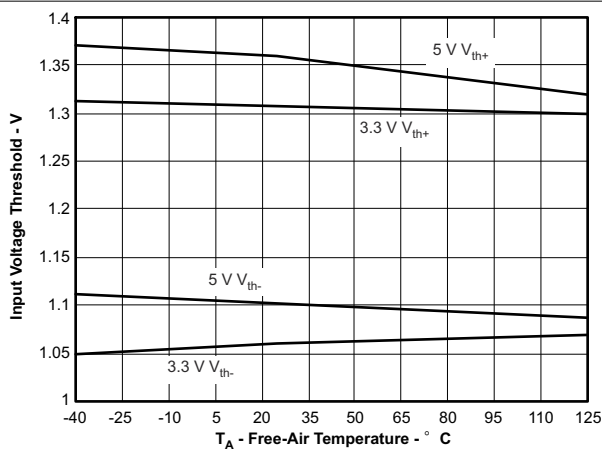


图 5-6. Input Voltage Threshold vs Free-Air Temperature

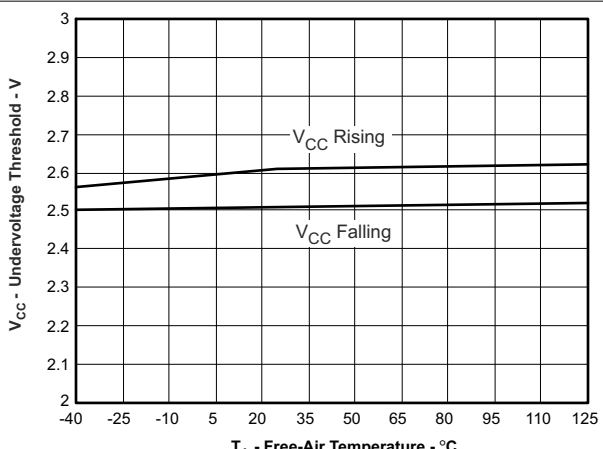
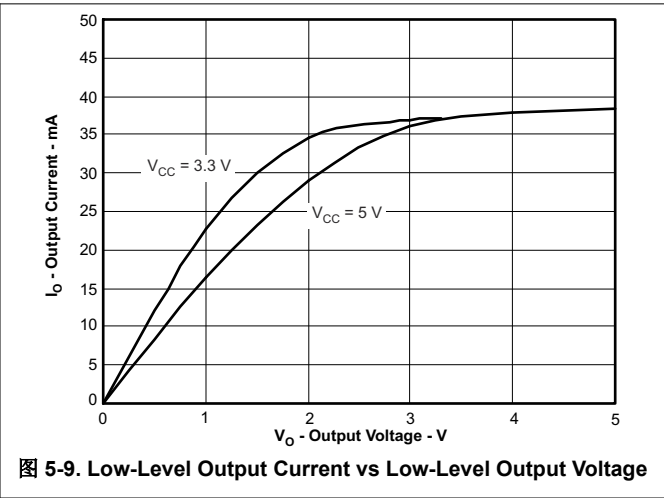
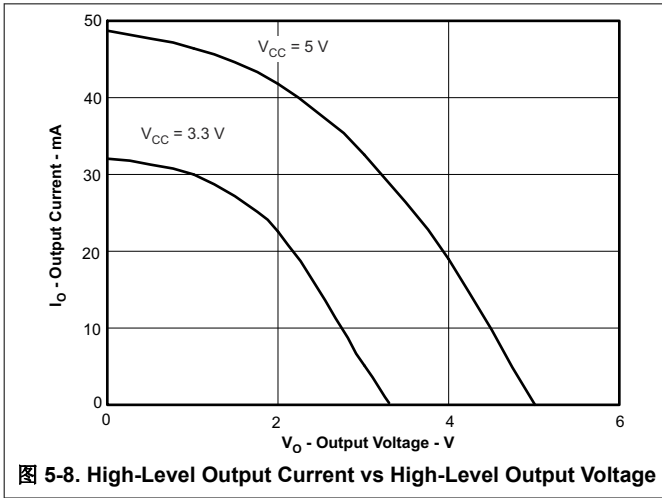
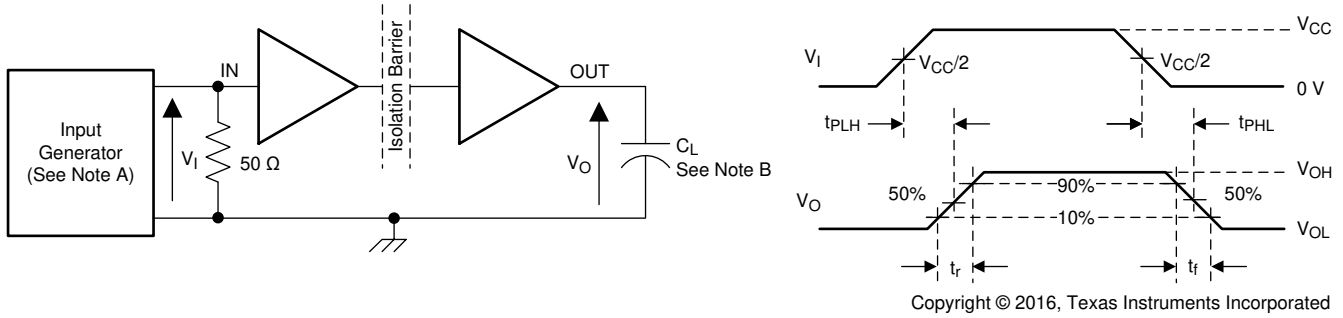


图 5-7. VCC1 Failsafe Threshold vs Free-Air Temperature

5.18 Typical Characteristic (continued)

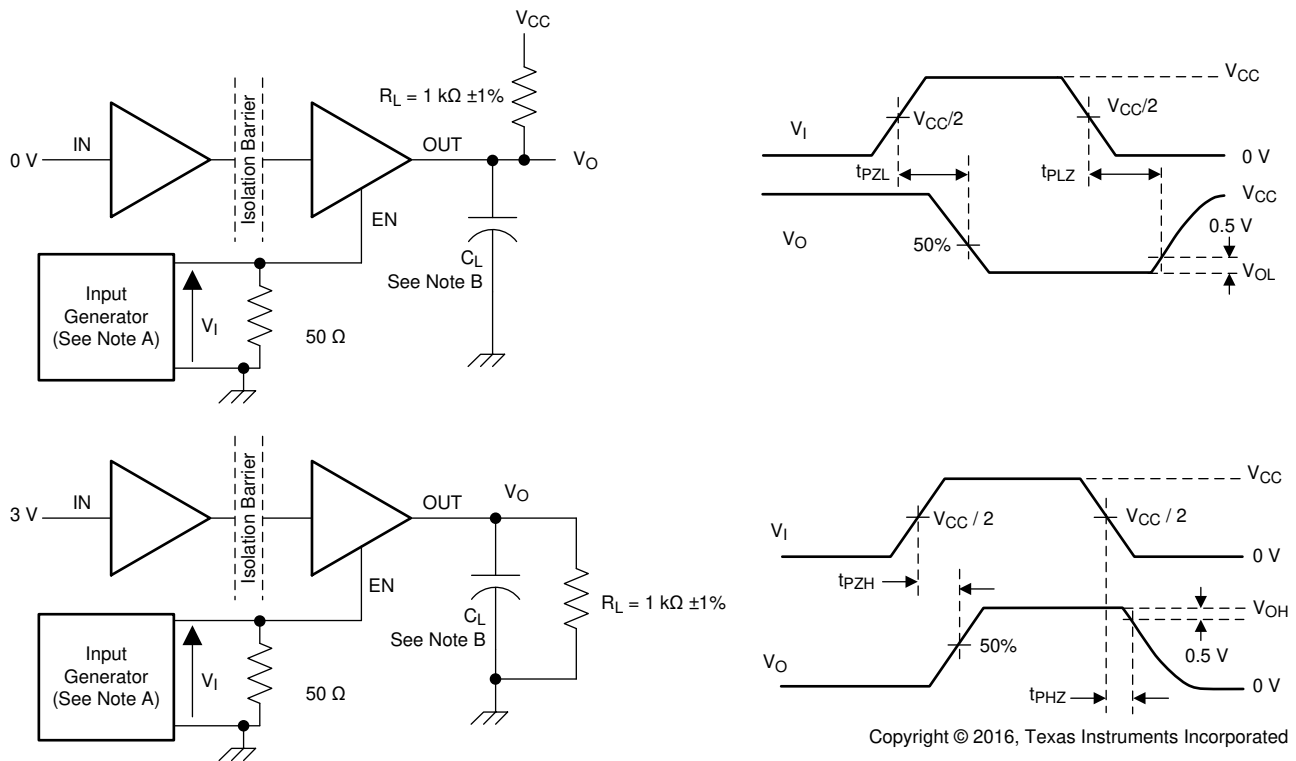


6 Parameter Measurement Information



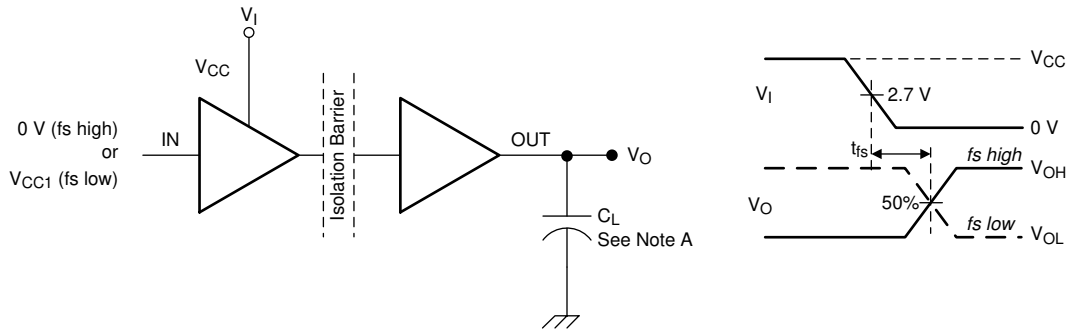
- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.
- B. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



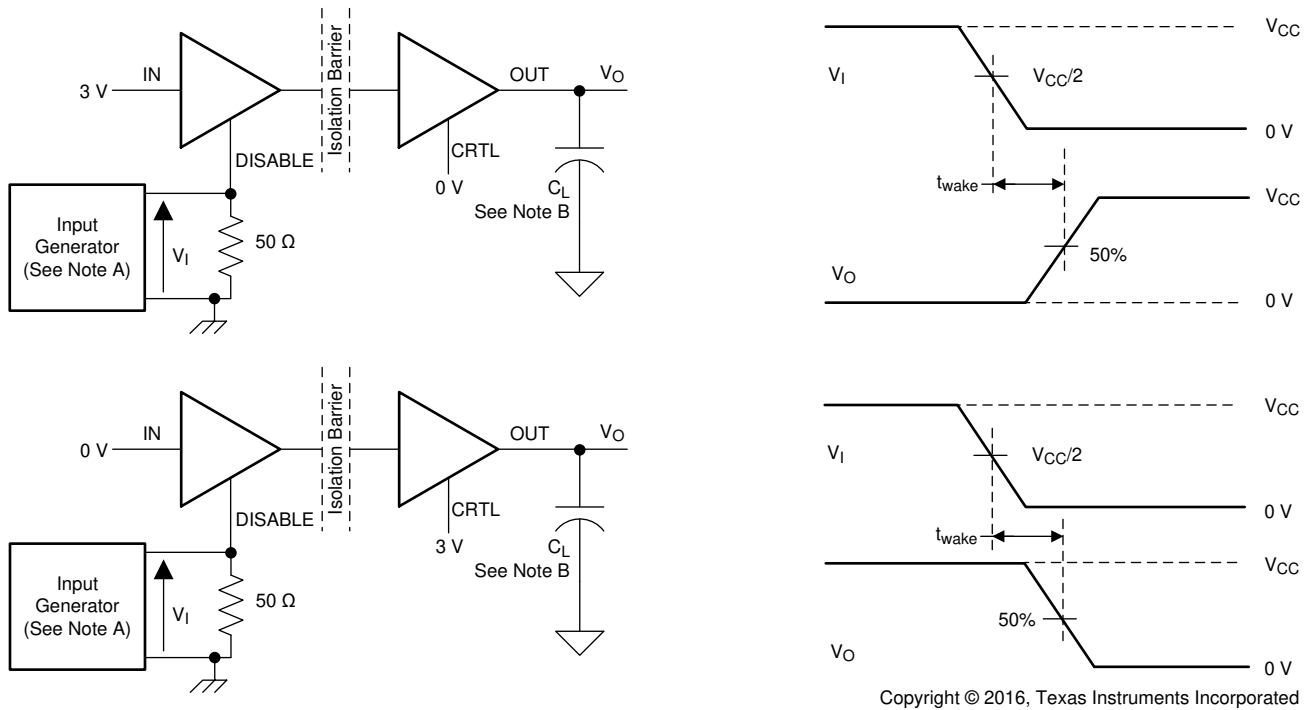
- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.
- B. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 6-2. Enable or Disable Propagation-Delay Time Test Circuit and Waveform



A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

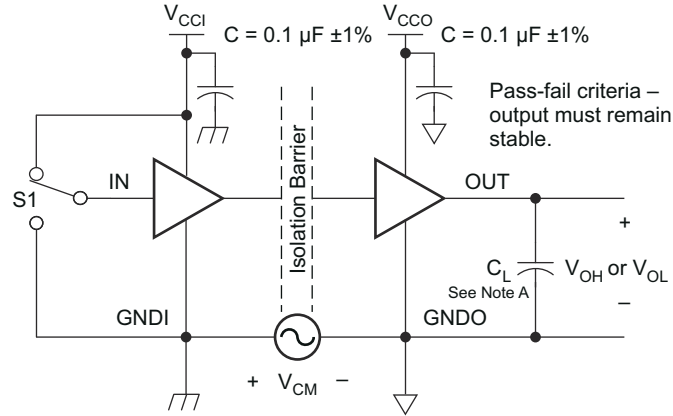
图 6-3. Failsafe Delay Time Test Circuit and Voltage Waveforms



The test that yields the longest time is used in this data sheet.

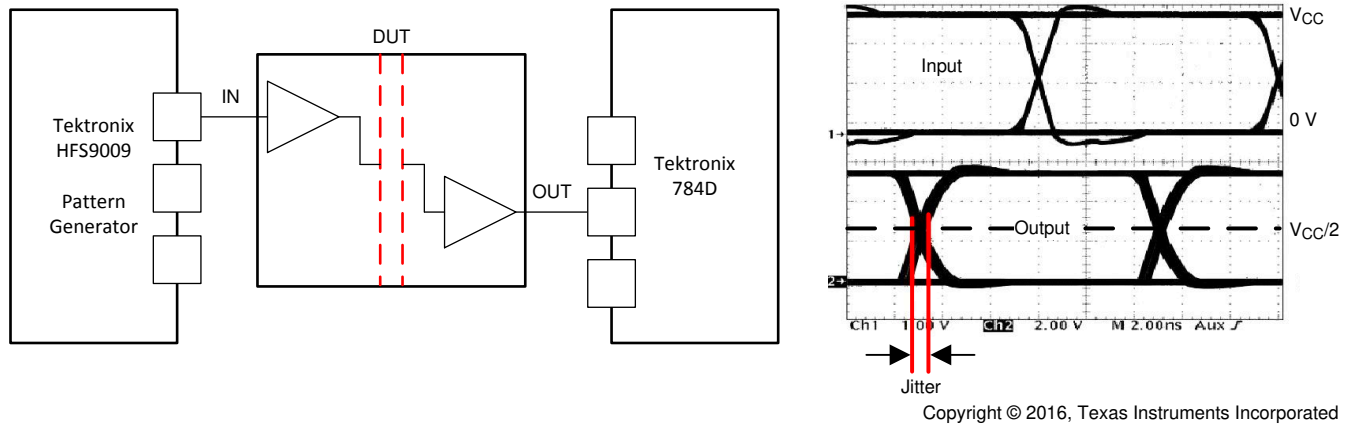
- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 6-4. Wake Time From Input Disable Test Circuit and Voltage Waveforms



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_0 = 50 \Omega$.

图 6-5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

图 6-6. Peak-to-Pek Eye-Pattern Jitter Test Circuit and Voltage Waveform

7 Detailed Description

7.1 Overview

The ISO724x-Q1 family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram

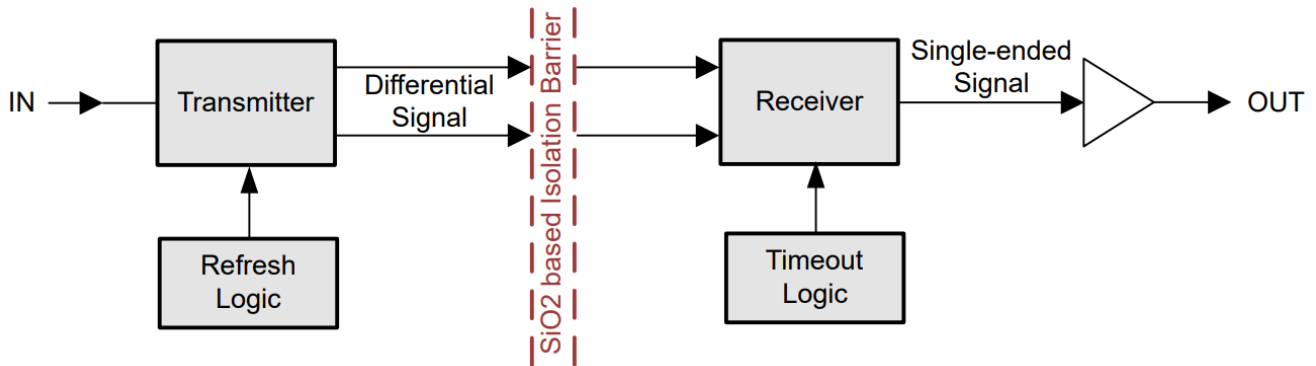


图 7-1. Conceptual Block Diagram of a Digital Isolator

7.3 Feature Description

The ISO724x-Q1 family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. 表 7-1 lists these device features.

表 7-1. Device Features

PRODUCT ⁽¹⁾	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240CF	25 Mbps	≈1.5 V (TTL)	4/0
ISO7241C	25 Mbps	≈1.5 V (TTL)	3/1
ISO7242C	25 Mbps	≈1.5 V (TTL)	2/2

(1) For the most current package and ordering information, see the 节 11 section, or see the TI website at www.ti.com.

7.4 Device Functional Modes

List of ISO724x-Q1 functional modes.

表 7-2. Device Function Table ISO724x-Q1

INPUT V _{CC}	OUTPUT V _{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

7.4.1 Device I/O Schematics

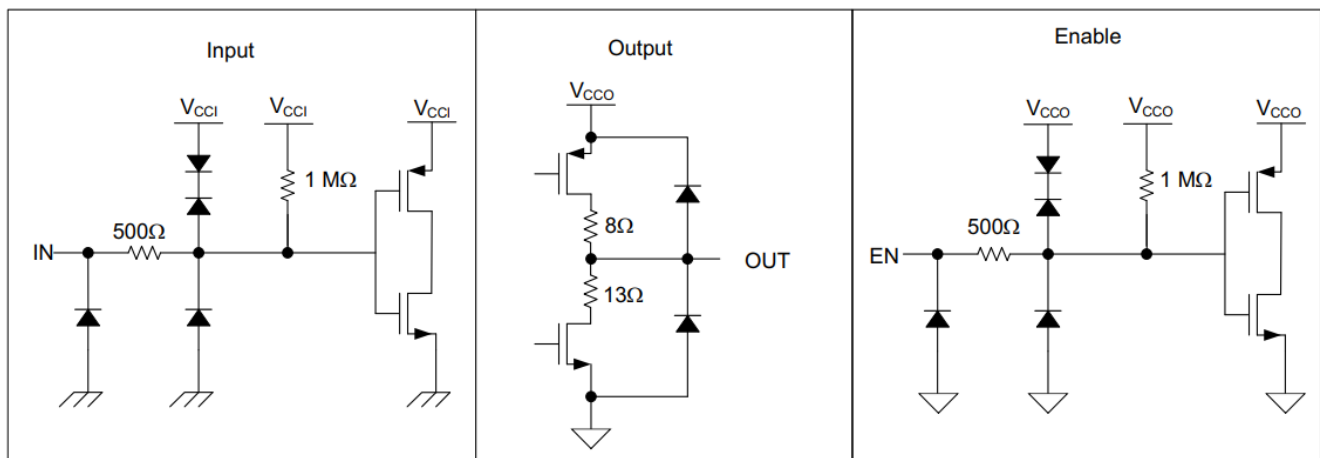


图 7-2. Device I/O Schematics

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

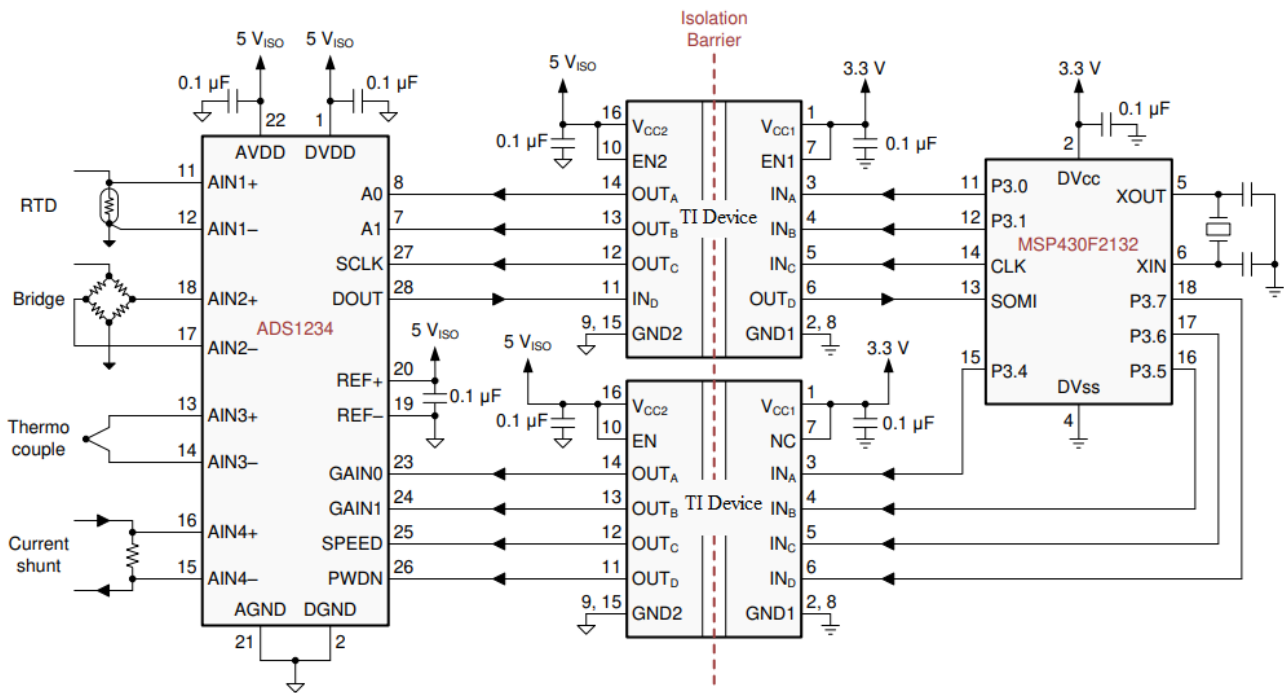
8.1 Application Information

The ISO724x-Q1 family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

8.2.1 Isolated Data Acquisition System for Process Control

The ISO724x-Q1 family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in 图 8-1.



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图 8-1. Isolated Data Acquisition System for Process Control

8.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x-Q1 family of devices only require two external bypass capacitors to operate.

8.2.1.2 Detailed Design Procedure

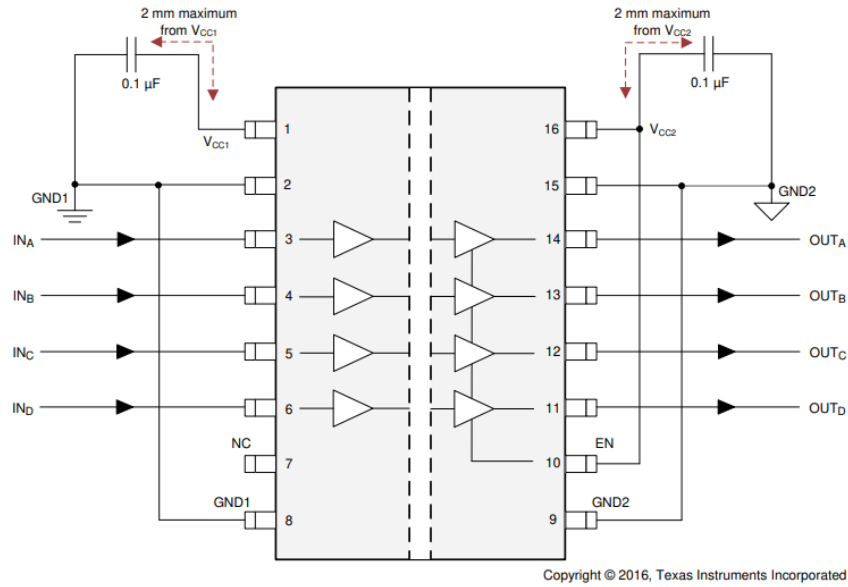


图 8-2. ISO7240x-Q1 Typical Circuit Hook-Up

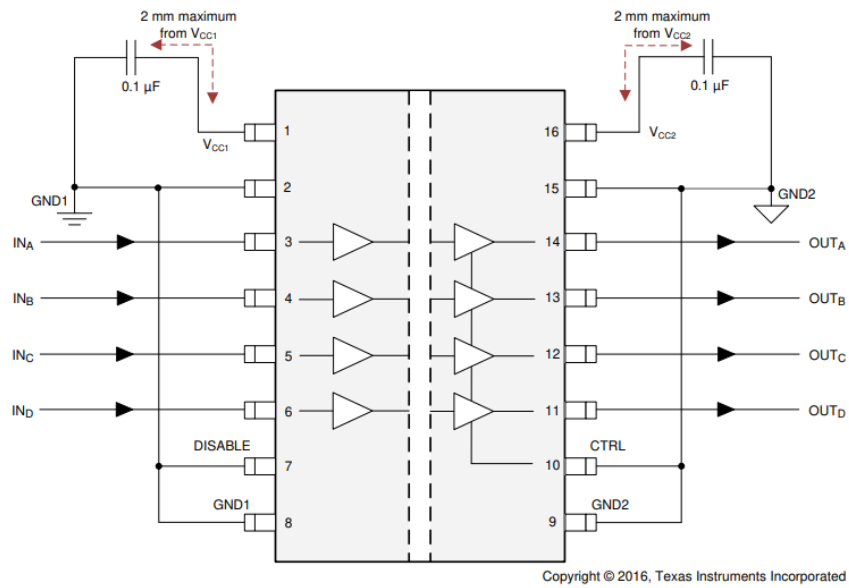


图 8-3. ISO7240CF-Q1 Typical Circuit Hook-Up

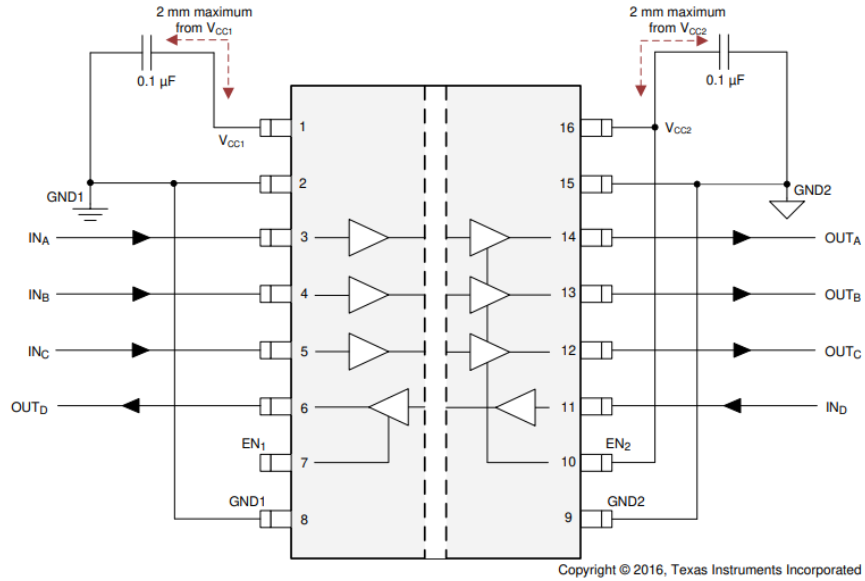


图 8-4. ISO7241x-Q1 Typical Circuit Hook-Up

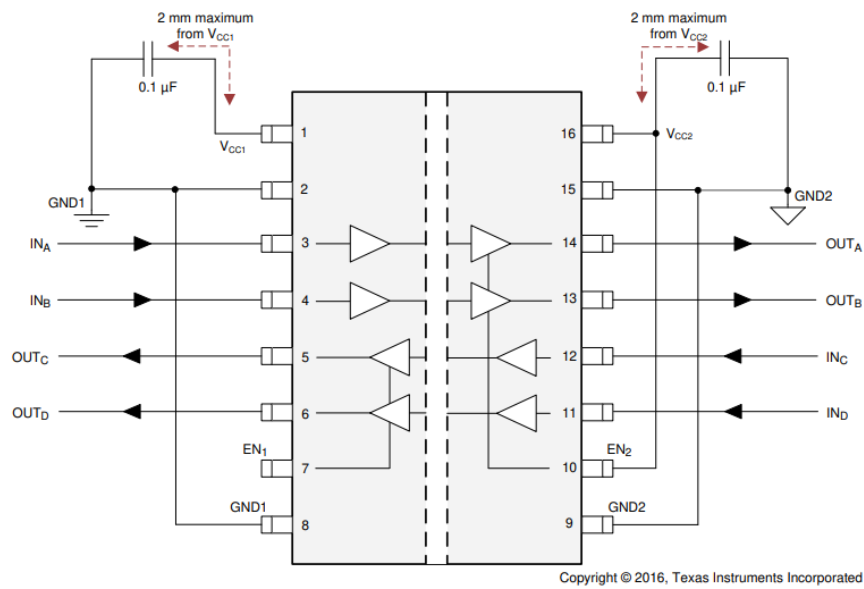


图 8-5. ISO7242x-Q1 Typical Circuit Hook-Up

8.2.2 Isolated SPI for an Analog Input Module with 16 Inputs

The ISO7241x-Q1 family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.

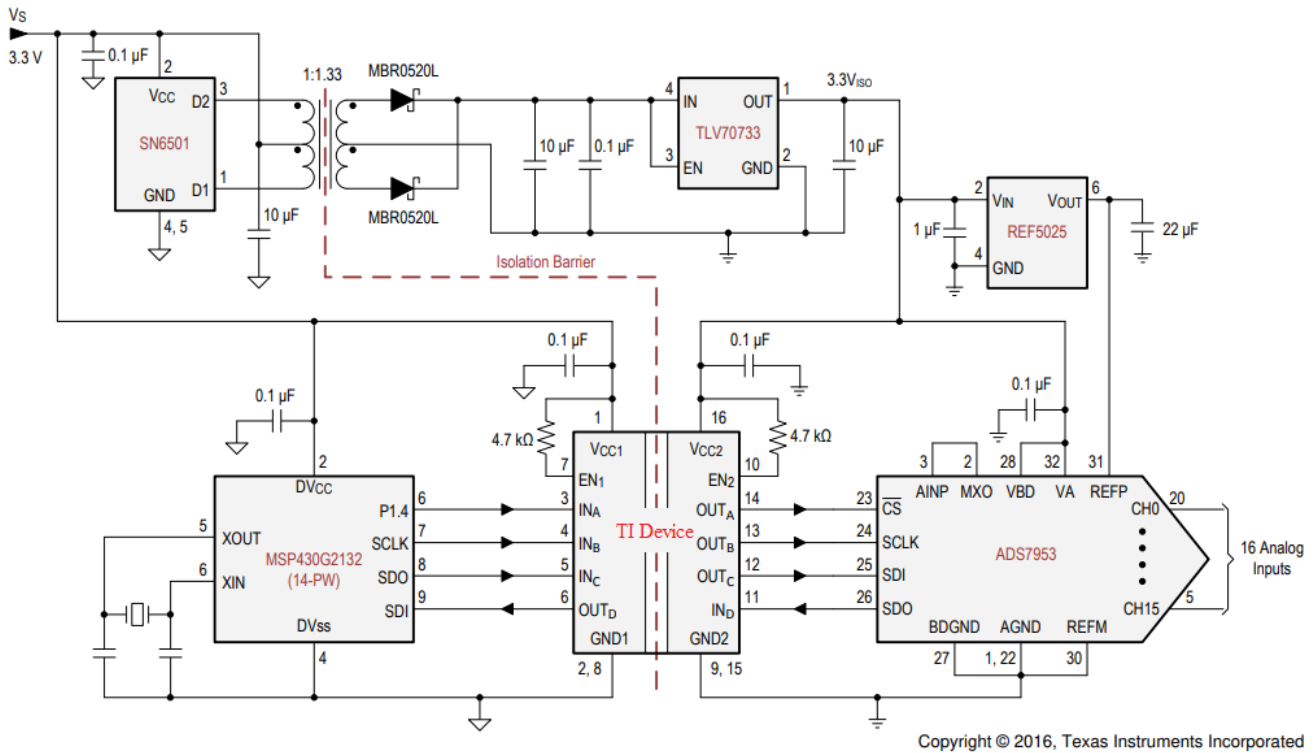


图 8-6. Isolated SPI for an Analog Input Module With 16 Inputs

8.2.2.1 Design Requirements

See the [Design Requirements](#) in [节 8.2.1](#).

8.2.2.2 Detailed Design Procedure

See the [Detailed Design Procedure](#) in [节 8.2.1](#).

8.2.3 Isolated RS-232 Interface

[图 8-7](#) shows a typical isolated RS-232 interface implementation.

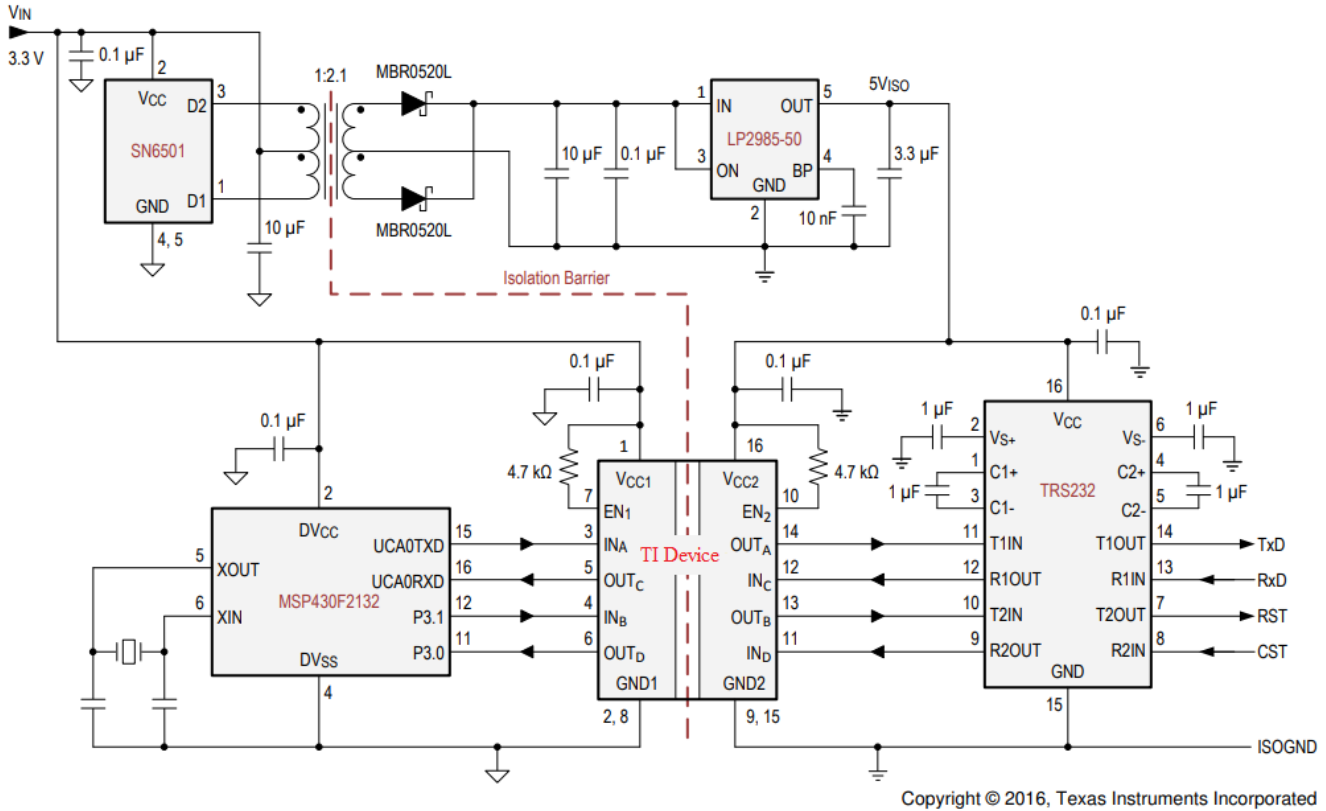


图 8-7. Isolated RS-232 Interface

8.2.3.1 Design Requirements

See the [Design Requirements](#) in [§ 8.2.1](#).

8.2.3.2 Detailed Design Procedure

See the [Detailed Design Procedure](#) in [§ 8.2.1](#).

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#).

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [图 8-8](#)). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to [Digital Isolator Design Guide](#).

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

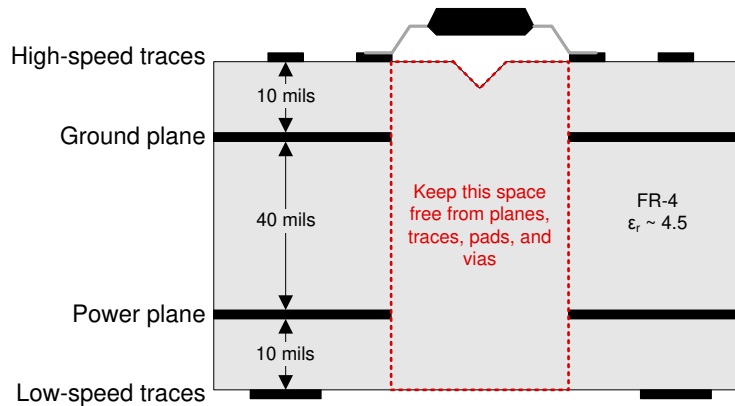


图 8-8. Recommended Layer Stack

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- [Digital Isolator Design Guide](#)
- [Isolation Glossary](#)

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要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

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所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (November 2024) to Revision C (February 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

Changes from Revision A (September 2011) to Revision B (November 2024)	Page
• 通篇将引用内容从电容隔离更新为隔离栅.....	1
• 通篇将“VDE V 0884-11”更新为“DIN VDE 0884-17”.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	5
• Updated electrical and switching characteristics to match device performance.....	7

- Added the *Detailed Description, Overview, Feature Description, Functional Block Diagram, and Device Functional Modes* sections..... 19
 - Added the *Typical Application, Power Supply Recommendations, and Layout* sections..... 21
-

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CFQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CFQ	Samples
ISO7241CQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241CQ	Samples
ISO7242CQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242CQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1 :

- Catalog : [ISO7240CF](#), [ISO7241C](#), [ISO7242C](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CFQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CFQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

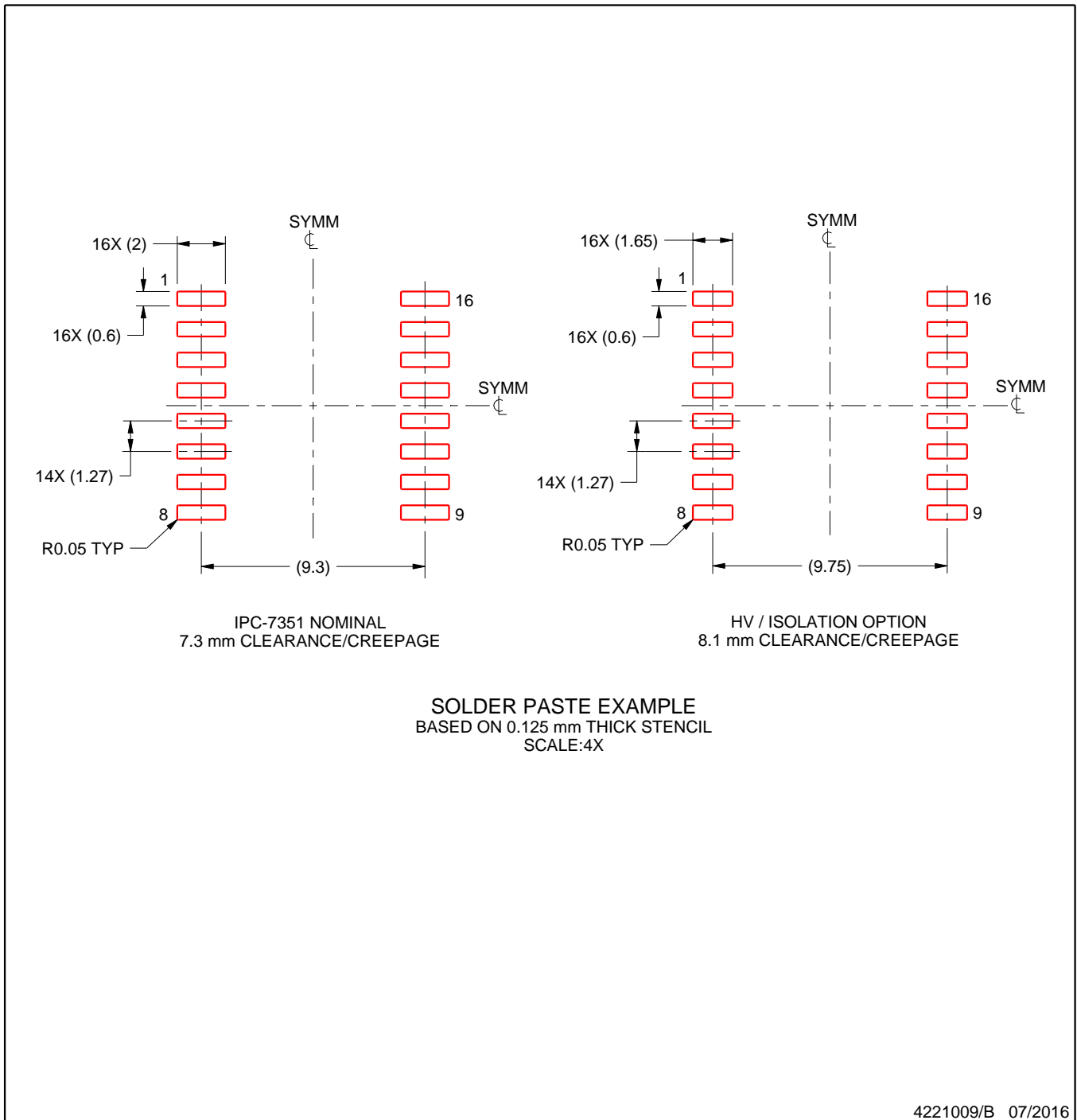
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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