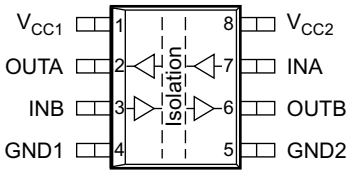
低功耗双通道数字隔离器

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H3A**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C5**
- 高信号传输速率：**50Mbps**
- 低功耗
- 低传播延迟 **- 9ns**（典型值）
- 低偏斜 **- 300ps**（典型值）
- **4kV** 峰值最大隔离，经 **UL 1577** 认证的 **2.5 kVrms**，经 **IEC/VDE** 和 **CSA** 批准，符合 **IEC 60950-1**，**IEC 61010-1** 终端设备标准。 所有的审批正在审理中。
- 瞬态抗扰度 **50KV/μs**（典型值）
- 在额定电压上超过 **25** 年的隔离装置完好性
- 运行在 **3V** 至 **5.5V** 电源和逻辑电平上

ISO7421A-Q1
D PACKAGE
(TOP VIEW)



说明

ISO7421A-Q1 按照 UL 标准，在 1 分钟内提供高达 2.5 kVrms 的电流隔离。 这个数字隔离器有两条具有双向通道配置的隔离通道。 每个隔离通道都有一个由二氧化硅 (SiO_2) 绝缘隔栅分开的逻辑输入和输出缓冲器。 通过与隔离电源一起使用，这些器件可防止数据总线或者其它电路上的噪音电流进入本地接地并干扰或者损坏敏感电路。

此器件有 TTL 输入阈值并要求两个介于 3V 和 5.5V 之间的电源电压，或者任一组合。 当由一个 3V 电源供电时，所有输入为 5V 耐压。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	ISO7421AQDRQ1	7421AQ

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	–	Ground connection for V_{CC1}
GND2	5	–	Ground connection for V_{CC2}
INA	7	I	Input, channel A
INB	3	I	Input, channel B
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	–	Power supply, V_{CC1}
V_{CC2}	8	–	Power supply, V_{CC2}

Table 1. FUNCTION TABLE(1)

INPUT SIDE VCC	OUTPUT SIDE VCC	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered up (V_{CC} ≥ 3 V), PD = Powered down (V_{CC} ≤ 2.4 V), X = Irrelevant, H = High level, L = Low level

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}			–0.5 V to 6 V
V_I	Voltage at IN, OUT			–0.5 V to 6 V
I_O	Output current			±15 mA
ESD	Electrostatic discharge	Human-body model (HBM) AEC-Q100 Classification Level H3A	All pins	4 kV
		Charged-device model (CDM) AEC-Q100 Classification Level C5		1.5 kV
		Machine model (MM)		200 V
$T_{J(Max)}$	Maximum junction temperature			150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
T_A	Operating temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC2} = 5 V ±10%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA, see Figure 1		V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, see Figure 1		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, see Figure 1			0.2	0.4	V
		I_{OL} = 20 µA, see Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1.2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, see Figure 3		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		2.3	3.6	mA
I_{CC2}			AC Input: C_L = 15 pF		2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			6	9.1	
I_{CC2}					6	9.1	

SWITCHING CHARACTERISTICS

V_{CC1} = V_{CC2} = 5 V ±10%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		9	14	ns
PWD (1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See Figure 1		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs
t_{ui}	Input pulse duration		7			ns
1 / t_{ui}	Signaling rate		0		50	Mbps

(1) Also known as pulse skew

ELECTRICAL CHARACTERISTICS

V_{CC1} = 5 V ±10%, V_{CC2} = 3.3 V ±10%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA, see Figure 1, 5-V side		V_{CC} – 0.8			V
		I_{OH} = –20 µA, see Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, see Figure 1				0.4	V
		I_{OL} = 20 µA, see Figure 1				0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1.2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, see Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		2.3	3.6	mA
I_{CC2}			AC Input: C_L = 15 pF		1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			6	9.1	
I_{CC2}					3.8	5.8	

SWITCHING CHARACTERISTICS

V_{CC1} = 5 V ±10%, V_{CC2} = 3.3 V ±10%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD (1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs
t_{ui}	Input pulse duration		7			ns
1 / t_{ui}	Signaling rate		0		50	Mbps

(1) Also known as pulse skew

ELECTRICAL CHARACTERISTICS

V_{CC1} = 3.3 V ±10%, V_{CC2} = 5 V ±10%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA, see Figure 1, 3.3-V side		V_{CC} – 0.4			V
		I_{OH} = –20 µA, see Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, see Figure 1				0.4	V
		I_{OL} = 20 µA, see Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, see Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		1.8	2.8	mA
I_{CC2}			AC Input: C_L = 15 pF		2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			3.8	5.8	
I_{CC2}					6	9.1	

SWITCHING CHARACTERISTICS

V_{CC1} = 3.3 V ±10%, V_{CC2} = 5 V ±10%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD (1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs
t_{ui}	Input pulse duration		7			ns
1 / t_{ui}	Signaling rate		0		50	Mbps

(1) Also known as pulse skew

ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC2} = 3.3 V ±5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA, see Figure 1		V_{CC} – 0.4	3		V
		I_{OH} = –20 µA, see Figure 1		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, see Figure 1			0.2	0.4	V
		I_{OL} = 20 µA, see Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, see Figure 3.		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V		1.8	2.8	mA
I_{CC2}			AC Input: C_L = 15 pF		1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			3.8	5.8	
I_{CC2}					3.8	5.8	

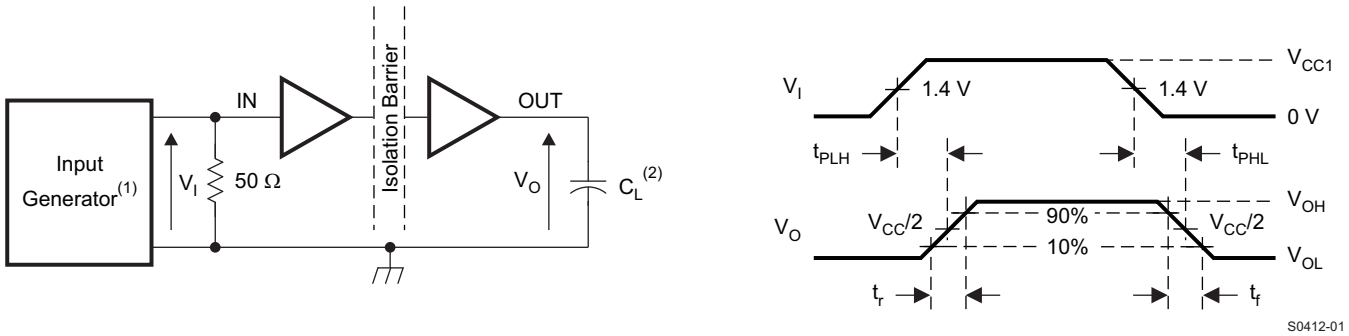
SWITCHING CHARACTERISTICS

V_{CC1} = V_{CC2} = 3.3 V ± 5%, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		12	20	ns
PWD (1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time				5.5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		µs
t_{ui}	Input pulse duration		7			ns
1 / t_{ui}	Signaling rate		0		50	Mbps

(1) Also known as pulse skew

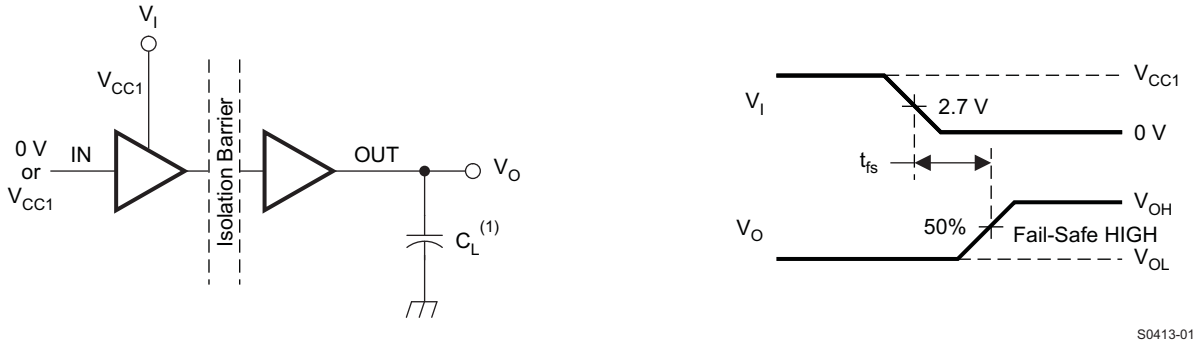
PARAMETER MEASUREMENT INFORMATION



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

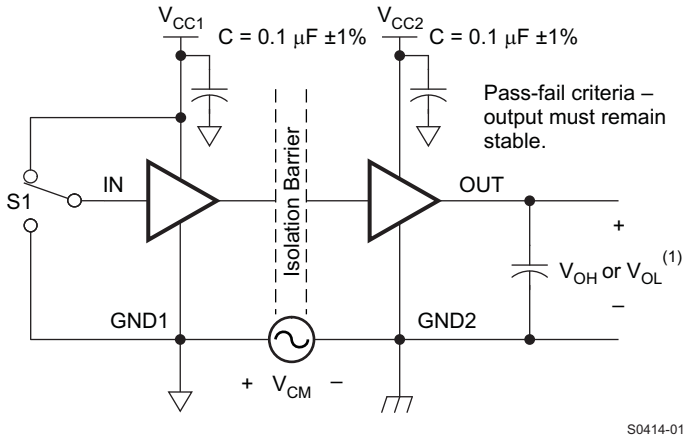
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>175			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input to output		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output	V_I = 0.4 sin (4E6πt)		1		pF

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input-to-output test voltage	t = 1 s (100% production), partial discharge 5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s (qualification)	4000	V
		t = 1 s (100% production)		
V_{ISO}	Isolation voltage per UL	t = 60 s (qualification)	2500	Vrms
		t = 1 s (100% production)	3000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 2. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	III-a
Installation classification	Rated mains voltage ≤ 150 Vrms	I–IV
	Rated mains voltage ≤ 300 Vrms	I–III
	Rated mains voltage ≤ 400 Vrms	I–II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File number: pending (40016131)	File number: pending (1698195)	File number: pending (E181974)

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

LIFE EXPECTANCY versus WORKING VOLTAGE

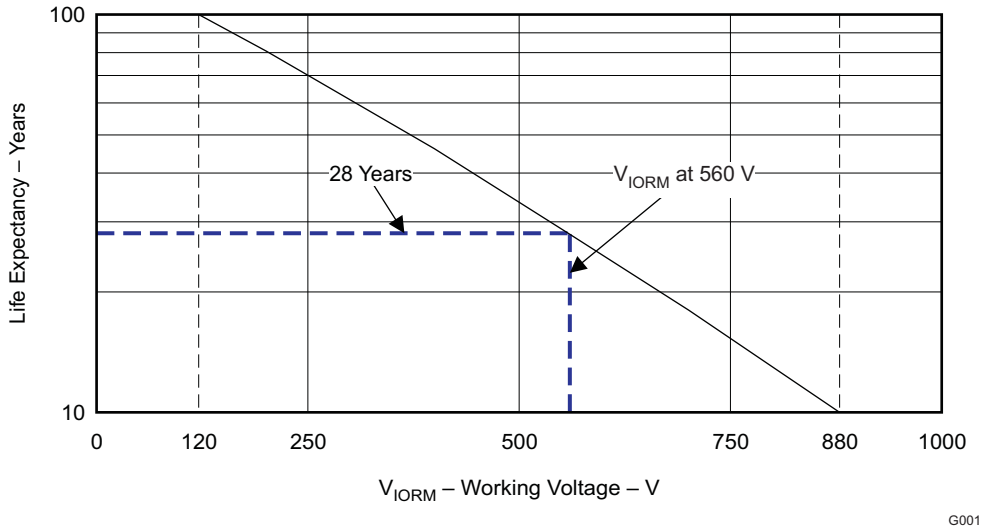


Figure 4. Life Expectancy versus Working Voltage

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			112	mA
		θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			171	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		212		°C/W
		High-K thermal resistance(1)		122		
θ_{JB}	Junction-to-board thermal resistance			37		°C/W
θ_{JC}	Junction-to-case thermal resistance			69.1		°C/W
P_D	Device power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, Input a 150-Mbps 50% duty-cycle square wave			390	mW

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages

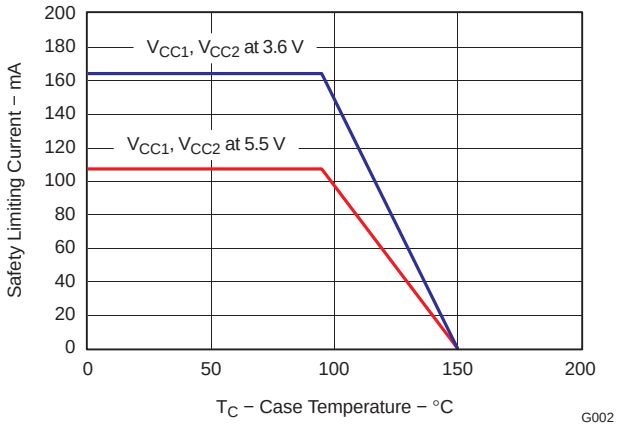


Figure 5. θ_{JC} Thermal Derating Curve per IEC 60747-5-2

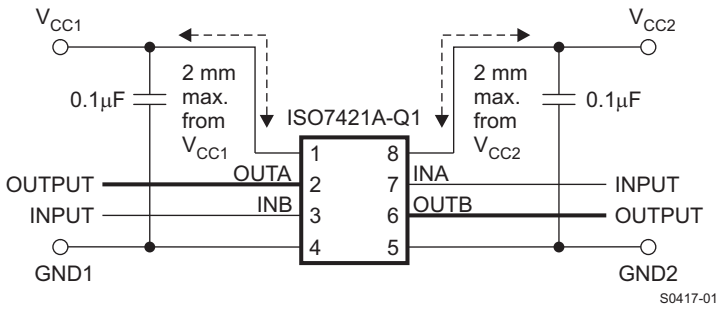


Figure 6. Typical ISO7421A-Q1 Application Circuit

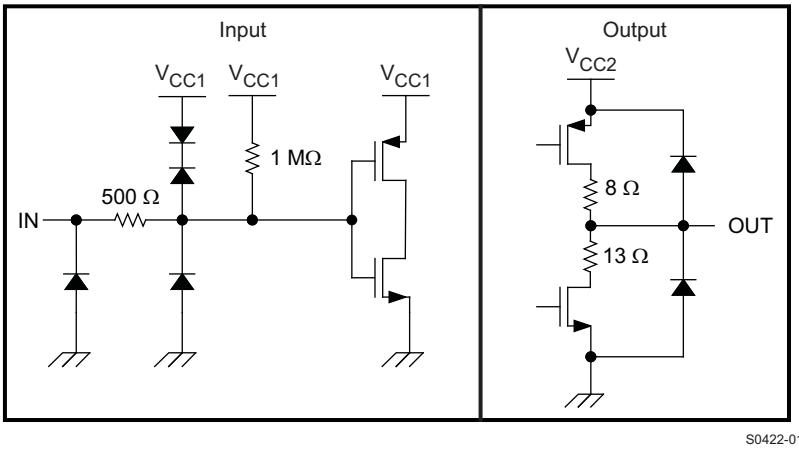


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

SUPPLY CURRENT versus SIGNAL RATE (ALL CHANNELS)

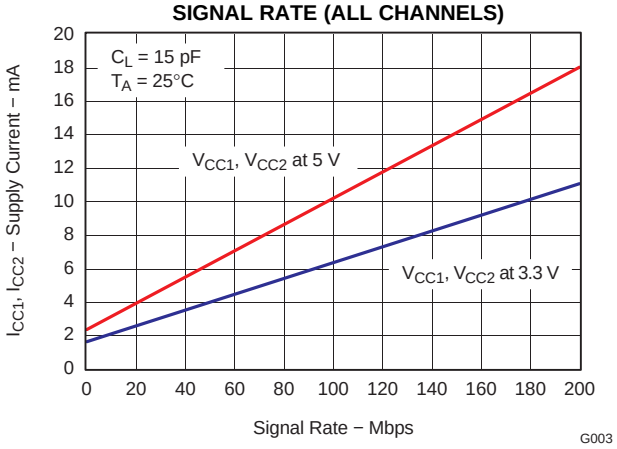


Figure 8.

PROPAGATION DELAY TIME versus FREE-AIR TEMPERATURE

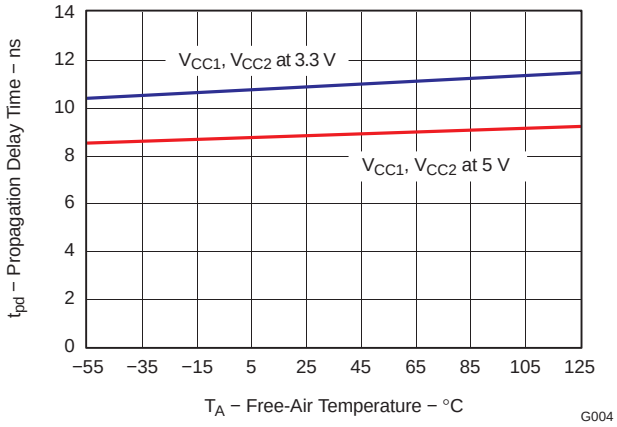


Figure 9.

INPUT VOLTAGE SWITCHING THRESHOLD versus FREE-AIR TEMPERATURE

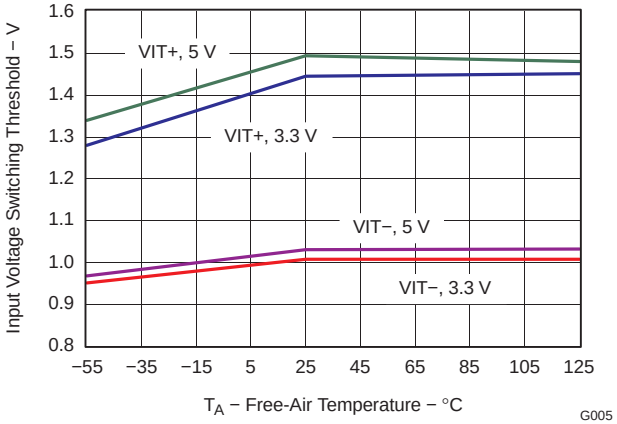


Figure 10.

FAIL-SAFE VOLTAGE THRESHOLD versus FREE-AIR TEMPERATURE

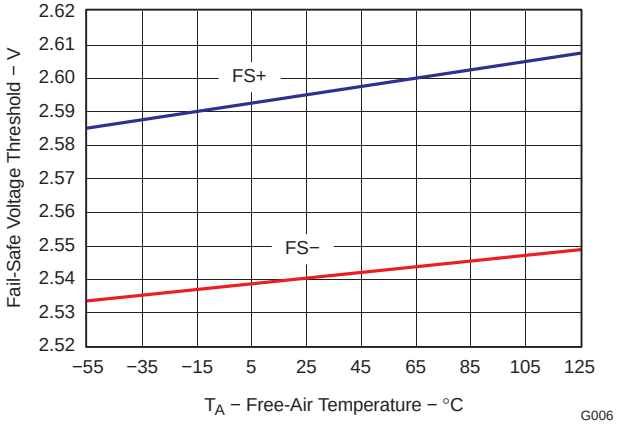


Figure 11.

HIGH-LEVEL OUTPUT CURRENT versus HIGH-LEVEL OUTPUT VOLTAGE

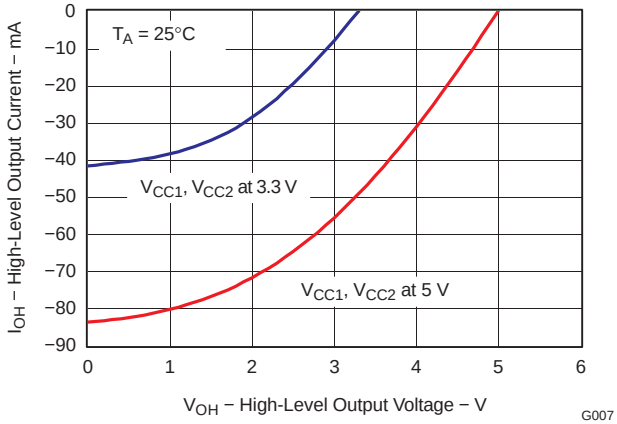


Figure 12.

LOW-LEVEL OUTPUT CURRENT versus LOW-LEVEL OUTPUT VOLTAGE

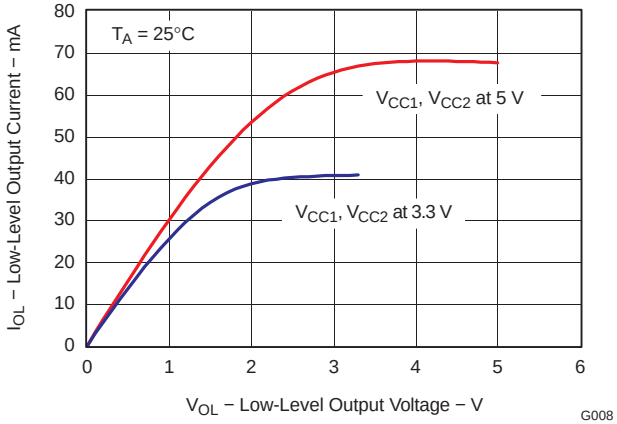


Figure 13.

TYPICAL CHARACTERISTICS (continued)

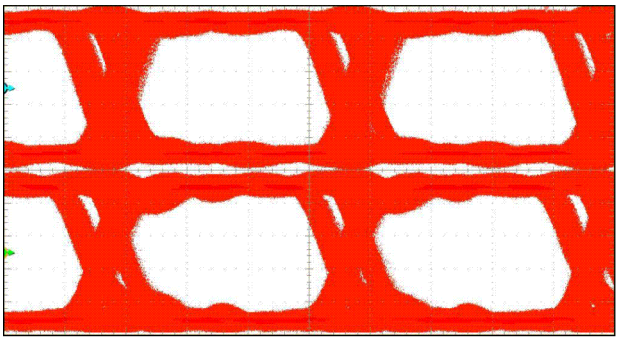


Figure 14. Eye Diagram at 250 MBPS, 5-V V_{CC}, Typical

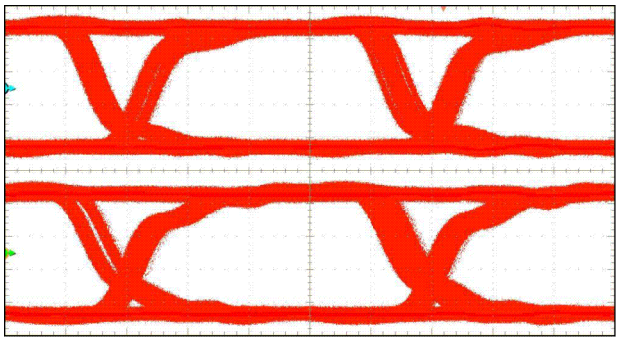


Figure 15. Eye Diagram at 200 MBPS, 5-V V_{CC}, 125°C

REVISION HISTORY

Changes from Revision A (September 2012) to Revision B **Page**

Changes from Original (March, 2012) to Revision A **Page**

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7421AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7421AQ
ISO7421AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7421AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

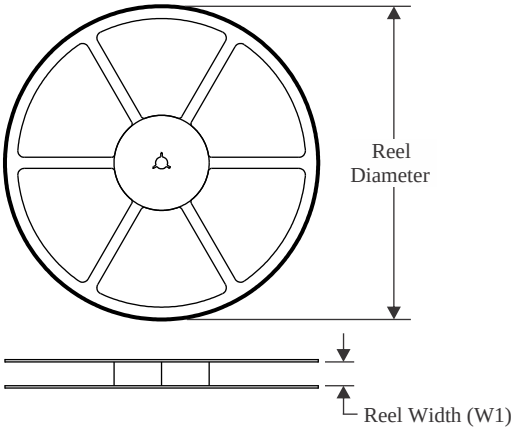
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

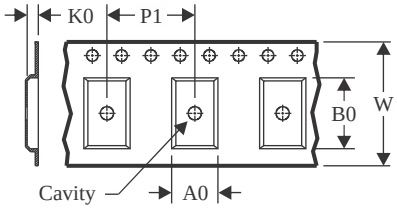
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

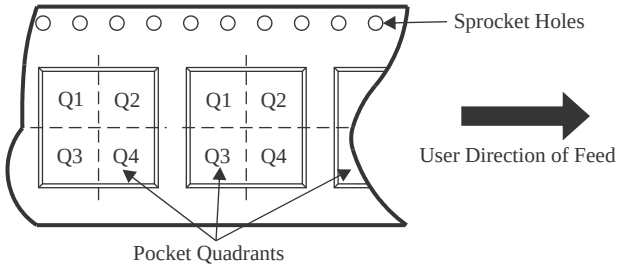


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

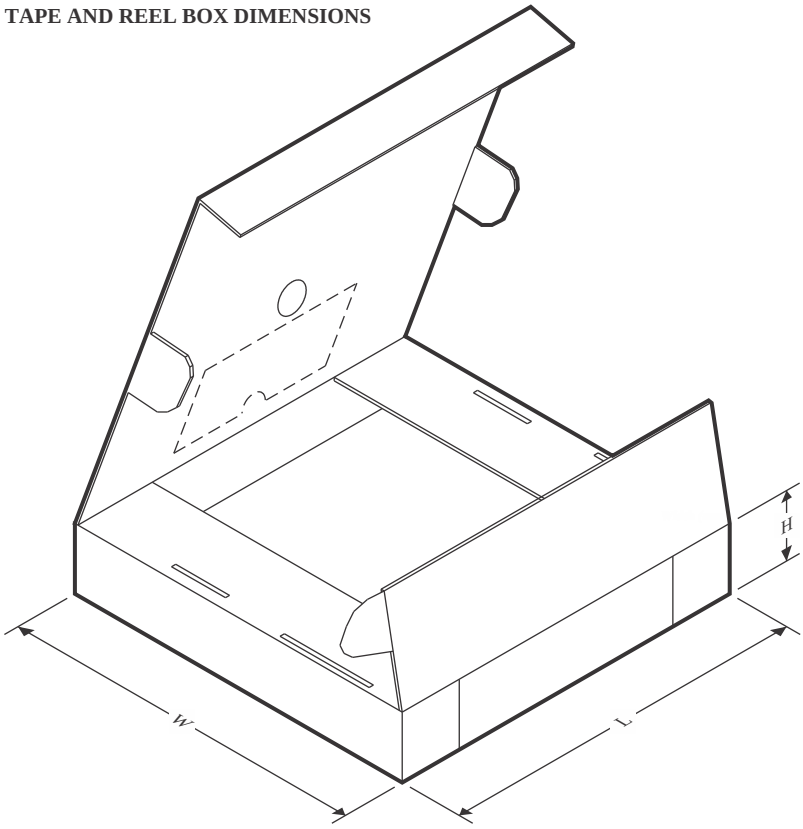
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

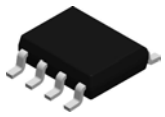
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7421AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7421AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

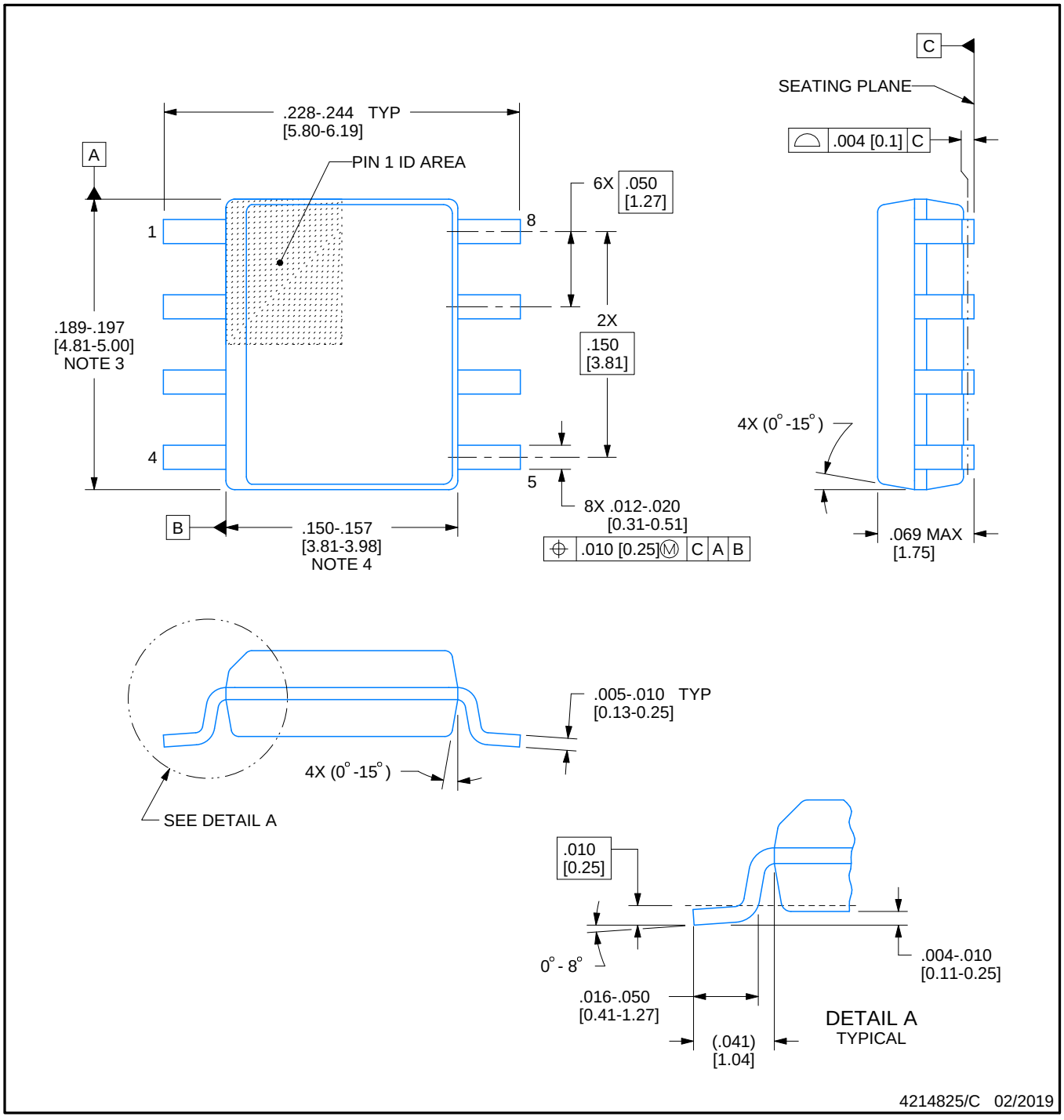


PACKAGE OUTLINE

D0008A

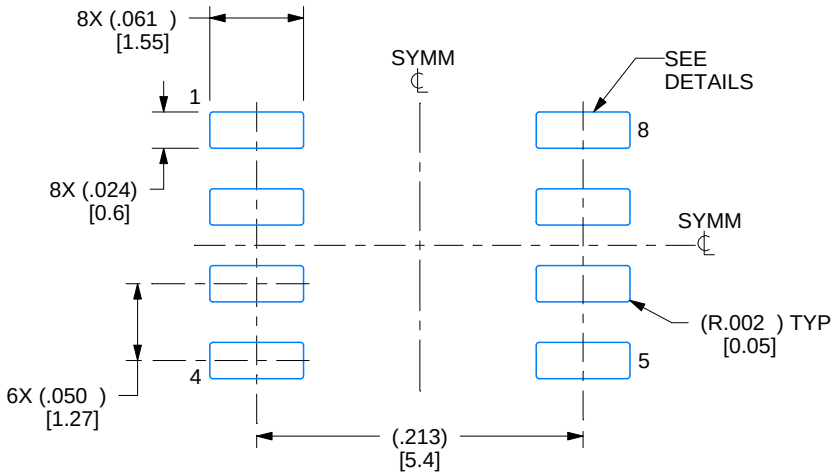
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

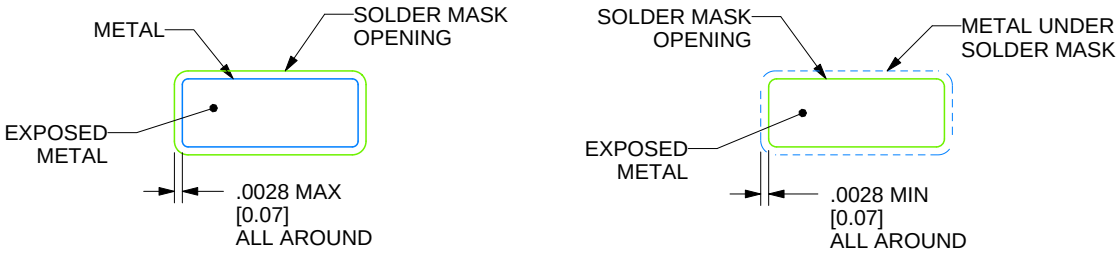


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

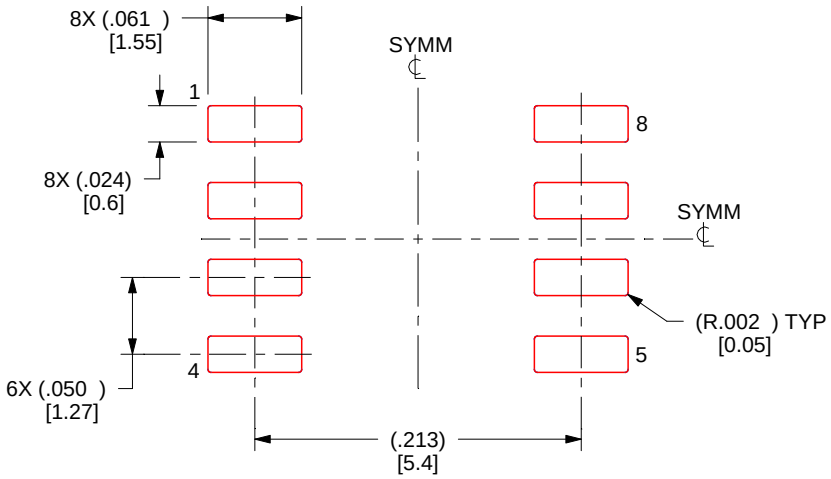
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月